Telescope to Test CMS Pixel Upgrade Detectors

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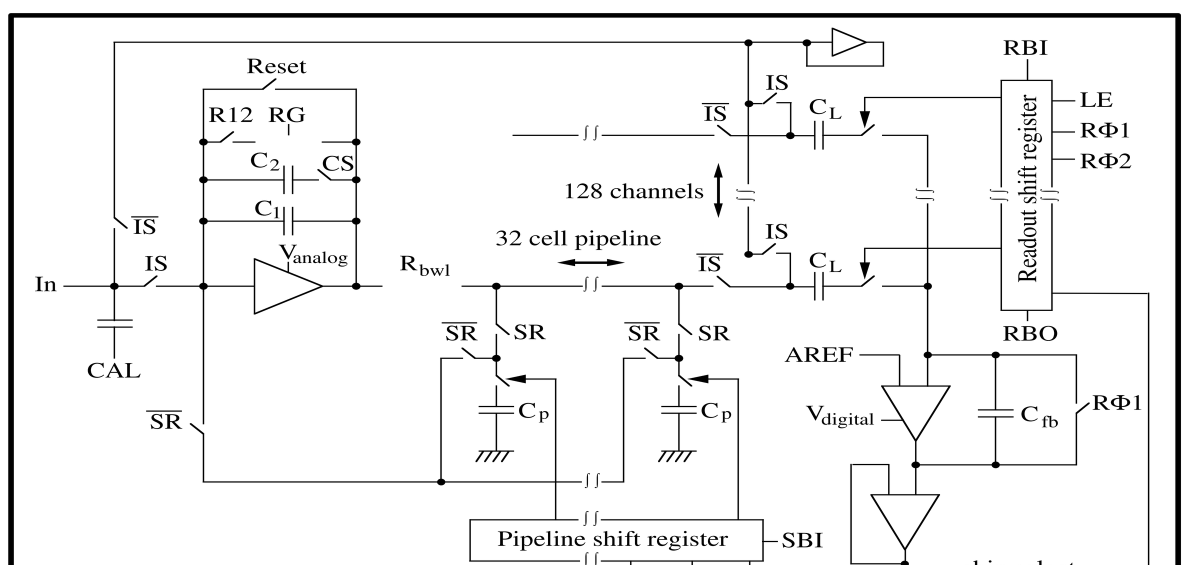
The innermost layer of the CMS Detector at the LHC is the silicon pixel tracker. The current version of the detector has performed well and been critical to the physics program of CMS. However, as the LHC produces higher instantaneous luminosities and higher center-of-mass energies, the detector must be upgraded to accommodate. The Phase-II Upgrade of CMS will replace the entire silicon tracking system. As part of this upgrade, a new section of the pixel tracker will be added in the so-called "very-forward" (TODO: η range)region of the detector. This new section of the detector will have different pixel geometries than the current detector, and these new geometries must be accurately characterized. Therefore, a telescope is being developed for the express purpose of characterizing these sensors so the pixel geometry can be optimized before settling on a final design to be placed in CMS. The telescope operates by using eight layers of silicon-strip sensors, with the device-under-test placed with four on each side. A charged-particle beam is directed so it passes through both the strip sensors and the device-under-test. Measurements from the telescope are taken to reconstruct individual particle tracks.

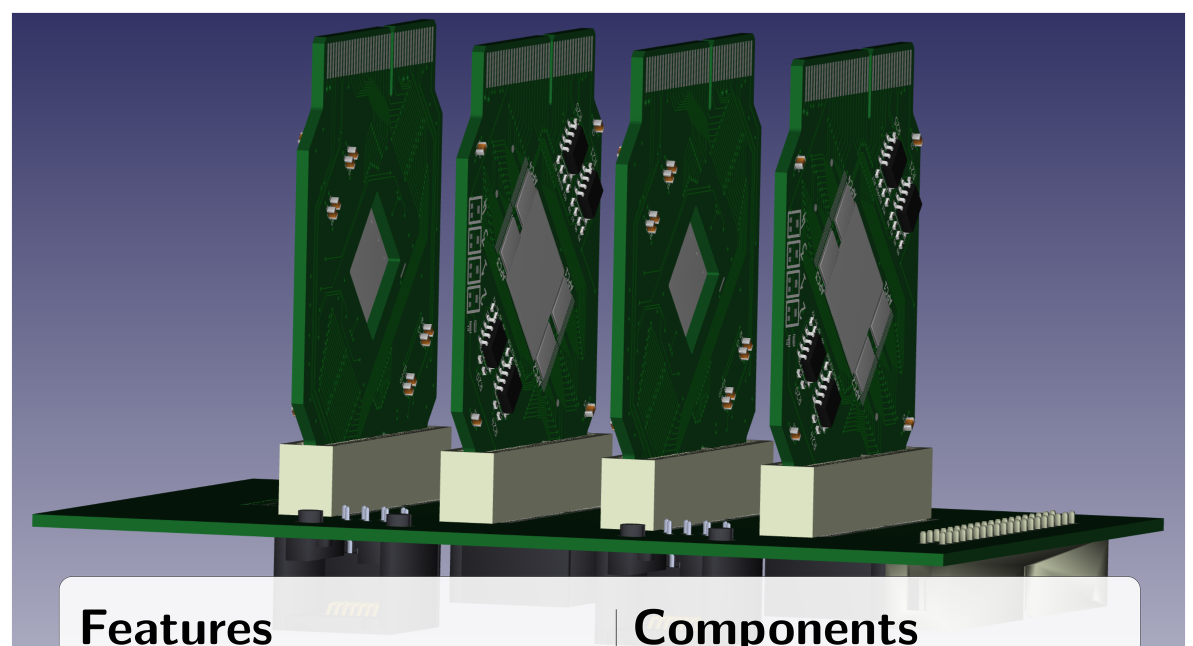
Hardware

Analog Pipeline Chip (APC-128)



- Originally developed tracker of the H1 detector at HERA
- Serializes the analog pulse-heights of 128 channels to dramatically reduce the number of required I/O lines
- Capable of sampling waveform data from of a strip sensor at upwards of 20MHz
- Features a very good signal-to-noise ratio of 40.
- Low noise combined with inter-strip charge-sharing give each layer of the detector a measurement precision of $\approx 1\mu$m

Sensor Board



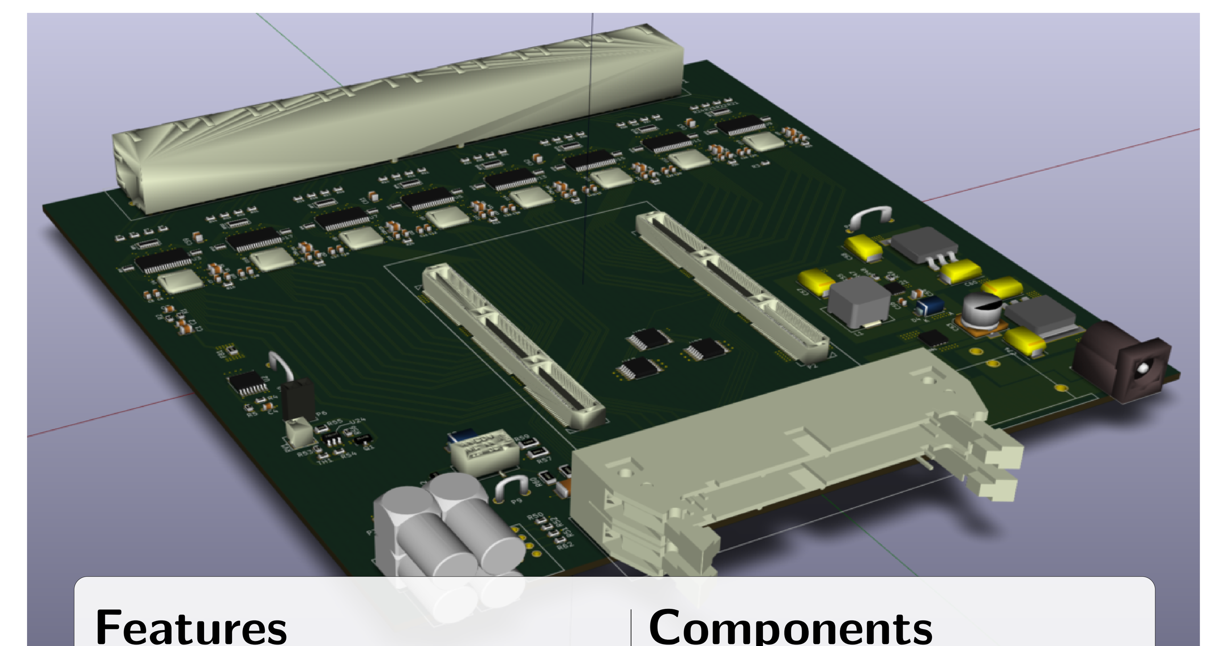
Features

- Each card can be used to measure either x or y track position
- Configuration shown has alternating x and y measurements
- Shared control signals for synchronous data taking
- Individual output channels for fast readout
- Fast readout is critical to minimize downtime

Components

- 4× Sensor Cards, each with
  - 1×512-channel microstrip sensor
  - 4×APC-128
  - 4×AD8138 buffer amplifiers
  - $4\times V_{analog}$ trimmer potentiometers
- 4×RJ-45 Ports
- 1×40-Pin .1" Header

Data Acquisition (DAQ) Board



Features

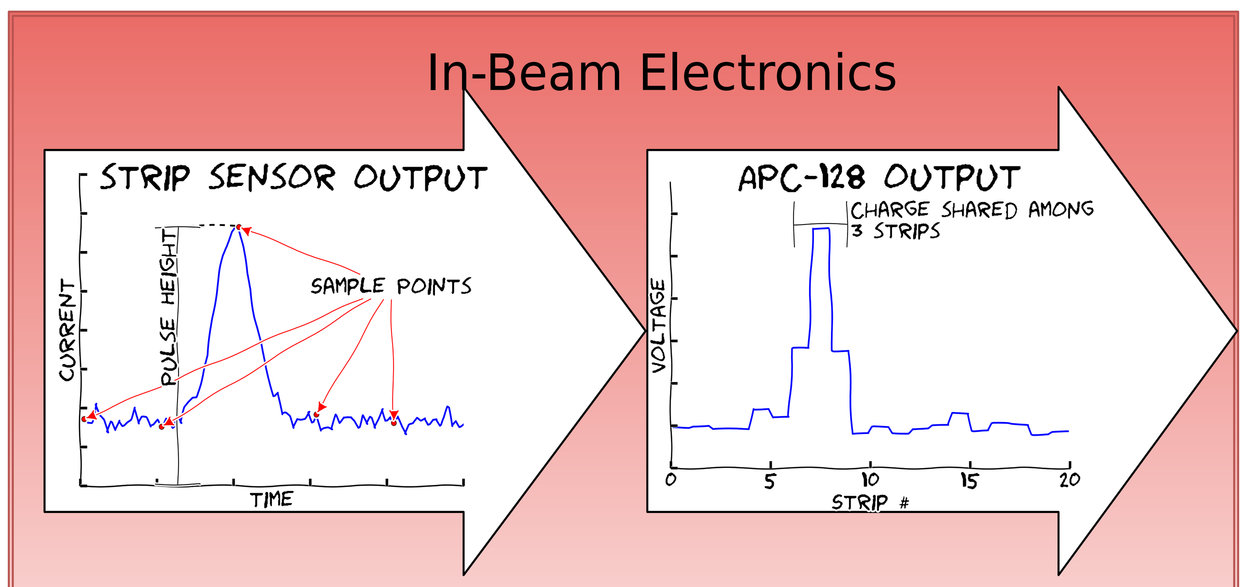
- Generates the control signals needed by the APC-128s
- 32 ADC Channels to read-out all APC128s in parallel, minimizing dead-time
- FPGA Board with associated USB hardware enables high-speed communication with online software.
- Handles external triggering from a variety of sources via an translator mezzanine card.

Components

- 1× ***Opal Kelly* ZEM4310** with
  - Cyclone IV FPGA
  - 128MB RAM
  - USB-3.0
  - 2×HSMC Connectors
- 8×AD9219 40MHz/10 bit ADCs
- 8×RJ-45 Ports
- 2×40-Pin .1" Header
- Bias-voltage control relay
- On-board power regulation

Readout Scheme

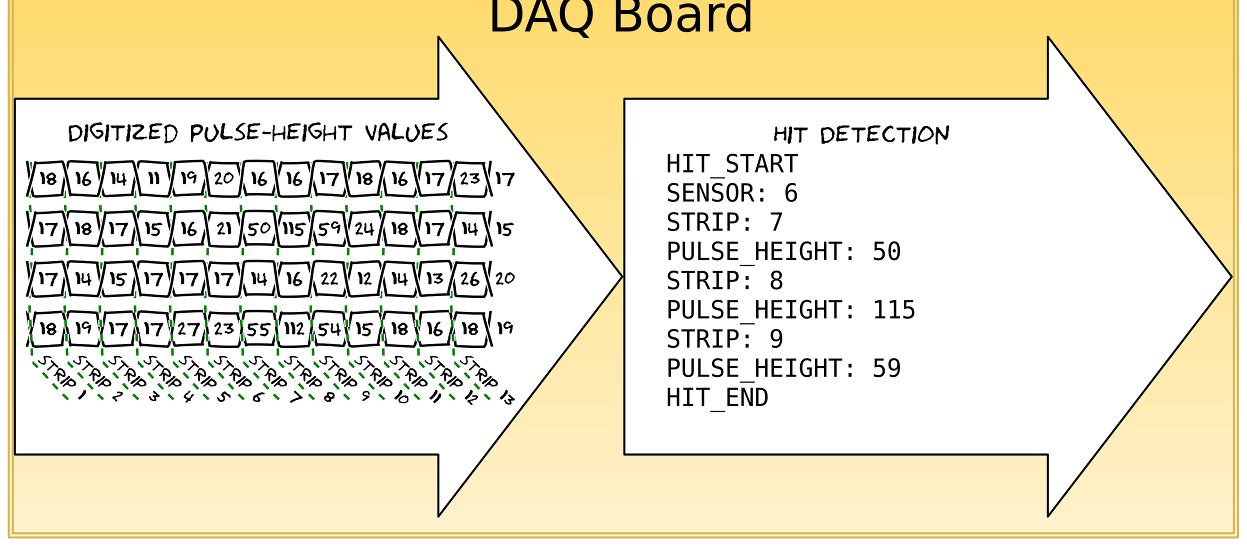
In-Beam Electronics



- The sensor is essentially a silicon NP-Junction operated in "reverse-bias" mode where all free charge carriers are evacuated
- An energetic charged particle passing through the silicon deposits energy to create free electron-hole pairs which are then separated by the electric field produced by the biasing voltage
- The electrons create a current spike that the readout chip, the APC-128, samples and stores
- Upon receiving a trigger, the APC-128 serializes the analog pulse-height sample from each of the 128 channels

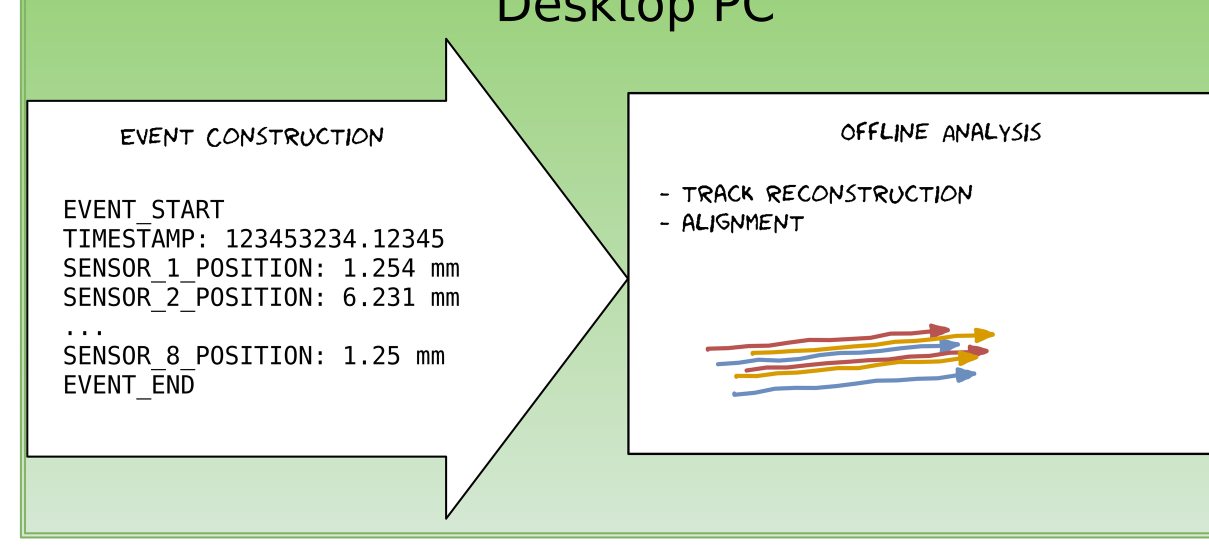
PUT SOMETHING HERE!!!!

DAQ Board



- The analog pulse-heights from the 32 APC-128 in the telescope are digitized by 8 high-speed 4-channel ADCs located on the DAQ board
- The digitized values passed to an FPGA board where they are processed into individual sensor hits
- Digitized values smaller than the noise-suppression threshold are dropped
- The sensor hit data is passed across a USB-3 connection to a PC.
- Its job finished, the DAQ Board becomes idle and waits for the next trigger.

Desktop PC



- Online softare organizes the hits into events and stores them to disk
- Since the detector layers can shift in space significantly during operation, alignment must first be done to accurately measure the geometry of the detector.
- After alignment, the various layer hits can be combined to construct extremely precise tracks.
- The tracks can then be compared for consistency with the data collected in parallel from the device-under-test, and, using the telescope as the ground truth, establish performance characteristics.

Progress

- ☑System design and parts selection
- ☑Circuit design and PCB Layout
- ☐Assembly and offline testing (in progress)
- ☐FPGA Firmware development and testing
- ☐Online/Offline software development
- ☐Commissioning runs with UNL Diocles electron beam

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References

- **PCB Design Files** https://github.com/cfangmeier/VFPIX-telescope-PCB
- **CMS Phase-II Upgrade**
- reference 3
- reference 4

Acknowledgments

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