VFPIX Silicon Telescope
Custom Electronics & DAQ Design

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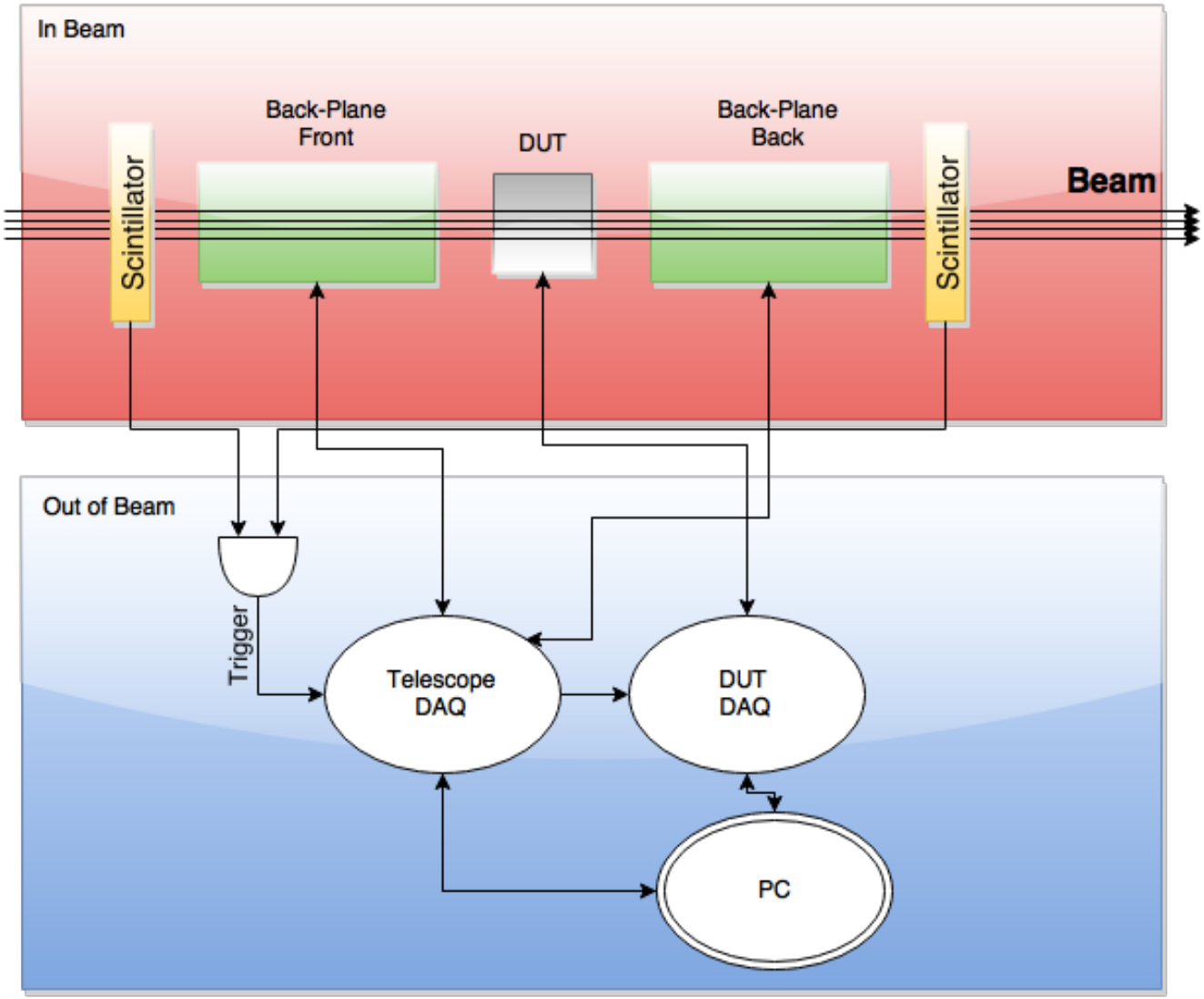
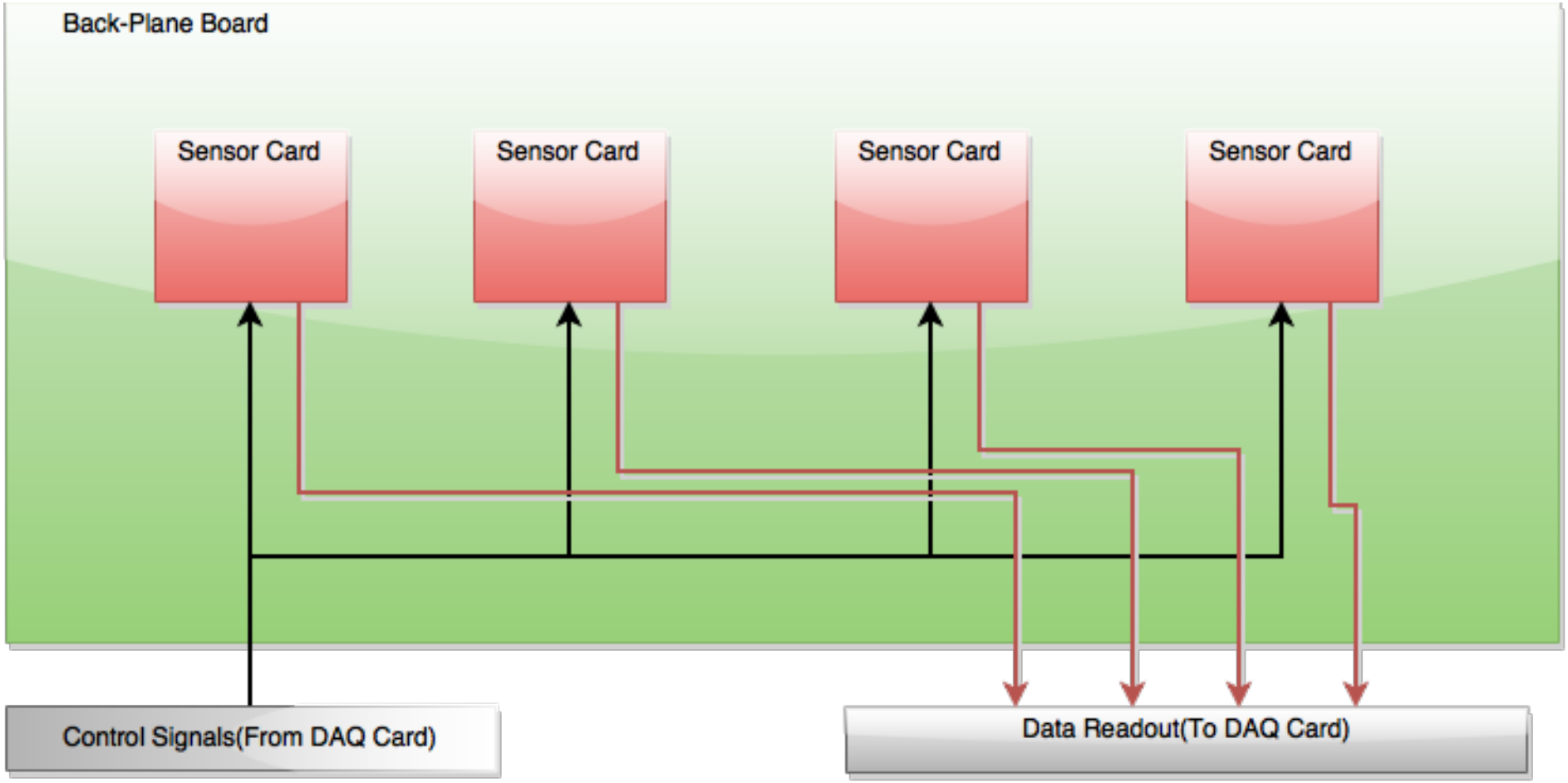
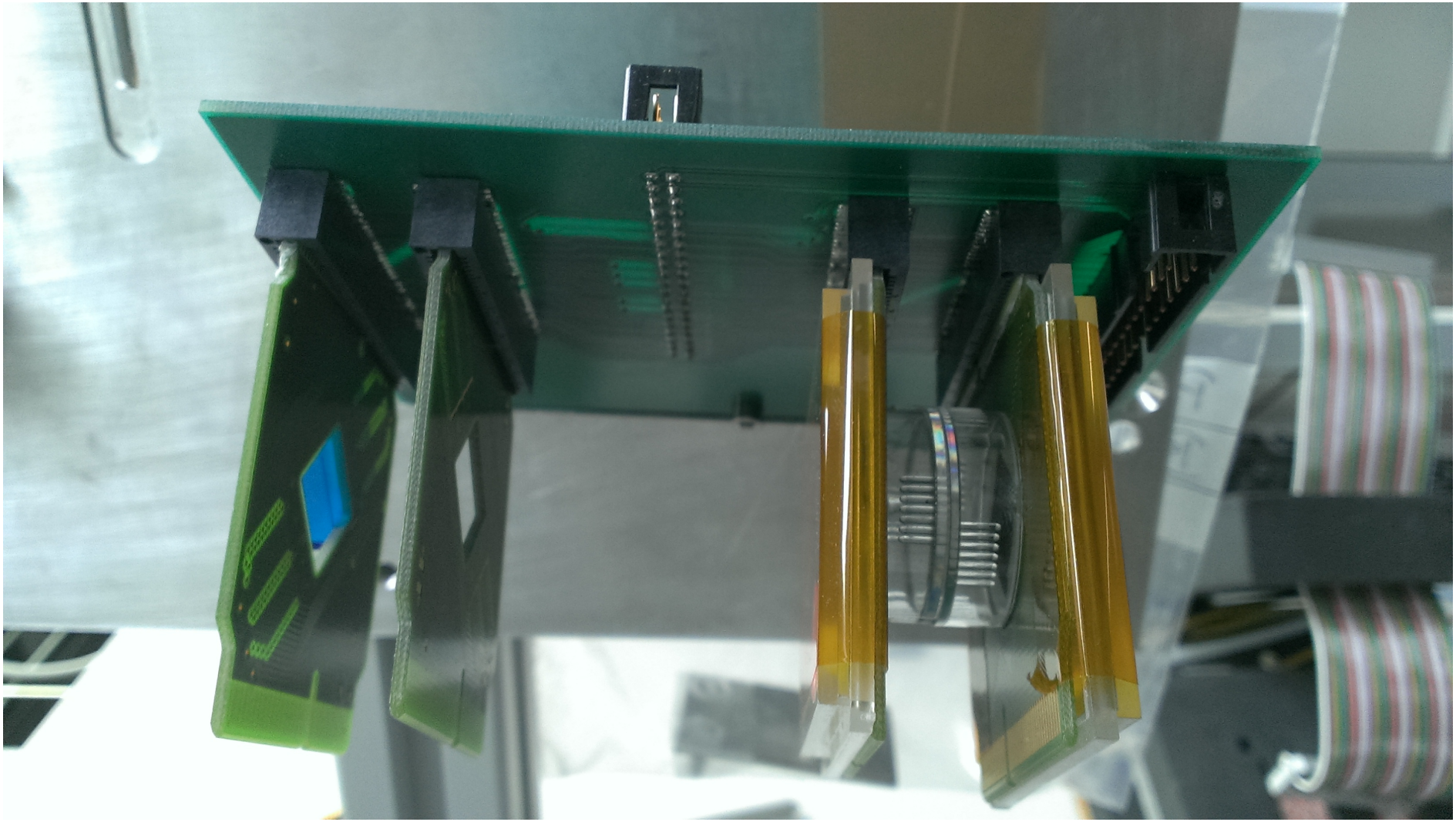
Telescope Block Diagram



The Back Plane Board



The Back Plane Board(Previous Iteration)



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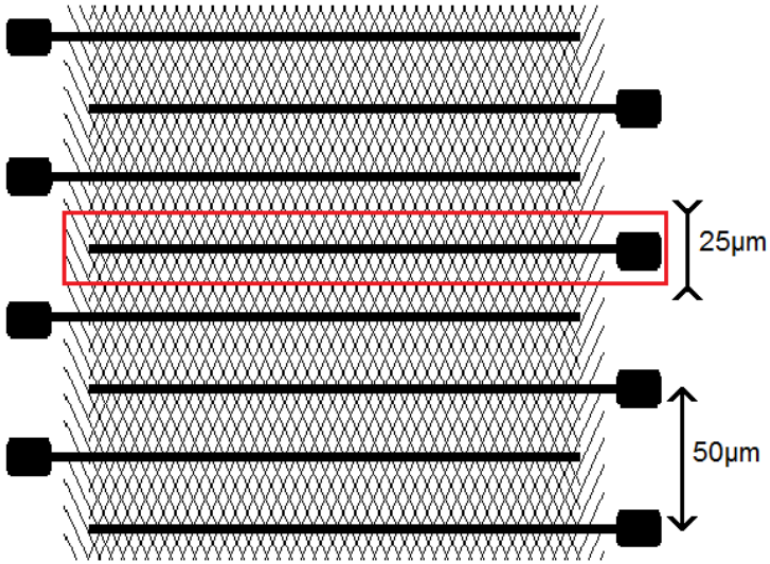
What parts of the system are fixed?

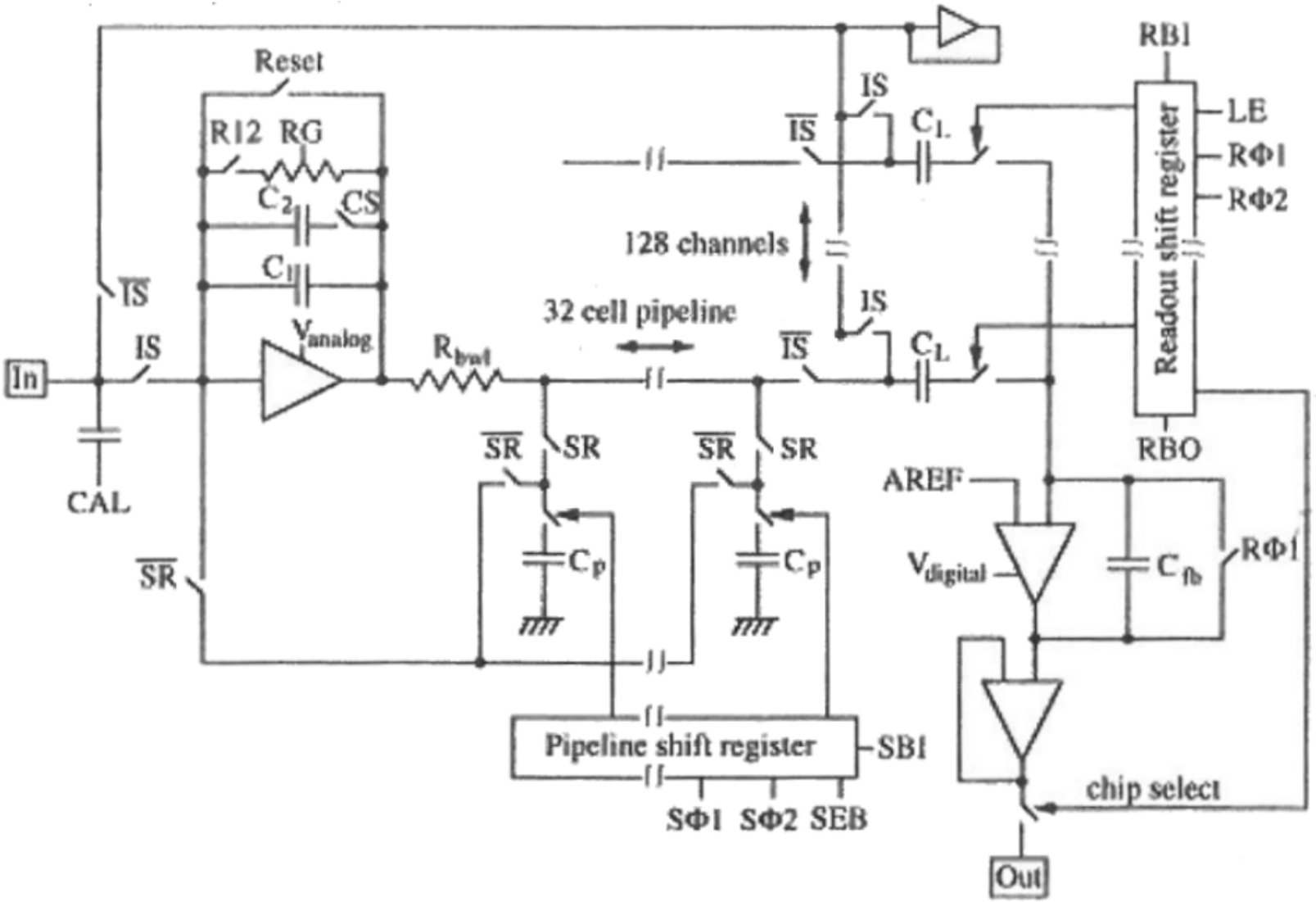
- Type and number of Micro-Strip Sensors
- APC128 Readout Chip
- Testbeam Constraints
  - Radiation Exposure
  - Mechanical Sizes

Micro-Strip Sensor

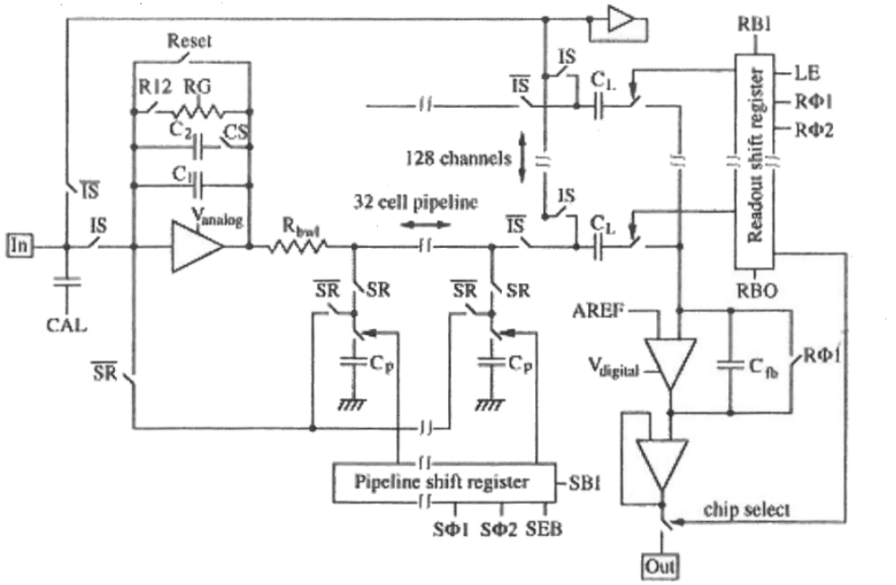
- 512 Strips per Sensor
- Adjacent Strips read out on opposite sides by APC128 Chips

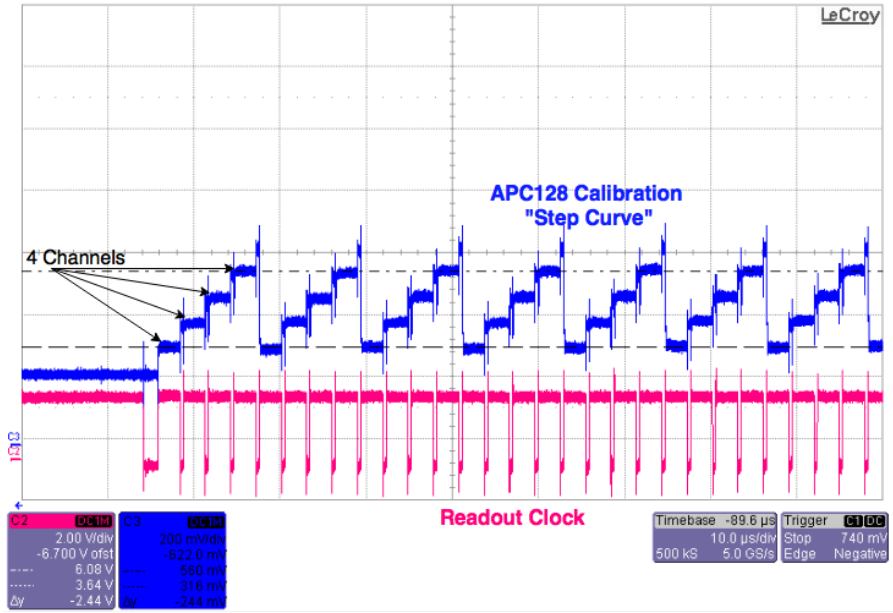


Analog Pipeline Chip 128



Analog Pipeline Chip 128





What parts are flexible?

- ADC location, precision(bitness), and sample rate
- Cabling
- Number/type of readout channels(Serial/Parallel, Analog/Digital)
- Digital Controller(FPGA,CPLD,Microcontroller, . . .)
- Amplifiers, DACs, Capacitors, Resistors, . . .
- PCB layouts of all boards including
  - Sensor Mount Card
  - Back-Plane Board
  - DAQ Card

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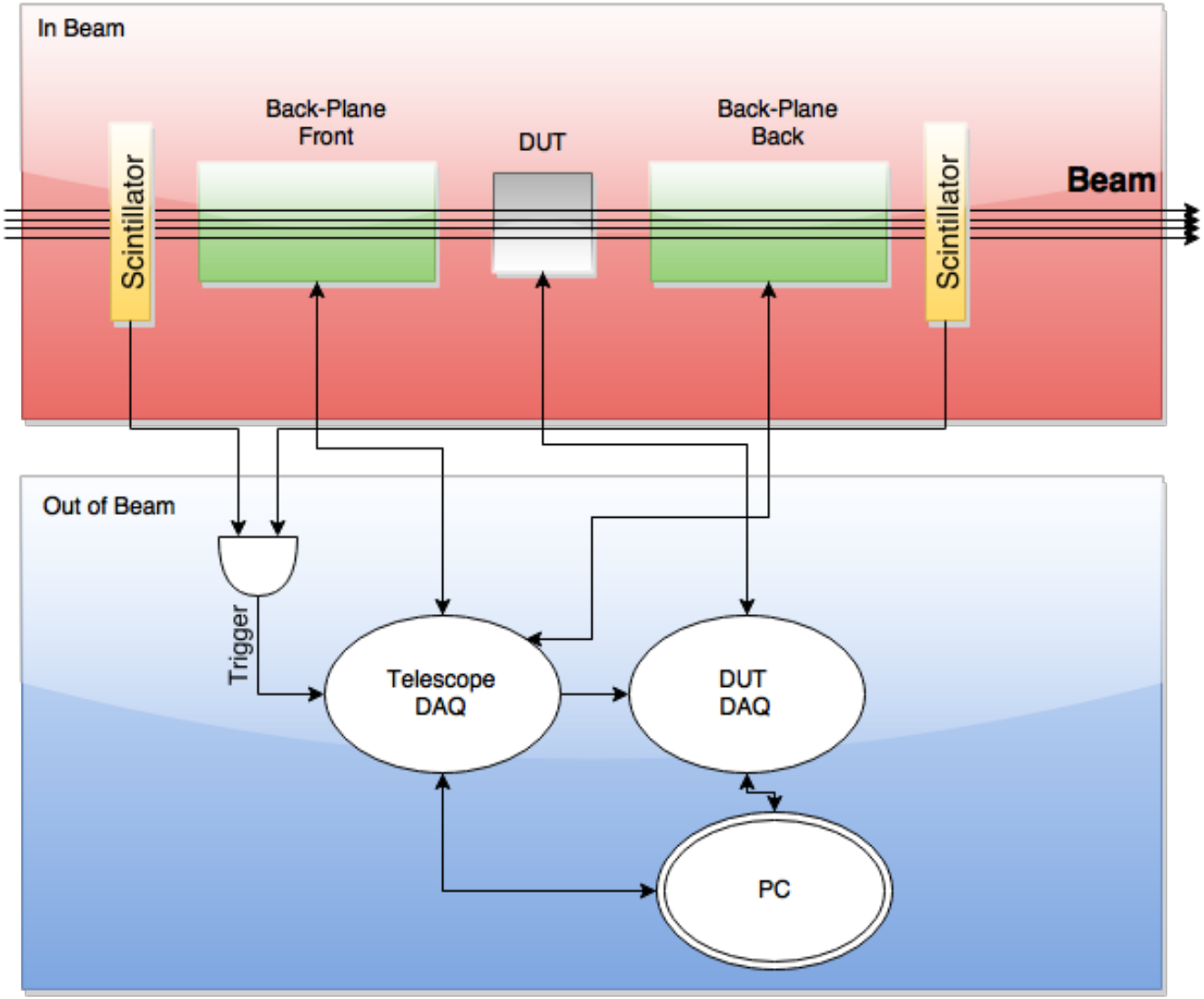
- 8 Sensors * 512 Strips/Sensor = 4096 Strips
- Each APC128 serializes 128 Strips
- $\rightarrow$ 32 Analog Channels with 128 Strips/Channel
- More serialization $\rightarrow$ fewer cables/ADCs, but slower readout
- Faster readout is critical to data rate!

Where to Digitize?


In Beam
Back-Plane
Front
DUT
Back-Plane
Back
Scintillator
Scintillator
Beam
Out of Beam
Trigger
Telescope
DAQ
DUT
DAQ
PC

- Any stateful electronics(e.g. ADCs, DACs, RAM, etc.) must be out of beam to avoid SEUs.
- Op-amps and other linear electronics are OK.
- However, less distance between sensor and ADC means less noise and, potentially, faster readout.
- Compromise is to place ADC on DAQ board $\approx$0.5m from telescope, but out of beam.

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APC128 Buffer/Line Driver

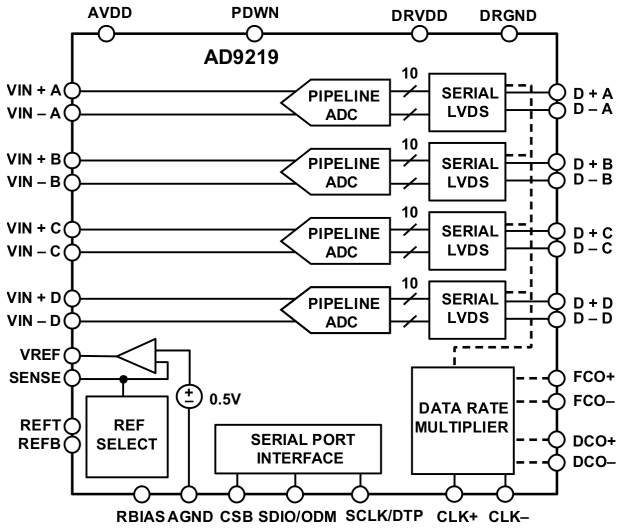
- Previous designs required APC128 to drive signal line directly.
- APC128 output very weak. $\approx 800\Omega$ output impedance.
- Cable capacitance resulted in slow rise times.
- Place buffer amp close to APC128

Choice of amp is the Analog Devices AD8138

- Very low noise, $5\text{nV}/\sqrt{Hz}$
- Appropriate bandwidth(300MHz) & slew rate($1150\text{V}/\mu\text{s}$)
- Differential output suitable for sending down a high-speed cable. e.g. CAT-5

ADC

Choice of ADC is the Analog Devices AD9219



- Sample speed up to 40MHz(will plan on oversampling signal)
- 10-bit precision
- 4-Channel differential inputs
- Requires a clock at sample frequency. Generates own readout clock.
- Must optimize PCB environment to achieve maximum performance.

Controller

Choice of Controller is Opal Kelly ZEM4310

- Integrated Module including
  - Altera Cyclone IV FPGA
  - USB 3.0
  - 128 MiB DDR2 SDRAM
  - 2xHSMC Expansion Header(on back)
- Appropriate for deserializing all 32 ADC channels in parallel
- Helps avoid design of difficult and expensive custom FPGA board

General Comments

- The design must incorporate parts one can actually order.
- Digikey is your friend!
- Keep a Bill-of-Materials with specific part numbers.
- Get used to reading datasheets.

PCB Design Gotchas

- Make sure the device pinout matches what you think it is. Sometimes multiple parts share a datasheet.
- There is no charge for extra writing on the silkscreen. *Use it!*
- Check part's datasheet for a recommended PCB footprint. Don't trust the built-in footprint library!
- Give some thought to how the board will be assembled. e.g. Avoid SMT parts on both sides.
- Respect the design rules of your PCB house. e.g. Min trace/via sizes
- Calculate power requirements and give yourself a 2x safety factor with your supplies.

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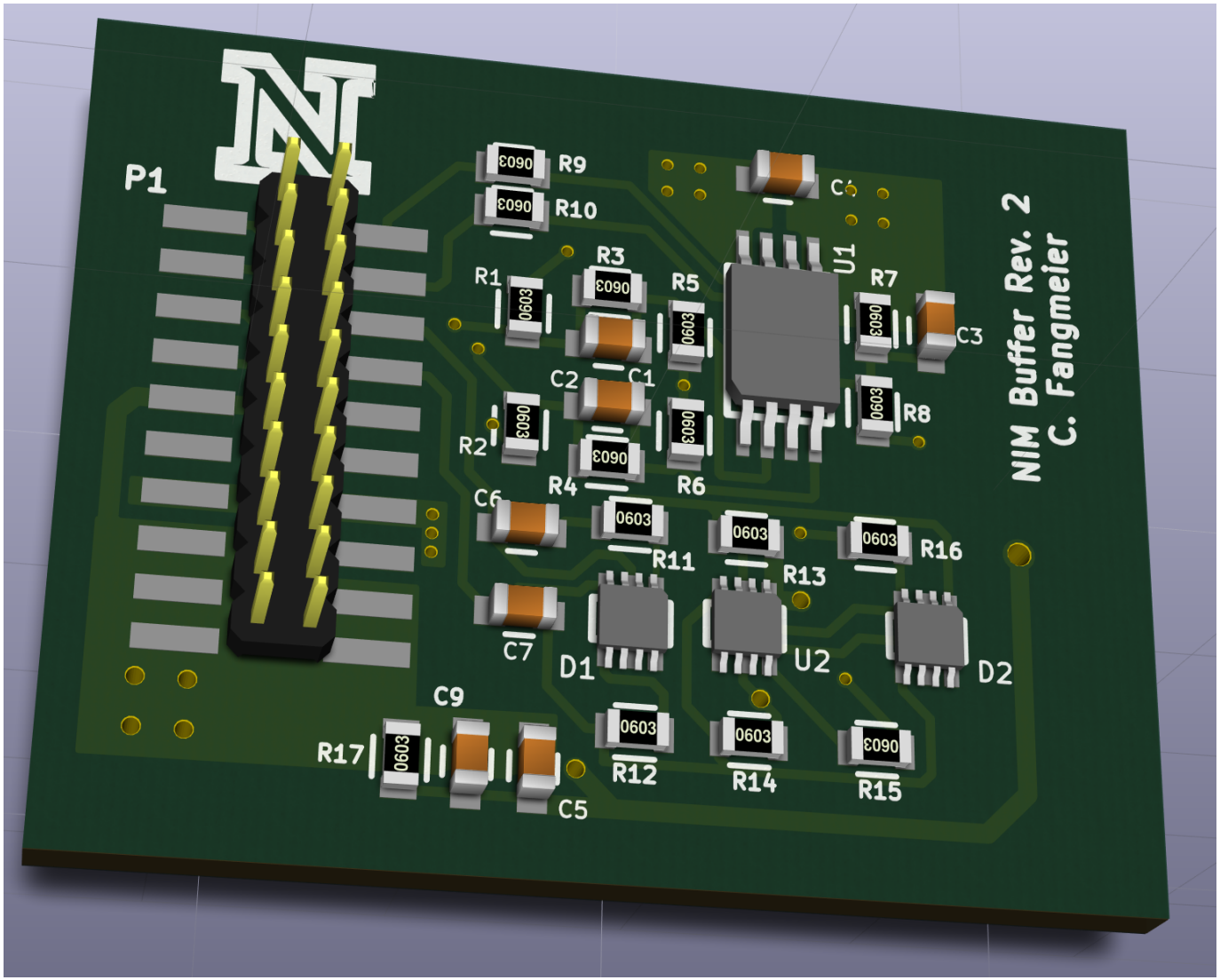
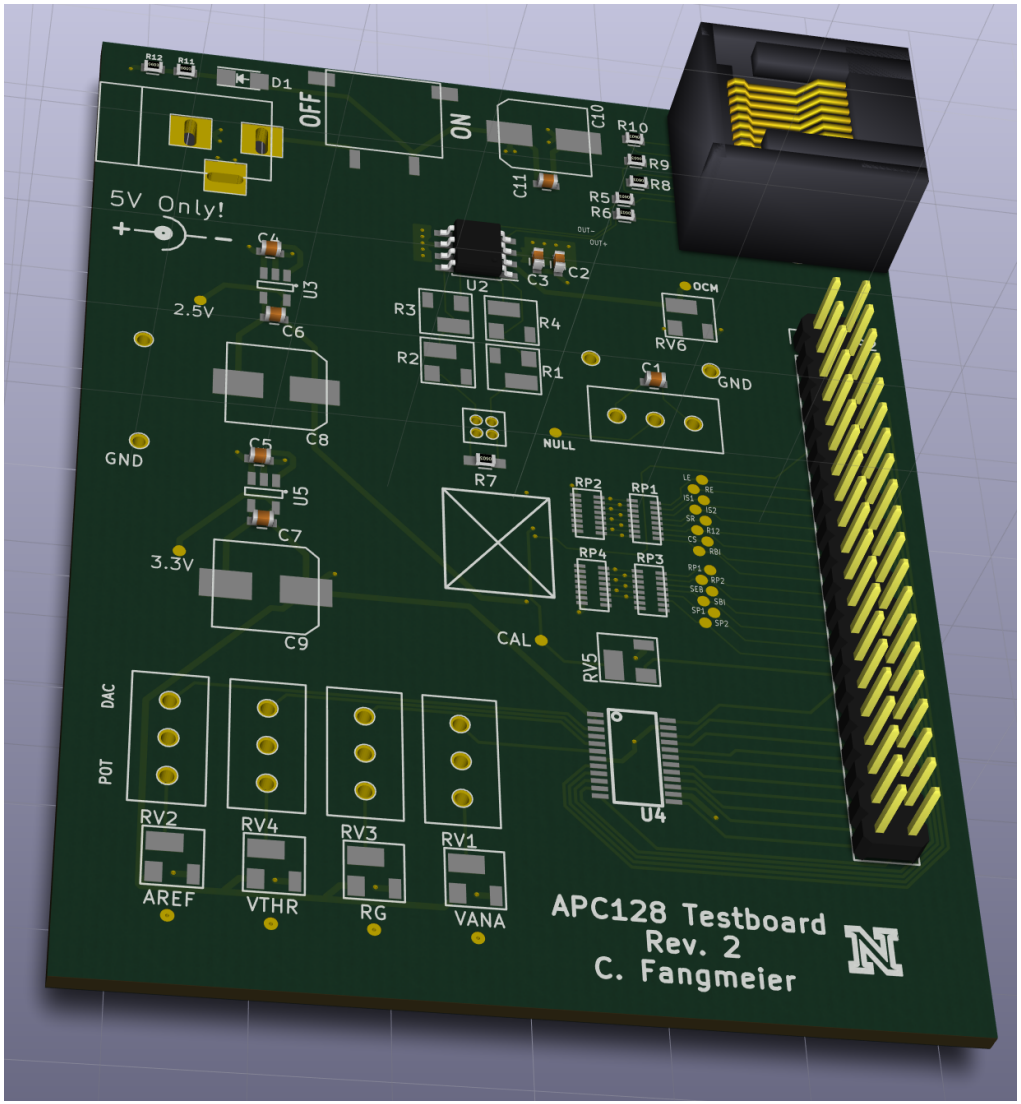
NIM-TTL Level Translator Board



APC128 Testboard



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- *Electronic Simulation* - **QUCS**
  - Free & Open Source
  - Great support for Linux.
  - Intuitive UI, Integrated Simulation Views
  - Good Support for Generic Simulation
  - Poor Integration of Spice Models
- *Circuit Design & PCB Layout* - **KiCAD**
  - Free & Open Source
  - No Limit on Board Size or Number of Layers
  - Under Active Development
  - Lacks some advanced features of commercial software
- *FPGA Design* - **Quartus II**
  - Proprietary
  - Developed By Altera (Same Company as FPGAs)
  - Can Develop Firmware Either Graphically with Block Diagrams or with an HDL (e.g. Verilog)

Custom Tools

- **PatternGen**
  - A Tool for converting ASCII waveform files to Verilog
  - Useful for generating multi-channel bit patterns with an FPGA
- **Make_Mapping**
  - A tool for mapping pins along a connection chain

References

All custom tools available here:
`https://github.com/cfangmeier/Small`

All Circuit/PCB Designs available here:
`https://github.com/frmeier/VFPIX-telescope-PCB`