VFPIX Silicon Telescope Design Document

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Abstract

A silicon strip detector based telescope is being designed for the purpose of testing a under-development silicon pixel detector for the VFPIX upgrade of CMS.

Here is documented the goals, constraints, and design decisions of the telescope.

Todo list

Contents

1 Introduction

The Compact Muon Solenoid (CMS) detector at CERN will undergo a second phase of upgrades during (year). A significant part of this upgrade will be the installation of the Very Forward Pixel (VFPIX) Detector. The VFPIX Detector is being designed to cover the range of $\eta > 2.5$[2]. To give adequate resolution of relevant physics parameters a new pixel shape is being proposed. As part of the R&D effort to design this new detector, a high resolution telescope is being built.

Year of Phase II install

2 Overview of Previous Work

This project is an iteration and redesign of an existing telescope. Previous work[4] has been done to design a versatile Sensor Mount Card (SMC)/Back-Plane Board (BPB) with features including the ability to chain multiple BPBs together to add aditional legs to the telescope. The SMC, in particular, was well designed to allow the sensor strips to oriented $\pm 45^o$ with respect to the plane of the BPB. This allows different sensors strips to be oriented either parallel or perpendicular to each other. The same telescope hardware can then be configured to measure to various degrees either vertical or horizontal accuracy by flipping the SMCs so the sensor strips align with either axis. This general design will be kept for the next iteration of the telescope, however the SMCs themselves will be iterated upon as described in 5.3.

Work has also been done to improve the readout properties of the Analog Pipeline Chip 128 (APC128) chips.[3] The APC128 has the unfortunate problem of a relatively weak output that has trouble driving a readout line at high frequencies. A proposed solution was to add a simple emitter-follower circuit on the BPB to reduce the load on the APC128 output and drive the line going to the ADCs with the transistor. This resulted in an improved readout speed of 250ns per channel. It is hoped that by using a dedicated differential line-driver instead of the basic emitter-follower, an even better readout speed can be achieved(see sec. 4.1).

It has also been discovered that there is significant variation between APCs where, all other things being equal, the output levels will vary from chip to chip by as much as 50mV.[3] However, this can be compensated for by adjusting the value of the Aref input per chip.

The precision of a strip telescope with charge sharing can be dramatically imporoved by improving its Signal-to-Noise Ratio (SNR). It has been demonstrated that by using a somewhat more complex readout pattern, wherein some background noise is removed by subtracting adjacent values in the readout pipeline, the SNR can be increased to approximately 25.An improvement from the 5-10 seen without this trick.[3]

3 System Components

The telescope consists of the following main components.

1. **Silicon Strip Sensor**

Find documentation for strip sensors.

2. **Analog Pipeline Chip x128 (APC128)** The APC128 (fig. 1) is a silicon chip designed for reading out charge from Silicon strip sensors. Each APC128 contains 128 channels. The sensor being used each have 512 strips. Therefore, each sensor requires four APC128 chips to read them out. The APC128's normal operation is as follows:

   A bit is shifted into the pipeline shift register. This allows the preamp (leftmost in the diagram) to push charge onto the C_p capacitors proportional to the current pulse-height. After the bit has shifted through the pipeline, another bit is shifted in. This pattern continues until a trigger is recieved, at which point a bit is placed into the pipeline to enable the proper C_p capacitor based on the trigger delay. This capacitor is then read back through the preamp and the charge gets placed on the C_L capacitor. Finally, when the charge is on each of the 128 C_L capacitors a bit is pushed into the readout shift-regiter which enables one channel at a time to serialize the output.

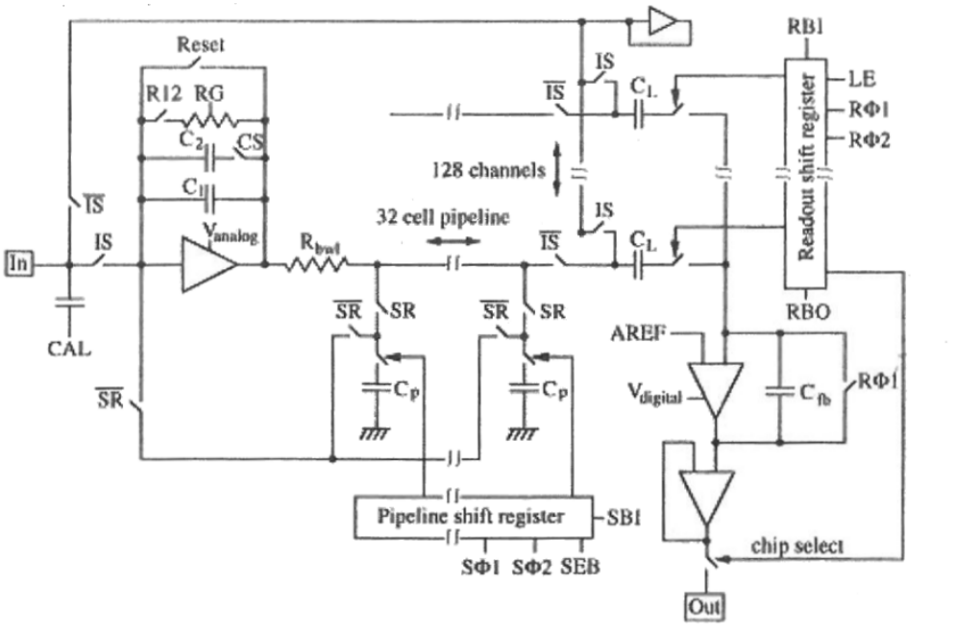


Figure 1: A schematic diagram of the APC128 chip.

3. **Sensor Mount Card (SMC)** The SMC holds the Strip Sensor, 4 APC128, and some auxillary components to facilitate the operation of the APC128.

4. **Back-Plane Board (BPB)** The BPB holds four SMCs. Its job is to physically hold the SMCs in place as well as route the signals between the SMC and the TRB.

5. **Telescope Readout Board (TRB)** The TRB is responsible for controlling the operation of the telescope. This means it must generate the control signals for the APC128 chips as well as the ADCs that will digitize and serialize the data being read from the APC128s. It will also contain an FPGA with supporting hardware to allow it to communicate with a connected PC via a USB connection. It must also

4 Performance Targets

- **SNR:** 40
- **Readout Speed:** 100ns/channel $\rightarrow$ 8kHz readout of entire telescope
- **Pipeline Speed:** 40MHz, will vary with source

4.1 Precision/Accuracy Targets

For charactering pixel sensors with pixel pitch as small as 25 μm, a tracking precision of better than 1 μm is desired. To achieve this, we require a SNR of better than 40.

check precision targets

4.2 Speed Targets

5 Hardware Proposal

5.1 Silicon Strip Sensor

The silicon micro-strip sensors that will be used to measure particle tracks in the telescope have 512 strips each. Fig. 2 shows the layout of a sensor.

5.2 Analog Pipeline Chip

The APC128 will be used to read charge from the silicon strip sensor.

5.3 Sensor Mount Card

The design choices of the SMC are especially critical becuase it is responsible for ensuring optimal operation of the APC128 chips during both control and readout.

The readout of the APC128 is analog so it is more susceptable to noise and interference than a digital signal would be.

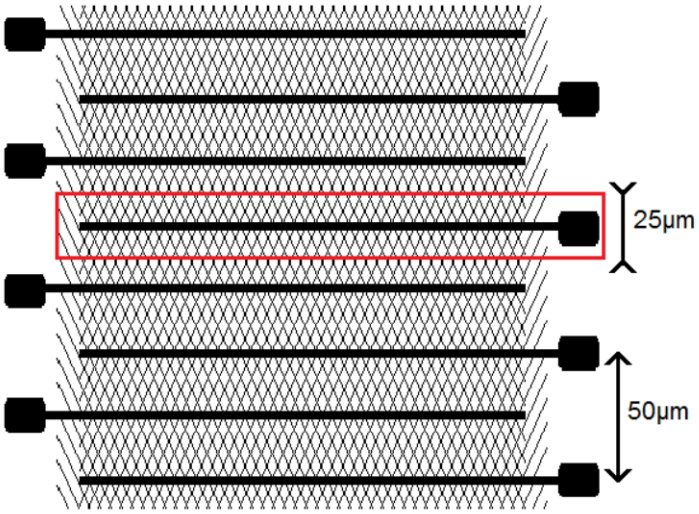


Figure 2: Layout of a silicon micro-strip sensor. As shown, there are 25μm between strips. The strips are divided between 2 layers so the separation between strips on the same layer is 50μm

The SMC will be subject to the highest radiation fluence of the entire system which limits the choices of hardware that can be placed on the it. Any FLASH memory dependent hardware will be subject to Single-Event Upset (SEU)s.

Because of these restrictions, only the minimum hardware necessary to ensure high quality APC128 operation and output will be placed on the SMC. This hardware consists of a 2-channel differential-line driver amp. The chosen amp is the ADA4950-2[1]. Two of these will be placed on each SMC, as close as possible to the APC128s to minimize the capacitave load on the outputs.

It has been determined (see sec. 2) that to achieve optimal operation of each APC128 in the telescope, it is important to be able to set each APC128s Aref voltage individually. To do this, four potentiometers will be placed on each SMC to allow for idividual calibration of each APC128s Aref value. Potentiometers were chosen for this task over DACs becuase of the risk of SEUs in the DACs are placed near the beam, and the addition of many new signal lines if they are placed far from the beam.

5.4 Back-Plane Board

The primary jobs of the BPB are to route signals between the and the SMCs and hold the SMCs in place. It has been considered to digitize the signals on the BPB by placing the ADCs on it. However, this has two major drawbacks. First, since ADCs are stateful devices, they are susceptable to SEUs

decide placement of ADCs, either on TRB or BPB

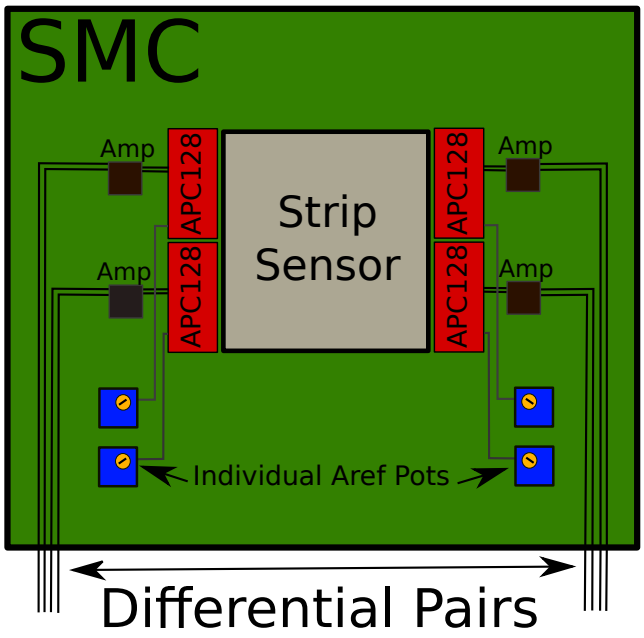


Figure 3: An illustration of the SMC. Not shown: APC128 control signals

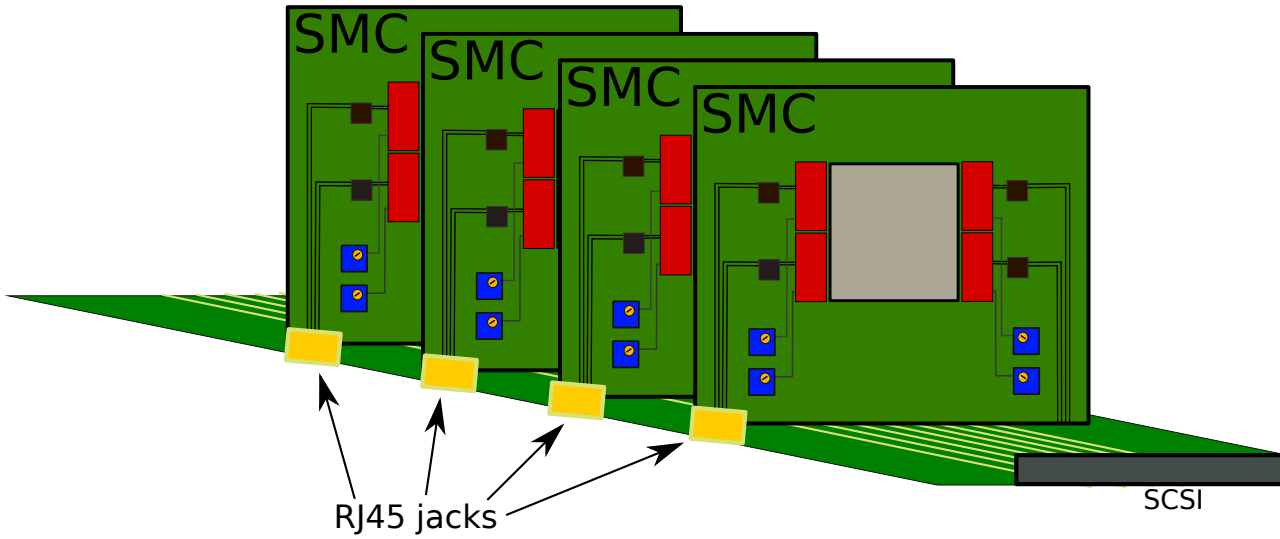
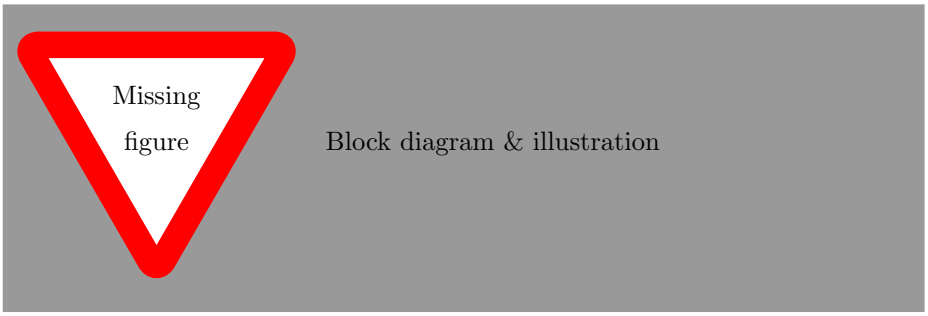


Figure 4: An illustration of the BPB

5.5 Telescope Readout Board



6 Timeline

Fill in timeline

References

[1] ADA4950: Low power, selectable gain differential adc driver.

[2] Aaron Dominguez. Proposal for r&d related to the module and sensor design for the phase-2 upgrade of the cms forward pixel detector. CMS-doc-12163-v1, 2013.

[3] Adrian Ryser. Semesterarbeit - pixel telescope. 2013.

[4] Paul Turner. Design and implementation of a high resolution telescope for cms pixel detector characterization. June 2012.

Glossary

APC128 Analog Pipeline Chip 128. 3–7, 9

BPB Back-Plane Board. 3, 6, 9

CMS Compact Muon Solenoid. 3, 9

LHC Large Hadron Collider. 9

SEU Single-Event Upset. 5, 6, 9

SMC Sensor Mount Card. 3, 5–7, 9

SNR Signal-to-Noise Ratio. 3, 5, 9

VFPIX Very Forward Pixel. 3, 9