DesignWare IP Prototyping Kit for USB 2.0 HS OTG Controller

Highlights

- DesignWare USB 2.0 HS OTG Controller
- Supports High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) USB standards
- Includes one USB 2.0 port
- USB 2.0 16-bits/30 MHz clock UTMI+ interface
- 32-bits AHB Master interface for DMA operation and 32-bits AHB Slave interface for register access
- Host Negotiation (HNP) and Session Request Protocol (SRP) capable OTG
- Supports Link Power Management (LPM) operating mode
- Enabled Hibernation Power optimization in Core
- Pre-instrumented deep-trace debug for most interfaces
- Support for Linux® OS; includes Linux driver and Linux application examples

Overview

The DesignWare® IP Prototyping Kits, part of the IP Accelerated initiative, center around a complete, out-of-the-box reference design that consists of a validated IP configuration and necessary system-on-chip (SoC) integration logic for a specific IP protocol, implemented on a Synopsys FPGA-based prototyping system.

With a proven reference design for the IP, designers can be instantly productive, enabling them to accelerate the integration of IP into their target SoC, optimize the IP configuration, and develop drivers with real world I/Os and hardware. The prototyping kit provides prototyping hardware with automation tools, and scripts and configuration files enabling fast iteration.

IP Prototyping Kit Processor Compatibility

To meet your exact IP prototyping needs, IP Prototyping Kits for USB 2.0 allow the target IP core to be implemented a Synopsys FPGA-based prototyping system using a PCI Express connection to a PC with the processor of your choice.

IP Prototyping Kit for USB 2.0 HS OTG Controller

The IP Prototyping Kit for USB 2.0 HS OTG controller supports OTG features, such as SRP and HNP.

- Includes filters for OTG specific PHY interface signals
- Enables bus filters for UTMI power control input signals
- Power optimization mode for clock gating

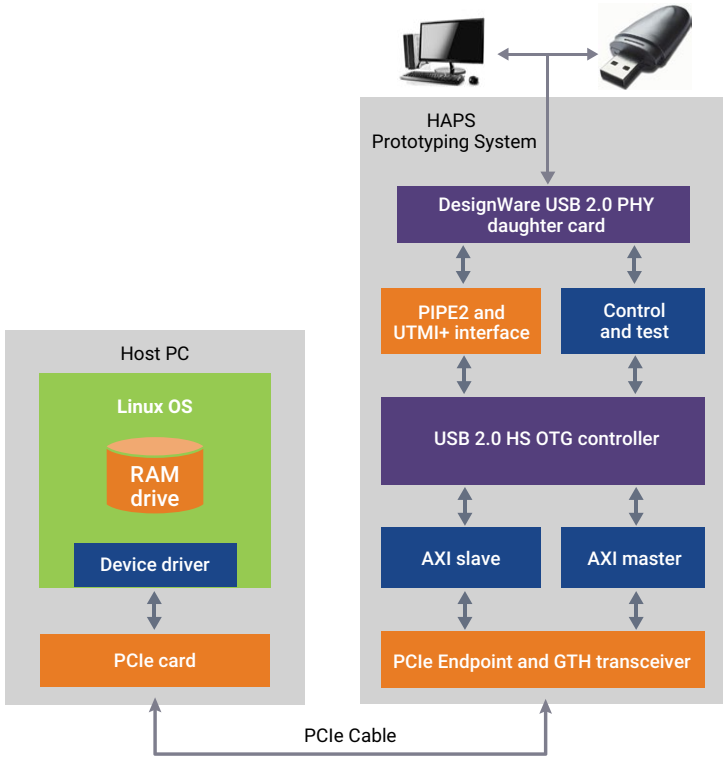

Figure 1: DesignWare IP Prototyping Kit for USB 2.0 HS OTG

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.

SYNOPSYS®
Silicon to Software™

08/06/18.CS257477750 DesignWare IP PrototypingKitForUSB3.0DRDinUSB2.0-OnlyMode.