Automatic White Balance for Digital Imaging

SCENIX

Application Note 12
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1.0 Introduction

Color digital imaging systems must be designed to accommodate light sources of different color temperatures (for example, sunlight and incandescent light). Each type of light source has a different color composition. For example, incandescent light contains more yellow than sunlight. This difference in color is not visually apparent because the human eye automatically adjusts to wide range of light sources, perceiving all of them as a neutral white. However, to photographic film designed for sunlight or to a CCD (Charge Coupled Devices) sensor system with a fixed color balance adjusted for sunlight, changing from sunlight to incandescent light results in a picture that looks very yellow-orange throughout.

In color film photography, color balance is typically achieved by using artificial light that is balanced to mimic sunlight (for example, photo strobe lights) or by putting a color-adjustment filter over the lens. A certain amount of correction can also be accomplished in the color printing process (when prints are made from color negatives).

In digital imaging applications, color balance is typically achieved by a technique called “automatic white balance.” This means that the imaging system adjusts its color spectrum sensitivity to the scene being photographed such that the resulting image has, on the average, an equal amount of all color components. In effect, the imaging system inserts whatever color filter is necessary to bring the overall image to a neutral white color tone, without any dominating color cast. This method usually works better if the imaging system looks at just the brightest parts of the picture and ignores the darker parts.

2.0 CCD Image Capture

In typical digital imaging systems, a light-sensitive CCD array is used to capture the image. Light striking the array produces a charge on each pixel in the array. To obtain an image, the charges are shifted out of the array, producing an analog signal. This signal is amplified, converted from analog to digital format, processed digitally, and then transmitted or stored as a mathematical representation of the image.

There are several different ways to represent a color image mathematically. One common way is the RGB (red-green-blue) format, in which each pixel is assigned three values to represent the brightness of the red, green, and blue components. Many broadcast, video and imaging standards use luminance and color difference video signals. These may exist as YCbCr or YUV color spaces. Although all are related, there is some difference. In the YCbCr (Luminance-Chrominance Blue-Chrominance Red) format, one value specifies the luminance (brightness) of the pixel and two other values specify the chrominance (color value) of the pixel. This format is a scaled and offset version of the YUV color space. Conversion between one format to the other is a simple mathematical operation.

The YCbCr and YUV formats are useful in data compression algorithms because the Cb/ Cr or U/V components can tolerate a higher compression ratio (and therefore loss of data) without loss of visual image quality. These formats are also useful in white balance adjustment algorithms because you are working with just two color values instead of three.

The operation of automatic white balance in a typical digital camera is shown in Figure 2-1. The lens on the CCD array focuses the image. The CCD produces an analog signal, which is amplified and then converted from analog to digital format. The digital data is processed by a DSP ASIC device. The processed image data is stored in a RAM-based buffer, from which it can be processed further for long-term storage or for display. A microcontroller handles the user interface and controls the overall operation of the camera. The automatic white balance algorithm modifies the gain of the amplifier to make the image have an overall neutral color balance.

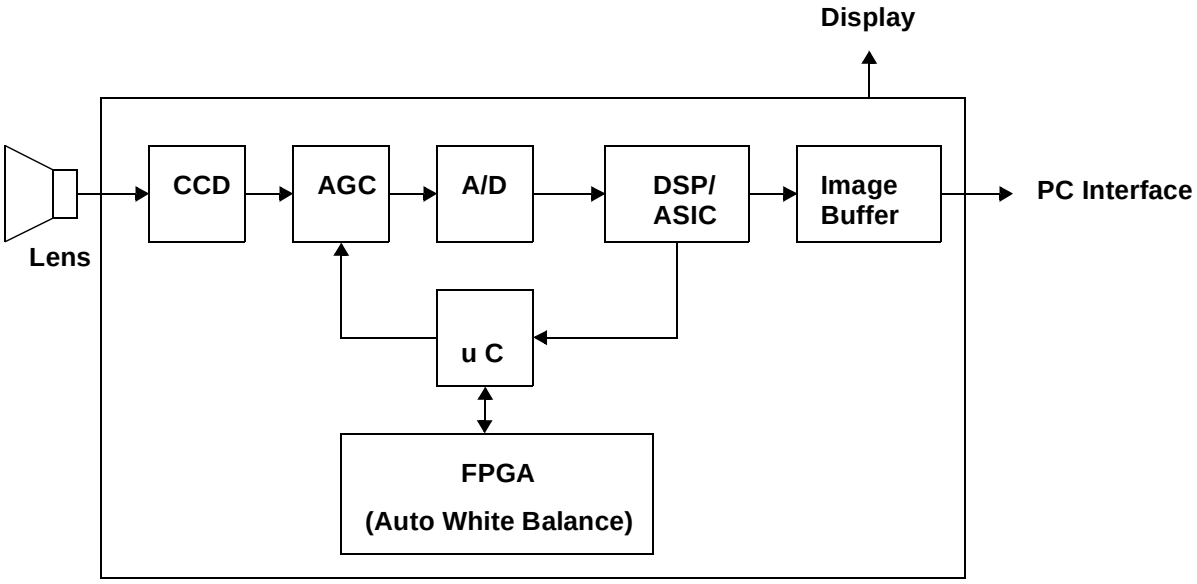

Figure 2-1. Digital Camera Block Diagram

3.0 Video Data Rate and Format

To meet NTSC and ITU-656 specifications, and for MPEG1/MPEG2 compatibility, the sampling rate of the CCD sensor output must be 27 MHz (27 million pixels per second). A 27 MHz clock divides each horizontal line of video into pixels. The clock has to be stable (a very small amount of jitter) relative to the incoming video in order to capture the data accurately.

The data words in the video data stream are multiplexed in a specific order: U, Y, V, Y, U, Y, V, etc. The Y values represent the brightness and the U and V values represent the color. The automatic white balance algorithm adjusts the signal gain to balance the resulting U and V values.

The video signal contains digital code words transmitted over eight parallel conductors organized into pairs. Each pair carries a multiplexed stream of bits of each of the component signals (U, Y, V, Y). Another conductor serves as a synchronous 27 MHz clock. The signal timing is shown in Figure 3-1.

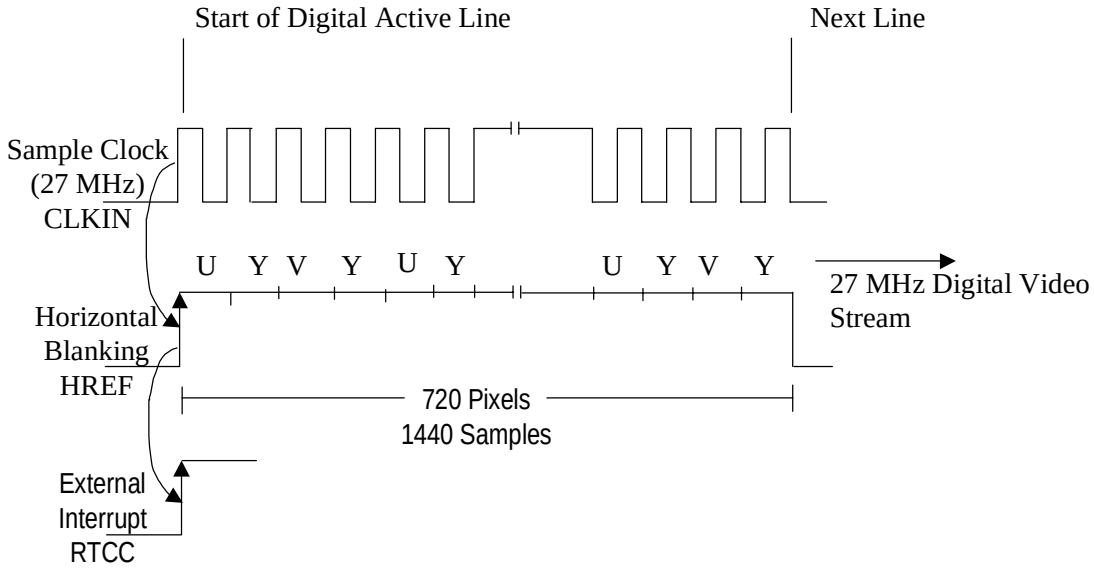

Figure 3-1. Video Steam Timing

4.0 Automatic White Balance

The automatic white balance algorithm described here is based on the assumption that the scene is neutral in color (at least when averaged over the whole image). Therefore, the brighter parts of the image need to be balanced to a neutral white. For speed, the algorithm only looks at a fraction of all the pixels, taking samples from a uniform grid over the image, and balances the color of the brighter samples found.

The algorithm uses four lines in the image spaced 32 lines apart, and looks at 16 samples spaced equally across each of the four lines. For each sampled pixel, if the luminance value is greater than 60% of the peak value and the chrominance value is greater than 50% of the peak value, a chroma counter is incremented. Otherwise, the counter is decremented. After processing all 64 samples, the counter value indicates the overall color balance. If the counter value is positive, the chroma gain is decreased. Otherwise, the chroma gain is increased.

5.0 SX Implementation of White Balance

White balance has typically been done by an FPGA device, or by an DSP/ASIC device that performs other image processing functions. Usually, a separate microcontroller manages the control functions of the camera. The microcontroller used in this application have typically not had enough performance to execute the real-time video functions.

However, if a relative inexpensive but high-performance communications controller were available, it could not only perform the general management and control functions, but could also provide white balance control. This would eliminate the need for an FPGA, with its design and other costs. It would offer the greatest flexibility and allow the algorithm to be modified if needed. In addition, the in-system programmability of the SX communications controller would significantly reduce time-to-market.

These are the main characteristics of the SX communications controller to be considered as an FPGA replacement:

- High operating frequency. The device is capable of operating at rates of at least 27 MHz, the sampling frequency of the ITU-656 standard, so that the oscillator frequency can be synchronized to the data sampling rate.
- True single-cycle instruction execution. The input clock rate should be equal to the instruction rate, rather than some multiple of the instruction rate. In microcontroller devices that divide the input clock rate to obtain the instruction clock, the phase of the instruction clock with respect to the input clock is unknown, introducing the additional problem of synchronizing the instruction clock to the data sampling clock. In devices that use the input clock directly as the instruction clock, there is only one input clock edge per instruction to deal with.
- Deterministic times for instruction execution and interrupt response. The instruction execution time and the interrupt response time must be known exactly under all conditions. This lets the program keep track of the number cycles after the rising edge of the HREF (Horizontal Blanking) signal (see Figure 2), including the interrupt response time, and correctly sample the desired data pair (U,Y or V,Y) anywhere within a horizontal scan line.

The SX communications controller from Scenix is a high-performance, RISC machine that meets all of these requirements. It uses a four-stage pipeline (fetch, decode, execute, and write back), resulting in execution throughput of one instruction per clock cycle. At the maximum operating frequency of 100 MHz, most of the instructions are executed at the rate of one per 10-ns clock cycle (100 MIPS performance). The interrupt response time is deterministic, taking only three cycles (30 ns) from interrupt acknowledgment to the beginning of the interrupt service routine. It also supports in-system programming and in-system debugging.

The high processing power of the SX allows the device to not only provide white balance control, but also to manage Automatic Gain Control (AGC) for a digital camera's analog front-end. In addition, the device can handle user interface, pushbutton scanning, and system power management.

Figure 5-1 shows how the video signals are connected to the SX18AC. The 27 MHz CLKIN signal is directly connected to the SX18AC clock input pin (OSC1). This clock is in sync with respect to the HREF signal, which is connected to the SX18AC RTTC (interrupt source) pin. VSYNC is used to indicate the end of the vertical scan. Port B of the SX18AC is used to read the 8-bit 27MHz data (8 Bit Mode of ITU-656 Format). White balance commands are sent via the I2C bus (SDA, SCL signals).

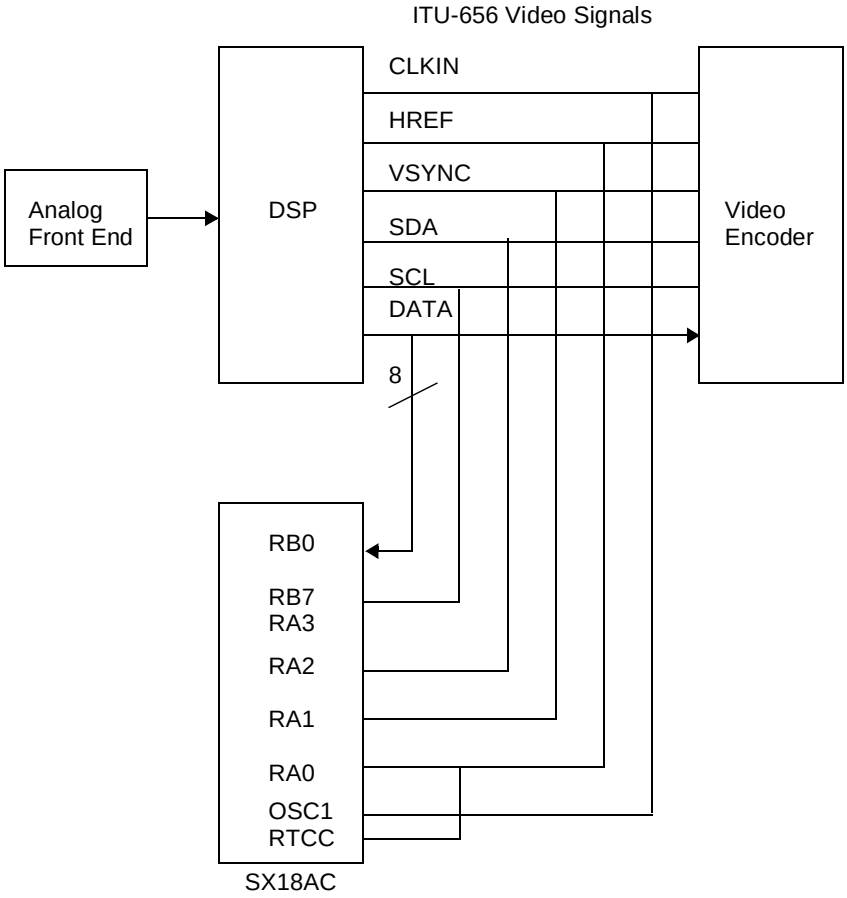

Figure 5-1. Automatic White Balance Implementation with SX Communications Controller

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Sales and Tech Support Contact Information

For the latest contact and support information on SX devices, please visit the Scenix Semiconductor website at www.scenix.com. The site contains technical literature, local sales contacts, tech support and many other features.

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