Sigma Delta ADC Implementation Using the SX Communications Controller

SCENIX

Application Note 2
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1.0 Introduction

The sigma delta ADC benefits from all the usual digital advantages, i.e. higher reliability, higher stability and increased functionality. In addition, as sigma delta converter uses mainly digital techniques, it is possible for it to be implemented as a software function in a high performance communications controller with minimal external hardware overhead.

Successive approximation, dual slope, and flash analog-to-digital converters are all based on the principle of sampling at around the Nyquist frequency and require a good anti-aliasing filter. Sigma delta ADC, on the other hand, use a low resolution ADC (one bit quantizer) with a sampling rate many times higher than the Nyquist frequency. To implement the sigma delta ADC function as a software module (Virtual Peripheral™) on an microcontroller, the device must offer sufficient processing power to accomplish the high sampling rate.

This paper demonstrates how the SX communications controller can be used to implement an 8-bit sigma delta ADC. Theoretically, the concept can be expanded to achieve even higher resolution by increasing the oversampling rate and using more involved external support circuitry. The paper reviews the theory of operation for a sigma delta ADC, explores techniques to simplify the concept, and adapt the concept to a microcontroller environment.

2.0 Theory of sigma delta ADC

A sigma-delta converter consists of a sigma-delta modulator that is essentially a high speed, low resolution ADC, and a digital signal processing stage that trades time for resolution and filters the output of the modulator. The modulator stage samples the analog signal at a large oversampling rate. In this stage, the difference between the input and the output signals is generated and integrated within one or more feedback loops. The output of the integrator is routed through a one-bit quantizer. At efficiently high oversampling rate, the signal change between successive samples is so small that a simple binary quantizer (1 bit converter) can be used. The Nyquist rate is the minimum rate, fs, at which a quantizer must sample the analog input (bandwidth fb) to prevent aliasing. The Nyquist rate is equal to twice the bandwidth of the analog input (fs=2xfb). When a quantizer samples at frequencies higher than the Nyquist rate, the digitized input can be faithfully converted back into a continuos analog signal. The sigma-delta converter samples the input signal at many times the Nyquist rate, thus the term “oversampling”. The output of the quantizer is a serial bitstream (pulse density modulated) with the high sampling frequency f_S. This serial bitstream representing the input signal is passed to a “decimation”, or rate reduction, filter

In the digital domain which averages the values and produces n-bit result at lower frequency (Nyquist sampling or at a higher frequency). A digital filter contained in the decimation stage is to suppress the high frequency noise produced by the quantizer.

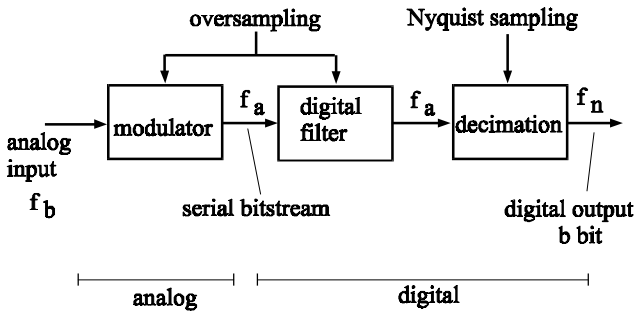


Figure 2-1. Building Blocks of a Sigma Delta Converter

2.1 Modulator

Figure 2-2a shows the block diagram of a sigma delta modulator. The difference (Δ) between the analog input and the comparator's previous output in integrated (∑) in such a manner that the average of the digital output is equal to the analog input. The ones and zeros of a modulator output represent the comparator's positive and negative full scale, respectively. For example, a modulator output of 1, 0, 1, 1, 1, 0, 0, 0, 1, 0, represents an analog input half way between positive and negative full scale (5 out of a possible 10 ones).

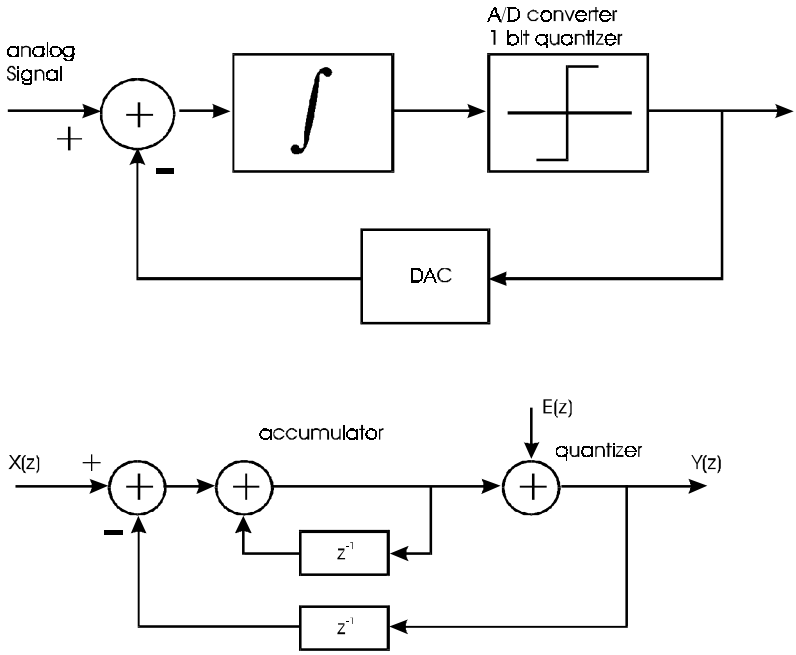


Figure 2-2. Principle of Sigma Delta Modulation a) Building Blocks b) Time Discrete Representation

Output signals are produced at discrete times. The simplest implementation is based on a first order integrator (Figure 2-2b). In Z-domain it represents an accumulator with transfer function:

$$H(z) = \frac{1}{1 - z^{-1}}$$

The quantizer is a non-linear system. For the sake of simplifying the analysis, a linear model of 1- bit ADC is used. Because of the crude approximation made by the comparator of a ∑Δ modulator, a large amount of noise is introduced into the system. This noise can be described as white noise E(z) which is spread out equally over the frequency spectrum. A sine wave input signal power density spectra $S_E(f)$ of the noise depends on the quantization step (Δ).

$$S_E(f) = \frac{1}{f_a} \cdot \frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12 f_a}$$

A quantizer produces white noise only if the following assumptions are met:

- Signal amplitude has to be large relative to the quantization step Δ. This means all quantization steps are really used.
- Input signal is always active, which means all quantization steps are gone through very often.
- Quantization error "e" is moving between -Δ/2 and +Δ/2. Then all values occur with the same probability and quantization error and seem independent of the input signal.

For low frequency signals ($f_b << f_s$), these assumptions are not met, because the real system properties are poorer than what the linear theory predicts. However, the linear model is still an effective tool that can be used to calculate modulator parameters and estimate performance limits.

The feedback loop of the modulator output signal contains a delay of one clock period. In Z-domain the modulator output signal (Figure 2-2b) can be described as:

$$Y(z) = \frac{H(z)}{1 + z^{-1} H(z)} X(z) + \frac{1}{1 + z^{-1} H(z)} E(z) = X(z) + \left(1 - z^{-1}\right) E(z)$$

The input signal X(z) is transmitted to the output with a signal transfer function W(z) = 1 (all pass filter). There is no deformation of the signal spectrum. The quantization noise E(z) is transmitted to the output with noise transfer function $N(z) = 1-z^{-1}$.

In the frequency domain, it is represented as a first order high pass filter (HP1) with characteristics shown in Figure 2-3. Shown also is the noise shaping effect being enhanced by increasing the order of a $\Sigma\Delta$ modulator (adding more integrators). The quantization noise contained in the output signal acquires strong frequency dependence. Due to large oversampling, a greater portion of the noise is shifted to frequencies much higher than the signal bandwidth f_b, which can be filtered through a high pass filter, while the input signal is passed unattenuated at low frequencies. The high-pass function shifts the quantization noise out of the baseband.

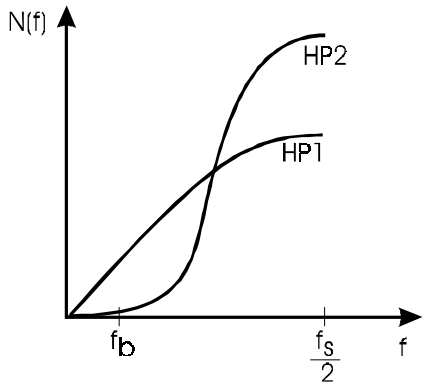


Figure 2-3. Noise Transfer Function

Figure 2-4 shows the timing behavior of integrator output and the binary output of a first order modulator with oversampling rate of 64. The integrator's output oscillates around the comparator's threshold value. Direction and gradient of the integrator output signal is determined by the difference between the analog input and the output of the 1-bit DAC contained in the feedback loop. The digital out changes when the integrator output crosses the comparator's threshold value, causing change to the integration direction. The analog value of the output signal represents the input voltage in the range (U_{Imax} to U_{Imin}). The larger the input voltage, the more "1" values come out of the converter. At low input voltages, "0" values dominate. If the input voltage is at the center, the output value is changed from a 0 to 1 or 1 to 0, depending on what the initial value is. Due to the integrating nature of the modulator, the average value of the output bit stream corresponds to input voltage. Consistency and precision of ADC output, effects the absolute precision of the created average value.

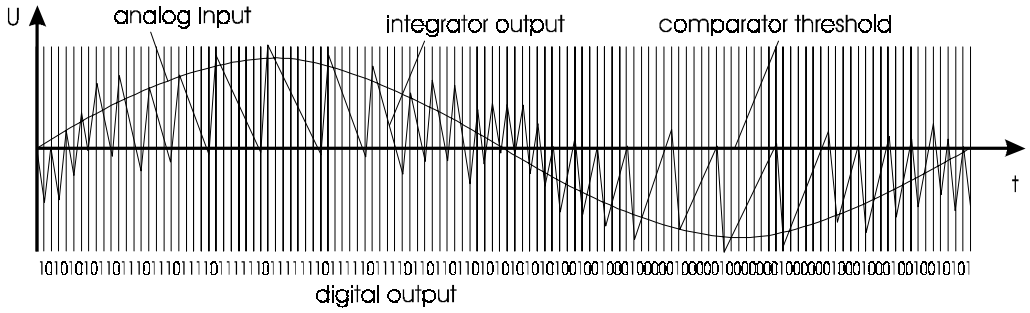


Figure 2-4. Signals in a First Order Sigma Delta Modulator

The signal to noise ratio SNR of the modulator output signal improves with increase in modulator order and the oversampling rate (OSR).

$$SNR_{\max} = 10\lg\left(\frac{3(2n+1)}{2\pi^{2n}}\right)dB + (2n+1)\cdot 10\lg(OSR)dB$$

To analyze the signal to noise ratio, the ratio is compared with the value obtained from an ideal DAC. This value is also called the dynamic range (DR) of a signal. It is calculated as the logarithmic difference between a signal with largest and smallest digital signal value.

Signal power of a sine wave signal with amplitude

$A = 2^{b-1}\,\Delta$, where Δ is quantization step, is:

$$P_S = \frac{A^2}{2} = \frac{\left(2^{b-1}\Delta\right)^2}{2}$$

Noise power of an equally distributed random signal like white noise can be expressed as:

$$P_R = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12}$$

Signal to noise ratio is:

$$DB = SNR_{\max} = 10\cdot\log\left(\frac{P_S}{P_R}\right) = b\cdot 6{,}02\ \text{dB} + 1{,}76\ \text{dB}$$

The relationship is shown in Figure 2-5.

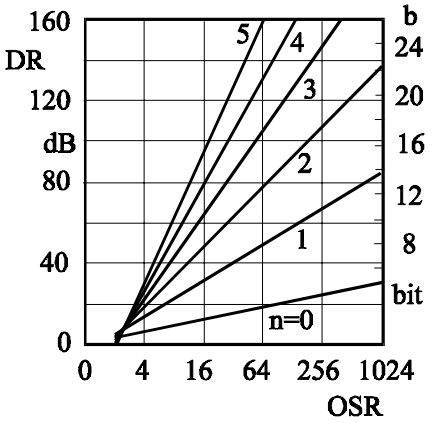


Figure 2-5. Dynamic Range of a Sigma Delta Modulator

As shown in Figure 2-5, to implement an 8- bit ADC with first order modulator, an oversampling rate of 64 is required.

2.2 Digital filter

The digital part of a sigma delta converter consists of a low pass filter to suppress high frequencies quantization noise and a decimator to reduce sampling frequency of the output signal up to twice the bandwidth of the input signal. The decimation factor "m" must be smaller or equal to the oversampling rate (m ≤ OSR). In simplest way, the low pass filter can be used to generate a moving average of the modulator output.

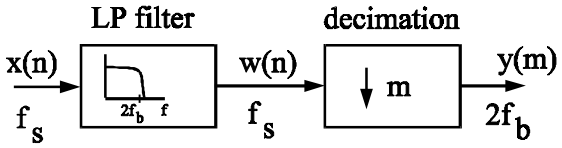


Figure 2-6. Digital Portion of a Sigma Delta Converter

One of the hardest concepts of sigma-delta converters to grasp is how a one bit modulator output is converted into an 8, 12, etc., output words. To achieve resolutions of greater than one bit, the modulator must be decimated. Through decimation, time may be traded for increased resolution. With decimation process, the modulator output is grouped into blocks bit samples. The ones and zeros in each block are summed, and values of one or zero is assigned to each block, depending on the total number of ones and zeros.

The possible "b" value achieved is limited by noise created in the digital filter and decimator. Noise has to be so small that the least significant bit must represent true information. An order k of a low pass filter must have the value k = n+1 (n is the modulator order) to make signal to noise ratio in digital section not worse than that of the modulator.

2.3 Moving Average Calculation

Transfer function of k-th order moving average over "m" sampling points with decimation factor m, can be described in Z-domain as:

$$H_{Si}(z) = \left[\frac{1}{m} \frac{\left(1 - z^{-m}\right)}{\left(1 - z^{-1}\right)} \right]^k$$

At multiples of decimator output frequency $f_D = f_s/m$, this transfer function has zeros. This function is specially effective for suppression of disturbances (Figure 2-7).

However, the relative flat frequency response is disadvantageous in the initial region of the transfer function 0 < f < f_D. Only for f_D values much larger then signal bandwidth f_b, the spectral signal influence remains small.

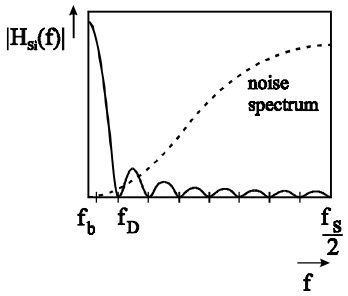


Figure 2-7. Frequency Response of si-function

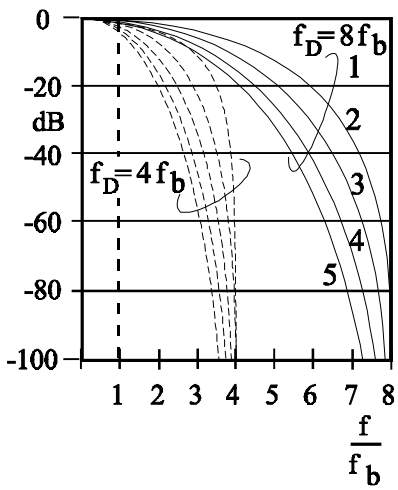


Figure 2-8. Initial Section of si-function with Different Orders

With a fourfold decimation, the maximum signal damps of a first order sigma delta ADC amounts to 0.91 dB (Figure 2-8). At $f_D = 8\ f_b$ this value is still 0.22 dB. Problems are also caused by stopband damping at frequency f_D - f_b. This damping is responsible for introducing aliasing into signal band at decimation. In this example, the values are 10.4 dB and 17.08 dB respectively. A moving average of small order is useful only if decimation frequency f_D is much higher than the input signal bandwidth. In all other cases, a much higher order filter must be used. Higher order filters will complicate the filter algorithms and will also limit the sampling frequency.

3.0 Sigma Delta Converter Implementation with SX

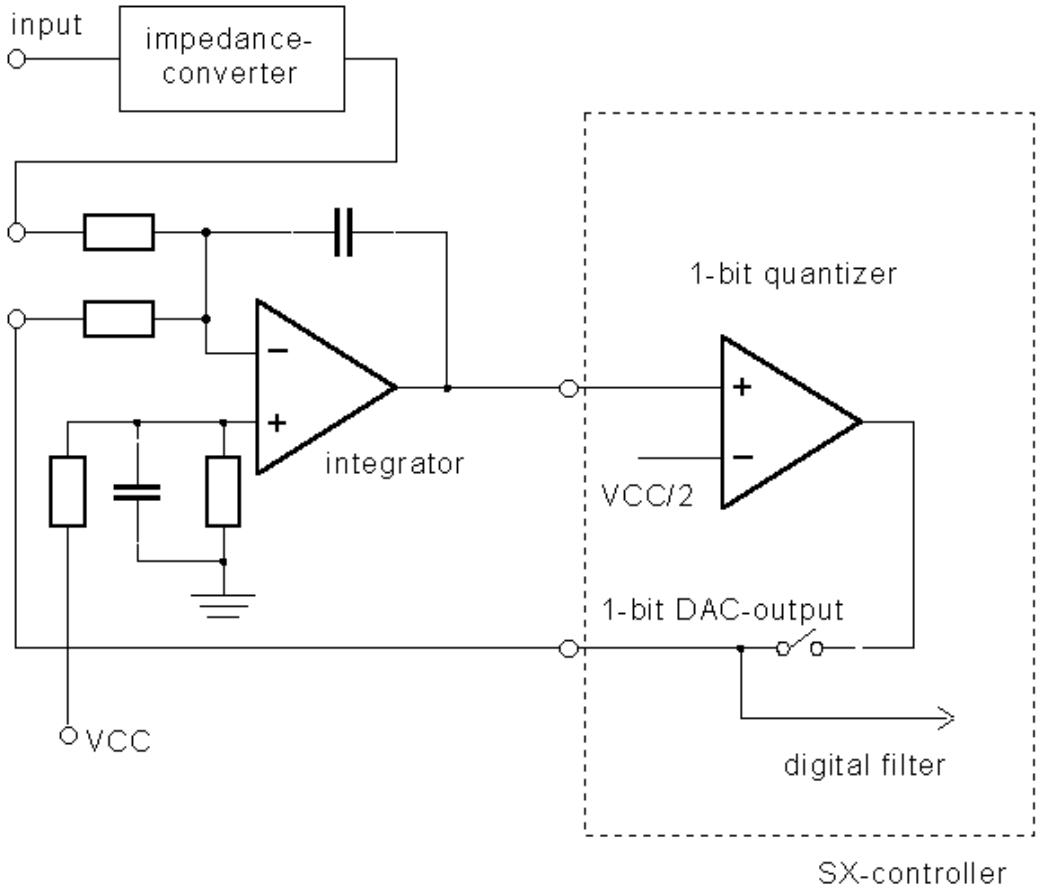
The high performance SX communications controller allows efficient implementation of a sigma delta converter as a software module (Virtual Peripheral™). The enhanced throughput (100 MIPS performance at 100 MHz) combined with deterministic interrupt response provides high speed sampling of an input signal. Sigma delta functions such as modulator, digital filter, and decimator can all be implemented as part of a jitter free interrupt routine with minimal external hardware overhead. The rest of this paper presents a practical SX based implantation of a sigma delta converter.

3.1 Sigma Delta Modulator

The SX implementation uses a first order modulator. Figure 3-1 shows the circuit diagram based on using an external opamp as the integrator. The 1-bit quantizer is simply using an input pin configured for CMOS input level. The 1-bit DAC function is implemented in software and use a single output pin. The precision of the modulator is mainly dictated by the resistors at the integrator input, consistency of the supply voltage, precision of the DAC output voltage. The integration capacity has to be stable for a short period only during the measurement period.

Since the frequency of the input signal is small relative to the sampling frequency, a sample and hold stage at the converter input is not necessary. An impedance converter (voltage follower) reduces the amount of load presented to the input signal. In addition, if the impedance converter is not present, the internal impedance of the input signal influences the transfer characteristic of the converter (gain). This internal impedance must be added to input impedance of the converter. If non-linearities at the edges of the measurement can be tolerated, the integrator can be replaced by a simple RC combination as shown in Figure 3-1.

implementation of a first order Sigma-Delta-Modulator with operational amplifier:



simple implementation of a first order Sigma-Delta-Modulator:

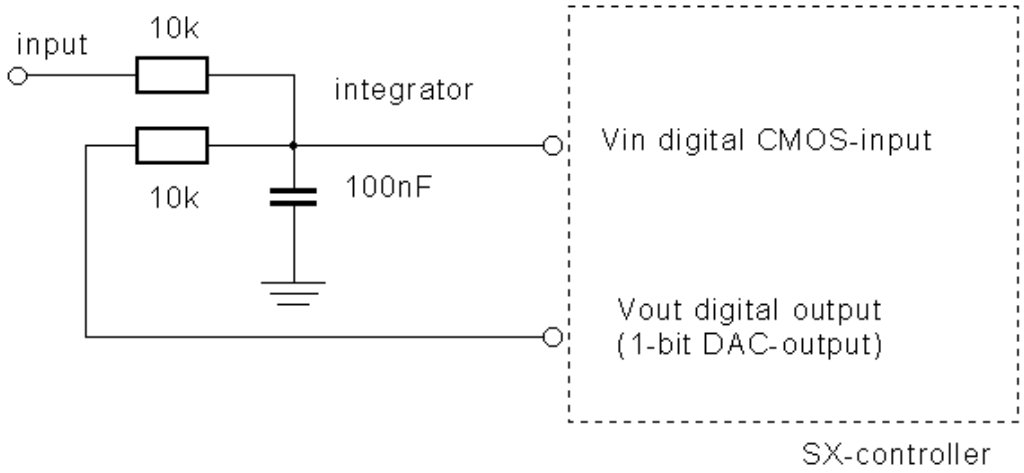


Figure 3-1. Sigma Delta Modulator a) with operational amplifier b) with RC network

3.2 Setup Observations

Figures 3-2 and 3-3 show the characteristics of the quantizer input. The threshold voltage is set at half the supply voltage (2.49 V) and has a hysteresis of approx. 2 mV. Undesired oscillation was observed when the threshold voltage was crossed at a very slow rate (milliseconds). This effect appeared only during measurement and was not observed during actual operation.

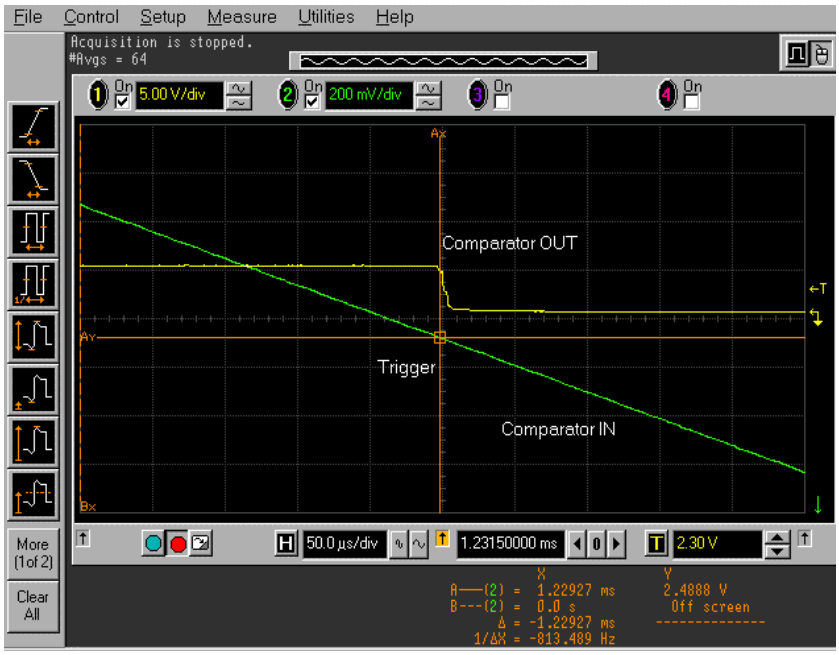


Figure 3-2. Transfer Characteristic of Digital CMOS Input with Linearly Decreasing Input Voltage

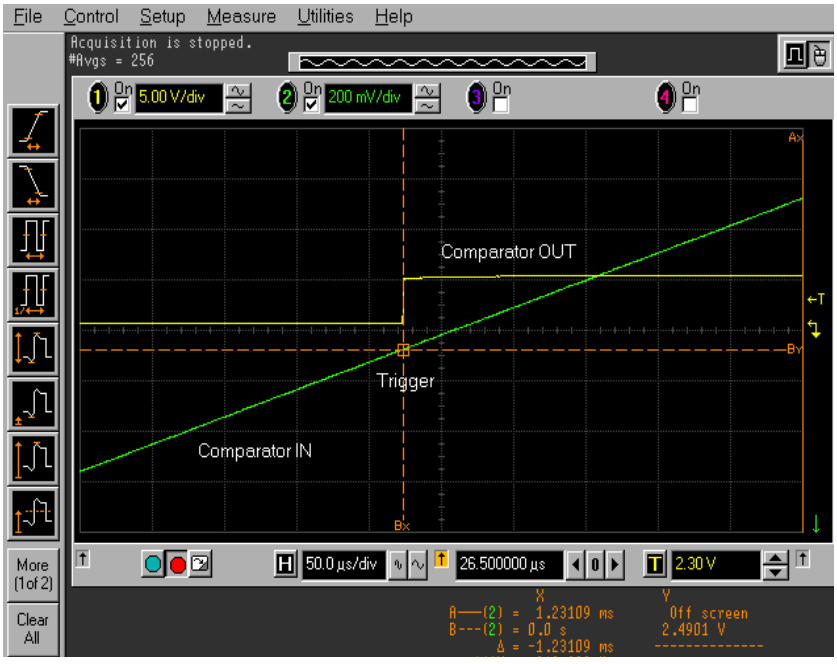


Figure 3-3. Transfer Characteristic of Digital CMOS Inputs with Linearly Increasing Input Voltage

The precision of comparator and DAC output is influenced by the quality of the reference voltage. This experiment relied directly on the SX supply voltage. A separate reference voltage was not used. Since the SX high operating frequency (50 MHz) generates higher current drain, a fair amount of supply voltage bounce was observed. Figure 3-4 shows peak to peak voltage bounce of amounts 276 mV on the SX Vdd pin

The influence of the supply bounce on system parameters can be partially compensated through fixed phase sampling that corresponds to the bounce. If the precision of the sigma delta modulator does not meet the application requirement, a separate reference voltage may be needed for the DAC output.

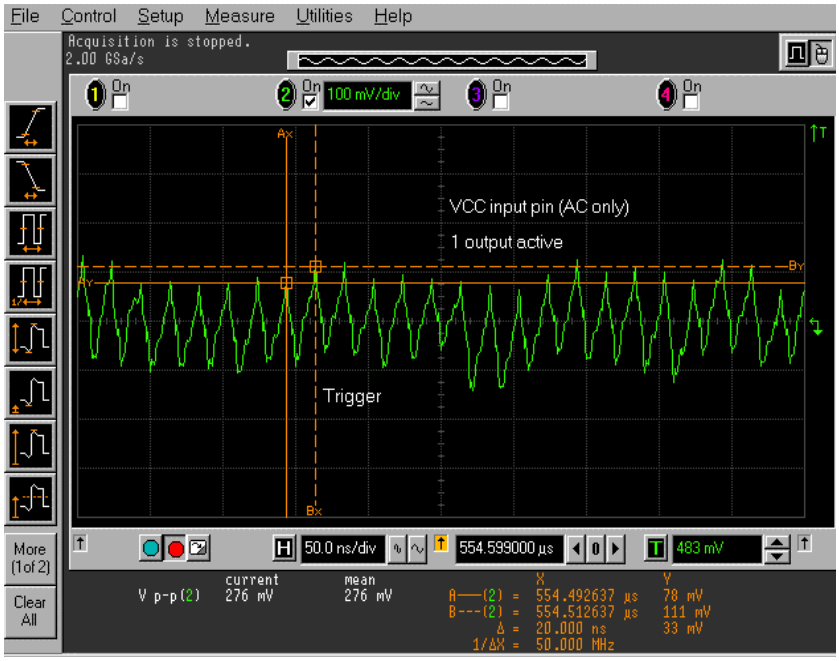


Figure 3-4. Voltage Bounce at Vdd Pin

Figure 3-5 shows the output pin voltage at high level. The average value is around 4.84 V with a voltage bounce of 385 mV. This small average value produces a systematic converter gain error.

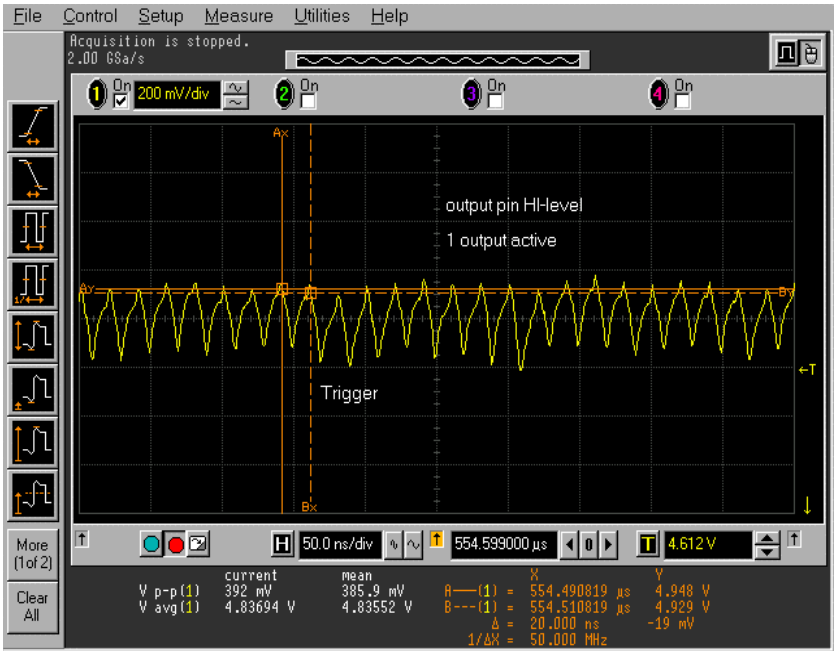


Figure 3-5. Output Voltage at High Level

Figure 3-6 shows the output pin voltage at low level. The voltage bounce level is the same, but the average value is nearly ideal.With the 1-bit DAC output signal present at the integrator input, the integrator output signal looks similar to the signal shown in Figure 3-6 output.

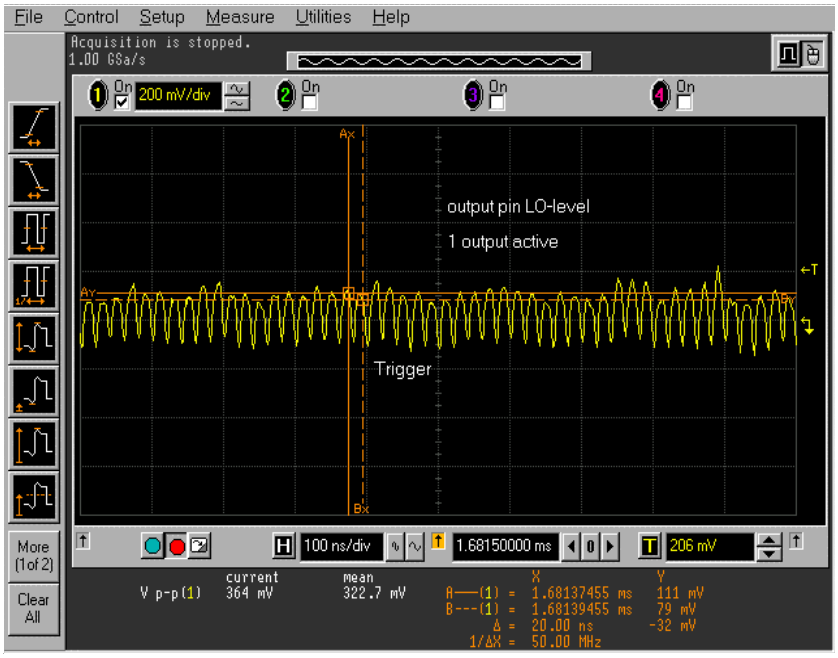


Figure 3-6. Output Voltage Low Level

An illustration of the signal characteristics is shown in Figure 3-7 for a sampling frequency of 30.6 kHz and a constant input voltage of 4 V.

A signal stroke of about 180mV is created at the integrator output containing the bounce shown earlier (the value varies around the threshold of 2.5 V).

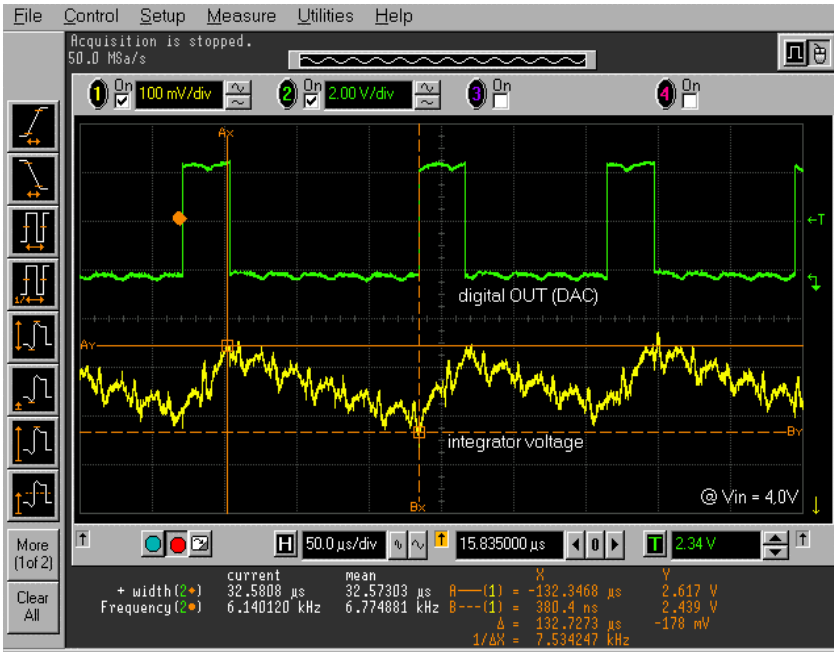


Figure 3-7. Integrator Voltage at 30.6 KHz Sampling Frequency

If the sampling frequency is raised to a realistic value such as 306 KHz, the signal stroke decreases to 20 mV (Figure 3-8). This level is enough to reliably switch the comparator . Sampling points are determined by software and are positioned 140 ns in front of the DAC output switching points. If the signal stroke is adequately small, the integrator behavior can be assumed to be linear.

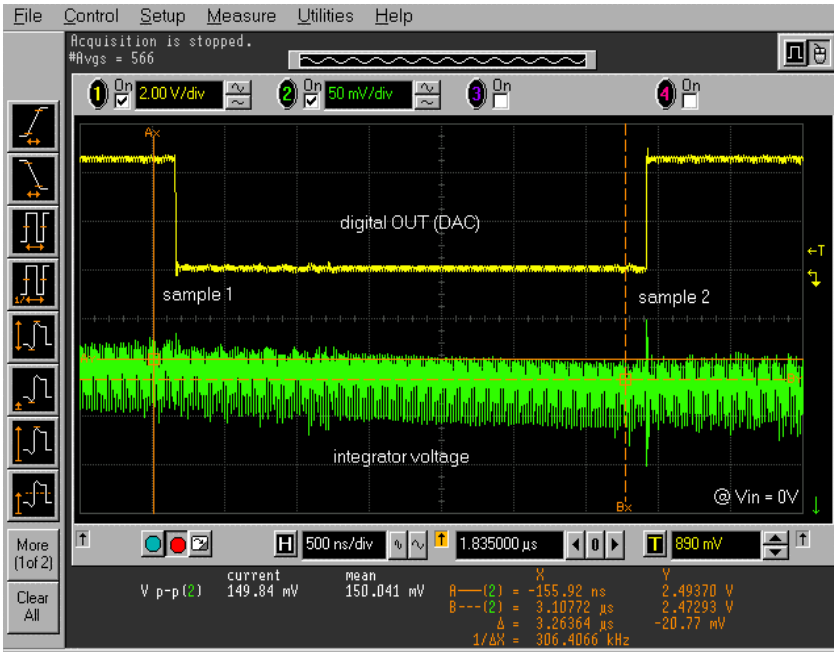


Figure 3-8. Integrator Voltage at 306 KHz Sampling Frequency

3.3 Definition of Parameters

To implement an 8- bit sigma delta ADC, an oversampling rate of 64 or more is necessary (Figure 2-5). The fact that a simplified linear model is used, higher oversampling rates will provide more accurate results. An oversampling rate of 2^8 , can be easily achieved with an appropriate software routine. Oversampling rates smaller than 2^8 require lower sampling frequencies, but the software routine demands a larger portion of the CPU time.

Theoretically, it is possible to increase the resolution of ADC by increasing the oversampling rate (e.g. 12 or 16 bit). In addition, higher orders of the modulator and digital filter may be required as well. Increased resolution will also decrease the useful signal bandwidth. To minimize the computation time of the digital filter, only a first order filter was used. Higher order filter need to be used if signal to noise ratio (Figure 2-6) and distortion of measured values at high signal frequencies (Figure 2-8) are not acceptable.

The distortion of measured values at high frequencies can be reduced if the digital filter and the decimator are divided into two separate stages. The first stage decimates only to twice or four times the Nyquist frequency. This defuses the problems of stopband and signal band damping. For the second stage, a higher order filter is needed (can operate at a much smaller sampling rate). It is possible to compensate the gain drop of the first stage at higher frequencies. If a bandwidth of half the Nyquist frequency ($f_d = 4xf_b$) is chosen, input signals of up to 300 Hz can be processed. With f_b = 300 Hz:

fn = 600 Hz

f_d = 1.2 kHz

f_s = 306 kHz

The decimation factor “m” is 256 at an oversampling rate of 512.

3.4 Software Considerations

Figure 3-9 shows a flowchart of the algorithm. The 1- bit quantizer and the digital filter are served in a jitter free interrupt routine. The routine reads the integrator voltage first (compare function) and then passes it out inverted through the DAC output.

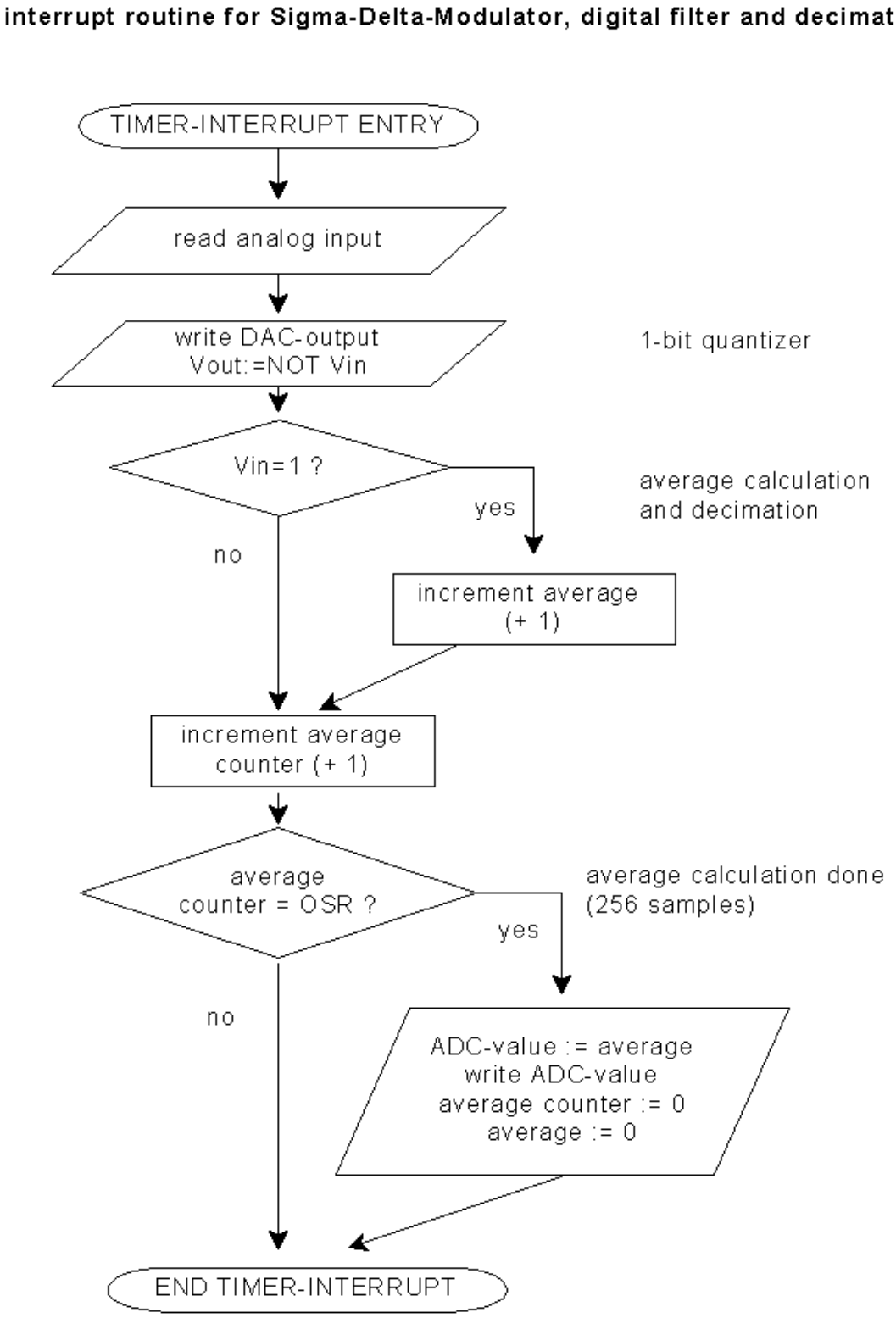


Figure 3-9. Software Routine

The routine calculates the moving average by adding 256 samples of the serial bitstream. Because the samples are 1s or 0s, the sum contains the average value. After 256 samples, a new converting cycle is started. This sample processing routine is executed at 240 ns. This results in a sampling rate of 1.2 KHz (after decimation). All peripheral components of sigma delta converter are addressed continuously at 3.26 µs intervals (interrupt routine execution time). The 3.26 µs translates to a sampling rate of 306.7 KHz.

The ADC characteristics in the frequency domain are determined only by the sampling frequency. If the RTCC interrupt rate is increased, sampling frequency is higher but calculation time for the software routine remains the same and more processor performance is needed.

3.5 Results

To determine the static transfer characteristic of the ADC, all measurement results are compared with values obtained from an industrial 12-bit ADC. Figure 3-10 shows the absolute error in digits as the input voltage is linearly increased from 0 to 4 V. The difference between input voltage and the measured value is plotted.

The systematic error (slope of error characteristic) is due to following:

- Low precision of the resistors used at the integrator's input
- Influence of the input signal internal impedance that is added to the integrator's input impedance

It is possible to suppress the systematic errors by using an input voltage follower and an external DAC output voltage and by equalizing the input resistances. Then the only disturbance that remains is noise.

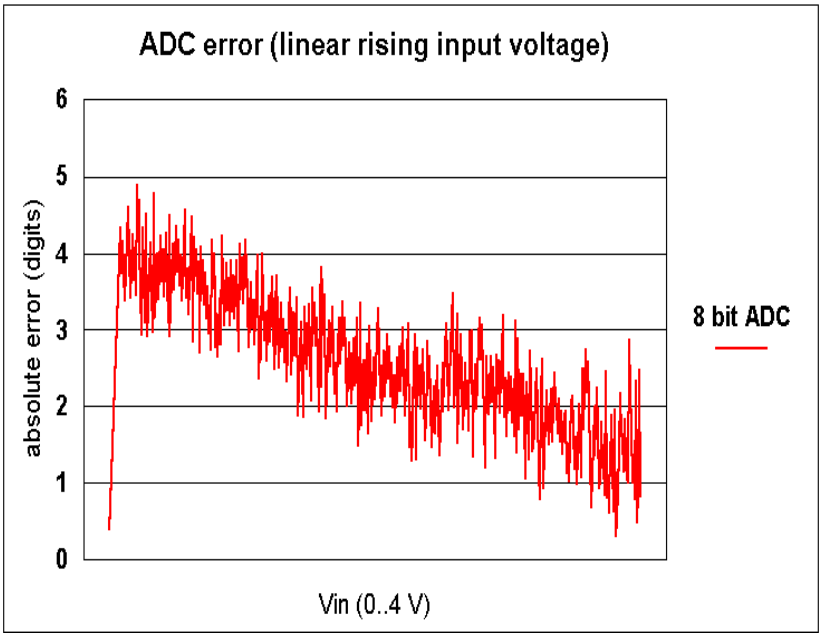


Figure 3-10. Absolute Error of 8 Bit Sigma Delta DAC in Digits (LSB)

Figure 3-11 shows the ADC noise error. The 1 to 2 LSB noise error is present due to the use of a first order modulator and a first order digital filter.

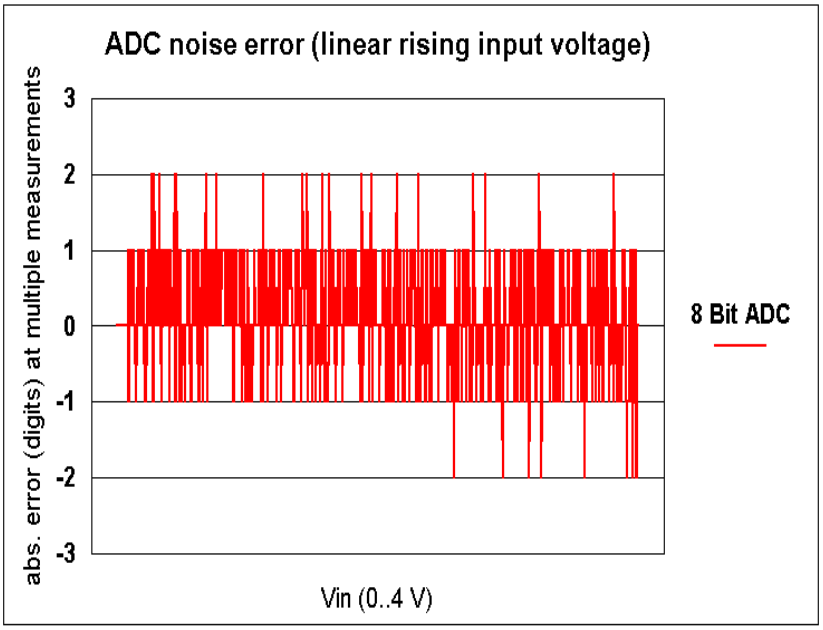


Figure 3-11. Absolute Noise of 8 Bit Sigma Delta DAC in Digits (LSB)

3.6 CONCLUSIONS

The high performance SX allows a simple and cost effective implementation of an 8-bit sigma delta ADC. With SX implementation, an accuracy of 2% can be achieved if systematic errors are compensated. Additional modifications of hardware and software are required to accomplish higher resolution and higher accuracy. Applications that do not demand high resolution and speed s (temperature compensation, sensors) can use the approach with its low cost and simple hardware.

3.7 References

Ardalan, S. H.; Paulos, J.J.: An Analysis of Nonlinear Behaviour in Delta-Sigma Modulators. IEEE Trans

Circuits and Sys., vol CAS-34, p. 593-603, June 1987.

Becker, S.: Entwurfskonzept für Sigma-Delta-A/D-Wandler. Diplomarbeit, Fak. Elektrotechnik, TU Dresden (Germany), 1996.

Candy, J.C.; Temes, G.C.: Oversampling Delta-Sigma Data Converters. IEEE Press, 1991.

Candy, J.C: Decimation for Sigma Delta Modulation. IEEE Trans. Commun., vol. COM-34, p. 249-258, Jan. 1986.

Gray, R.M.: Quantization Noise Spectra. Trans. Inform. Theory, vol. IT-36, p. 1200-1244, Nov. 1990.

Lüke, H. D.: Signalübertragung. Springer-Verlag, 1990.

Wurlitzer, Th.: µController mit virtueller Peripherie, Design&Elektronik, vol. 6/98 p.32-34.

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