AR_Hardware_518DS001_7SR5_Platform.docx

Product / Function: **7SR5 Native 61850**

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1 Introduction

There are currently two modern Reyrolle development platforms: 7SR1 and 7SR2.

The 7SR1 platform comprises two architectures:

- E4 case size with either Infineon TC1130 or NXP LPC4437 CPUs.
- S6 case size with an Infineon TC1130 CPU and with optional NXP LPC4337 slave processor for protection communication applications.

The TC1130 CPU part is now obsolete and the LPC4337 is unsuitable for native IEC61850, due to limited internal Flash memory and no cache for external memory.

The 7SR2 platform uses an Infineon TC1796 CPU and there are no suitable upgrades which have Ethernet capability which would make for a cheaper IEC61850 solution; currently an EN100 board has to be added. Despite an ongoing DTC exercise, the 7SR2 platform is still more expensive than the 7SR1 for a device with similar functionality.

A new platform development is therefore proposed which will provide IEC61850 functionality in S6 and S12 case sizes, which will be able to be expanded to cater for all of the relays in the 7SR2 range and also exceed it. The most basic relay in the range will have a BOM cost of €200. The platform is designated: 7SR5 Native 61850 and will use the product designation 518.

2 Requirements

There are two basic requirements for the platform refresh:

- Reduce the cost of a full-functionality IEC61850 device by at least 15%, with a target price of €200.
- Produce a platform that can be expanded with the addition of new modules, for example, to create a 3- or 4-winding Duobias.

The platform will also be improved with the following “stretch” requirements added:

- Graphical display, including mimic diagrams and non-English text
- Native IEC 61850
- Updated CT and VT inputs, increasing resolution and sampling speed
- New BI circuit, including AC handling and optionally basic voltage measurement
- Output contacts with higher current/inductive load rating
- Faster input and output response
- CE2016 compatibility
- Minimise number of PCBs and PCBA variants. Ideally one PCB per function and only one or two PCBA builds e.g. single fascia design for S6 and S12.
- Minimise number of test adapters e.g. one adapter to test both S6 and S12 fascias
- Reduce assembly cost – use plug-in cards which require no or minimal screws

The current requirement list is as follows:

Table 2-1 Requirements from PLM Backlog

Rank	Requirement ID	Description	Fulfilled
1	7SRn-HW-001	BOM TARGET + Must not exceed €200 for basic O/C with IEC 61850 low	Yes
2	7SRn-HW-002	HARDWARE ARCHITECTURE Device shall use a modular architecture with serial or parallel digital bus arrangement to enable additional PCB's to be added to device models at a later date without major re-design e.g. RTD, 4-20mA, Process Bus etc.	Yes
3	7SRn-HW-003	COMMON REQUIREMENTS + Conducted Immunity IEC 60255-25, IEC61000-4-6 + Fast Transient IEC 60255-26 (Zone A), IEC 61000-4-4 + High Frequency 1MHz Burst IEC 60255-26, IEC 61000-4-18 + Surge Immunity IEC 60255-26 (Zone A) IEC 61000-4-5 + IEC 61000-4-16: Power frequency – Zone A + IEC 60255-1	Yes
4	7SRn-HW-004	NATIVE 61850 + Electrical 61850 as standard + Option for fibre optic + All redundancy protocols (RSTP/HSR/PRP)	Yes
5	7SRn-HW-005-2	Withdrawable element: An integrated, ergonomic and robust method of element withdrawability to be provided.	Yes
6	7SRn-HW-068	Case Dimensions: To allow installation, withdrawability and operation within same 'En x 4U' panel space used by 7SG/7SR relays.	Yes
7	7SRn-HW-005-1	WITHDRAWABLE Element Interlock: S6 & S12 withdrawable element to be securely located for mounting angles up to negative 45 degrees.	Yes
8	7SRn-HW-006-1	FASCIA Layout S6 & S12 fascias to have a common layout.	Yes
9	7SRn-HW-006-2	FASCIA Pushbuttons 5 Standard Keys + 2 Control keys.	Yes
10	7SRn-HW-006-3	FASCIA Pushbutton durability Product lifespan is 20 years, pushbutton durability to be consistent with this.	
11	7SRn-HW-006-4	FASCIA Graphical LCD 50 x 50 Graphical LCD suitable for displaying a graphical mimic diagram vertically.	Yes
12	7SRn-HW-006-5	FASCIA LCD To provide user adjustable contrast and backlight settings	Yes
13	7SRn-HW-006-6	FASCIA USB Port	Yes

Rank	Requirement ID	Description	Fulfilled
		Front USB port to be provided for local data comms	
14	7SRn-HW-006-7	FASCIA USB Port Data transfer rates shall be higher than those achievable with the 7SR1/2 relays	Yes
15	7SRn-HW-006-8	FASCIA LEDs Minimum of 20, 32 preferred tri-colour LEDs on both S6 & S12.	Partial. 28 tri-colour LEDs
16	7SRn-HW-006-9	FASCIA LED Labels User definable slip-in labels or software labels also acceptable.	Yes
17	7SRn-HW-006-10	FASCIA LED Labels Access If there are slip-in labels, case design to facilitate LED label removal and replacement without tools and with no requirement to withdraw the relay element.	Yes
18	7SRn-HW-006-11	FASCIA Relay labelling case/fascia design to allow labelling in accordance with IEC 60255-27	Yes
19	7SRn-HW-018	CASE Contacts Durability Contact integrity to be maintained for > 1000 removal/insertion operations. Contact design to allow any element to be inserted into any compatible case.	Yes
20	7SRn-HW-019	CASE Contacts CT Shorting All CT inputs and normally closed contacts to be automatically short circuited at the case when the relay element is withdrawn	Yes
21	7SRn-HW-007	CURRENT INPUTS + From 0 --> 16 Current Inputs + Standard Measurement up to 15th Harmonic + Special Measurement up to 50th Harmonic for Capacitor Relay. + Phase & Earth Inputs 15th Harmonic, 0.005-50 xIn + High accuracy differential CT inputs + Sensitive Earth Fault Inputs 0.001-5 xIn + 100 x In for 1 second + < 0.1 VA burden (1A) + < 0.3 VA burden (5A)	Partial 0.005xIn phase range unknown
22	7SRn-HW-008	VOLTAGE INPUTS + From 0 --> 8 VT inputs + 40-160V + 300V 10 seconds/continuous + < 0.1VA @ 110V burden	Yes
23	7SRn-HW-009	BINARY OUTPUTS + Options up to approximately 20 Binary Outputs + ENA TS 48-4 + IEC60255-1	Yes
24	7SRn-HW-010	BINARY INPUTS *Universal binary inputs with settable thresholds *Options up to a minimum of 40 binary inputs + ENA TS 48-4	Yes
25	7SRn-HW-070	BI nominal voltage: 24/110/220V dc 'High' level >80% Vn, 'Low' level <40% Vn ??V ac BI quantities derived from (separate) PCBA proposals	Partial 15, 75, 160V levels
26	7SRn-HW-011	COVER REMOVAL Remove need for plastic cover whilst maintaining or improving IP rating	Yes
27	7SRn-HW-012	INTERNAL WIRING + Internal wiring should be kept to a minimum and be restricted to PCBA assembly in Goa factory. + No wiring should be required at final assembly in assembly locations around the world.	Yes
28	7SRn-HW-013	THROUGH HOLE COMPONENTS + All through hole components (including fingers if fitted) must be mounted on the same side of the PCB	Yes
29	7SRn-HW-017	MODULE DESIGN All modules should be, wherever practical, re-usable in all standard case sizes to maximise future product options. Principle - "any module fits in any position".	Yes
30	DTC_FY16_0188	Terminal block redesign + Designed to improve HK / assembly times + Reducing number of flying lead connections + New terminal block arrangement, making it easier to assemble and reduce cost + Mechanical fixing of the block to case to be simplified - no screws	Partial No screws might not be possible

Rank	Requirement ID	Description	Fulfilled
		+ Block assembled in Goa or externally	
31	DTC_FY16_0189	CT/VT card redesign + Reuse of designs and components from Siemens design library + SIP5 CTs and analogue circuits + Easier to assemble, using captive/potted mouldings for the CTs + Reduce number of flying leads, none for the VTs	Yes
32	DTC_FY16_0190	CPU card redesign + New cheaper processor, that has more support for low cost memory and storage technologies + Removal of SD card	Yes
33	DTC_FY16_0191	Integrated IEC61850 + Saving the cost of the EN100/EN100+	Yes
34	DTC_FY16_0192	Digital I/O redesign + Programmable BI range will reduce the number of card variants by 50% + Reuse of designs and components from Siemens design library - Cheaper BO circuit	Yes
35	DTC_FY16_0193	Fascia redesign + Reduce manual operations to improve assembly and HK + Optimise the number of slip in pockets and labels + Reuse of designs and components from Siemens design library - Cheaper LEDs/switches + Simple to mount LCD + Standardise light pipes	Yes
36	DTC_FY16_0194	Front cover removal + Remove front cover to save material and HK, and integrate functionality into fascia design	Yes
37	DTC_FY16_0195	Integrate handles + Integrate the handles into the case or fascia wrap	Yes
38	DTC_FY16_0196	New case design + New lower cost case + Inner mechanical housing to be plastic + Outer case to use standard Siemens case materials (if cheaper) + Plug in cards to minimise assembly - reduce the number of screws and brackets	Partial Inner mechanicals still metal.
39	7SRn-HW-018-1	CASE Enclosure IP Rating + IP52 minimum, IP54 preferred. + Previous KEMA 7SR tests certified cases as front IP5x, all other aspects IP21 (all gaps <1mm).	No
40	7SRn-HW-018-2	CASE Earthing All required terminal and case earth connections to be identified	Yes
41	7SRn-HW-062	Fascia Layout: S6 fascia will be standard design, S12 etc. Will consider future requirements for additional LEDs, 'function keys' etc.	Yes
42	7SRn-HW-019	Standard Data comms - Front USB port	Yes
43	7SRn-HW-020	Standard Data comms - Rear RS485 serial port	Yes
44	7SRn-HW-021	Standard Data comms - Rear RJ45 Ethernet port	Yes
45	7SRn-HW-022	Optional Data comms - Rear optical Ethernet port	Yes
46	7SRn-HW-023	Hardware to support enhanced fault monitoring and diagnostics 7SR2 functionality and additional A/D monitoring etc.	Yes
47	7SRn-HW-024	Hardware construction to facilitate 0, 4, 8 or 12 CT inputs dependent on relay functionality	Yes
48	7SRn-HW-025	Current Inputs suitable for 1A/5A CT secondary's	Yes
49	7SRn-HW-026	Current Input measuring range 0.005 - 50 x In As per 7SR5-HW-007.	Partial. 0.005xIn may not be possible
50	7SRn-HW-027	Current Inputs thermal rating: 4 x In continuous 100 x In for 1 second	Yes
51	7SRn-HW-028	Current Inputs instrumentation accuracy 1% or ±1% In (0.1 - 2 In)	Yes
52	7SRn-HW-029	Hardware construction to facilitate 0, 4 or 8 VT inputs dependent on relay functionality	Yes
53	7SRn-HW-030	Voltage Inputs suitable for 40 - 160V nominal operation	Yes
54	7SRn-HW-031	Voltage Inputs measuring range 0 - 300V	Yes

Rank	Requirement ID	Description	Fulfilled
55	7SRn-HW-032	Voltage Inputs thermal rating:300V continuous	Yes
56	7SRn-HW-033	Voltage Inputs instrumentation accuracy 1% or ±1% Vn (0.1 - 1.2 Vn)	Yes
57	7SRn-HW-034	Auxiliary supply nominal voltage 24, 48, 60, 110, 125, 220, 250V dc 100, 110, 115, 120, 200, 230V ac	Yes
58	7SRn-HW-035-1	Auxiliary supply operate range 80 - 110% Vn	Yes
59	7SRn-HW-035-2	Auxiliary supply capacity It is preferred that all outputs can be continuously energised simultaneously. Any operational limits to be stated.	Yes
60	7SRn-HW-036	Minimum I/O combination + The minimum I/O possible using the minimum spec hardware is 3BI & 4BO. + However, the preferred number for a device would be 8BI & 6BI.	Yes
61	7SRn-HW-039	Standard binary output Rating >= 300V	Partial Resistive break only, 0.15A max.
62	7SRn-HW-040	Standard Binary output rating These to be suitable for CB trip duty i.e. As specified in IEC60255-1	Yes
63	7SRn-HW-045	Certification: CE Marking (compliance with applicable EC directives).	Yes
64	7SRn-HW-046	Certification: RoHS 2	Yes
65	7SRn-HW-047	Certification: 2014/30/EU (EMC Directive)	Yes
66	7SRn-HW-048	Certification: 2014/35/EU (Low voltage directive)	Yes
67	7SRn-HW-049	Certification: EN60950 (LV safety directive)	Yes
68	7SRn-HW-050	Certification: EN50178 (Electronic equipment for use in power installations)	Yes
69	7SRn-HW-051	Certification: EN61010-1 (Safety requirements for electrical equipment)	Yes
70	7SRn-HW-052	Certification: EN61508 (Functional Safety of Electronic Safety Related Systems including SIL categories)	Yes
71	7SRn-HW-053	Certification: IEC60694 (Common specifications for HV switchgear and control standards)	Yes
72	7SRn-HW-054	Certification: ISO9001 (Quality management system)	Yes
73	7SRn-HW-055	Compliance: IEC60255-1	Yes
74	7SRn-HW-056	Compliance: IEC60255-26	Yes
75	7SRn-HW-057	Compliance: IEC60255-27	Yes
76	7SRn-HW-061	Method of terminal shrouding to be defined + At higher PSU voltage levels some customers require exposed terminal at rear of relay to be shrouded allowing safe working practices.	No
77	7SRn-HW-062	Method of terminating cable sheaths/screens to be defined For example, Screened cabling recommended for RS485, RJ45, temperature inputs.	Yes
78	7SRn-HW-071	Binary Outputs: + BO quantities derived from (separate) PCBA proposals + Requirement is in line with the present proposal to use the Siprotec BO. This is proposed to ensure compliance with the essential considerations of project timescales and hardware test performance.	Yes

3 High-level view

A device can be broken down into several distinct modules. The diagram below shows the breakdown of the high level modules that make up the internal removable device of an S6 relay.

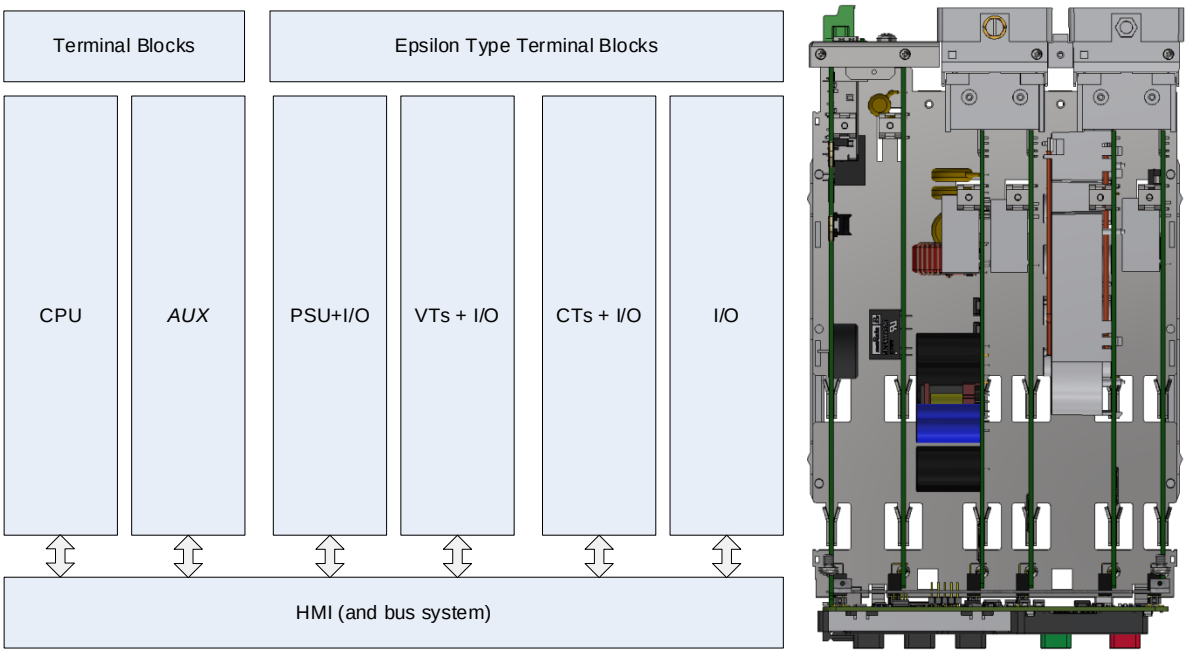


Figure 3-1 High level device architecture

The following sections will give a brief overview of each module; more detailed information on the modules can be found in Section 12 - Functional blocks.

3.1 Outer Wrap

A new design of outer wrap for the S6 and S12 builds will be implemented in order to achieve a higher IP rating, as well as provide a more convenient connection to the earth terminal on the power supply.

Initially only S6 and S12 case sizes will be available, thus minimising the number of hardware variants. If there is a market demand, S8 or S10 devices may be produced as part of a future project.

3.2 Internal Device

Metal top and bottom plates will be used to provide the main mechanical structural strength to the internal removable device. These plates will be designed to minimise assembly complexity.

In general, the internal device will be divided into E2 slots and each slot will have two connectors to access the bus system on the fascia card.

For maximum flexibility, any card (or card combination) should be capable of being plugged into any connector on the fascia card, subject to mechanical limitations e.g. PSU transformer or bulk storage capacitor height may fix the PSU position.

The terminal blocks will be an updated version of the existing Epsilon terminal block which provide vertical CT shorting. This is needed to eliminate the wiring from the CT primaries to the terminal blocks.

Where the CPU and optional card are positioned, there will be a metal blanking plate and various types of connectors mounted therein: RJ45, SFP, Phoenix type etc.

The internal device will be withdrawable. It is accepted that Disconnection of communications leads before withdrawal may be required.

The internal device will be optimised for production and simple assembly, minimising the number of screw fixings needed.

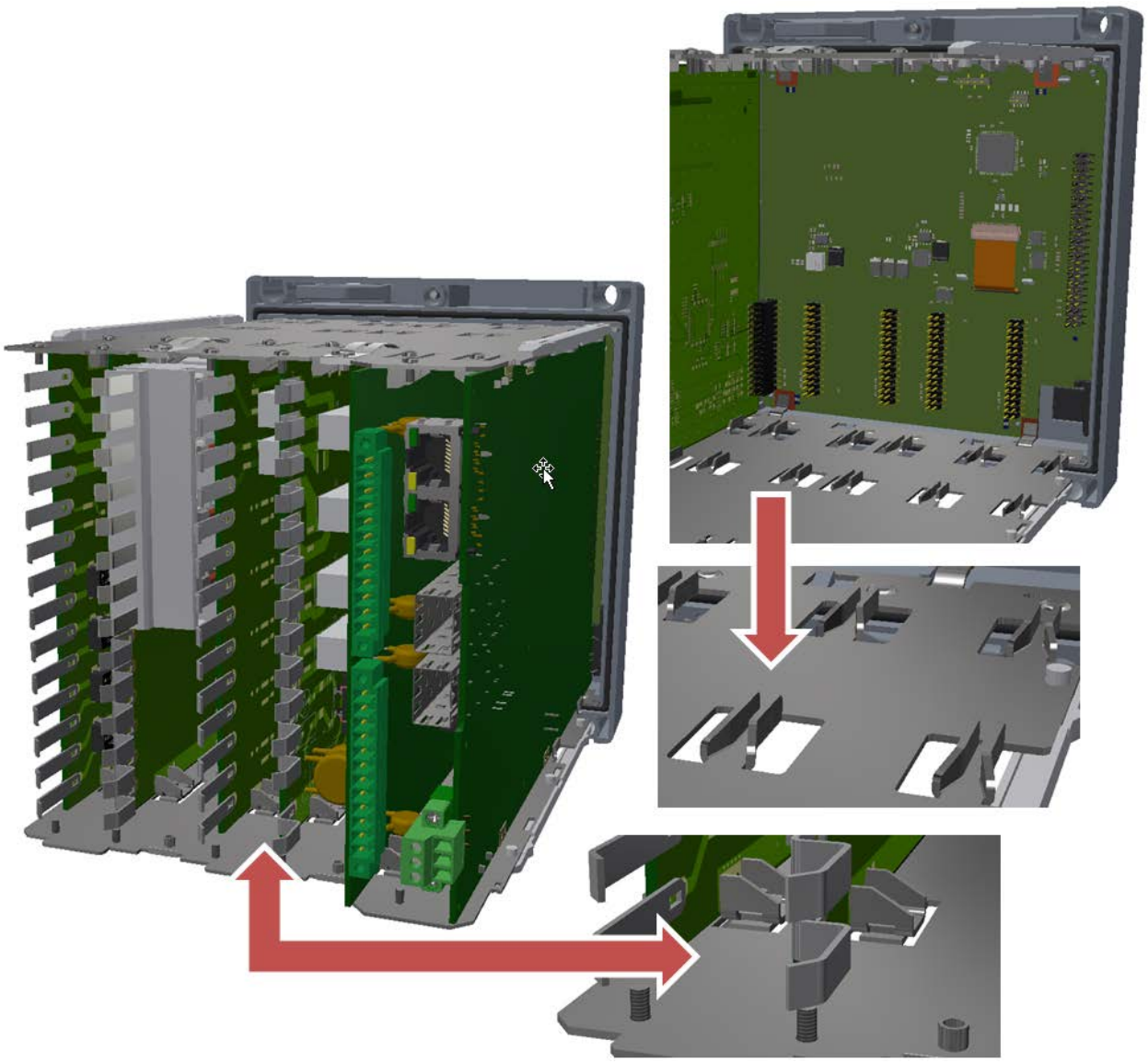


Figure 3-2 Card slots and fixings

Here, PCB guides are formed into the top and bottom plates to help the assembly process, and only two screws are required to fix each PCB into place, as well as provide good earthing points.

3.3 CPU

The CPU will be mounted on a card on the left, as viewed from the front panel. The main processor will be a NXP i.MX6SX dual core device, see **/1/.**

It will provide dual redundant IEC61850 connections in either fibre or electrical and a single RS485 channel (3 terminals only).

A front USB port for the user will be provided, which will protrude through the fascia moulding.

3.4 Modules

Each module will feature a small microcontroller that will be responsible for communicating with the main CPU card, and it will control all aspects of the card's functionality.

Data can then be passed to the main CPU card using a common dual SPI bus interface. This will allow for an open and expandable architecture that can handle future requirements.

3.4.1 Auxiliary Card

The architecture allows for future communications or protection cards that can be mounted next to the CPU card. Examples include:

- Line-diff protection communications options added as a daughterboard to the CPU card, or
- RS485, RTD inputs, 4-20mA inputs/outputs, arc detection or a Process Bus card as a plug-in module.

3.4.2 PSU card

This is a universal power supply that will span all input voltage ranges (24-220VDC, 115/230Vac).

The initial design already exists and is being implemented on the 7SR1 and 7SR2 during the FY17 period.

Binary outputs will be included to maximise terminal block use.

3.4.3 CT Card

There may be two CT input cards required.

- A high accuracy (HA) card that is intended to be used on the transformer differential and other high-end relays will be offered first.
- A cheaper design suitable for overcurrent use may be developed at a later date.

Both cards will contain 4 CT channels and binary inputs.

3.4.4 VT Card

There will be one design of VT input card, which will have 4 VT channels and a mix of binary inputs and outputs.

3.4.5 IO Card

This will be one Standard I/O card, which will fit in various locations on the device. It will contain a mix of binary inputs and outputs.

3.4.6 Fascia Card

There will be one common fascia design for both the S6 and S12 fascia cards. The S12 fascia will only extend the bus system and will not provide extra LEDs or Keys.

The fascia card will maintain the familiar Reyrolle user interface by having five buttons – Up, Down, Enter, Cancel and Test/Reset. Two further buttons will provide Open and Close functionality for use with the mimic display.

A large graphical display will be used, offering 128x128 pixels, which should equate to 21x16 characters.

The fascia will include 28 tri-coloured LEDs.

The fascia will use a plastic moulding, removing the need for a clear plastic cover. The fascia will provide an easily accessible area so that the user can fit a label which describes the functions of the 28 LEDs.

3.5 Cost Position

The aim is to increase the functionality of the product whilst decreasing the manufacturing cost of the relay. The comparison of cost vs. I/O for 7SR1, 7SR2 and 7SR5 Native 61850 is shown in Figure 3-3:

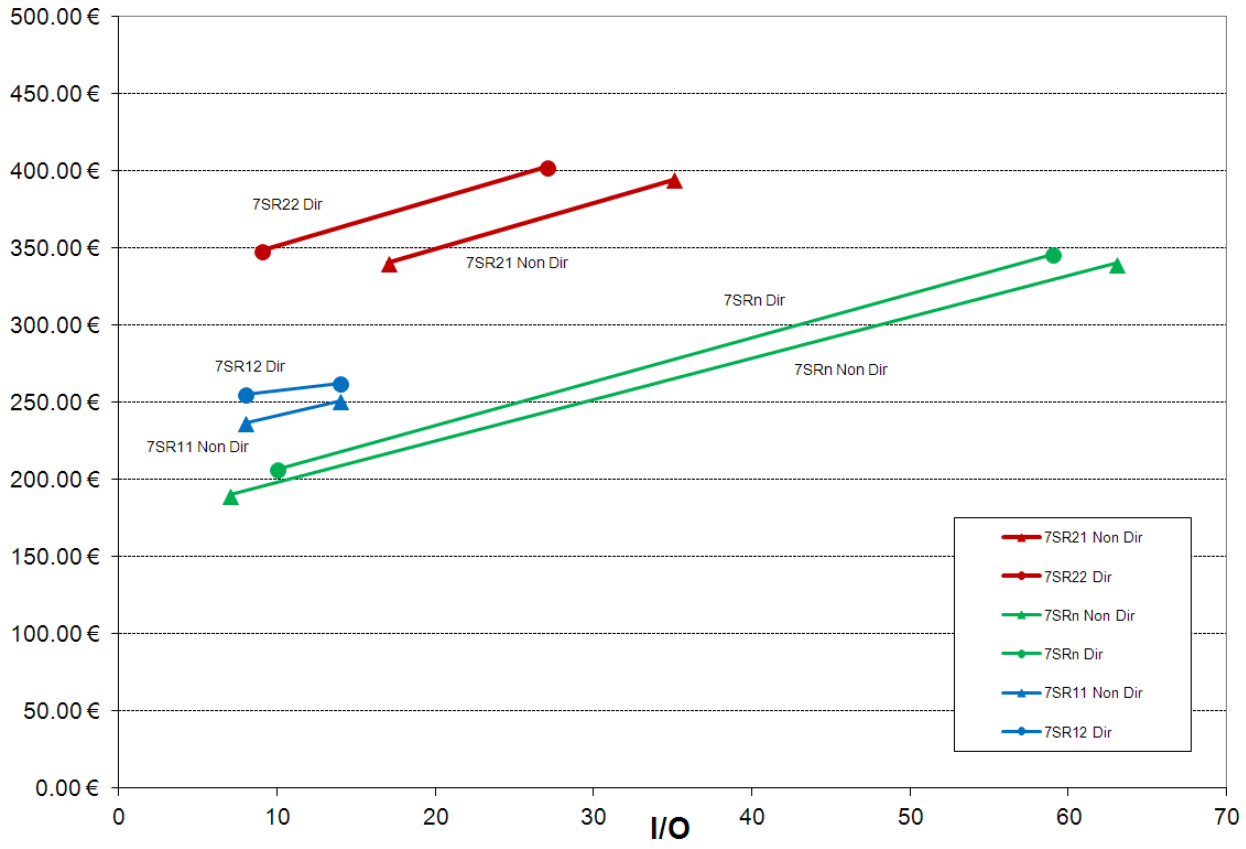


Figure 3-3 7SR Native 61850 Cost Position

3.6 Example Devices

The target launch devices, following the NPI project, will be overcurrent, directional overcurrent and a 3-winding Duobias. Many other devices are also possible, and will follow the launch of these products:

- Motor Protection
- CB Control
- Voltage/Frequency/Synchronisation
- Line Differential Protection
- High Impedance Bus-bar Protection
- A 4-winding Transformer Protection is also possible, albeit with reduced I/O

4 Interfaces

4.1 External interfaces

The rear terminal blocks will be Epsilon designs, but modified to allow for vertical CT shorting (as shown by the vertical blue bars). A typical example layout for an S6 relay would be:

	VT+I/O		CT+I/O	
1	BO 4 NO		CT 1 Strt	2
3	BO 4 COM		CT 1 Fin	4
5	BO 5 NO		CT 2 Strt	6
7	BO 5 COM		CT 2 Fin	8
9	BI 1 +ve		CT 3 Strt	10
11	BI 1 - ve		CT 3 Fin	12
13	VT 1 Strt		CT 4 Strt	14
15	VT 1 Fin		CT 4 Fin	16
17	VT 2 Strt		BI 1 +ve	18
19	VT 2 Fin		BI 1 - ve	20
21	VT 3 Strt		BI 2 +ve	22
23	VT 3 Fin		BI 2 - ve	24
25	VT 4 Strt		BI 3 +ve	26
27	VT 4 Fin		BI 3 - ve	28

	STD I/O		PSU	
1	BO 4 NO		BO 1 NC	2
3	BO 4 COM		BO 1 COM	4
5	BO 5 NO		BO 1 NO	6
7	BO 5 COM		BO 2 NO	8
9	BI 1 +ve		BO 2 COM	10
11	BI 1 - ve		BO 2 NC	12
13	BI 2 +ve		Life NC	14
15	BI 2 - ve		Life COM	16
17	BI 3 +ve		BO 3 NO	18
19	BI 3 - ve		BO 3 COM	20
21	BI 4 +ve		DC+	22
23	BI 4 - ve		DC-	24
25	BI 5 +ve		Not Used	26
27	BI 5 - ve		Earth	28

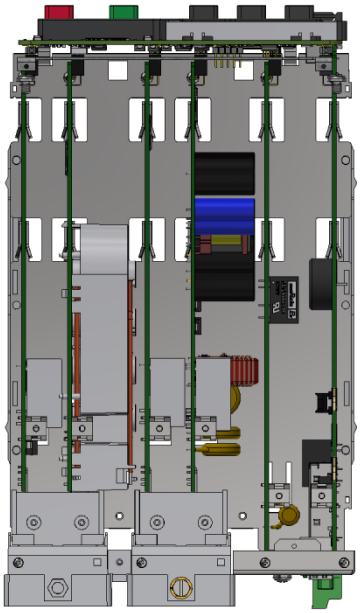


Figure 4-1 S6 rear terminal design

4.2 Internal interfaces

The main bus runs along the fascia card module, picking up all of the E2 dual-slot connectors. All modules plug into the rear of the fascia card.

The bus includes three SPI buses that are used to pass data between modules in the internal architecture. Initially only the first two SPI buses will be used.

For more detailed information on the SPI interface, see section 12.12 - SPI Interface.

The diagram below shows how the modules will interact with the two SPI buses.

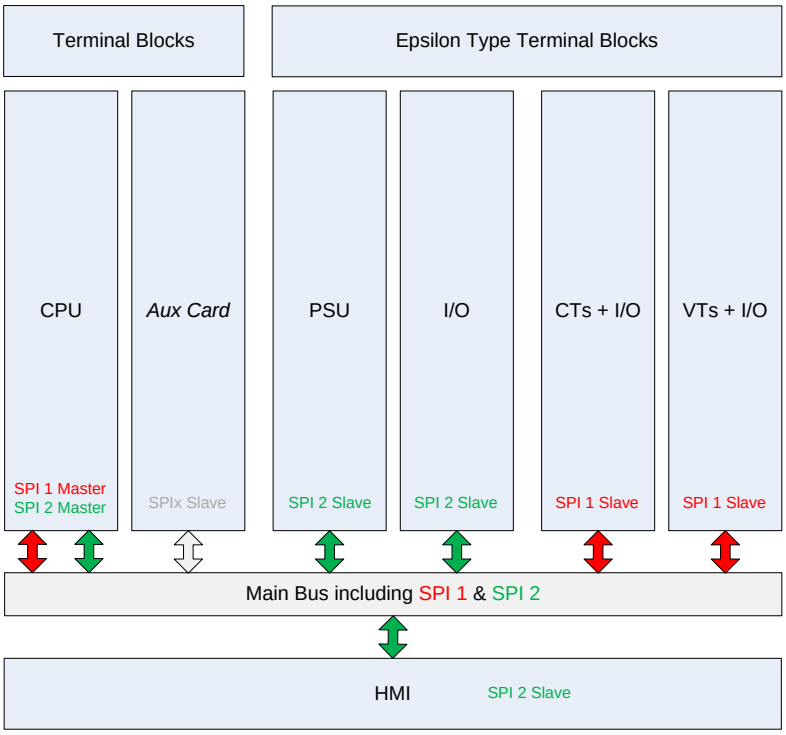


Figure 4-2 Primary and Secondary SPI bus interface

4.2.1 SPI 1

SPI 1 is used exclusively to pass sampling data between the CT / VT module and the CPU master.

The SPI1 slaves are controlled by the Cortex-M4 micros which are on every module.

4.2.2 SPI 2

SPI 2 is used to communicate with the micros handling the HMI, PSU, I/O and future optional modules.

4.2.3 SPI 3

Passed to the fascia, but currently unused. Used internally on CPU board for access to SPI flash parts.

4.2.4 Protection Comms

An MII interface will be provided on the CPU card to connect to a daughterboard carrying either optical or SHDSL interfaces for a Line Differential protection.

A reduced Address/Data bus is also included for accessing the SHDSL chip (6 address, 8 data). This is dedicated to Chip Select 3 on the EIM (CPU address/data bus) interface.

GND	1	2	GND
GND	3	4	GND
+3V3	5	6	+3V3
+12V	7	8	+12V
D7	9	10	ADDR5
D6	11	12	ADDR4
D5	13	14	ADDR3
D4	15	16	ADDR2
D3	17	18	ADDR1
D2	19	20	ADDR0
D1	21	22	/PCOMMS_CS
D0	23	24	/PCOMMS_RST
EIM_R/W	25	26	EIM_/LB
EN_WAIT	27	28	spare
I2C_SCL	29	30	I2C_SDA
ETH2_PHYINTRP	31	32	I2C_WP
ETH2_RXCLK	33	34	ETH2_TXCLK
GND	35	36	GND
ETH2_COL	37	38	ETH2_CRS
ETH2_MDC	39	40	ETH2_MDIO
ETH2_RXEN	41	42	ETH2_RXER
ETH2_TXEN	43	44	ETH2_TXER
GND	45	46	GND
ETH2_RXD0	47	48	ETH2_RXD1
ETH2_RXD2	49	50	ETH2_RXD3
GND	51	52	GND
ETH2_TXD0	53	54	ETH2_TXD1
ETH2_TXD2	55	56	ETH2_TXD3
GND	57	58	GND
GND	59	60	GND

Figure 4-3 Protection Comms Daughterboard

4.3 Process interfaces

4.3.1 Main bus

The main bus is designed for high-speed operation.

It will allow for slow-speed modules to be connected, as this will overcome problems seen on the 7SR1 platform with buffers causing delays and reducing the range of bus speeds allowed.

To reduce cost and increase functionality, all modules will feature intelligence via a cheap NXP Cortex-M4 micro. This removes the need for expensive SPI-GPIO chips and the restricted analogue acknowledge pulse feature of the 7SR1 and 7SR2.

Each card will have a single chip select, fixed by its position in the relay.

4.3.2 Main bus connectors

4.3.2.1 SPI Master (CPU card)

This 50 way connector (W73580-A8-A2) will be used on the CPU card, as it is the SPI master for both SPI 1 and SPI 2.

It will carry all the connections available on the main bus.

This will include:

- 3x SPI buses.
- 12 chip selects (shared between SPI1 and SPI2)
- Power and ground.
- 1x UART (for a future expansion module).
- Control signals (e.g. reset, sync, attention request).
- Multiple GND connections to reduce communication problems

SPARE OUT	49	50	SPARE IN
/PROGRAM	47	48	/BOOT
SPI3_CLK	45	46	SPI3_CS
SPI3_MOSI	43	44	SPI3_MISO
SPI2_CLK	41	42	GND
SPI2_MOSI	39	40	SPI2_MISO
GND	37	38	GND
SS11	35	36	GND
SS9	33	34	SS10
SS7	31	32	SS8
SS5	29	30	SS6
SS3	27	28	SS4
SS1	25	26	SS2
SPI1_CLK	23	24	SS0
SPI1_MOSI	21	22	SPI1_MISO
GND	19	20	GND
GND	17	18	GND
GND	15	16	GND
TXD1	13	14	RXD1
/SYNC	11	12	/ACK
/ATNRQ	9	10	/RESET
+3.3V	7	8	+3.3V
+5V	5	6	+5V
+12V	3	4	+12V
GND	1	2	GND

Figure 4-4 SPI master bus connector

4.3.2.2 SPI Slave (all other modules)

This 30 way connector (W73580-A8-A126) will be used on all slave modules attaching to the main bus.

It has a reduced set of pins which is the minimum required to operate a single plug-in module.

This will include:

- Two SPI ports (to allow different rate, or simultaneous data transfer). Each PCB will be hard wired to decide which SPI port it is connected to. Main CPU to probe for correct SPI port.
- One SPI chip select
- Power and multiple ground.
- Sync, reset, acknowledge and request pins.
- UART
- /PROGRAM pin for module FW upgrades.

SPI2_CLK	29	30	/PROGRAM
SPI2_MOSI	27	28	SPI2_MISO
GND	25	26	GND
SPI1_CLK	23	24	BoardSel
SPI1_MOSI	21	22	SPI1_MISO
GND	19	20	GND
GND	17	18	GND
GND	15	16	GND
TXD1	13	14	RXD1
/SYNC	11	12	/ACK
/ATNRQ	9	10	/RESET
+3.3V	7	8	+3.3V
+5V	5	6	+5V
+12V	3	4	+12V
GND	1	2	GND

Figure 4-5 SPI slave bus connector

4.3.3 Modules

4.3.3.1 Module Identification

Module identification will be done digitally, without any jumpers or timing pulses.

Each card can identify itself as part of the SPI protocol.

The Personality (article number, serial number, text description etc.) will be programmed into the flash on the ICT test jig, along with the card's capabilities e.g. counts-per-amp or number of BI/BO. (See Figure 12-5)

4.3.3.2 Module Programming

With so many microcontrollers in the relay, a method must be developed to upgrade the firmware in each module.

The microcontrollers can be programmed from the CPU using a modified SPI Flash interface (the SPI bus will be re-directed to the JTAG pins on the µC, which allows new code to be uploaded and verified).

The CPU will have copies of each module's FW as part of the relay's binary; if any card is found to be out of date, the CPU will reprogram the card during start-up.

The circuit for this feature can be found in Figure 12-3.

4.3.3.3 Module Reset

The /RESET line will be gated with the /BoardSelect line on each card to allow the CPU to reset each board in turn. This functionality is required for programming the cards, but can also be used to reset any card which fails to respond without having to kill the whole relay. See Section 12.11.

4.3.3.4 Exceptions

The Protection Comms daughterboard does not have an SPI interface. Instead, there is an I^2C interface which can be used to interrogate an EEPROM holding its Personality.

4.4 User interfaces

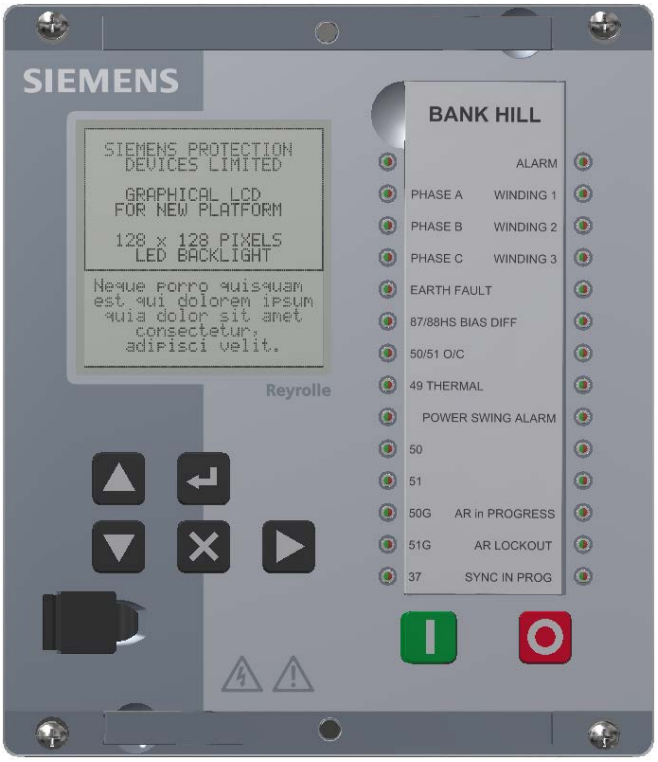


Figure 4-6 S6 Fascia

Figure 4-7 S12 Fascia

4.4.1 LCD

The device will use a large graphical LCD – 128x128 pixels.

This will allow for up to 21x16 text characters to be displayed on the fascia.

The LCD is used to display settings, instruments, events and fault information – similar to existing 7SR1 and 7SR2 devices.

The LCD will also be capable of displaying mimic diagrams.

Contrast and backlight brightness are under SW control – no trimpots are required

4.4.2 Key switches

The five button Reyrolle keypad design will be used to keep a familiar feel to the user interface.

Two additional buttons will be included to control plant items on the mimic display – Open and Close.

4.4.3 LEDs

There will be 28 tri-coloured LEDs on the fascia for indication.

4.4.4 USB

The USB Type-B interface will be included.

Unlike the 7SR1 and 7SR2 devices this will be a high-speed (480Mbps) solution, so data transfer speeds should be much greater.

4.4.5 PC Tools

All existing PC tools (Reydisp, ReyLogic, Reydisp Manager) should be compatible – or made compatible with the new platform. New USB drivers for both relay and PC will be required to handle the native USB connection.

5 Usability and design

5.1.1 Surrounding conditions

The following conditions have to be taken into account as part of the design:

- Poor lighting conditions.
- Noisy environment.

These conditions are observed in the following ways:

- All labels are clearly visible even under poor lighting conditions.
- All terminals and interfaces are easily accessible.
- The display has a sufficient contrast to be readable in low-light conditions, and will be backlit.
- The key labelling has sufficient contrast and colour coding can easily be distinguished.
- Tactile feedback is used as the only direct feedback mechanism, there is no acoustic feedback.

5.1.2 Front panel

See section 4.4 - User interfaces for information on the front panel / fascia.

5.1.3 Feedback

Feedback about operations on the HMI is given in the following way:

- Visual – changes on the display.
- Tactile – each button on the keypad has a pressure point which makes it apparent to the user when the keystroke is registered.

5.1.4 Installation

Installation has to be made as easy as possible.

- One person has to be able to complete the installation of the hardware without help from other people.
- One person can steady the device in one hand for mounting.
- The device can be mounted without needing to remove the inner chassis.
- The number of tools needed for installation is kept down to a minimum.
- The time for mounting of a device will be reduced as far as possible.
- The correct orientation of the device for mounting is clearly visible.
- The inner chassis cannot be inserted upside-down
- Required parts like holes for screws etc. can be found easily by touch and/or vision.

5.1.5 Maintenance

There are no user serviceable parts inside the device.

5.1.6 Extensions

There are no planned user hardware extensions to devices on this platform.

Published software upgrades can be installed by the user to extend or alter functionality.

5.1.7 Operating instructions

In order to ensure a common set of operating instructions all devices will use the same system manual.

For installation no other device (e.g. a computer) will be needed to read the product information instructions.

A short installation guide will be delivered in paper form.

6 Extensibility, Scalability and Configurability

6.1 Extensibility

Using the SPI bus architecture allows many other types of card to be developed and, physical properties notwithstanding, placed in any location in the relay.

The bus architecture can be used to abstract the I/O design from the relay, potentially simplifying implementation.

Each card will report its capabilities to the CPU card to allow future functionality to be supported.

6.2 Scalability

There will be initially two versions of the platform: S6 and S12 case sizes. The S12 case provides for up to 6 additional cards to be fitted, over the S6 case.

Future models may include S8 and S10 case sizes.

6.3 Configurability

Each card will be configured in the factory during ICT. It will have its performance fixed, calibrated and defined, which can be interrogated by the CPU card.

There are no requirements for mechanical jumpers or switches.

All performance-changing functionality will be under software control, either on instruction from the CPU card or as part of the normal board operation by the on-board microcontroller.

7 Testability

7.1.1 Test interfaces

Each card has a JTAG interface, allowing the Flash memory on the Cortex-M4 microprocessor to be loaded and configuration data programmed. It will also be possible to program this Flash from the SPI port.

Calibration data will be stored on the card, so each card can be calibrated during ICT.

7.1.2 Test strategies

7.1.2.1 Functional test during development

Functionality can be tested by the developer using the on-board microcontroller with basic test software. This test software will exercise the board's functionality e.g. read/write I/O, run the ADC, change gains etc. Connection to a relay is not required, so each board can be developed in isolation.

Each board can be programmed and debugged with JTAG.

For integration, a standard board-to-controller SW framework will be provided into which the card functionality can be included.

7.1.2.2 Environmental tests during development

Environmental tests should be performed as early as possible, perhaps in a framework relay in which the card is only running its own test code.

7.1.2.3 Test during production

In addition to the standard AOI and ICT, each board can be tested and calibrated in isolation which increases the flexibility of production testing. All boards should be designed to work stand-alone; unprogrammed boards should be stable with only power applied. Programmed boards should boot into HWT mode.

All signals will be brought out onto test points and, unless absolutely impossible, on one side of the PCB only.

Board FW can be programmed either through the JTAG (using needles in ICT) or using SPI from the bus connector. The personality for slave cards can be programmed using a 3.3V UART connection and the built-in HWT program on each board.

The entire relay software and scripts can be programmed using the USB port. ReyMonitor, using HWT, will also connect to the RS485 port for complete functionality testing.

7.1.3 Non-testability issues of the architecture

Some signals are not testable e.g. DDR3 runs at 400MHz, and adding test-points compromises the operation and may lead to excessive noise being radiated. If DDR is to be tested, it should be done through HWT or JTAG.

8 Reliability and safety

8.1 Reliability

The platform will be based on the existing 7SR1 and 7SR2 architectures, which are well understood. The platform will be designed for long service life using, for example:

- Industrial specification components where cost pressures permit.
- Components with high lifetime specification.
- Reduced numbers of electrolytic and tantalum capacitors.
- Reduced operating speed and supply voltage where possible e.g. run the processor at 500MHz instead of 800MHz, or at 1.2V instead of 1.375V.

Reliability (or lower risk of mal-operation) can be increased using other techniques, such as:

- Power supplies can be monitored on each card (by the resident M4 micro ADC) to ensure correct operation. In the event of a problem, the relay could self-reset.
- Each card can be reset individually e.g. a communications card with errors could be restarted without affecting the protection functionality.
- As part of the SPI communication protocol, all data is check-summed, providing additional security on raw sample data and BI/BO operation. This is new functionality that has not been available on previous generation relays.

8.2 Safety

All rear input process signals will have isolation to protect the operator.

A plastic front panel will provide insulation in the event of any internal problems.

The USB port will have clamping to protect the relay against ESD.

Where possible, all high voltage spikes will be diverted to PE as soon as possible after entering the relay (or simply tolerated in the case of un-earthed inputs).

No live terminals will be exposed in normal operation.

The inner relay will be locked in place to allow for angled mounting e.g. at 45°, above head height, and will not fall out when subject to vibration.

CT shorting prevents CTs becoming open-circuit when the relay is withdrawn.

In the event of unmanaged high voltages being present on rear terminals (e.g. induced voltages on pilot wires) additional isolation transformers and/or clamping should be specified externally.

9 Limits

9.1 Power

The PS53 Universal PSU has a higher output power (18W) than 7SR2 (13W), allowing more BO to be specified.

The LCD backlight has a lower power (about 1/4W instead of 1W) freeing up more power. It is under PWM control, so can be dimmed, saving more power.

The LEDs can be driven with greater efficiency under software control, since the fascia has a dedicated microcontroller. The LEDs can be driven at a high frequency (200Hz+) and can be multiplexed so that only 4 out of 28 are on at any one time. This will also save power.

It is estimated that the maximum internal power consumption (3W Duobias, max. I/O) will be 12.5W. See ***/4/***

9.2 PCB size

The following sections describe the board geometries and any relevant important component locations. Note pin positions are to the centre of the physical pin.

9.2.1 S6 Fascia

Note that on this figure the connectors are mounted on the reverse side. In the areas of the fascia PCB which lie directly beneath the edges of the plug-in cards using the 30-way connectors, the maximum height of component allowed in these areas is 6.0mm. For the area beneath the CPU card, which uses the 50-way connector, the maximum height is 3.2mm.

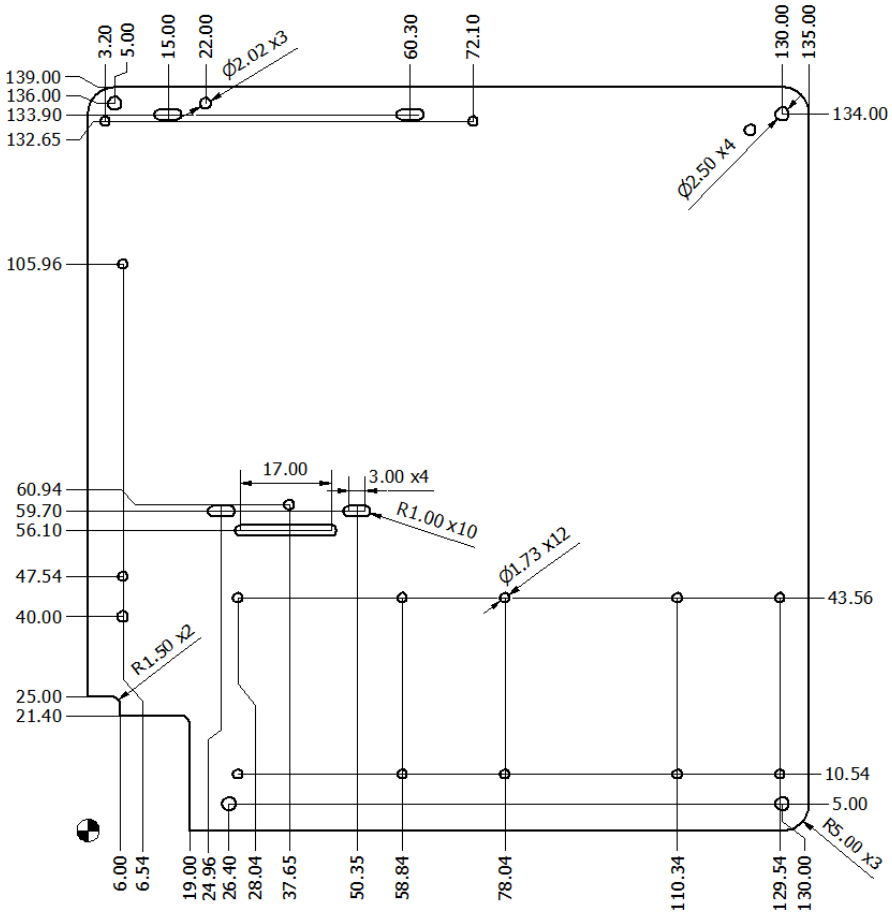


Figure 9-1 PCB Size and connector placement for S6 Fascia

9.2.2 S12 Fascia

Note that on this figure the connectors are mounted on the reverse side. In the areas of the fascia PCB which lie directly beneath the edges of the plug-in cards using the 30-way connectors, the maximum height of component allowed in these areas is 6.0mm. For the area beneath the CPU card, which uses the 50-way connector, the maximum height is 3.2mm.

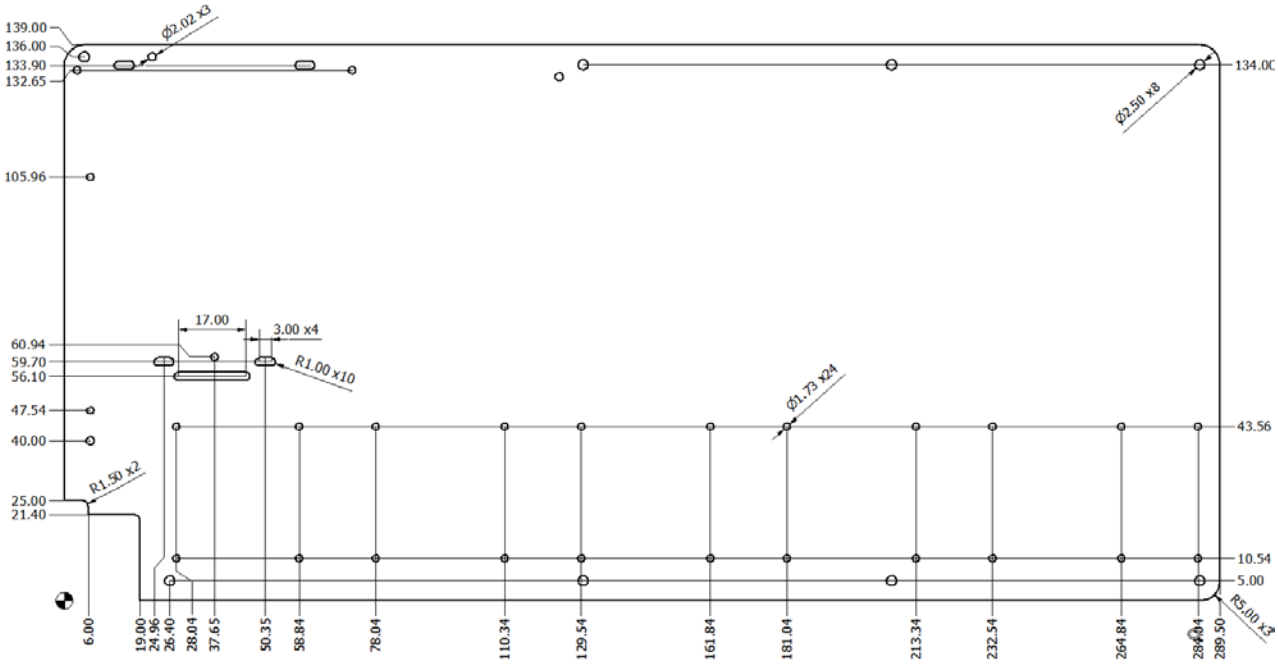


Figure 9-2 PCB Size and connector placement for S12 Fascia

9.2.3 CPU

It should be noted that the necessary placement of the two SMT right angle mounting brackets at the top and bottom edges of the PCB are close to these edges. This may compromise the design of the mounting hardware used during production assembly, and this will probably require that the PCB is designed with break-off strips along these edges.

Note the keep-out areas along the top and bottom edges. These are there to provide clearance to the PCB guides which are formed in the top and bottom plates, and which help alignment of the PCBs during assembly.

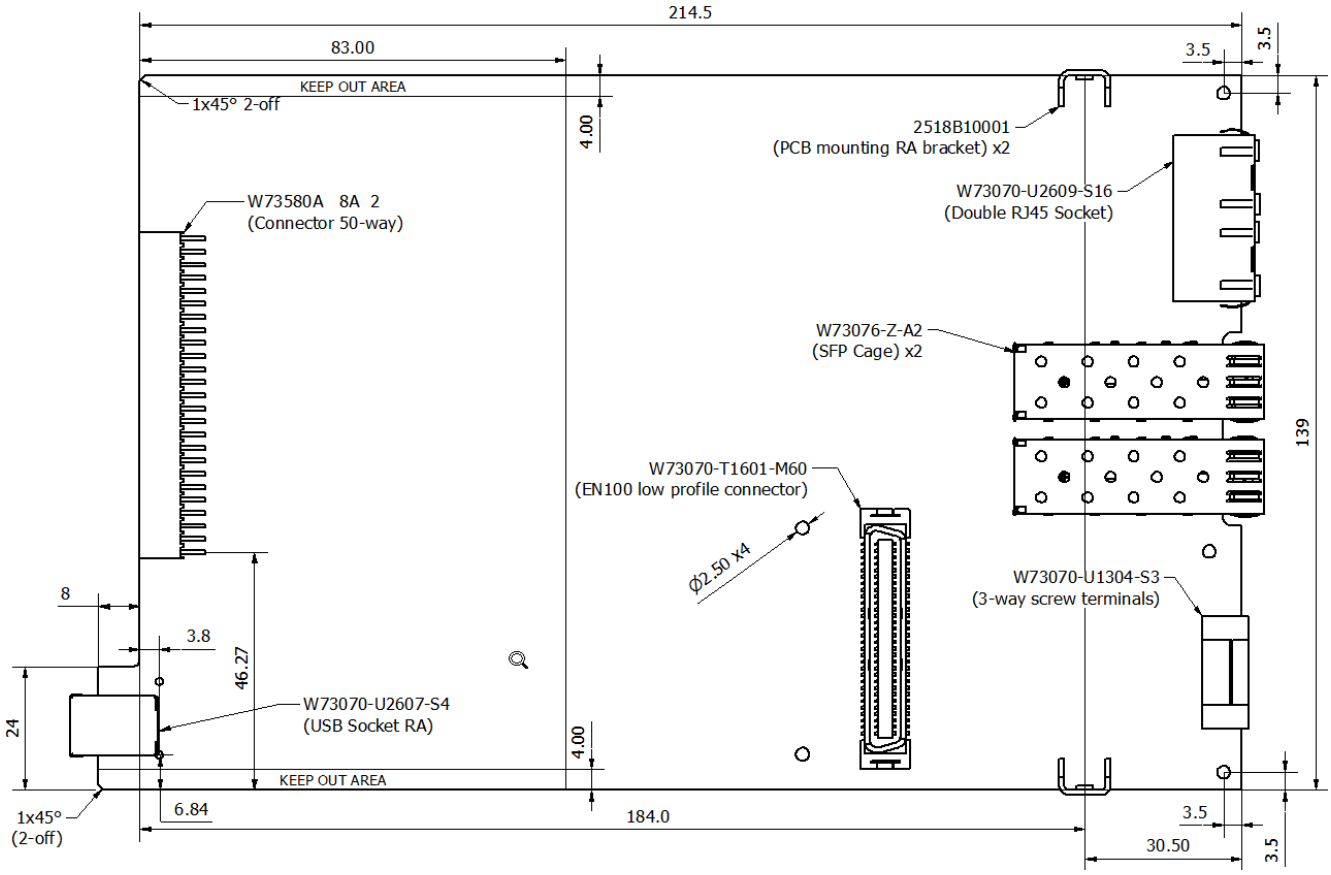


Figure 9-3 PCB Size and connector placement for CPU

9.2.4 AUX

This PCB is mounted adjacent to the CPU card and will provide functionality for additional comms options, RTD inputs etc.

It should be noted that the necessary placement of the two right angle mounting brackets at the top and bottom edges of the PCB are close to these edges. This may compromise the design of the mounting hardware used during production assembly, and this will probably require that the PCB is designed with break-off strips along these edges.

Note the keep-out areas along the top and bottom edges. These are there to provide clearance to the PCB guides which are formed in the top and bottom plates, and which help alignment of the PCBs during assembly.

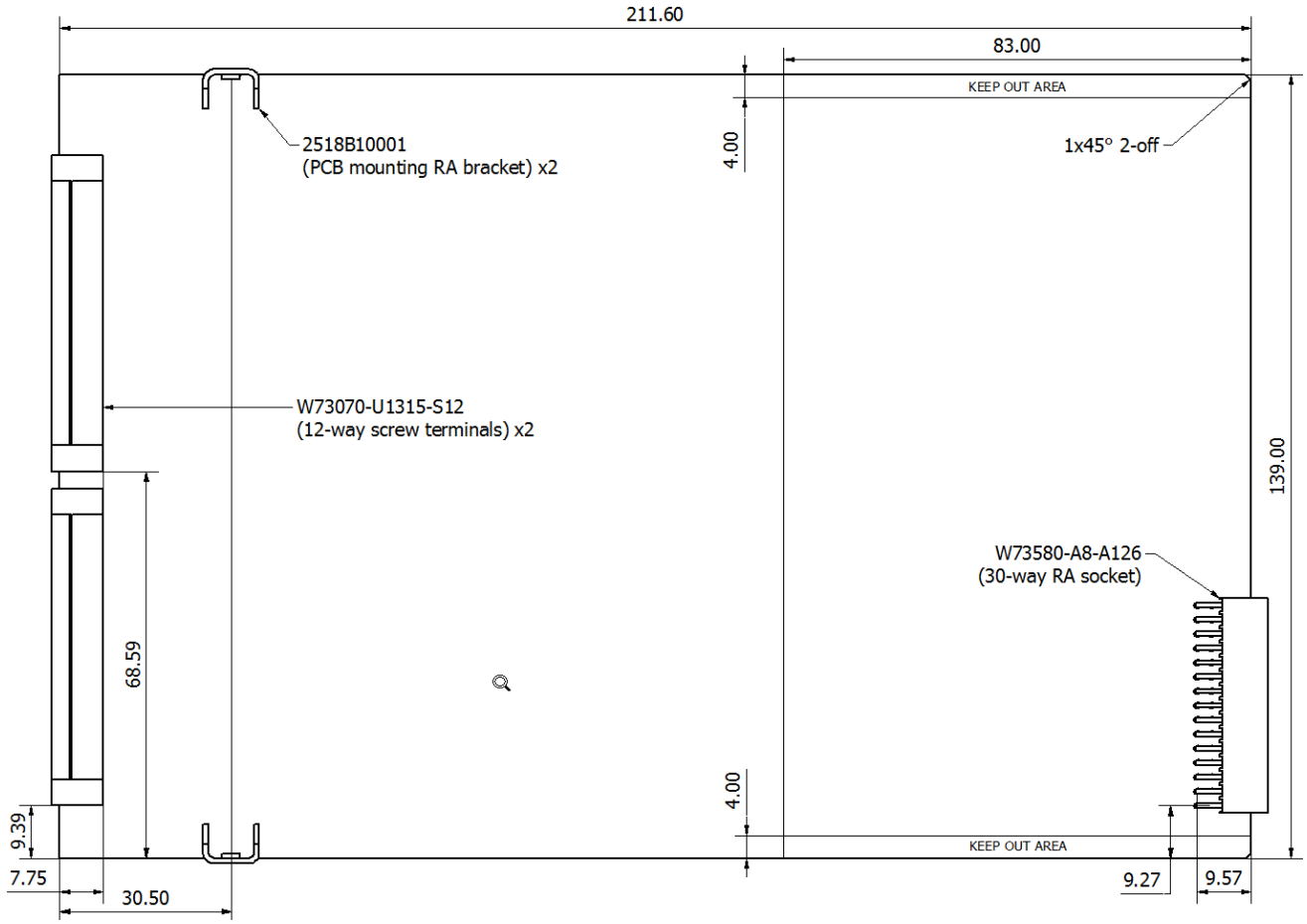


Figure 9-4 PCB Size and connector placement for AUX (RTD Variant)

9.2.5 CT

It should be noted that the necessary placement of the two right angle mounting brackets at the top and bottom edges of the PCB are close to these edges. This may compromise the design of the mounting hardware used during production assembly, and this will probably require that the PCB is designed with break-off strips along these edges.

Note the keep-out areas along the top and bottom edges. These are there to provide clearance to the PCB guides which are formed in the top and bottom plates, and which help alignment of the PCBs during assembly.

On this board the four CTs will be mounted into an assembly which integrates the primary and secondary wiring, PCB connectors, PCB fixings and Epsilon blades into a carrier module, which will be supplied complete by a partner manufacturer.

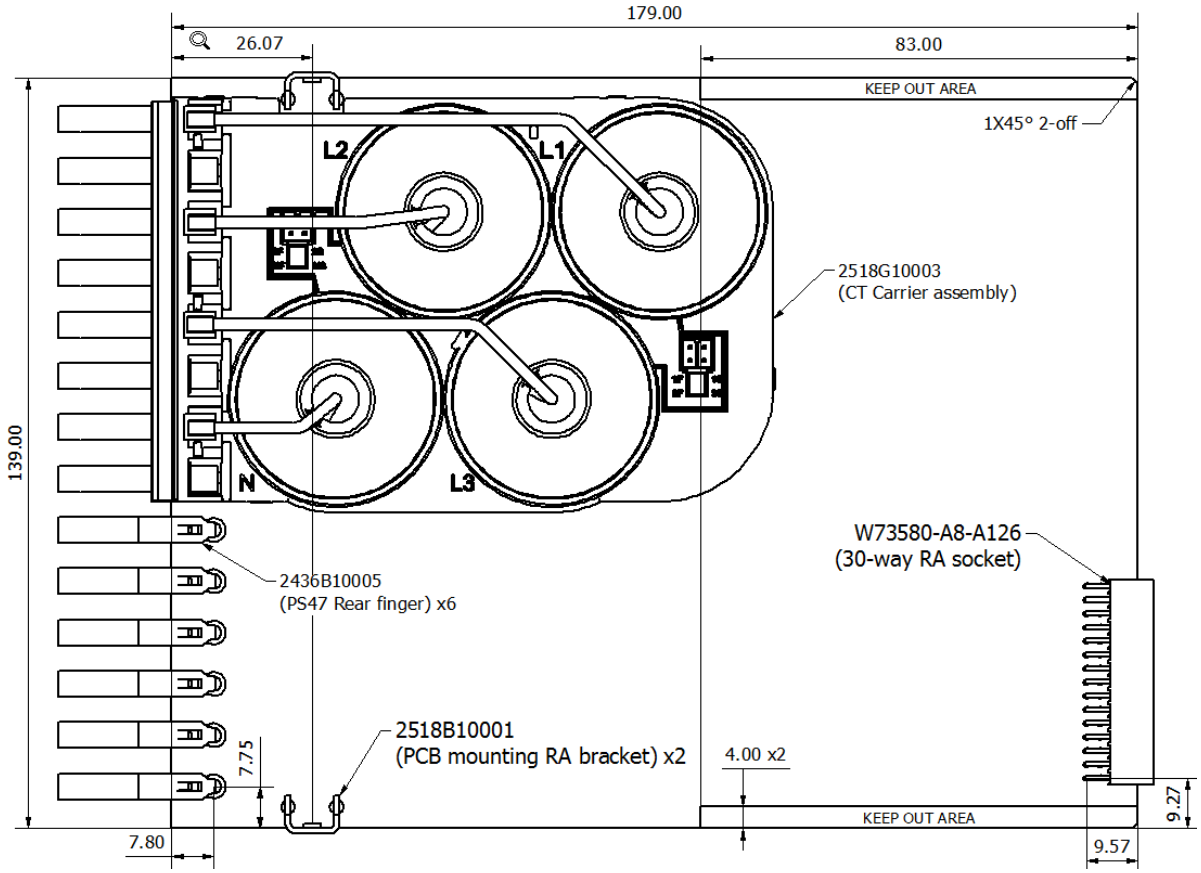


Figure 9-5 PCB Size and connector placement for CT

9.2.6 PSU (PS53)

It should be noted that the necessary placement of the two right angle mounting brackets at the top and bottom edges of the PCB are close to these edges. This may compromise the design of the mounting hardware used during production assembly, and this will probably require that the PCB is designed with break-off strips along these edges.

Note the keep-out areas along the top and bottom edges. These are there to provide clearance to the PCB guides which are formed in the top and bottom plates, and which help alignment of the PCBs during assembly.

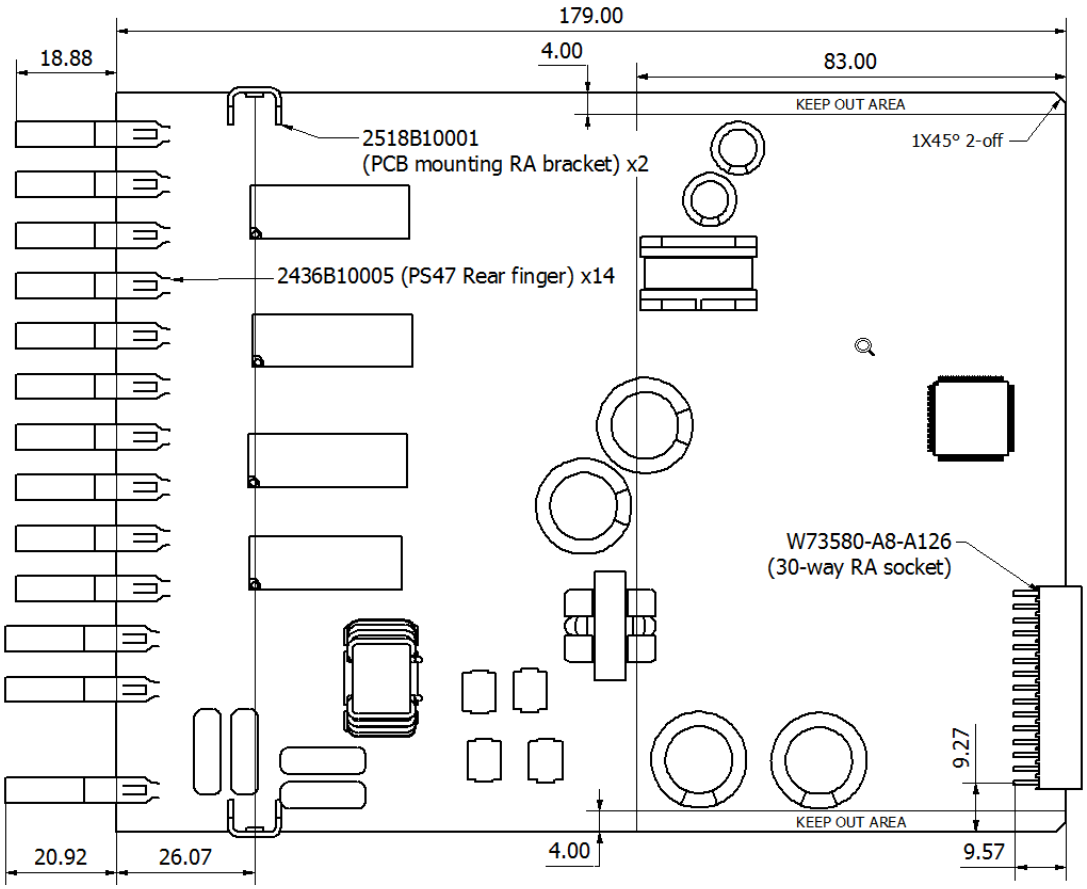


Figure 9-6 PCB Size and connector placement PSU

9.2.7 VT and I/O

These PCBs have the same mechanical outline dimensions and connector/fixing positions. It should be noted that the necessary placement of the two right angle mounting brackets at the top and bottom edges of the PCB are close to these edges. This may compromise the design of the mounting hardware used during production assembly, and this will probably require that the PCB is designed with break-off strips along these edges.

Note the keep-out areas along the top and bottom edges. These are there to provide clearance to the PCB guides which are formed in the top and bottom plates, and which help alignment of the PCBs during assembly.

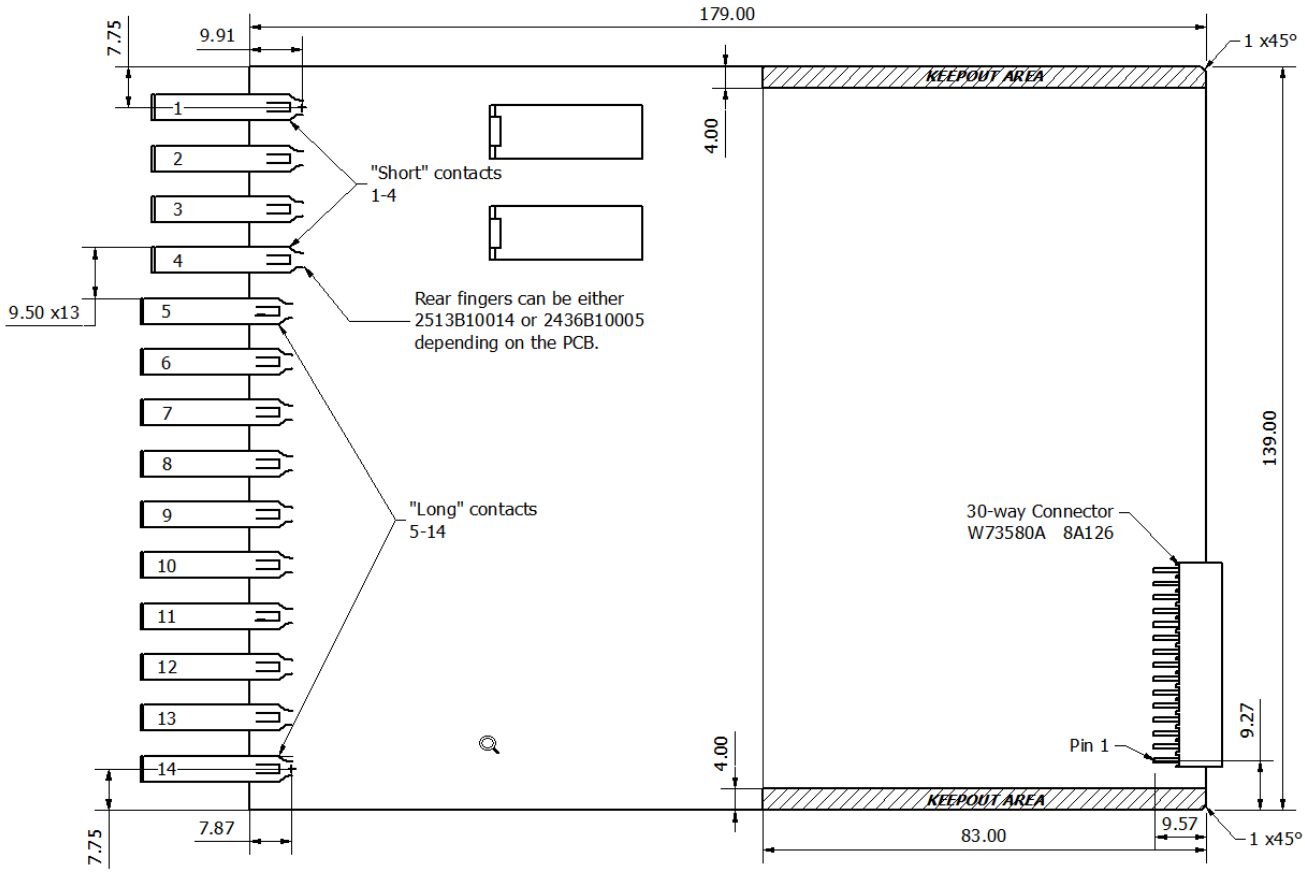


Figure 9-7 PCB Size and connector placement for VT and I/O

9.3 Temperature range

Climatic Tests

Temperature

IEC 60068-2-1/2, IEC 60068-2-48	
Operating Range	-10 °C to +55 °C (Also -40 °C, -20 °C to +70 °C)
Storage range	-25 °C to +70 °C

Humidity

IEC 60068-2-78, IEC 60068-2-14, IEC 60068-2-30	
Operational test	56 days at 40 °C and 93 % relative humidity

The relay is designed to operate in an ambient air temperature from -10 to +55°C.

10 Security

10.1 Firmware

A Secure Boot facility is included. Code uploads are staged in RAM, the digital signature is checked and only if it passes will it be burned into flash.

10.2 Physical

The relay is screwed into the case from the front. This will allow the relay to be mounted at an angle without the possibility of it falling out.

10.3 Controls

Although there has always been a password feature in Argus, 7SR1 and 7SR2 relays, this has been a bit of an unused feature. As the current clear plastic, tamper-evident front cover is no longer used, the software must have a default password to protect the relay settings from accidental change.

Several levels of password may be required, for example one to prevent viewing settings, another to prevent changing settings and a third to access “linesman” mode, which could directly control breakers and other plant.

11 Standards and Regulations

A list of standards to be tested against is contained in the Hamilton Laboratory list of Type Tests and Standards. See ***/3/***

12 Functional blocks

12.1 General Rules

1) Each module should be stable in isolation i.e. during ICT. Any dedicated bus lines should be pulled up with a standard pull-up (4k75). Any shared bus lines (e.g. /RESET, /PROGRAM) should be pulled up with a weak pull-up (100k). Intermediate lines (i.e. signals which have been buffered) should also have appropriate pull-ups or pull-downs to ensure stability before the module has been initialised.

2) All SPI outputs (DOUT / MISO on the cards) should be shunt-terminated on the CPU board. CLK and MOSI should be shunt-terminated at the far end of the fascia. Different values of termination may be needed for S6 and S12 boards.

3) Bulk storage capacitors should be carefully evaluated. Are they really required? Are they away from sources of heat? Tantalum capacitors should be replaced by ceramic where possible. Remember to over-rate the voltage by 1.5x and take into account the capacitance de-rating with increasing DC voltage.

4) A Mentor project template is available to start a new board, and it should be used for all boards. It contains the basic circuits required to implement a new board. (No PCB definition is supplied, as this requires the number of layers to be defined in advance.)

5) Logic levels are 3.3V.

12.2 Earthing Concept

A general point about our earthing concept for our existing devices, 7SR1 and 7SR2 is that something has gone amiss with our designs over time. We currently have difficulty in passing certain tests, when we may not have had issues on older, more robust designs. This is because of a lack of an overall earthing strategy for the current devices.

The problem: it appears that we have, over time, lost the concept of a protective earth (PE) or chassis earth on our PCBs. Our internal removable chassis is now nominally DGND and is connected by our chassis earth spring to the relay case which is ultimately connected to the substation PE/GND. The problem with this is that any HF disturbance coming into the back of the device has now got multiple paths to DGND through either screw connections from the PCB to the inner chassis, or via GND planes and other parasitic paths through the PCB. The HF currents thus supplied can and sometimes do cause problems for us e.g.

1. FT applied to our current and voltage inputs can be seen on our waveform recorder to some extent. (A test of a Siprotec Compact device shows a much better filtering of this; in fact evidence of 4KV FT is non-existent on their current inputs).

2. On our 7SR1 device we have a problem with the USB Type-B connector and point-contact 8KV ESD. This is because the shell of the USB is tied to DGND, not to PE and this appears to cause a problem with the local DGND and Microprocessor, causing a reset.

The solution:

We shall re-introduce the concept of a PE on all of our cards. The diagram below, Figure 12-1, shows the concept using the example of the Microprocessor PCB. The current 7SR1 device problem with USB and ESD will be cured with the shell of the connector being connected directly to PE on the PCB and via a spring to the bottom plate. Direct application of 8KV ESD to the USB shell will not have a direct path to the DGND of the microprocessor; it will hopefully find a low impedance path through the spring to the bottom plate and ultimately to the case earth terminal via the earth springs.

The relay removable chassis metalwork will be our PE point, connected to the relay case via multiple earth springs.

The DGND on the processor PCB will not have a direct connection to the top and bottom plates and therefore no direct connection to PE. The DGND net will be generated on the PSU card and pass along the Fascia bus in multiple places. All microprocessor supplies will be referenced to DGND and derived on this PCB. The only connection from DGND to PE will be capacitive coupling on each PCB.

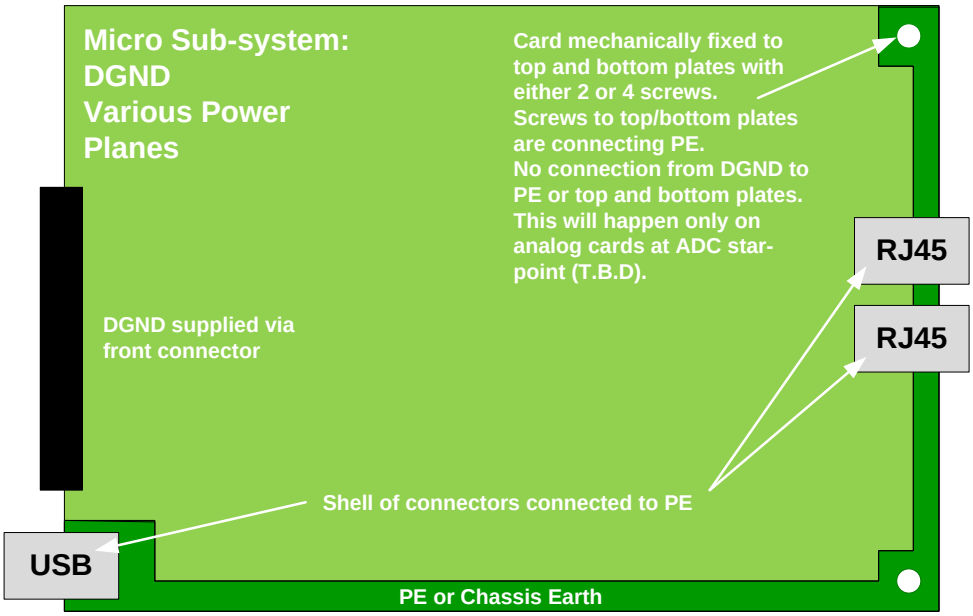


Figure 12-1 Earthing Concept – CPU Card

To make a more robust solution for our analogue measuring circuits we will need to also introduce the PE concept. As we will be utilising the Sip 5 CTs which have no screen between primary and secondary and which have a ratio of 1:5000 making the secondary voltage levels very low, we need to efficiently remove coupled FT to the primary wires. This can be largely achieved as shown in Figure 12-2 below.

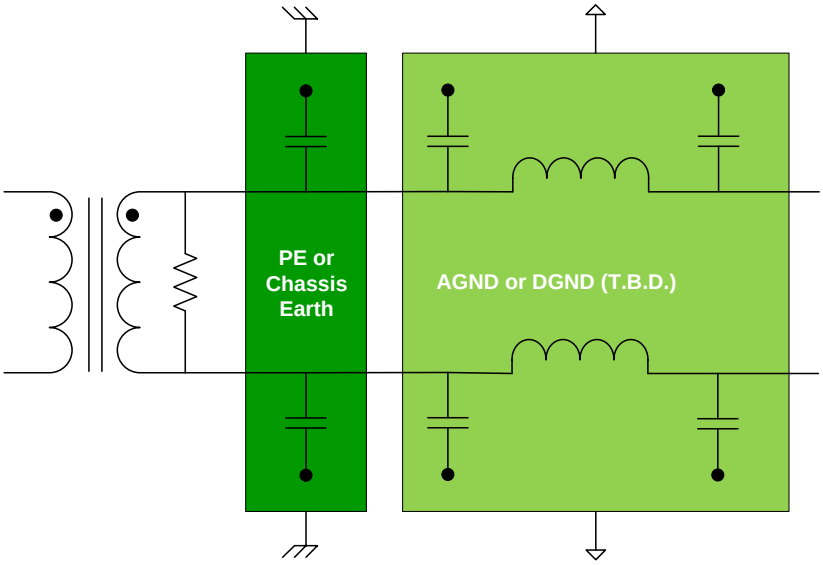


Figure 12-2 Earthing Concept – Analogue Cards

The secondary side of the CT should have high-frequency shunt capacitors connected to a PE plane. This should help remove some of the HF noise. Following this should be extra shunt capacitors and series inductance (either inductor or ferrite) and more capacitance which are all encompassed within the AGND (or DGND) plane. Due to the small signal size, all signal paths should be run as differential pair signals and ideally followed by a differential to single-ended op-amp solution.

All other types of PCB which are intended for this platform will be required to follow the same philosophy: I/O boards, VT boards, PSU etc.

12.3 CPU Module

12.3.1 Usage

The CPU module will feature an NXP i.MX6 SoloX microprocessor, see **/1/**. This features an 800MHz Cortex-A9 and a 227MHz Cortex-M4 core. The A9 is the boot core, and it is proposed that the IEC61850 comms is handled by this core, as it generally requires an RTOS to be used. The M4 core will be reserved for the relay protection code. Both cores have a L1 cache. The A9 core also has a 256KB L2 cache and the M4 core has 64KB of fast (tight-coupled) memory which is visible to the A9 core.

Storage will be comprised of 2x16MB of 32-bit parallel NOR flash and 2Gb (256MB) of 32-bit DDR3L SDRAM. As an option, the flash can be upgraded to 2x32MB with a BOM change. A 128MB SPI NAND flash is also included for additional future storage requirements. After the problems with the 7SR1 SPI chip, this could be used for “re-formattable” storage (waveforms etc.), or to separate the firmware from the data.

The A9 core will run a commercial RTOS (VxWorks) as this is already used for the EN100 code. The M4 will run a combination of SPDL’s proprietary OS and OpenRTOS.

12.3.2 Interfaces

Two Ethernet interfaces are available on the CPU. One will be reserved for IEC61850 and the other will be used for the 7SR18 protection comms.

For IEC61850, an FPGA will be added; this will handle the L2 switch, HSR/PRP and MAC filtering. The existing EN100 FPGA design will be re-used, without the dual-port memory. The switch and HSR/PRP functionality can also be bought off-the-shelf for use in an FPGA but is likely to be €10k+ to license.

A Xilinx Spartan-6 FPGA has been selected for cost reasons. The Xilinx part can run from just 2 voltage levels, both of which are already available for the SoloX. The alternative, an Altera Cyclone V E, requires 3 voltage rails, two of which must be generated. As the Cyclone V is already more expensive than the Xilinx, the additional regulator cost would be prohibitive.

A single, isolated RS485 interface will be provided. This will use a CPU-controlled Transmit line to simplify the circuit.

To the fascia, the module will present the following signals:

- 2x SPI ports running at up to 12.5MHz with 12x Board/Chip Select lines
- 1x SPI port running at up to 12.5MHz with 1 chip select line
- 1x UART
- Reset, Sync, AtnRq, Ack, Program and spare GPIO lines

A header will pass the MII interface of the second Ethernet port and small 8-bit parallel bus to a daughterboard for the Protection Comms.

A USB Type B connector will protrude from the front of the PCB to provide a PC connection.

12.3.3 Technical Data

It is expected that the CPU board will require around 4W when populated with 2x Fibre IEC61850 interfaces and a 40km Protection Comms interface.

The RS485 will be modified to make the CPU control the transmitter using the RTS line, removing the need for an ADE converter. The receive line will be permanently on to allow bus fault monitoring i.e. whatever is transmitted should be received.

12.3.4 Limits

To limit power, especially with the S6 variant, the CPU should be run at the lowest possible speed. Supply voltages can also be trimmed in the PMIC to reduce power e.g. reduce the 3.3V rail to 3.1V

12.4 Protection Comms

12.4.1 Usage

This board will provide both 40km singlemode fibre and single twisted pair copper SHDSL interfaces for line differential protection use.

12.4.2 Interfaces

One LC-connector SFP module will provide the 40km fibre link. This runs at 100Mbps.

One 2-pin 3.81mm-pitch plug and socket (a version of the RS485 connector on the CPU board) provides the SHDSL signal.

12.4.3 Technical Data

12.4.3.1 Fibre

Interface ETH2 of the iMX6 CPU will be connected to a PHY chip which in turn is connected to an SFP module. This PHY-SFP hardware will be the same as on 7SR18, which should simplify the software port.

12.4.3.2 Pilot Wire

For this mode, the ETH2 port will be connected to an Intel PEF21628E SHDSL line driver chip. The PEF chip emulates a PHY chip for data comms and converts this into an SHDSL signal. It also has an 8-bit data bus for control and monitoring e.g. firmware load, SNR checking, CO/CPE configuration.

12.4.3.3 Ethernet Switch

As two PHYs cannot be connected directly to the CPU's MAC, a switch needs to be incorporated. There are many off-the-shelf switch chips, but these usually incorporate a PHY for direct connection to an end device (for use in a traditional desktop or rack-mount network switch, for example). These are not suitable for driving an external PHY.

One solution would be to re-use the FPGA, remove the HSR/PRP components and just use the switch. This can drive two external PHYs, but it adds significant cost.

Another solution is to use an analogue switch. Maxim produce an 8-channel 2:1 analogue switch with a 625MHz bandwidth. Although it is targeted at switching the 4 output pairs of a PHY, it can also be used to switch the MAC signals. (It's just a bi-directional analogue switch…) Two chips would be required, but these are cheaper than an FPGA.

12.4.4 Limits

The fibre-optic connection is limited to 40km on singlemode fibre. (100km or 20km variants of the SPF are available but are not offered to limit the number of variants.)

Multimode fibre should be usable up to around 3.5km, but this will depend on the bandwidth-distance product of the fibre and the number of joints in the total run (based on a typical 500MHz.km 50/125µm fibre)

It is harder to quantify the Pilot Wire interface, as the link speed obtainable depends several factors:

- wire diameter
- capacitance-per-metre
- whether it is screened or unscreened
- twisted-pair or untwisted
- how much noise is present on the line
- how much crosstalk is present
- how much induced a.c. voltage is present
- whether isolation transformers are used

The aim is to achieve 10km over a good quality line.

The ideal cable will be low-capacitance twisted pair with solid cores of at least 0.8mm diameter, insulated with PE (not PVC). Although a screen is not strictly necessary, it will provide additional noise immunity and should be recommended. The use of unscreened, untwisted wires should be discouraged, especially if the wires run alongside other high-frequency signals or high currents.

The recommended telecoms transformer only provides 3kVrms isolation. Higher isolation is achieved with an external transformer. These must be rated for high-frequency use (in excess of 2MHz). 6kV and 20kV models are available as a standard Siemens product.

12.5 Power Supply (PS53)

12.5.1 Usage

The PSU will be a derivative of the PS52, which can operate from 24-220V batteries, and also 115-230Vac.

The 7SR1 supply can only deliver 9W. At minimum voltage, the 7SR2 supply could only deliver 13W, and limited the number of I/O on the larger relays. The Goa supply is currently specified at 18W, which should help increase the available I/O.

It has been proposed that the RS485 interface be dropped from the new PSU board and instead placed on the CPU board. This would allow additional BO on the PSU board, boosting the standard I/O mix.

12.5.2 Interfaces

Only +12V should be provided to the fascia. All other common voltages will be derived from this by the fascia and CPU boards, including 3.3V for the digital circuits on the PSU. No negative supply is provided, as analogues can be designed as single-ended rail-rail or negative supplies can be derived on slave boards.

The remaining space on the PCB should be used to provide BO. A minimum of 4 should be provided.

12.5.3 Technical Data

If possible, at least 2 BO should be heavy-duty, capable of direct tripping. Two BO will be configured as NC and two as NO.

12.5.4 Limits

High temperature components should be placed above and away from electrolytic capacitors to lengthen their lifetime.

12.6 CT+I/O

12.6.1 Usage

A current transformer (CT) card will be developed which contains 4x CTs and 3x Binary Input circuits. The 4x CTs will be configured as either 3x P/F and 1x E/F, or if possible, 3x P/F and 1x E/SEF (combined earth and sensitive). This card will be capable of being located in multiple positions in the case as 4, 8, 12 and possibly 16 CTs will be required for different device variants.

It is proposed that, due to the timescales involved, BLN re-use circuit(s) will be employed. CTs similar to those used on Sip 5 will be used on this platform.

There may be two versions of analogue measuring stage: one for the cheapest Overcurrent devices and another higher performing version for the Transformer Differential devices. This has yet to be determined and is largely cost related; however, certain algorithm requirements for the differential product may mandate the use of the more expensive solution.

The choice of re-use analogue conditioning circuits is as follows:

1. Siprotec Compact (using Max1228 ADC).
2. Siprotec 5 non-modular (using Max11060 ADC).
3. Siprotec 5 modular (using Max11040K ADC).
4. A new HBB design (using a TI ADS131E04 – as used by Goa).

There are a number of issues relating to non-conformance of the requirements with this choice of analogue solution:

1. Measuring range 80Arms: with the proposed CT and single-bar primary solution, 80Arms measuring is unlikely to be achieved. It is highly likely that a top measuring range of 50Arms (1A) and 250Arms (5A) is all that can be achieved. We do not consider this to be a problem for the basic Overcurrent and Differential devices that we intend to have on this platform.

2. Metering accuracy: our specification calls for Metering accuracy of 1% between 0.1-2.0xIn. This may not be achievable with the cheapest Siprotec Compact solution. It may be that the minimum solution we can consider is Sip 5 non-modular, or a solution based on the TI sigma-delta part.

3. CT 1 sec thermal rating: we will not meet 500A 1 sec thermal rating requirement with our existing terminal block design and Faston method of terminating the CTs. The CT input has been re-modelled in a single carrier block which now passes 500A/1s.

12.6.2 Interfaces

To improve the terminal density, a single 1A/5A primary will be used. A software selectable setting will determine which nominal tap is selected. A Sync pin from the CPU should be used to synchronise the sampling across multiple modules. This should be connected to the board's micro and used as an interrupt to trigger a sampling cycle.

Data is passed back to the Controller over SPI1 using a pre-defined protocol.

12.6.3 Technical Data

The device will provide a minimum of 32 samples per cycle (spc) for Waveform storage, so that it is not inferior to the 7SR1 and 7SR2 relays in this regard. Higher sampling rates may be possible

12.6.4 Limits

Not defined as yet.

12.7 VT+I/O

12.7.1 Usage

4VT channels should be provided, with 1x BI and 2x BO circuits. The fundamental design of the voltage measuring circuit will be based upon the proven 7SR1/7SR2 design. The input applied voltage produces a current using a resistor chain. This is then passed through a 1:1 isolating telecoms transformer and fed into a zero-flux circuit to produce a single-ended signal which goes through other conditioning circuitry and to the ADC.

12.7.2 Interfaces

The VT circuit connects to the rear terminal block with a pair of Epsilon blades.

Data is passed back to the Controller over SPI 1 using a pre-defined protocol.

12.7.3 Technical Data

For high-speed sampling, it should be investigated whether the board's microcontroller could be used to handle the sampling and take the interrupt load off the main CPU. Currently, the CPU has a 625µs interrupt for 32 samples/cycle at 50Hz and 520.83µs at 60Hz. To double, or quadruple, the sampling frequency will increase the interrupt overhead of the CPU significantly, to the detriment of the other relay functions.

A small €1.50 Cortex-M4 micro with 2 SPI ports would be able to use the Sync pin to start a sample period, take 2 or 4 sets of samples using its SPI Master, and pass them back to the main CPU in one burst using its SPI slave.

12.7.4 Limits

This circuit currently does not allow 440Vac input. Levels this high would require re-design and significant re-testing which may be beyond the scope of the initial prototype project.

12.8 Standard I/O Board

12.8.1 Usage

It is proposed that a version of the Sip 5 BI circuit (ver. X12-1) is used on this platform. If possible, this should also be altered to achieve AC performance.

It is also proposed that the Sip 5 BO circuits are re-used. This is because they also offer the secure, double-write feature all our relays possess, but which is a better and cheaper solution than provided on 7SR1/2.

The requirements of CE2016 should be taken into account for the new developments i.e. they should be able to pass all of the latest standards.

5BI and 2 BO will be provided.

12.8.2 Interfaces

Connections are made from the rear terminal block to the board using Epsilon blades.

Data is passed back to the Controller over SPI2 using a pre-defined protocol.

12.8.3 Technical Data

Re-use blocks X12-1 and X65-2 are the current BI and BO circuits. Output relay article number W73052-D4008-A5 should be used for SPST contacts and W73052-D4001-A5 for SPDT.

A small Cortex-M4 micro acts as an SPI slave to send and receive data from the Controller.

12.8.4 Limits

BI will have switchable input ranges of 15, 75 and 160V, up to a maximum input voltage of 300Vdc. Pick-up and drop-off time is max 4ms each.

BO will be able to make and carry 8A@250Vac and 30Vdc with a resistive load.

12.9 Fascia

12.9.1 Usage

The aim is to include a graphical fascia. This will not only provide non-English character sets, but also allow mimic diagrams to be displayed.

Native USB type B will be provided, although the actual USB connector will be fitted to the CPU card. Type A (for memory sticks) is an option which should be investigated, or it could be provided using a Type B-A adaptor cable and USB-OTG.

The standard Reyrolle 5-key layout will be used by default: Enter, Cancel and Test/Reset. Start/Stop (or Open/Close, On/Off, or just 0 and 1) keys will also be provided. No “soft keys” are envisioned as being required under the LCD, nor is a numeric keypad.

Two basic fascias will be produced in the first products. Both S6 and S12 will have 28 LEDs. No user-configurable function keys will be provided, although it is recommended the functionality should be catered for in the fascia design to save on future Test Adapter costs.

It should be remembered that this is a 61850 platform. A lot of the configuration is done at the master station and simply handed down to the relays en masse. The majority of the local interface use will be during commissioning, and these functions should be given priority.

12.9.2 Interfaces

A new layout of a 30-way connector will be used to connect to each card. A 50-way connector is provided for the CPU board, as it has to provide all the chip select lines in addition to the other bus signals.

A 30-way FPC connector is used for the LCD. This connects the interface and backlight in one.

All fascia functionality will be handled over SPI 2. A dedicated microcontroller will handle the keys, LEDs and LCD.

The main Controller will send commands to this microcontroller to read and write the keys and LEDs, and the LCD memory map.

Using a micro decouples the circuitry from the relay. On the 7SR2 and 7SR1, each bank of LEDs or switches required a dedicated chip-select and a value was written to a latch. Now, the controller simply needs to pass its internal data (set LED15 to Red) and the fascia will decide which latch to set.

12.9.3 Technical Data

Power to each card (except CPU) will be provided by regulators on the fascia. These rails will be +3.3V for the logic and +5V for output relays. This will save the cost of regulators on each board, as one high-current supply is only slightly more expensive than a low-current regulator. +12V is also available should other voltages need to be derived for additional functionality. No negative rail is provided.

Although micros have many GPIO ports, it will not be able to drive 28LEDs. The existing latch architecture should be maintained. This will mean an 8-bit port will control all keys and LEDs, with GPIO lines being used for chip selects.

LEDs should be driven from the lowest possible voltage to minimise power losses in the series resistors. Where possible, LEDs should be pulsed to save power.

Keys may either be wired individually direct to the micro or arranged in a grid pattern. Doing so, however, may remove the ability to have our “Special” key presses (Enter-Test-Cancel etc.)

The LCD backlight can be driven from a PWM output to reduce power (although the new display only requires around ¼ of the power of the 7SR1/2 backlight)

12.9.4 Limits

Each regulator is capable of supplying up to 3.5A. This is sufficient to power all boards, as exceeding the rated output would also exceed the rated capacity of the PSU board.

A reduced grid spacing is required for the keys due to the larger LCD. This is reduced from 25mm (7SR1) to 20mm.

Due to the height of the components, it is not possible to mount the USB socket on the fascia. The solution is to extend the controller PCB and place a right-angle version of the connector on there. The USB connections will then poke through the plastic surround, with the shell connected to the bottom plate by a spring clip.

12.10 Board Programming

12.10.1 Usage

Some additional circuitry is required to switch the SPI bus from the micro’s SPI port to the EzPort (JTAG) pins.

12.10.2 Interfaces

The EzPort requires a chip select, clock, data in and data out. 74VHC logic should be used to provide this switching, controlled by the /PROGRAM pin gated with the /BoardSelect line.

12.10.3 Technical Data

A 74LVC244 buffer can be used to switch the 4 SPI lines between SPI and EzPort modes

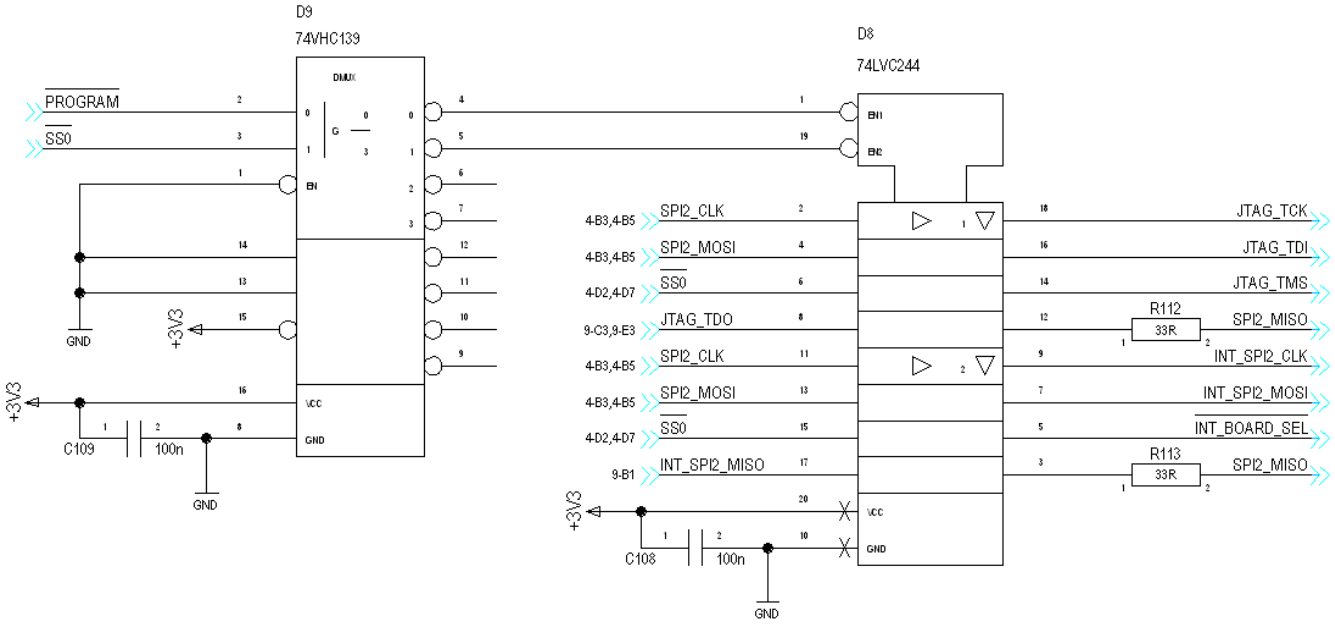


Figure 12-3 Board Programming SPI Switch

To force a board into EzPort mode, assert the /PROGRAM and /SS line for the board, then assert the /RESET line. The micro's flash will now be accessible over SPI.

12.10.4 Limits

Although this circuit uses some of the fastest discrete logic available, it delays the SPI bus clock, limiting the maximum speed of the bus to 8MHz.

12.11 Reset

12.11.1 Usage

There are two resets for the board – system reset and bus reset.

12.11.2 Interfaces

System reset is generated by the PMIC and resets the Controller. The PMIC decides when the power levels are stable and releases the processor from reset.

Bus reset is generated by the Controller and provides a controlled reset for each module.

No module can assert bus reset. Only the Controller can assert bus reset. It does this by first asserting the /RESET line on the bus, then asserting the appropriate Slave Select line (/SS0-/SS12). Only one /SS line must be active with /RESET to prevent possible problems with the MISO lines being driven by more than one card simultaneously.

12.11.3 Technical Data

The recommended circuit for each module's reset is shown in Figure 12-4.

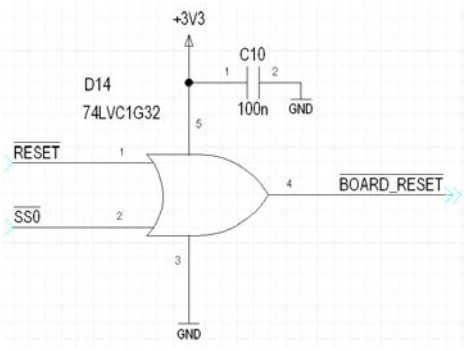


Figure 12-4 Module Reset circuit

12.11.4 Limits

It is recommended that bus reset is active for at least 5µs.

12.12 SPI Interface

12.12.1 Usage

Communication between the main CPU card and other boards in the system, i.e. CT card, Fascia, I/O boards etc, is done using an SPI interface. This allows a transfer speed up to a 12.5MHz baud rate to all of the cards. SPI is used with the main CPU card being the Master and all other cards being the Slaves.

12.12.2 Interfaces

SPI requires 4 I/O lines for operation: /CS, CLK, MasterOutSlaveIn (MOSI), and MasterInSlaveOut (MISO).

1. /CS: Active low signal – should be pulled high with a pull-up resistor.

2. CLK: the SPI clock. This should be configured with a pull-up resistor and the clock polarity should be set to an inactive state of value high (CPOL = 1). The Clock Phase should be set to capture data on the leading edge and change data on the following edge (CPHA = 0).

3. MOSI: data transmitted from Master to Slave – should have a pull-up resistor fitted.

4. MISO: data transmitted from Slave to Master – should have a pull-up resistor fitted.

Initially the baud rate should be set to a maximum of 1MHz to enable initialisation of the Slave card.

12.12.3 Technical Data

12.12.3.1 SPI Mode of Operation

The SPI supports three modes of operation: Header Mode, Control Mode and Operate Mode.

Header Mode is used to establish communication between the Master and Slave. It is a read only mode and allows the Master to retrieve information from the Slave regarding the operation of the SPI, the board ID and manufacturing information and also configuration about the register memory. It does not allow access to the register memory. This frame format uses a Modulo-256 checksum on the data it has transmitted and also for the data it has received ensuring that the data has been transferred correctly.

Control Mode uses the same basic frame type as the Header Mode except that it allows both reading and writing of the register memory. It can be used to initialise and transfer data between the Master and Slave cards.

Operate Mode is used once the Slave card has been initialised when in Control Mode. This mode can only be entered by sending a special Control Mode frame. Operate Mode is designed for speed to minimise access time to the card and it allows the Master and Slave to transfer bi-directional or uni-directional data. This is defined by the Slave card.

12.12.3.2 Register Memory

Each Slave card will present data to the Master and receive data from it using a register based architecture. The register memory is split into 3 sections: Header Info Block, Operate Mode Block, and the Data Register Block.

The Header Info Block provides information about how the SPI works, how the Operate Mode works, and also the size of the Data Register Block of memory. It is split into 2 sub-blocks with the first being the SpiInfo block and the second the BoardInfo block. The Header Info Block is used during the initialisation sequence and is accessed when in Header Mode.

The next block of register memory is the Operate Mode Block which under normal circumstances is only available when accessed in Operate Mode. The size of this memory is defined in the BoardInfo register block.

Finally is the Data Register Block of memory that is used for configuration/status information of the Slave device. This block of memory can have a maximum size of 1024 bytes. These registers are accessed when in Control Mode and the size of this memory is defined in the BoardInfo register block.

The Operate Mode Block and the Data Register Block are defined by the type of card (see design documentation for specific card) but the Header Info Block is fixed and each card type must adhere to it.

An example of the register memory is shown in Figure 12-5 where the number of Data Registers is 255 and the number of bytes to transfer in Operate Mode is 4.

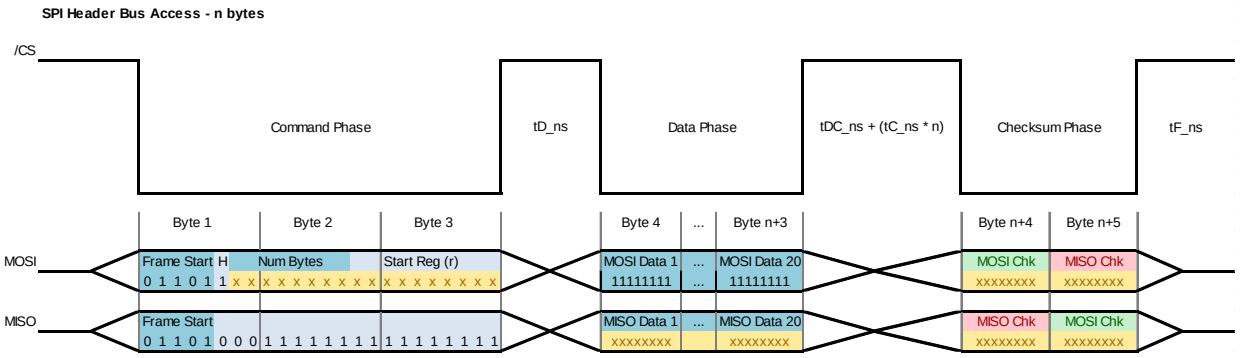
Memory Address H = 0	Memory Address H = 1		Size	Flags H	Flags O	Flags R	Access	Description	
		Header Info							
-	0	SpiInfo	4	1	-	-	RO	Maximum baud rate supported	
-	4		4	1	-	-	RO	tD_ns - Command to data delay	
-	8		4	1	-	-	RO	tDC_ns - Min data to checksum delay	
-	12		4	1	-	-	RO	tC_ns -Char delay before checksum	
-	16		4	1	-	-	RO	tF_ns - Time between frames	
-	20	BoardInfo	2	1	-	-	RO	Board ID	
-	22		32	1	-	-	RO	Board Name	
-	54		2	1	-	-	RO	Number of data registers	
-	56		2	1	-	-	RO	Number of Operate registers	
	58		1	1	-	-	RO	Register Memory Version & Checksum Type	MSB defines the checksum type. 1=Fletcher16, 0=Module 25
-	59		1	1	-	-	RO	Operate mode Master To Slave Enabled	
-	60		1	1	-	-	RO	Operate mode Slave To Master Enabled	
-	61		20	1	-	-	RO	Board Article Number	Programmed by MF
-	81		20	1	-	-	RO	MF Number	Programmed by MF
-	101		20	1	-	-	RO	Software Article Number	
-	121		20	1	-	-	RO	Test Date	Programmed by MF
-	141		20	1	-	-	RO	Test Time	Programmed by MF
-	-	Operating Registers							
			4	-	1	-	RO	Operating mode - Slave To Master Data	
-	-		4	-	1	-	WO	Operating mode - Master To Slave Data	
		Data registers							
0	-		254	0	0	x	R/W	Register memory - usages will be defined by the card type	
...	...		...	...	...	...			
254	-		1	0	0	x	R/W	Last data register	

H Header Mode - 1 = Access header information, 0 = Access data registers
O Operating Mode - 1 =Operate mode, 0 = Control Mode
R Read/write mode - 1 = read, 0 = write

Figure 12-5 Slave Card Register Memory

12.12.3.3 Header Mode Access

In Header Mode the Master device can access the header information memory on the Slave device using the frame format shown in Figure 12-6. It is a read only mode so only data can be transferred from the Slave device to the Master device.



Frame Start	0x0d – defines this is a Header/Control Mode Frame
H	Header Access: 1 = Access header information
MOSI Chk	Modulo-256 checksum of the MOSI data transmitted by the Master
MISO Chk	Modulo-256 checksum of the MISO data transmitted by the Slave

Figure 12-6 SPI Header Mode Access

NOTE: Accessing memory past the Header Info block is indeterminate and should not be used.

The Header Mode consists of 3 phases: Command, Data, and Checksum. The Command phase consists of the frame start, the Header Mode access flag (H), the number of bytes (n) to read/write and the start address of the first register to access (r).

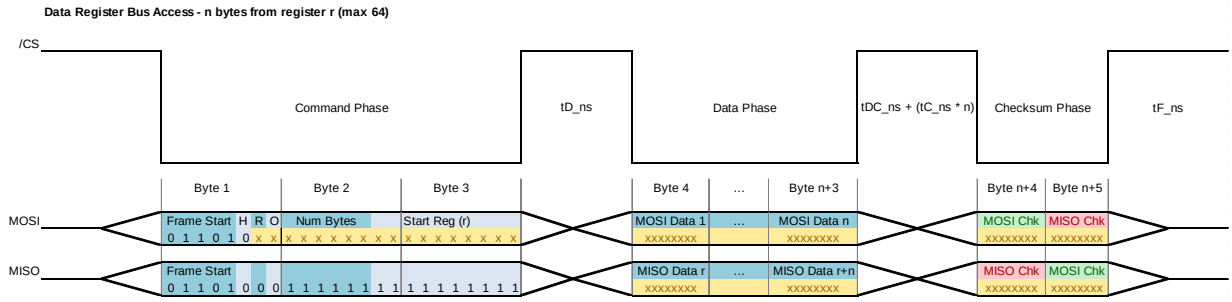
The Data phase transmits n bytes of data (maximum 256 bytes) from the Slave to the Master starting from register r specified in the Command phase. During this phase the Master will transmit the 0xFF to the Slave and the Slave will transmit the data contained in the header register memory to the Master.

The final Checksum phase is used to ensure that the data transferred between Master and Slave is valid. Both Master and Slave will calculate the Modulo-256 checksum of the data they have transmitted and also of the data they have received. These values can then be used to check the transfer was error free. E.g. After transmitting the data from the Command and Data phases the Master first transmits the checksum of the data it has previously sent (MTx). Immediately after this the Master will then transmit the checksum of the data it has received from the Slave (MRx). Likewise the Slave will transmit the checksum of the data it has transmitted (STx) followed by the checksum of the data it has received (SRx). At this point both devices have the checksum of the data they transmitted and also the checksum of what the other end calculated when it received the data. For a valid frame MTx = SRx and MRx = STx.

The timings between each phase (tD_ns, tDC_ns, tC_ns, tF_ns) is defined by the Slave device during the initialise routine.

12.12.3.4 Control Mode Access

In Control Mode the Master device can access the register memory on the Slave device using the frame format shown in Figure 12-7. This is a similar frame format as used when in Header Mode except the number of bytes that can be transferred is reduced from 256 to 64 and two control flags are available in the frame: R(ead) and O(perate Mode).



Frame Start	0x0d – defines this is a Header/Control Mode Frame	
H	Header Access:	0 = Access data registers
R	Read/write mode:	1 = Read, 0 = Write
O	Operate Mode:	1 = Switch to Operate Mode, 0 = Control Mode
MOSI Chk	Modulo-256 checksum of the MOSI data transmitted by the Master	
MISO Chk	Modulo-256 checksum of the MISO data transmitted by the Slave	

Figure 12-7 SPI Control Mode Access

In the command phase there are two extra flags available: R – read/write (flag used to indicate the direction of the data transfer) and O – Operate Mode (used to put the bus into Operate Mode).

The Data phase transmits n bytes of data (maximum 64 bytes) between the Master and Slave starting from register r specified in the Command phase. If the Read flag has been set (1) in the Command phase then the Master will transmit 0xFF to the Slave and the Slave will transmit the data contained in the data register memory to the Master. If the command issues is a write command (R = 0) then the Master will transmit the data it wants to write to the data registers and the Slave will transmit 0xFF in response.

The final Checksum phase is the same as defined in Header Mode. Once the checksums match correctly the Slave device will then proceed to store the data received into the data registers if R = 0. Data is only stored at this point to ensure that erroneous data is not stored or an impartial frame hasn't been received.

12.12.3.5 Slave Initialise

In order to establish connection between the Master and Slave devices, the Master must first retrieve information from the Slave regarding its Operate Mode. This will first be done at a maximum speed of 1MHz.

On start up the Master and Slave will be configured in Header Mode and the Master must first access the Slave's SpiInfo header information block stored in register memory. This access is done using a Header Mode frame with the Header Access flag (H) set to 1 and number of bytes requested is 20 (the size of the SPI information block) with a Start Reg (r) of 0. During this phase tD_ns, tDC_ns, and tF_ns should be a minimum of 10ms, and tC_ns can be set to 0.

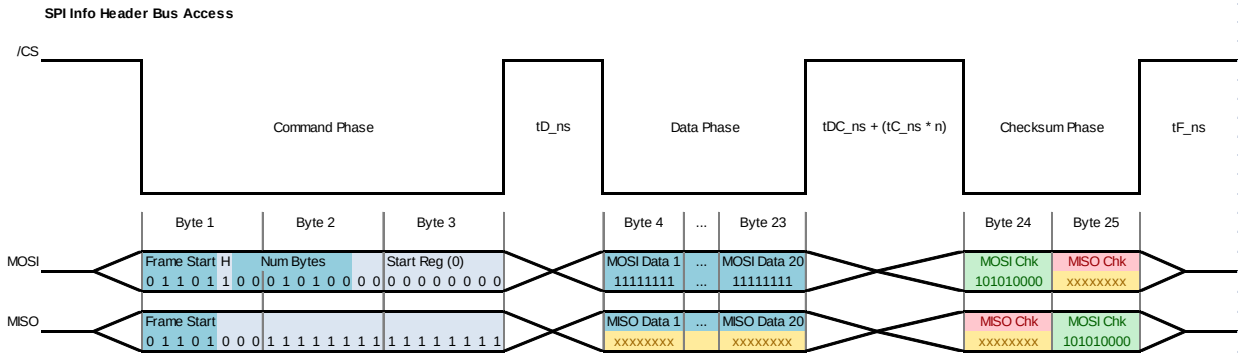


Figure 12-8 Header Mode Access to Spi Info Memory Region

Once the SpiInfo header block has been retrieved then the Master can switch to the maximum baud rate and start using the delays specified in the SpiInfo header block. Now the Master needs to get information about the Slave board itself by accessing the BoardInfo Header block. Again this is done using the Header Mode frame with H=1, the number of bytes to transfer set to 101 and the Start Reg (r) being 20.

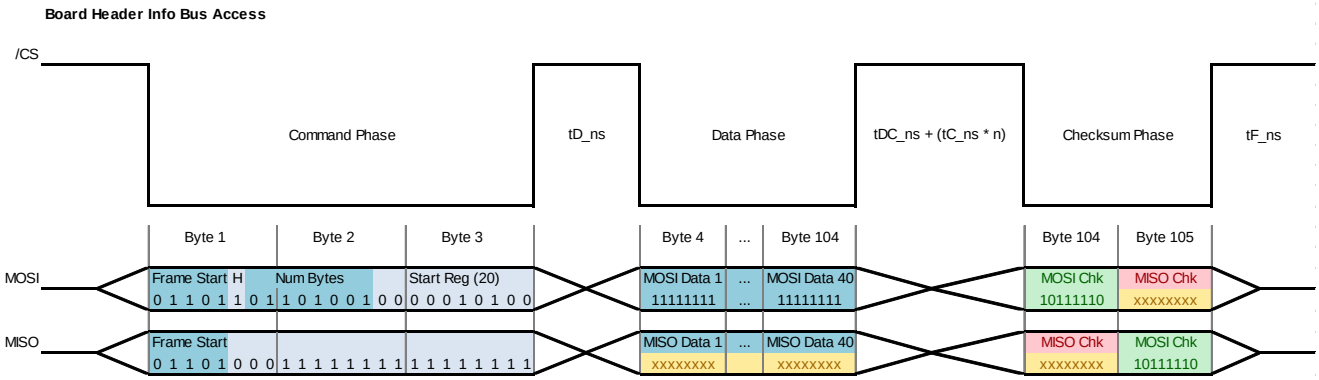


Figure 12-9 Header Mode Access to Board Info Memory Region

12.12.3.6 Slave Configuration

Once the Slave device is initialised and identified the Master can then start to configure the Slave by reading/writing to the Data Register block of memory using Control Mode frames with H=0 and O=0. The definition of the Data Register memory is dependent upon the type of card – see design documentation for the individual card.

12.12.3.7 Changing from Control Mode to Operate Mode

After the communication has been established between the Master and Slave using Header Mode and the device has been initialised using Control Mode then the Master can switch the Slave into Operate Mode if it is supported. This is done by using a Control Mode frame format as shown in Figure 12-10.

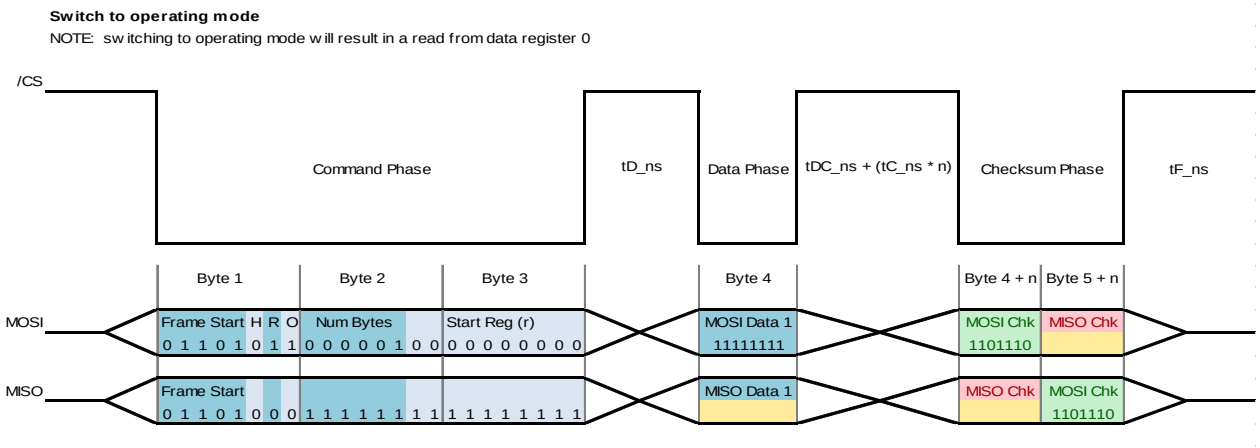


Figure 12-10 Switching from Control Mode to Operate Mode

The frame flags must be set as H=0, O=1, R=1 and it should be noted that switching to Operate Mode will result in a read from data register 0. This read can be discarded and ignored. After this command has been issued then all subsequent commands must be in Operate Mode.

12.12.3.8 Operate Mode

Once the Slave device is initialised and configured the Master and Slave may then swap to Operate Mode. This mode uses a simpler frame format than the Control Mode format and only uses 1 access phase instead of 3. This size of the frame is determined by information stored in the Slave header block and remains fixed. The frame is intended to enable fast access for transfers between the Master and Slave devices. The checksum used for data integrity of the frame can be one of two and is defined in the header register Register Memory Version & Checksum Type. The checksum type is determined by the MSB in this 8-bit registers. If set to 1 then a Fletcher-16 checksum will be used and if set to 0 then a Modulo-256 checksum is used.

Fletcher-16 checksums use 2-bytes for a checksum and Modulo-256 use 1-byte and the algorithms are shown below.

Modulo-256 Checksum

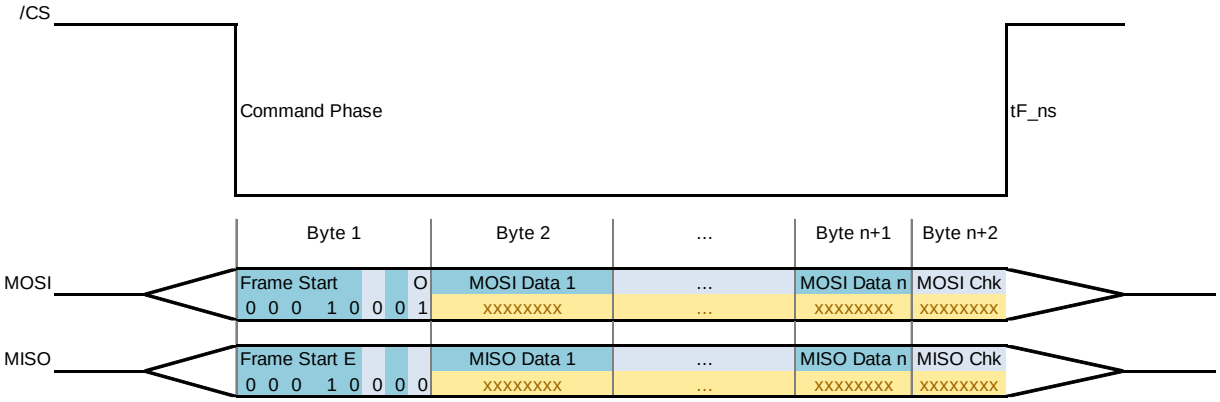
```
byte Checksum = 0;


for (int Loop = 0; Loop < NumberOfRegisters; Loop++)
  {
  Checksum += Data[Loop];
  }
```

Fletcher-16 Checksum

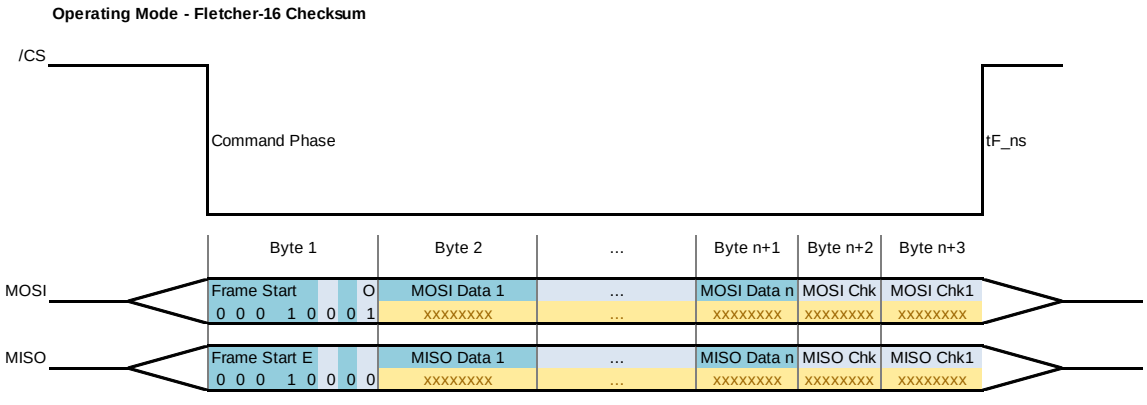
```
UWORD16 Checksum  = 0;
UWORD16 Checksum1 = 0;
for (int Loop = 0; Loop < NumberOfRegisters; Loop++)
  {
  Checksum  += Data[Loop];
  Checksum1 += Checksum;
  }
Checksum  = Checksum  % 255;
Checksum1 = Checksum1 % 255;
```

Operating Mode - Module-256 Checksum



Frame Start	0x02 – defines this is an Operate Mode Frame
E	Extra bit of Frame Start used to indicate previous frame received had an error detected
O	Operate Mode: 1 = Operate Mode
MOSI Chk	Modulo-256 checksum of the MOSI data transmitted by the Master
MISO Chk	Modulo-256 checksum of the MISO data transmitted by the Slave.

Operating Mode - Fletcher-16 Checksum



Frame Start	0x02 – defines this is an Operate Mode Frame
E	Extra bit of Frame Start used to indicate previous frame received had an error detected
O	Operate Mode: 1 = Operate Mode
MOSI Chk, MOSI Chk1	Fletcher-16 checksum of the MOSI data transmitted by the Master
MISO Chk, MISO Chk1	Fletcher-16 checksum of the MISO data transmitted by the Slave.

Figure 12-11 Operate Mode

This frame allows n bytes of data to be transmitted from the Master to the Slave, from the Slave to the Master, or from both devices to one another at the time. The mode of operation and the number of bytes to transfer is defined during the Slave initialise routine using the DeviceInfo block:

Number of Operate registers - the number of bytes to transfer in each frame

Operate Mode Master to Slave Enabled - if TRUE then the Master can read from the Slave

Operate Mode Slave to Master Enabled - if TRUE then the Master can write to the Slave

These fields are dependent upon the type of card being access – see design document for the card.

Each frame has a Modulo-256 checksum (or Fletcher-16) that can be used by the receiving end to check if the data has arrived correctly. Unlike in Control Mode where the Master knows if the slave received its data correctly by the 2 checksums, operate mode must do this in a different way. In Operate Mode the Frame Start flag in direction of Slave to Master contains an Error Flag. This is used by the Master to detect if the previous frame received by the Slave card had any errors. For good previous frames the Frame Start should read 0x02 but if the slave detected an error in the previous frame then the Frame Start will return 0x03.

The Flags H and R are not used in this mode and O must be set to 1.

12.12.3.9 Changing from Operate Mode to Control Mode

It may be necessary to revert the communication back from Operate Mode to Control Mode so that extra configuration can be performed or extra status information can be retrieved from the Slave card. This is achieved by setting the O flag to 0 in an Operate frame. Any data transmitted from the Master to the Slave will be ignored and not acted upon. However, the data transmitted from the Slave to the Master will be valid and can be used if required. NOTE: the example below shows the checksum as a Module-256 type.

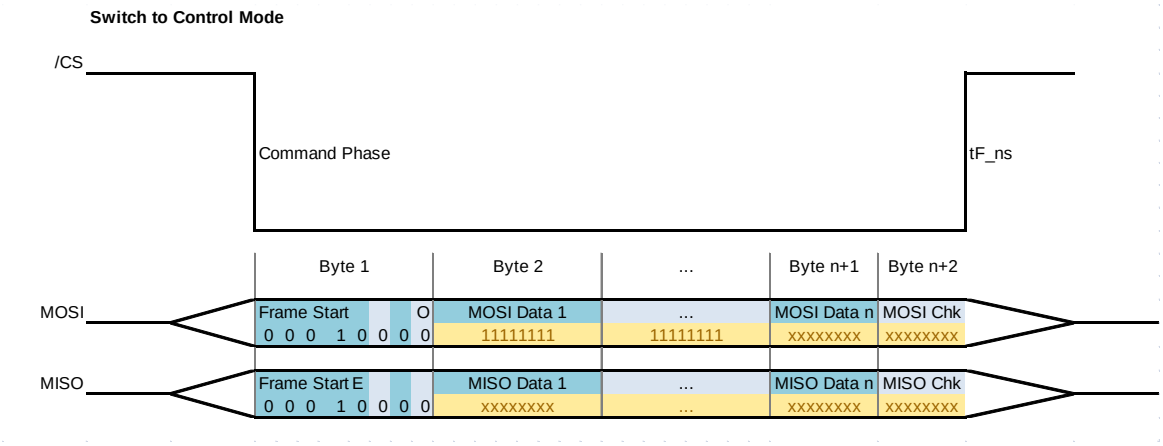


Figure 12-12 Switching from Operate Mode to Control Mode

12.12.4 Limits

Each card should support a maximum clock speed of 1MHz during the initialisation phase. Once communication has been established to the card then the operating limits of the card can be read by the master in Header Mode by accessing the SpiInfo block of register memory. See Figure 12-13 for information regarding timing limits.

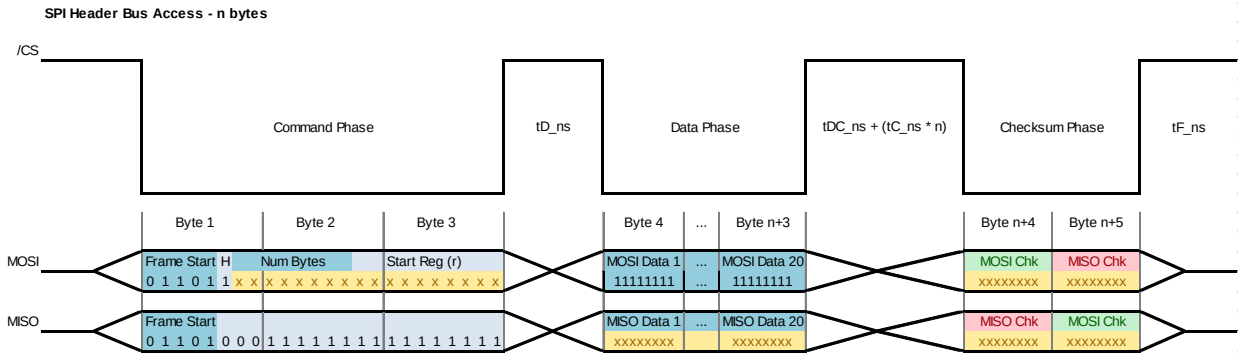


Figure 12-13 SPI limits

Below are the limits assigned by each slave card enabling access to them. These must be adhered to by the Master to ensure correct operation.

tD_ns Specifies the delay between the command phase and the data phase. After the command phase the master must wait tD_ns before starting transmission of the data phase. This enables the slave card to decode the command and prepare reception/transmission for the data.

tDC_ns Specifies the minimum delay between the data phase and the checksum phase and is used in conjunction with tC_ns.

tC_ns Specifies the delay to add per character transmitted and is used in conjunction with tDC_ns.

Both tDC_ns and tC_ns are used to calculate the delay required between the data phase and the checksum phase. This allows the slave to calculate the checksum of the received data before accepting data in the checksum phase. The more data transferred required a bigger delay. To calculate the delay use: tDC_ns + (tC_ns * number of bytes of data transmitted)

E.g if tDC_ns = 1500 and tC_ns = 100 and the number of bytes transmitted was 10 then the total delay required is 1500 + (100 * 10) = 2500ns.

tF_ns Specifies the delay before another frame can be transmitted. Before the master can transmit another frame it must wait tF_ns to allow for the slave to prepare for the next frame.

13 Technical data

Further technical data will be included in the SPC reports for each PCBA.

Note: These are the externally relevant technical data. Internally relevant technical data are listed with the respective components in chapter 12.

Table 13-1 Sample table of technical data for the 7SR5 Native 61850

Parameter	Value

14 References

/1/ NXP i.MX6SX Datasheet

/2/ NXP Kinetis K22 Datasheet

/3/ Hamilton Laboratory list of Type Tests and Standards.

/4/ 7SR5 Power Consumption

15 History

Author

Name	Department	Version	Date
Marcus Bainbridge	EM DG SPDL R&D	0.01	2016-07-12
Keith Stenson	EM DG SPDL R&D	0.02	2016-09-19
Lawrence Cuthbert	EM DG SPDL R&D	0.03	2016-09-20
Neil Dosdale	EM DG SPDL R&D	0.04	2016-09-27
Lawrence Cuthbert	EM DG SPDL R&D	0.05	2016-09-28
Neil Dosdale	EM DG SPDL R&D	0.06	2016-09-28
Mike Ellis	EM DG SPDL R&D	0.07	2016-09-28
Marcus Bainbridge	EM DG SPDL R&D	0.08	2016-10-05
Marcus Bainbridge	EM DG SPDL R&D	0.09	2016-10-06
Marcus Bainbridge	EM DG SPDL R&D	1.00	2016-10-11
Lawrence Cuthbert	EM DG SPDL R&D	1.10	2016-12-08
Lawrence Cuthbert	EM DG SPDL R&D	1.11	2017-05-22
Lawrence Cuthbert	EM DG SPDL R&D	1.20	2018-06-20
Keith Stenson	RC-GB EM DG SPD R&D 2	1.21	2019-01-08
Marcus Bainbridge	SI DG SA&P PR GB-R&D 1	1.30	2019-08-15

Updates

Chapters / Pages changed	Version	Object and reason of change / Reference to change requirements
	0.01	Draft release for platform direction
Chapter 12.10 added	0.02	Added SPI protocol
	0.03	Mechanical updates
	0.04	Updated sections 1-4.
Chapter 9	0.05	Added PCB size diagrams
	0.06	Added the requirements.
Sections 12.2 and 12.7	0.07	Added CT section and Earthing Concept.
	0.08	Added MII header and tidied up. Reduced PCB lengths (except CPU) by 3mm.
	0.09	Updated PCB sizes, added reference to standards, added BI input characteristics. Released for internal review.
	1.00	Released following review. See review comments.
Figures 9.x	1.10	Updated/added figures to show new PCB sizes
Figure 9.1	1.11	Position of USB hole changed to 24.00 mm
Figures 4.5 & 4.6	1.11	Updated fascias for S6 and S12
Figures 9.1 & 9.2	1.12	Updated PCB sizes for S6 and S12
Whole document	1.20	Updated all mechanical details for assemblies and PCBs

Section 12.12.3	1.21	Updated SPI frame formats to add Fletcher-16 checksum and more fields.
Whole document	1.30	Updated to include Protection Comms module. Various changes made to reflect current builds of all boards.