

SPECIFICATION

Customer : _____
Model Name: SAT070AT50D18Y0-35100T048ZN
ERP NO. : 1010700021
Spec Vision: V.2
Date: 2018/08/13

- ☒ Preliminary Specification
☐ Final Specification

Approved by	Comment

Prepared by	Reviewed by	Approved by

Record of Revision

[illegible]

Contents

1. General Specifications.....	4
2. Pin Assignment.....	5
3. Operation Specifications.....	6
3.1. Absolute Maximum Ratings.....	6
3.1.1. Recommended Operation Range.....	6
3.1.2. Backlight Driving Conditions.....	7
3.2. Power Sequence.....	8
3.2.1. Power On Sequence.....	8
3.2.2. DC characteristics	9
3.3. Timing Characteristics.....	10
3.3.1. Timing Table	10
3.3.2. Date input format.....	11
3.3.3. Timing Diagram.....	12
4. Optical Specifications.....	14
5. Reliability Test Items.....	15
6. Mechanical Drawing.....	16
7. Package Drawing.....	17
8. Numbering System.....	18

1. General Specifications

NO.	Item	Specification	Remark
1	Panel Size	7.0 inch(Diagonal)	
2	Resolution	800 x 3(RGB) x 480	
3	Driver Method	A-Si TFT active matrix	
4	Active Area	154.08(W)× 85.92(H) mm	
5	Dot Pitch	0.0642(W)× 0.1790(H) mm	
6	Pixel Arrangement	RGB-stripe	
7	Module Size	165.0(W)×100.0(H)×3.3(D) mm	
8	Display Mode	Normally White	
9	Display Color	16.7M	
10	Viewing Direction	6 o'clock	
11	Interface	TTL RGB-24Bit parallel interface	
12	Driving IC	EK9713CA+EK73002ACGB	
13	Weight	TBD	g

2. Pin Assignment

No.	Symbol	Function	Remarks
1~2	VLED+	Power for LED backlight (Cathode)	
3~4	VLED-	Power for LED backlight (anode)	
5	GND	Power ground	
6	VCOM	Common Voltage	
7	DVDD	Power for Digital Circuit	
8	MODE	DE/sync mode select	
9	DE	Data input enable	
10	VS	Vertical Sync input	
11	HS	Horizontal Sync input	
12~19	B7~B0	Blue data	
20~27	G7~G0	Green data	
28~35	R7~R0	Red data	
36	GND	Power ground	
37	DCLK	Pixel clock	
38	GND	Power ground	
39	L/R	Left/right selection	
40	U/D	Up/Down selection	
41	VGH	Gate on Voltage	
42	VGL	Gate off Voltage	
43	AVDD	Power for Analog Circuit	
44	RESET	Global reset pin	
45	NC	No connection	
46	VCOM	Common Voltage	
47	DITHB	Dithering function	
48	GND	Power ground	
49~50	NC	No connection	

3. Operation Specifications

3.1. Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	DV _{DD}	-0.3	5.0	V	
	AV _{DD}	6.5	13.5	V	
	V _{GH}	-0.3	40.0	V	
	V _{GL}	-20.0	0.3	V	
	V _{GH} -V _{GL}	-	40.0	V	
Operation Temperature	T _{OP}	-20	55	°C	
Storage Temperature	T _{ST}	-20	60	°C	

Note: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings case ,the module may be permanently destroyed.

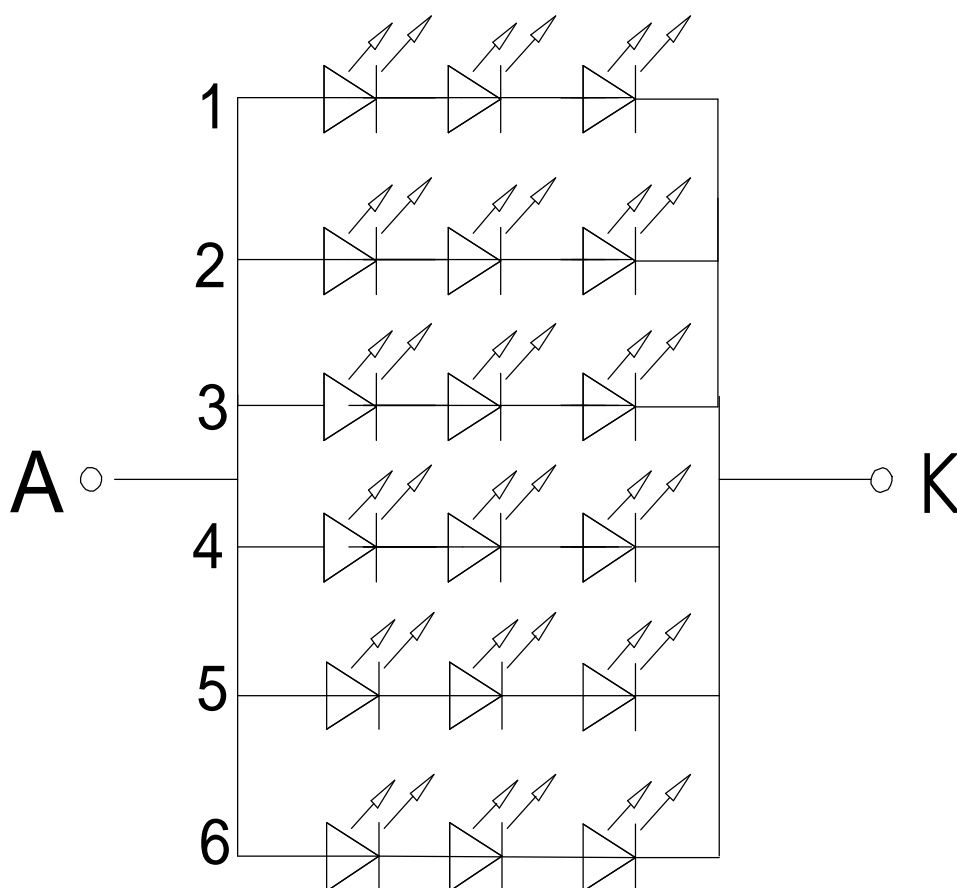
3.1.1. Recommended Operation Range

(Note 1)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV _{DD}	3.0	3.3	3.6	V	Note 2
	AV _{DD}	9.80	10.0	10.2	V	
	V _{GH}	15	16	17	V	
	V _{GL}	-7.7	-7.0	-6.3	V	
Input signal voltage	V _{COM}	3.9	4.1	4.2	V	Note 4
Input logic high voltage	V _{IH}	0.7 DV _{DD}	-	DV _{DD}	V	Note 3
Input logic low voltage	V _{IL}	0	-	0.3 DV _{DD}	V	

3.1.2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage of white LED backlight	V_L	8.7	9.6	10.5	V
Current for LED backlight	I_L	90	120	150	mA
Luminance (on the module surface ,BM-7)		190	250	-	cd/m ²
LED life time	-	50000	-	-	Hr



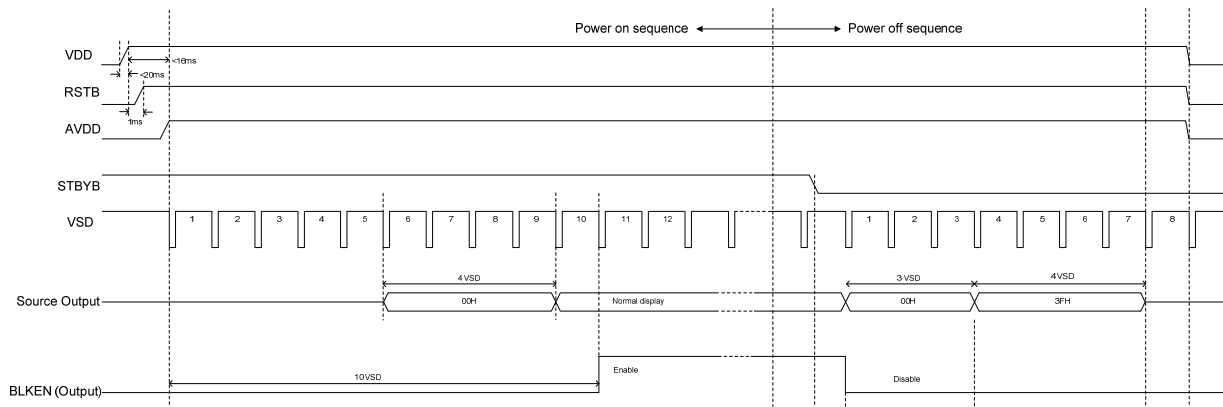
3.2. Power Sequence

3.2.1. Power On Sequence

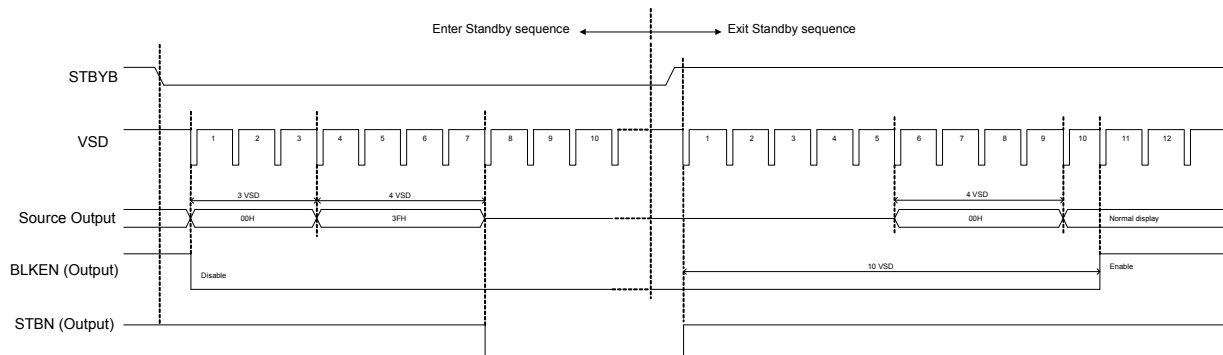
Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

This is another paragraph of sub-function description.



Power-On/Off Timing Sequence



Enter and Exit Standby Mode Sequence

3.2.2. DC Characteristics

DC Characteristics

(TA = -20 to 85°C, VDD = 1.8 to 3.6V, AVDD = 6.5 to 13.5V, GND = AVSS = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD-0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	GND+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD=3.3V	150K	250K	350K	ohm
Digital Operation current	Idd	Fclk=40 MHz, FLD=37.88KHz, VDD=3.3V	-	8	10	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=40MHz, FLD=37.88KHz @ AVDD=10V, V1=8V, V14=0.4V	-	10	12	mA
Analog Stand-by current	Ist2	No load, Clock and all functions are stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input	0.4×AVDD	-	AVDD-0.1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input	0.1	-	0.6×AVDD	V
Output Voltage deviation	Vod1	Vo = AVSS+0.1V ~ AVSS+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AVSS+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AVSS+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ SO1200	0.1	-	AVDD-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ SO1200; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ SO1200; Vo=13.4V v.s 12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7×Rn	1.0×Rn	1.3×Rn	ohm

3.3. Timing Characteristics

3.3.1. Timing table

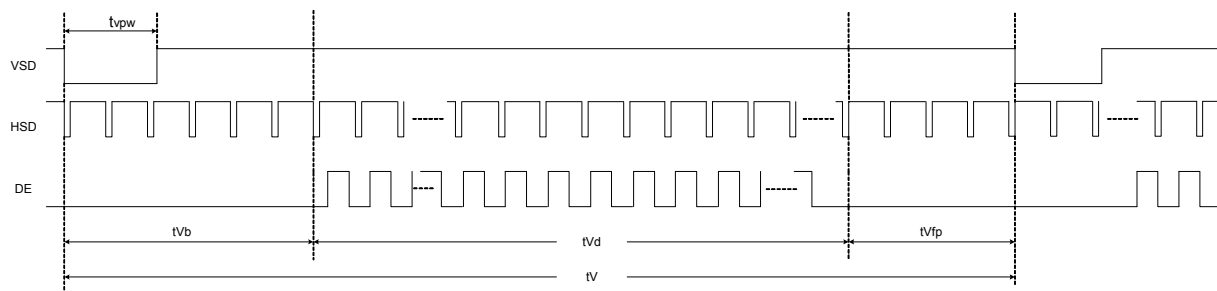
Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency		fclk	Min.	Typ.	Max	MHz
			-	33.3	50	
1 Horizontal Line		th	862	1056	1200	DCLK
HSD pulse width	Min.	thpw	1			
	Typ.		-			
	Max.		40			
HSD Back Porch (Blanking)		thb	46	46	46	
HSD Front Porch		thfp	16	210	354	

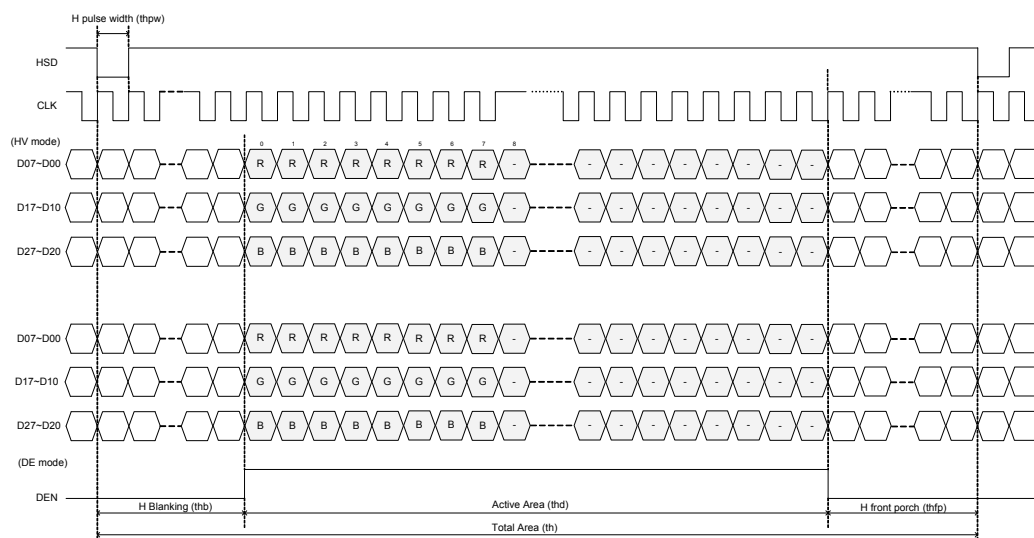
Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical display area	tvd	480			H
VSD period time	tv	510	525	650	H
VSD pulse width	tvpw	1	-	20	H
VSD Back Porch (Blanking)	tvb	23	23	23	H
VSD Front Porch	tvfp	7	22	147	H

3.3.2. Date input format

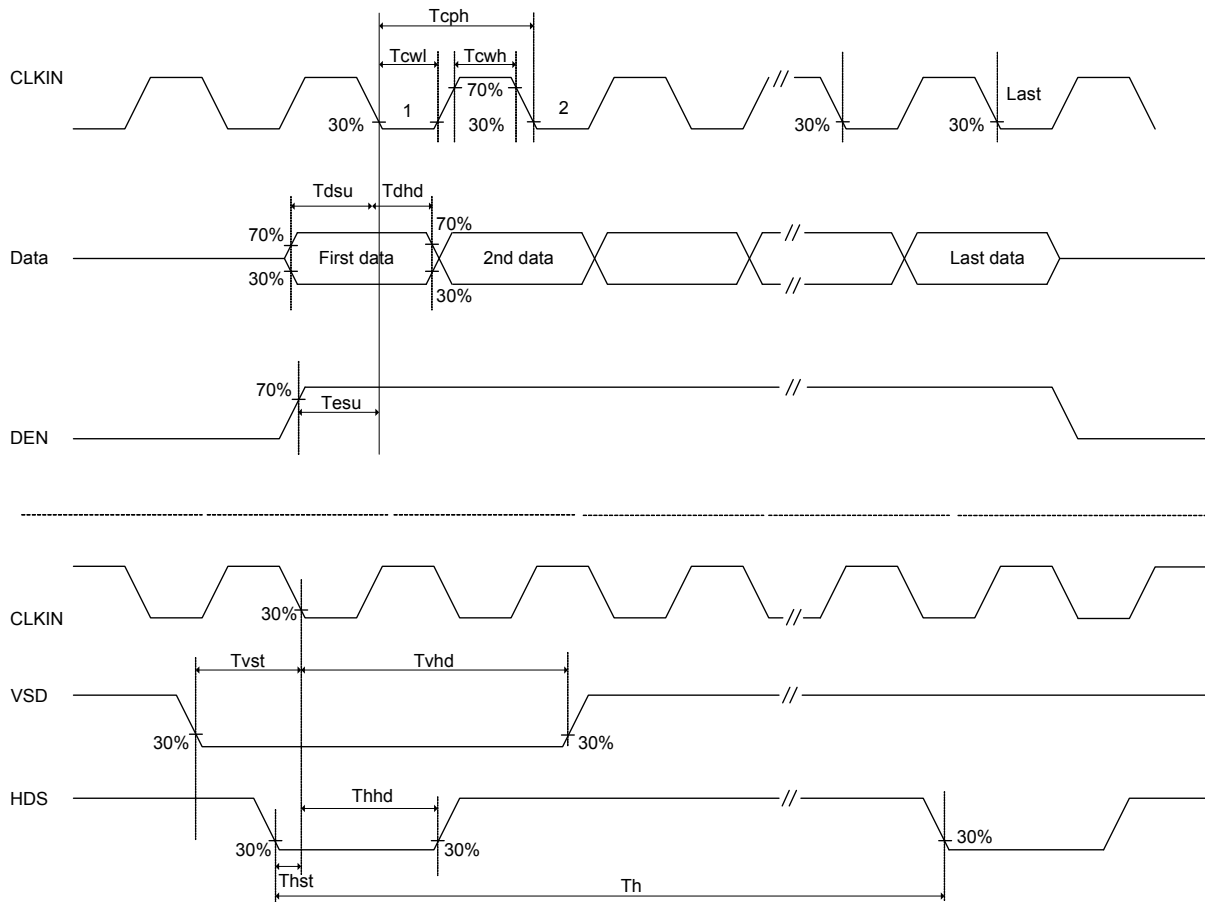


Vertical input timing

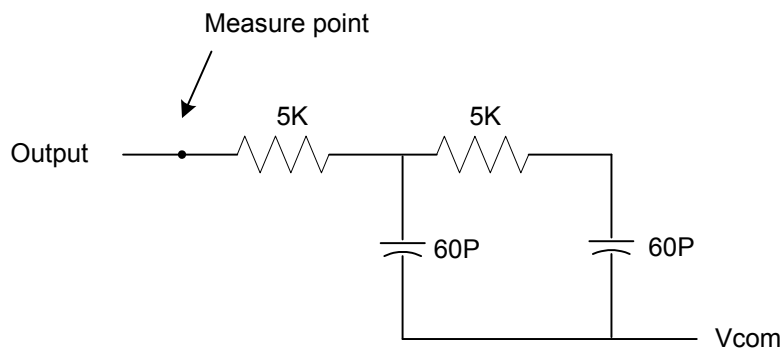


Horizontal input timing

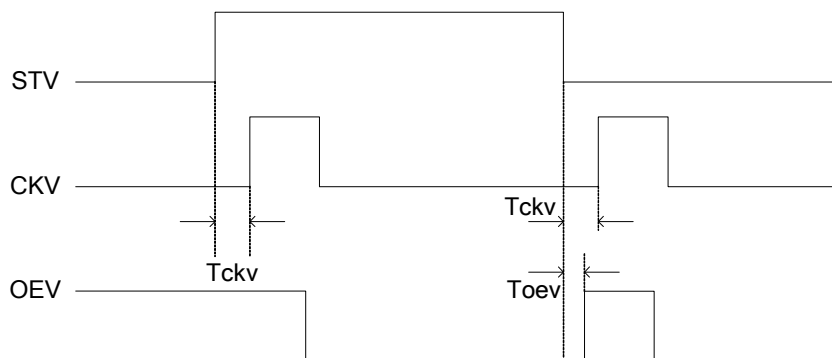
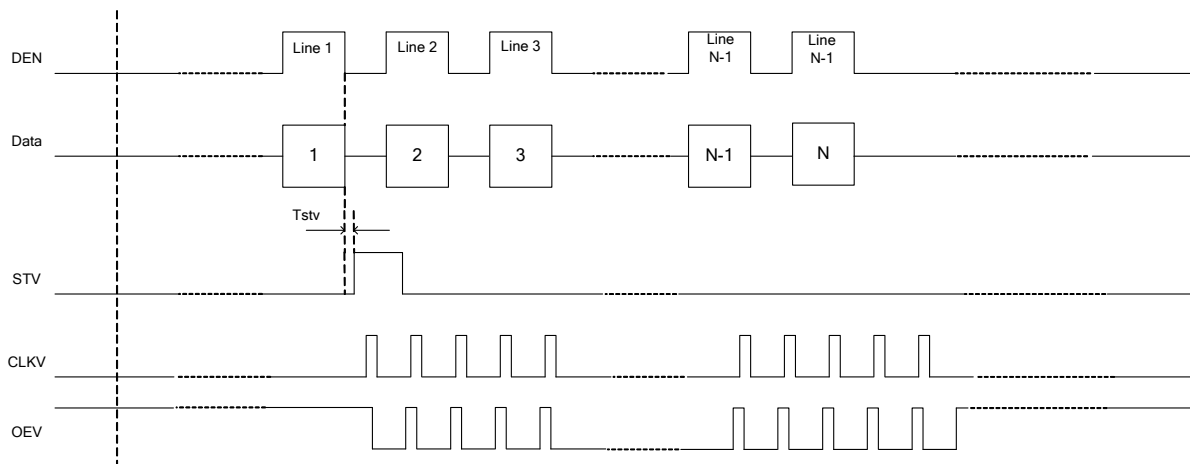
3.3.3. Timing Diagram



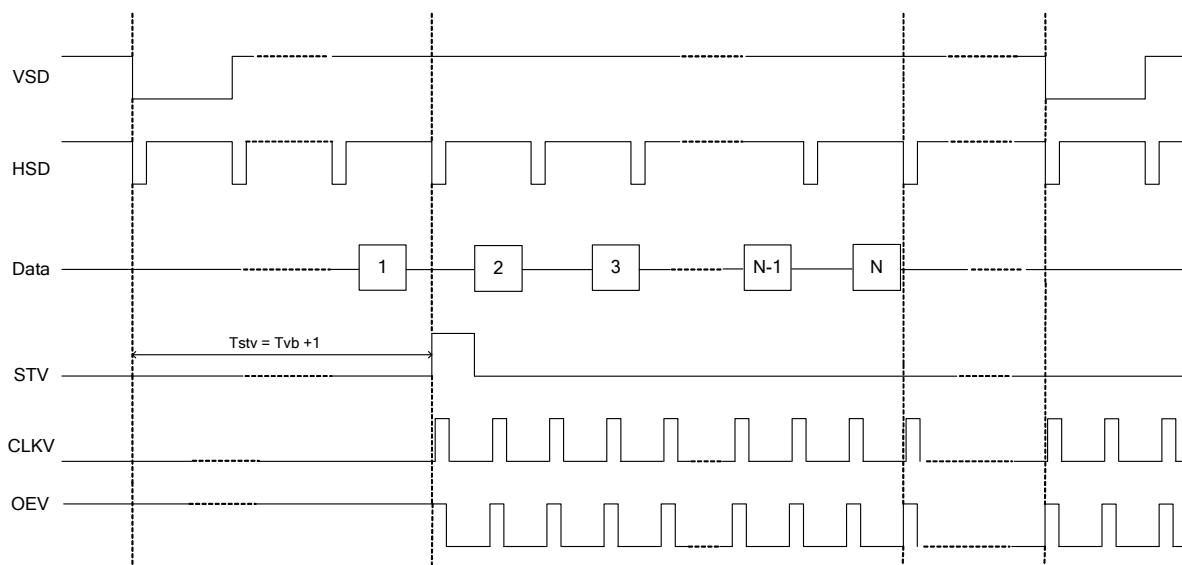
Input Clock and Data Timing Diagram



Output load condition



Vertical Timing Diagram DE



4. Optical Specifications

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles	θT	$CR \geq 10$	30	40	--	Degree	Note1
	θB		40	45	--		
	θL		40	45	--		
	θR		40	45	--		
Contrast Ratio	CR	$\theta=0^\circ$	400	500	--		Note4
Response Time	T_{ON}	25℃	--	10	20	ms	Note3
	T_{OFF}		--	15	30		
Chromaticity	White	Backlight is on	0.278	0.285	0.338		Note2 Note5 Note6
			0.297	0.306	0.357		
Luminance	L		190	240	--	cd/m ²	Note6

Test Conditions:

1. $DV_{DD}=3.3V$, $I_L=120mA$ (Backlight current),the ambient temperature is 25℃.
2. The test systems refer to Note 2.

5. Reliability Test Items

Item	Test Conditions		Remark
High Temperature Storage	Ta=60℃	120h	Note1 ,Note4
Low Temperature Storage	Ta=-20℃	120h	Note1, Note4
High Temperature Operation	Ts=55℃	120h	Note2 ,Note4
Low Temperature Operation	Ts=-20℃	120h	Note4
Operation at High Temperature and Humidity	+60℃,90%RH	120h	Note4
Thermal Shock	-20℃/30min~+60℃/30min for a total 100 cycles , Start with cold temperature and end with high temperature		
Package Drop Test	Height 60cm 1corner , 3edges , 6surfaces		
Elector Static Discharge	±2KV,Human Body Mode, 150pF/330 Ω		

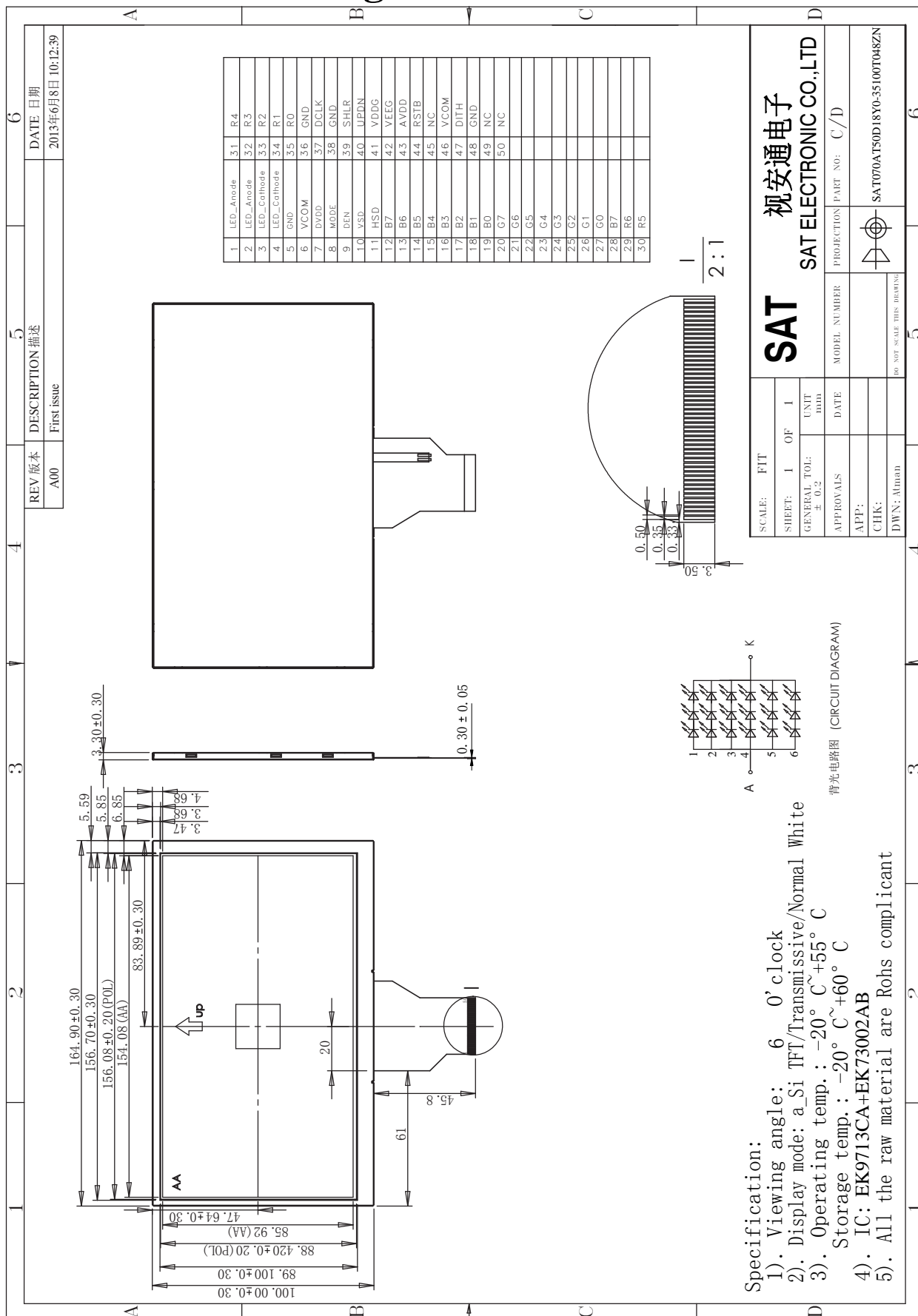
Note1: Ta is the ambient temperature of samples.

Note2: Ts is the temperature of panel's surfaces.

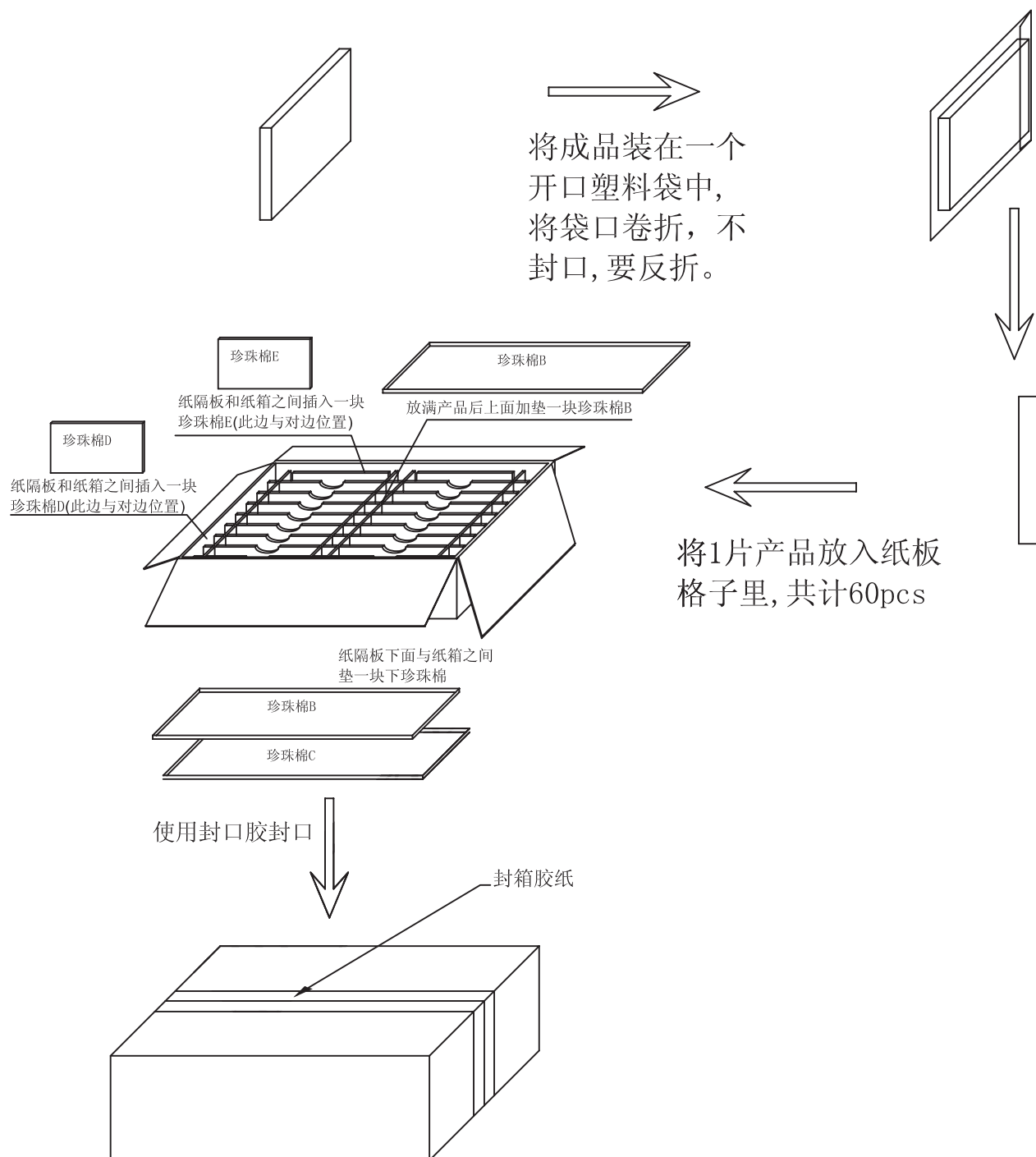
Note3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all of the cosmetic specification.

Note4: before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

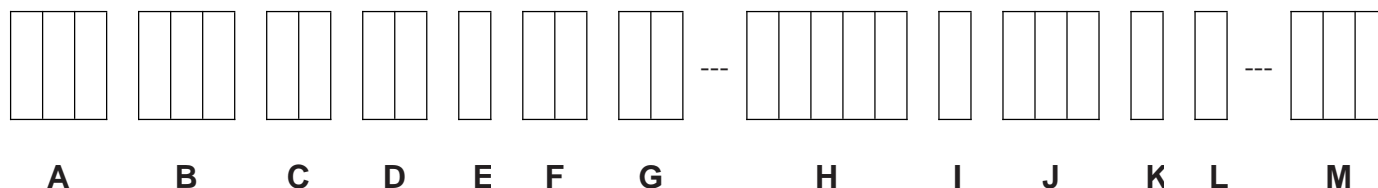
6. Mechanical Drawing



7. Package Drawing



8. Numbering System



NO.	Definition	Specifications
A	Company code	SAT INTERNATIONAL CO.LTD.
B	Display monitor opposite angle line size	Unit : inch (size<10inch:take two integers;size>=10inch:takes three integers)
C	LCD Brands	AU-AUO; CP-CPT; IV-IVO; TM-TIANMA; HS-HSD; CM-CMO; BO-BOE; AT--INNOLUX;
D	Interface PIN Number	Arabic numerals from 01 to 99
E	LCD Type	A--Alternated Video Signal; D--Data Video Signal; H--High Definition ; I--IPS
F	Backlight LED Number	Arabic numerals from 01 to 99
G	Backlight Color Are	Include R1、R2、Y0、Y1、B1、B2;
H	Structure Size	Include module length and width size
I	Interface Mode	T:TTL L:LVDS M:MIPI
J	FPC Length	It represents the length of FPC with three figures, divided into long rows ,middle rows and short rows
K	View Angles	Z : represent narrow viewing angle K : represent wide viewing angle I : represent all viewing angle
L	Operating Mode	D: DE mode V: VSD mode F: Inverting mode N: No mode requirements
M	Suffix	1. NULL ; 2. TP/CTP-- Touch panel; 3. other--Insignificance