|  |  |
| --- | --- |
| LILLEBAKK cmyk |  |

Datasheet

Project NAME: LE\_NB\_IOT\_CONTROLLER

Customer: <AAA\_BBB\_CCC\_NX>

Features

* …
* …
* …
* …
* …
* …

Table 2: Key parameters

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Supply voltage** | **Placement** | **ΔX (largest)** | **ΔY (largest)** | **ΔZ (largest)** | **Sertifications** |
| <xxx V> | <Core/ IO> | <xxx µm> | <xxx µm> | <xxx mm2> | <Yes / No> |

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# Module Interface

Table 3: Pin description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin name** | **Type** | **Domain (V)** | **Description** | **Comments** |
| mix33vdd! | Power | - | Power supply |  |
| mix33vss! | Power | - | Ground |  |
| vdd! | Power | - | Power supply |  |
| vss! | Power | - | Ground |  |
| i12input | Digital input | vdd! |  |  |
| o12output | Digital output | vdd! |  |  |
| aio33input | Analog input | mix33vdd! |  |  |
| aio33output | Analog output | mix33vdd! |  |  |
| ci33input | Current input | mix33vdd! |  |  |
|  |  |  |  |  |

# Electrical Characteristics

Verification levels:

1. Specification
2. Schematic simulation- PVT with 100 MC runs
3. Post layout simulation - PVT only
4. Characterization – will be part of the device characterization – see link in Table1. Optional to be added!

Table 4: Electrical characteristics

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Test name** | **Parameter name** | **Condition** | **Ver. level** | **Min** | **Typical** | **Max** | **Unit** |
| **Operating Conditions** | | | | | | | | |
| Ambient temperature |  |  | Within specification | I | Tbd | 25 | Tbd | °C |
| Functional | I | Tbd |  | Tbd |
| Battery voltage |  | Vbat |  | I | tbd | 3,6 | tbd | V |
| Ground |  | Gnd |  | I |  | 0 |  | V |
| Supply voltage sensor |  | Vsense |  | I |  | tbd |  | V |
| Supply voltage MCU[[1]](#footnote-1) |  | Vmcu |  | I | 3,1 | 3,8 | 4,2 | V |
| Supply voltage RF |  | Vrf |  | I |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| **DC Characteristics** | | | | | | | | |
| BOD level |  |  |  | I | Tbd |  |  | V |
| II |  |  |  |
| III |  |  |  |
|  |  |  |  | I |  |  |  |  |
| II |  |  |  |
| III |  |  |  |
| **Transient Characteristics** | | | | | | | | |
| Power on reset time |  | Tpor |  | I | 535 |  |  | us |
| II |  |  |  |
| III |  |  |  |
|  |  |  |  | I |  |  |  |  |
| II |  |  |  |
| III |  |  |  |
| **AC Characteristics** | | | | | | | | |
|  |  |  |  | I |  |  |  |  |
| II |  |  |  |
| III |  |  |  |
|  |  |  |  | I |  |  |  |  |
| II |  |  |  |
| III |  |  |  |
| **Notes** | | | | | | | | |
| Note 1: <Notes on electrical characteristics> | | | | | | | | |

## Parameter definitions

<This is more detailed explanations on parameters>

## Verification Plan

<Delete this text and add a verification plan here – what is verified how (distinguish between schematic and PLS)>

## Simulation result plots

### DC Simulations

<Delete this text and paste DC simulation plots here (max recommended width on pictures is 25cm)>

### Transient Simulations

<Delete this text and paste TRAN simulation plots here (max recommended width on pictures is 25cm)>

### AC Simulations

<Delete this text and paste AC simulation plots here (max recommended width on pictures is 25cm)>

# Deliverables

Table 5: Design schematics

|  |  |  |
| --- | --- | --- |
| **Library** | **View** | **Comments** |
| [<library name>](http://syncserver-lib-nor1.norway.atmel.com:26611/scripts/isynch.dll) | <view name> |  |

Table 6: Design testbenches

|  |  |  |  |
| --- | --- | --- | --- |
| **Library** | **ADE XL view** | **Test name** | **Comments** |
| [<library name>](http://syncserver-lib-nor1.norway.atmel.com:26611/scripts/isynch.dll) | <view name> | dc\_test\_name\_1 |  |
| “ | “ | tran\_test\_name\_2 |  |
| “ | “ | ac\_test\_name\_3 |  |

# Module Background

This module is based upon the LPWAN SRD: [..\LE\_LPWAN\_SYSTEM\doc\lpwan\_system\_requirement.docx](../LE_LPWAN_SYSTEM/doc/lpwan_system_requirement.docx)

## Dependencies

<This module is dependent on such-and-such libraries/modules>

## Derivate

<This module has been derived from so-and-so module designed in such-and-such technology>

## Relevant Literature

<This is the literature based on which this module was designed>

## Footprint

<Delete this text and paste the layout snapshot picture here (max recommended width on pictures is 25cm) >

Figure 1 : Layout snapshot of the module.

# Control Modes

Table 7: States

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | | |  |
| **i12intputA** | **i12intputA** | **i12intputC** | **o12output** | **ao33outputA** | **ao33outputB** | **Comments** |
| 0 | X | 0/1 | 0 | 0 | 0 |  |
| 1 | 0 | 0/1 | 0 | Not valid | 0 |  |
| 1 | 0 | 0/1 | 1 | 1.1V | 0 |  |
| 1 | 1 | 0/1 | 0 | Not valid | Not valid |  |
| 1 | 1 | 0/1 | 1 | 1.1V | 750mV |  |

Table 8: Calibration

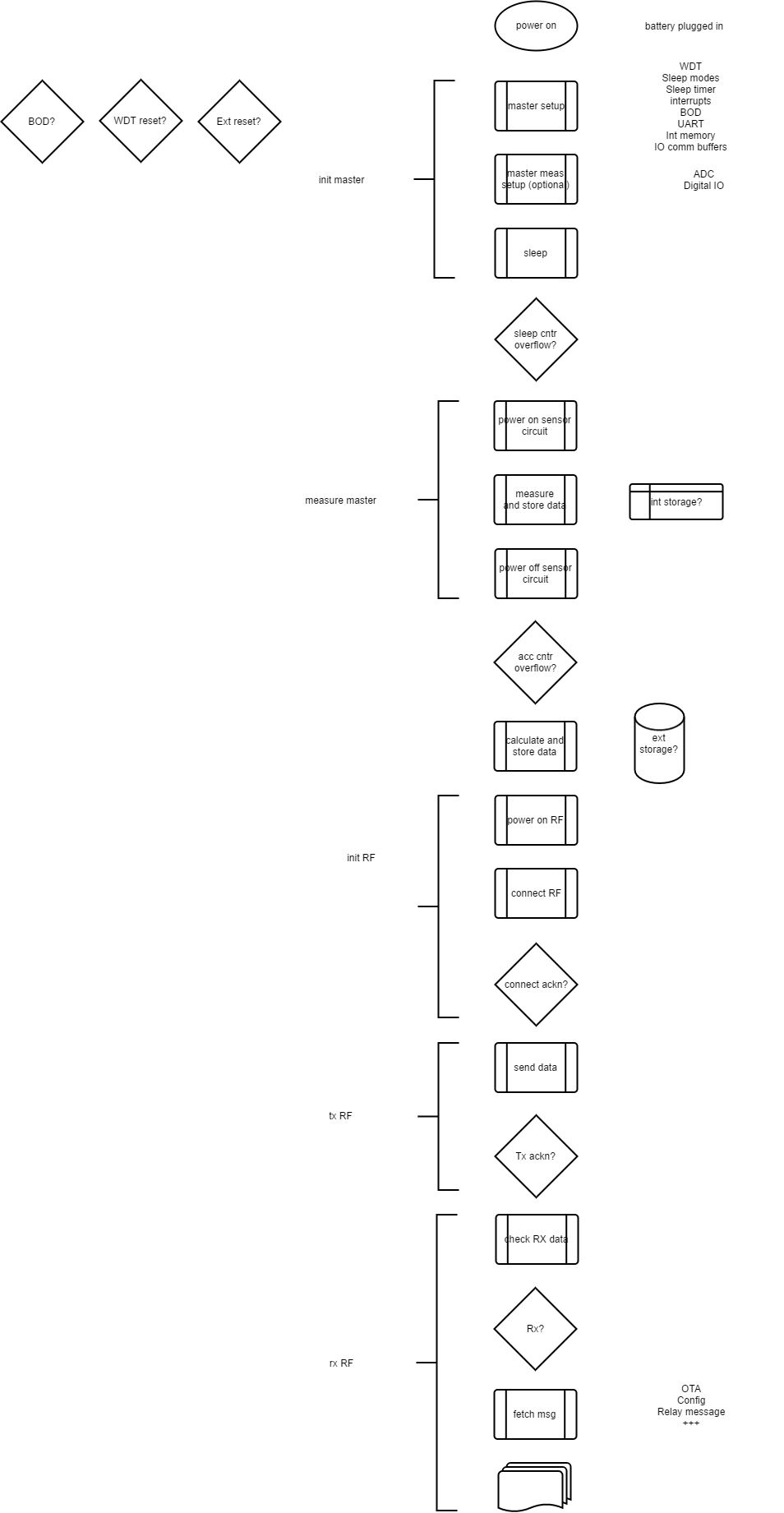
|  |  |  |  |
| --- | --- | --- | --- |
| **Signals** | **Descriptions** | **Settings** | **Results** |
| i12inputD<3:0> |  | 0000 |  |
| “ |  | 0001 |  |
| “ |  | 0010 |  |
| “ |  | 0100 |  |
| “ |  | 1000 |  |

# Operation system description

AT commands are listed in: quectel\_docs\Quectel\_BC95\_AT\_Commands\_Manual\_V1.0.pdf

## Operation system overview

The operation system runs as shown in the below flow chart.



## Error messages

Tbd.

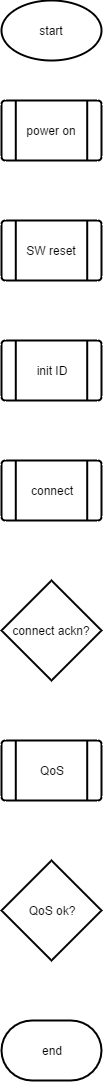
## Init master

MCU setup

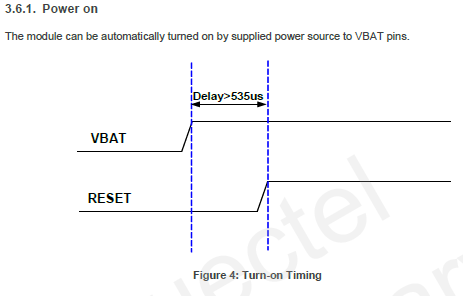
## Measure master

MCU measure

## Init RF



### Power on and HW reset



### Init ID

## Tx RF

## Rx RF

## Schematics

<Delete this text and paste snapshots of the schematics here (max recommended width on pictures is 25cm)>

# Test Plan

Table 10: Test conditions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Temperature** | **-40°C** | **Room** | **85°C** | **Range [min:step:max]** |
| X | X | X |  |
| **Analog power supply** | **2.5V** | **3.3V** | **3.6V** | **Range [min:step:max]** |
| X | X | X |  |
| **Load** | **20pF** | **260pF** | **500pF** | **Range [min:step:max]** |
| X | X | X |  |

## Test Modes for this Module

<Explain clearly what kind of test modes are implemented in the module>

## Prototype Verification and Characterization

<Explain clearly how the prototype should be verified and characterized. List and sequence the signals that should be applied for each parameter>

## Production Test

<List and explain the tests that should be carried out in production to be able to catch the defective devices.>

## Probe Points

<Delete this text and paste the layout snapshot picture with marked probe points>

Figure 2 : Probe points on the module.

Table 11: List of probe points

|  |  |  |
| --- | --- | --- |
| **Probe point #** | **Node** | **Test usage** |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

1. Extracted from the preliminary datasheet of BC95. [↑](#footnote-ref-1)