ADD

Circuit 6

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

15:14   13:12   11:10   9:8   7:6   5:4   3:2   1:0

15:12   11:8   7:4   3:0

15:8   13:8   7:0   5:0

15:8   13:0   11:0   9:0

15:0 14:0 13:0 12:0 11:0 10:0 9:0 8:0 7:0 6:0 5:0 4:0 3:0 2:0 1:0 0:0

(f) Ladner-Fischer

1: Bitwise PG Logic

2: Group PG Logic

3: Sum Logic
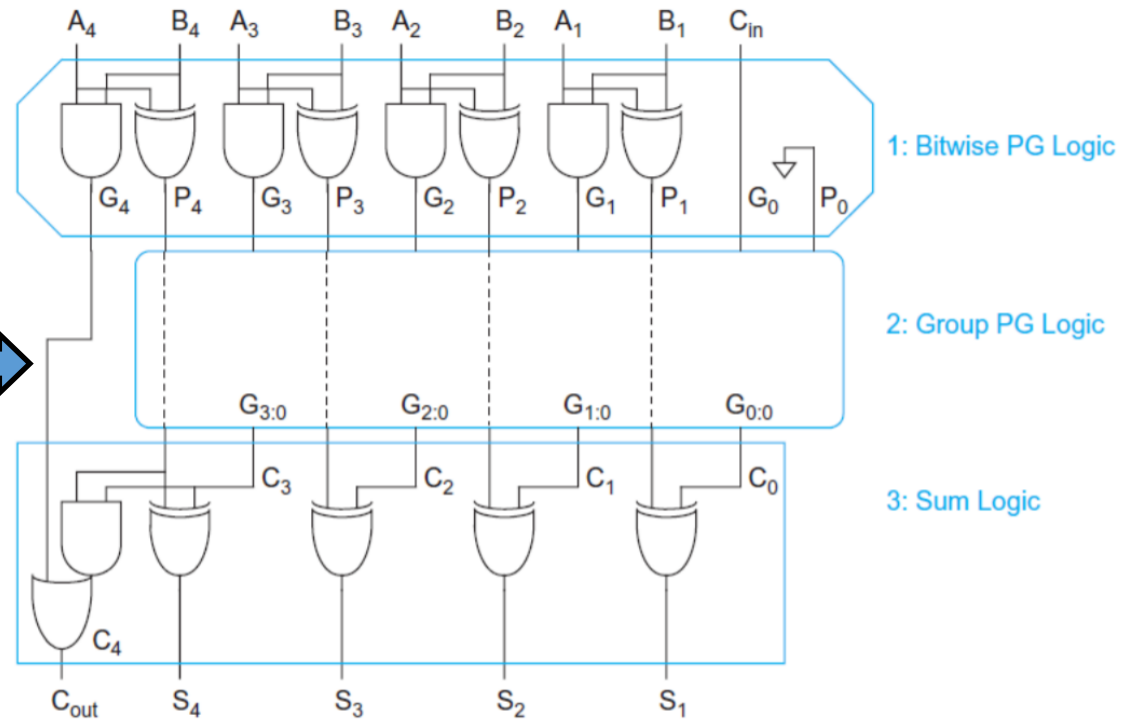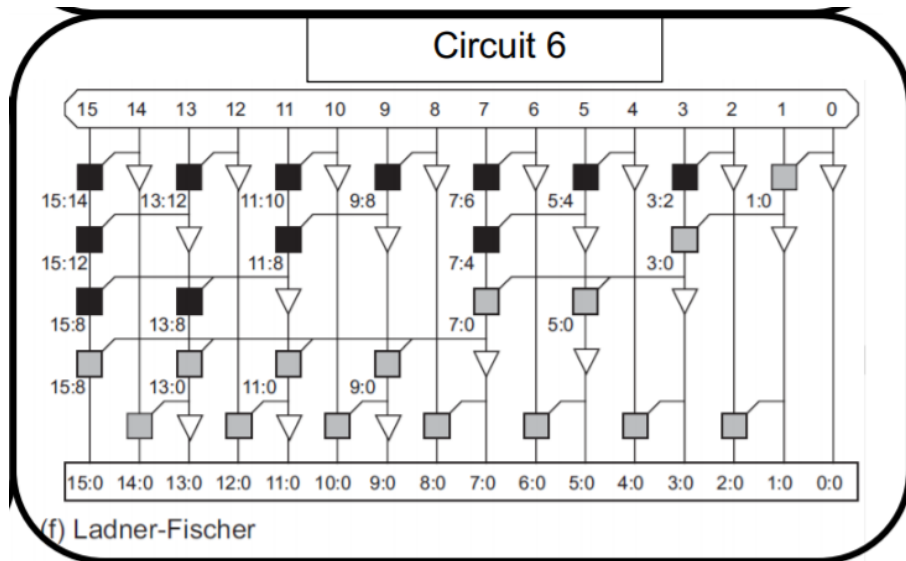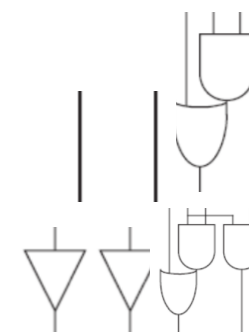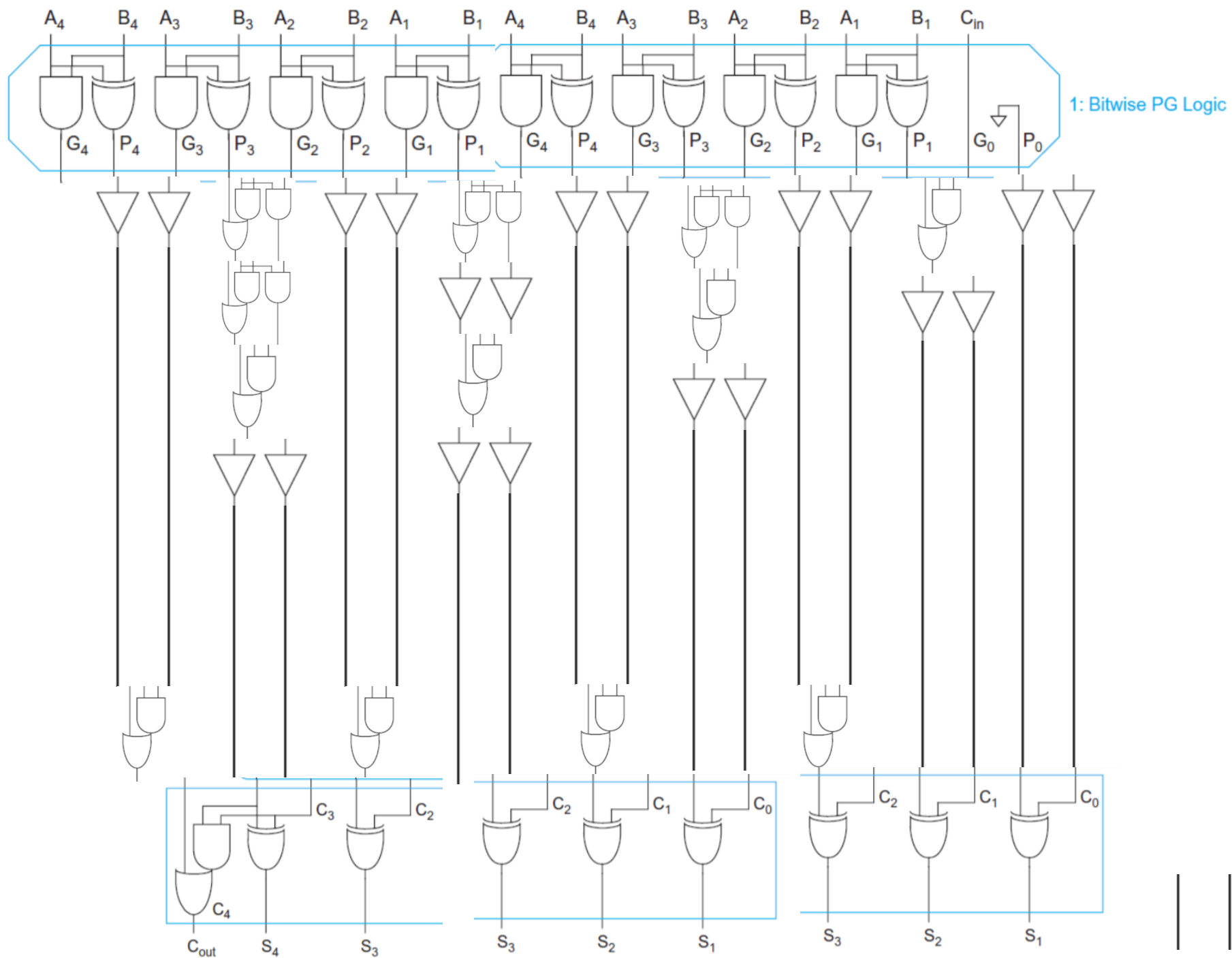
FIGURE 11.12 Addition with generate and propagate logic

1: Bitwise PG Logic

SUB

Register B   Register A   C_in

8x

Circuit 6

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0

15:12 11:8 7:4 3:0

15:8 13:8 7:0 5:0

15:8 13:0 11:0 9:0

15:0 14:0 13:0 12:0 11:0 10:0 9:0 8:0 7:0 6:0 5:0 4:0 3:0 2:0 1:0 0:0

(f) Ladner-Fischer

A_4 B_4 A_3 B_3 A_2 B_2 A_1 B_1 C_{in}

G_4 P_4 G_3 P_3 G_2 P_2 G_1 P_1 G_0 P_0

1: Bitwise PG Logic

2: Group PG Logic

$G_{3:0}$ $G_{2:0}$ $G_{1:0}$ $G_{0:0}$

C_3 C_2 C_1 C_0
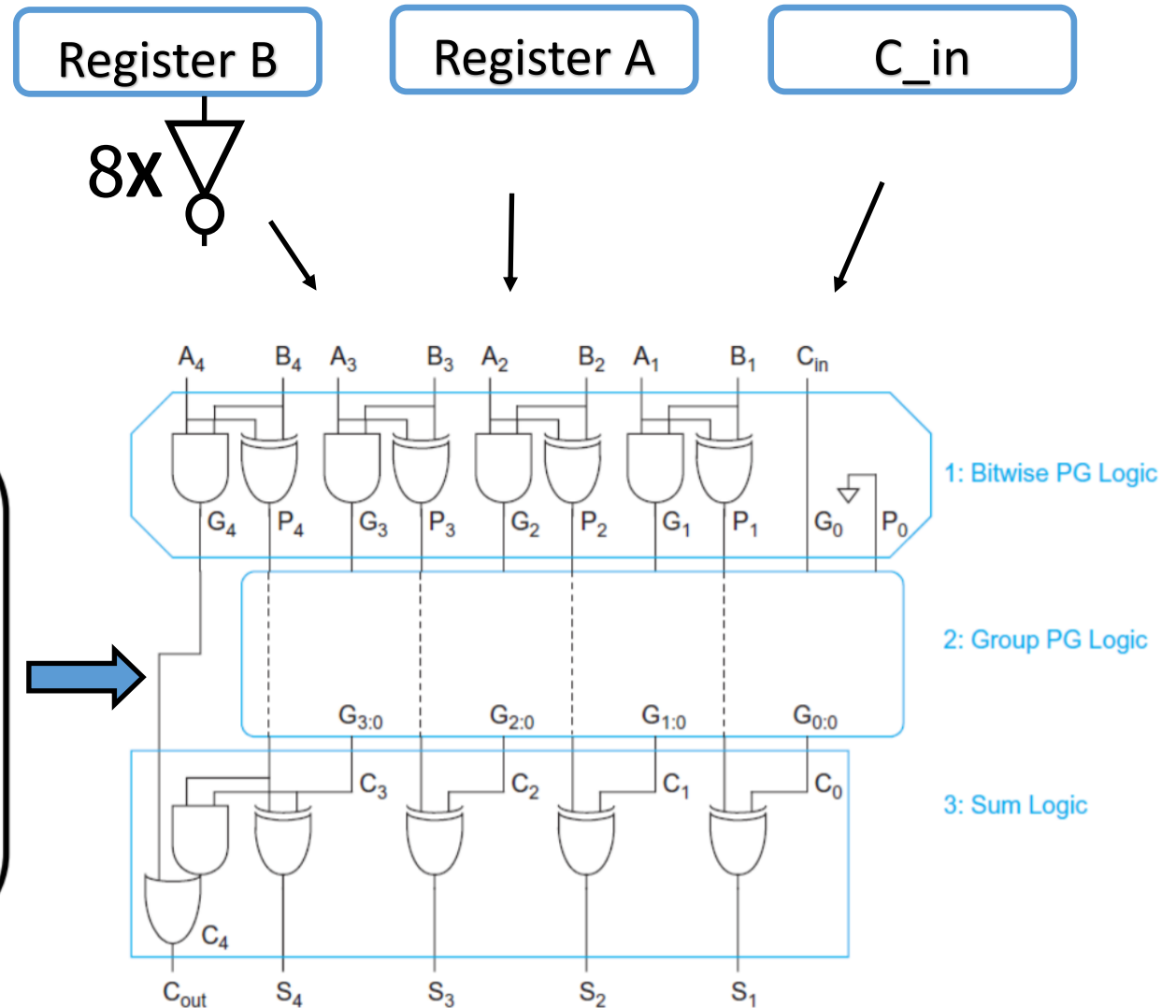
3: Sum Logic

C_4

C_{out} S_4 S_3 S_2 S_1

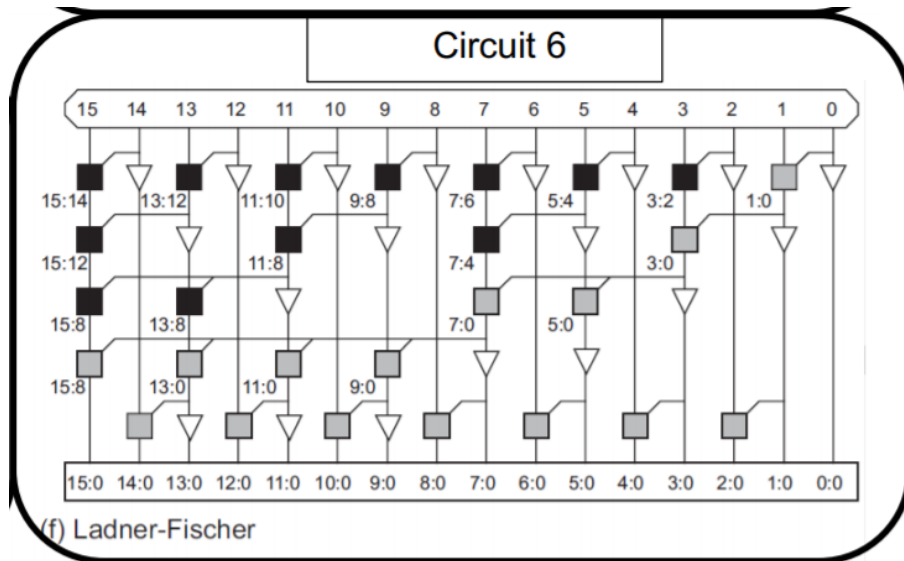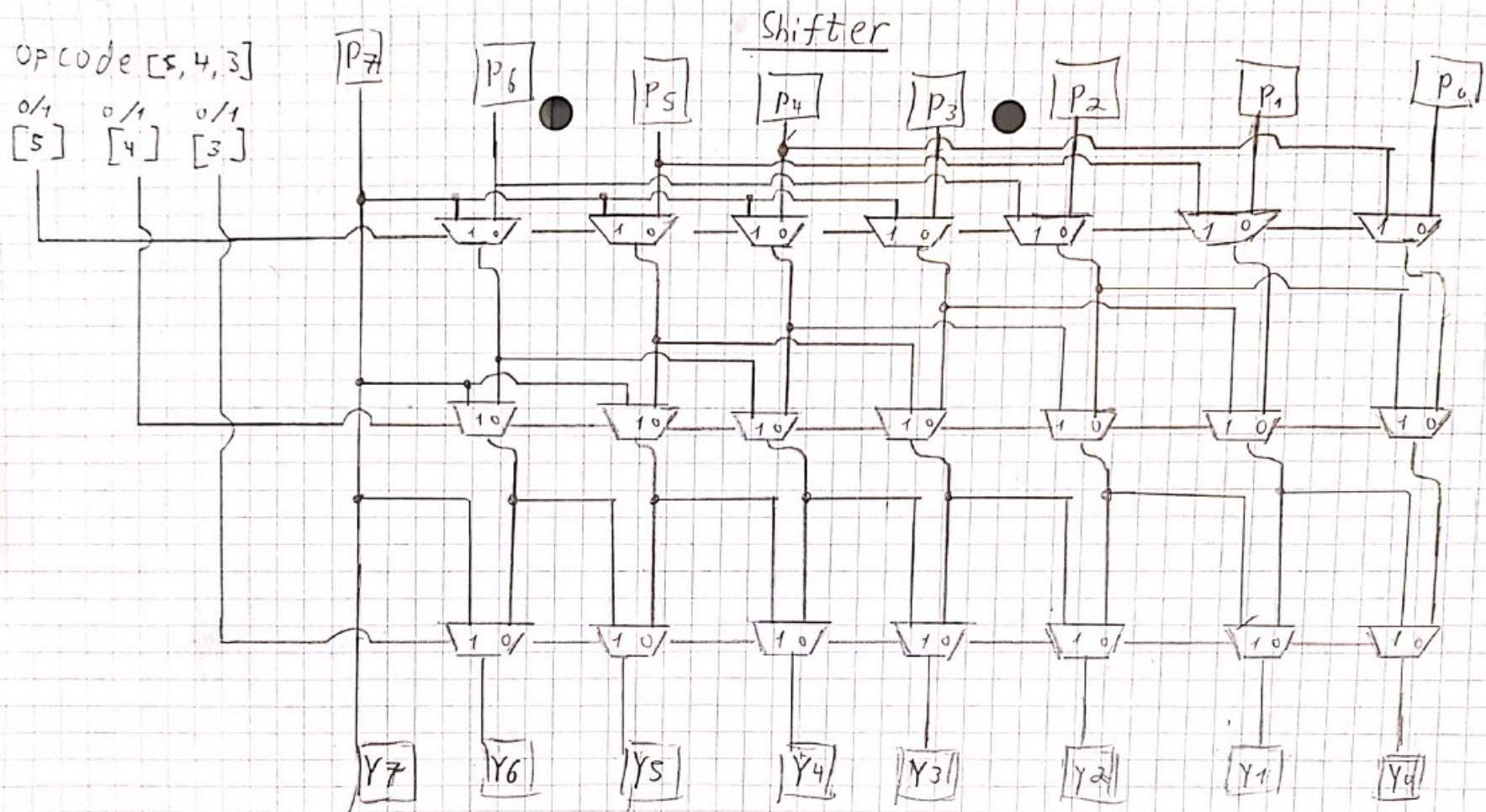**FIGURE 11.12** Addition with generate and propagate logic

Op code [5, 4, 3]

0/1 0/1 0/1
[5] [4] [3]

P7 P6 ● P5 P4 P3 ● P2 P1 P0

Shifter

Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

Logic Block

Opcode:
[4] [3]

B7 A7 B6 A6 B5 A5 B4 A4 B3 A3 B2 A2 B1 A1 B0 A0

2 1 0   2 1 0   2 1 0   2 1 0   2 1 0   2 1 0   2 1 0   2 1 0

Y7   Y6   Y5   Y4   Y3   Y2   Y1   Y0

OPCODE

4		2	1		
	OR	AND	SUB	ADD	A/Y

XOR   SHIFTER