Opcode

OPCODE[0]

Decide source of Register A:

5	4	3	2	1	0

Bit value	Source
0	input
1	Register Y

OPCODE[3:1]

Enable group (bit per group)

5	4	3	2	1	0

Bit value	Group
00**1**	ADD/SUB
0**1**0	LOGIC
100	SHIFT

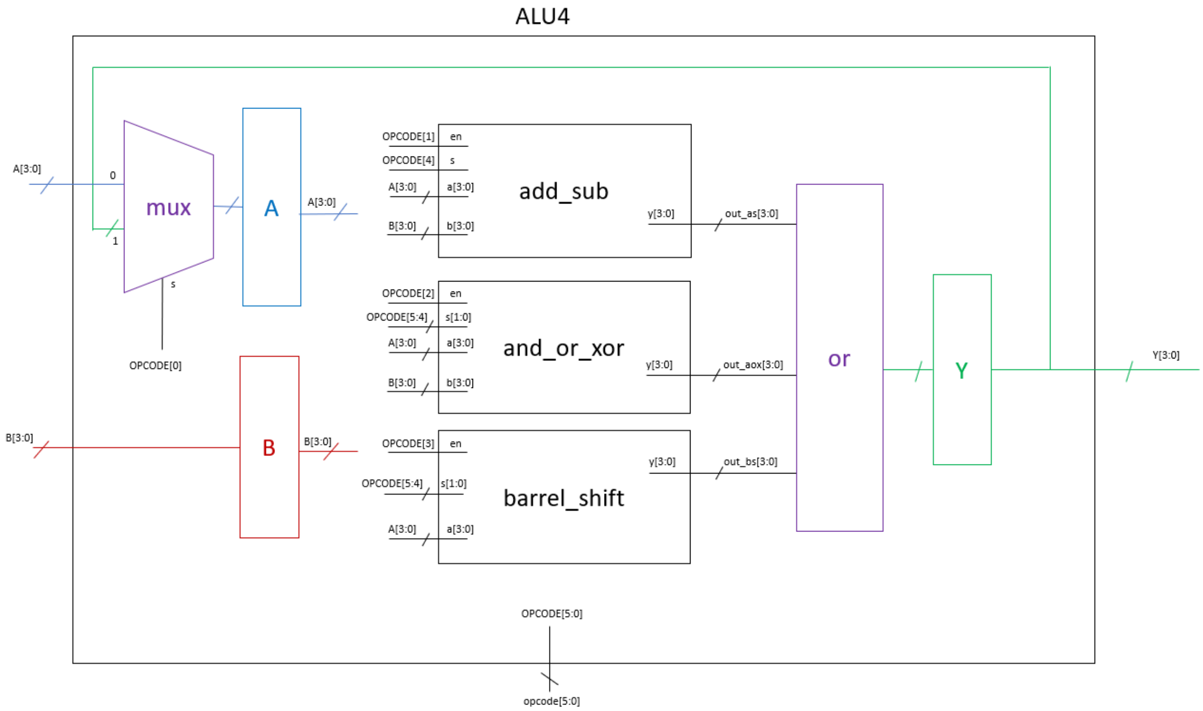
OPCODE[5:4]

Group function

5	4	3	2	1	0

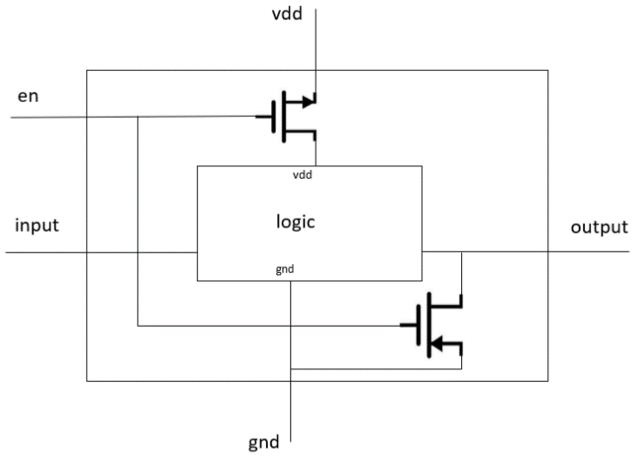
Group	Bit value	Function
ADD/SUB	00	ADD
	01	SUB
LOGIC	00	XOR
	01	OR
	10	AND
SHIFT	00	SHIFT4
	01	SHIFT1
	10	SHIFT2
	11	SHIFT3

TOP



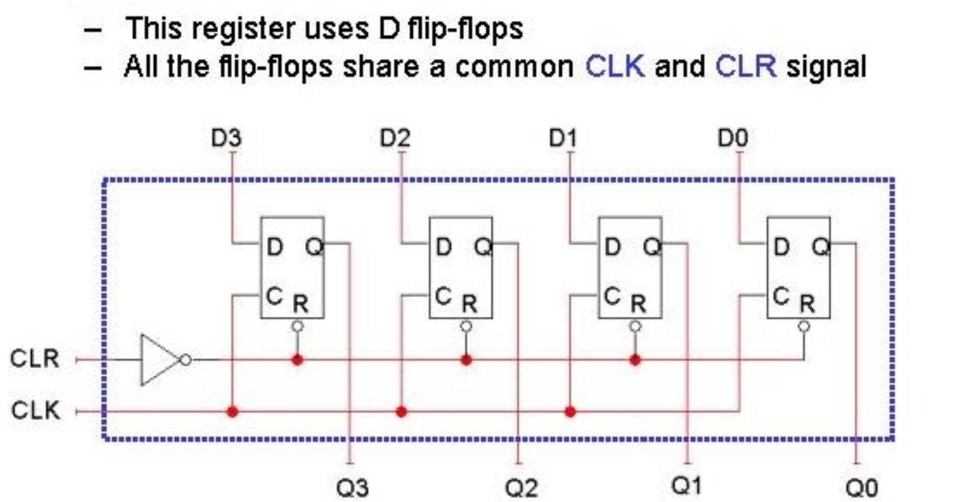
Logic gate	count
INV	0
AND2	0
AND3	0
AND4	0
OR2	0
OR3	4
OR4	0
XOR2	0
XOR3	0
DFF	0
MUX2:1	4
MUX3:1	0
MUX4:1	0

The way we achieve blocking of operations is by an **enable** bit for each logic unit. This is done by placing a switch (nmos transistor) that will block vdd for that block, and a pmos that will pull down the output to 0. This is described in figure below.



Registers A, B and Y

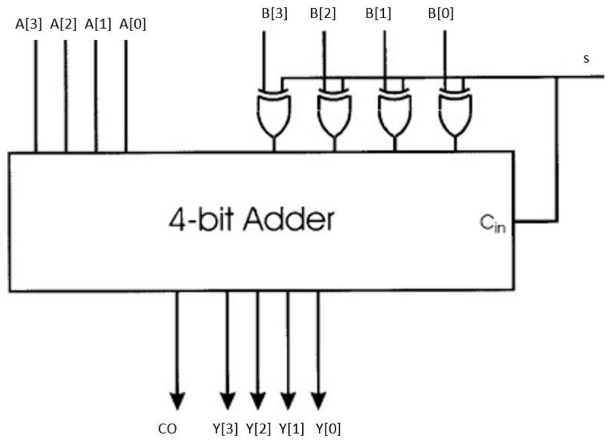
Since not specified otherwise and it is not really needed, we will remove the clear logic.



Logic gate	count
INV	0
AND2	0
AND3	0
AND4	0
OR2	0
OR3	0
OR4	0
XOR2	0
XOR3	0
DFF	4
MUX2:1	0
MUX3:1	0
MUX4:1	0

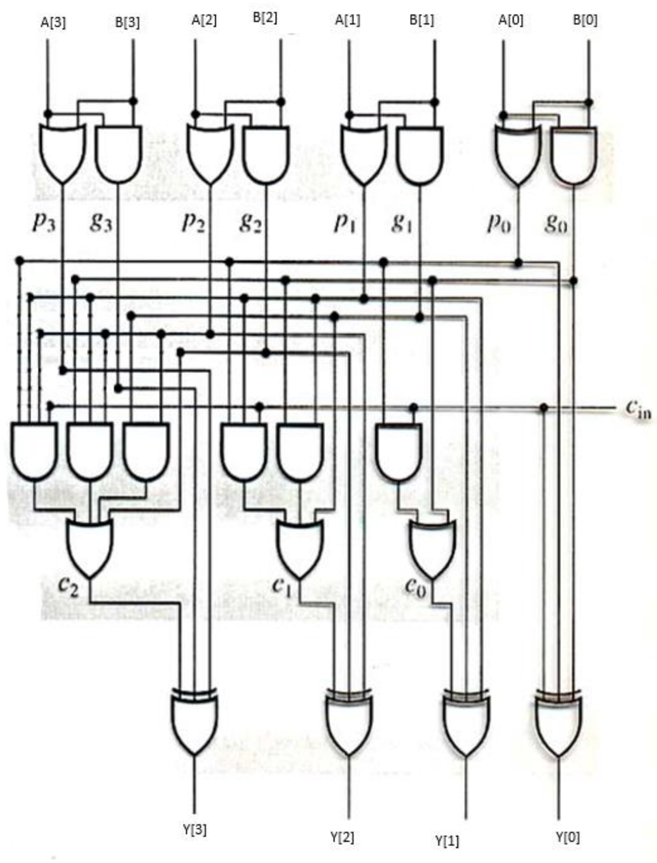
add_sub

s: '0' to ADD, '1' to SUB (this takes care of converting B to 2's complement)



Inside the **4-bit Adder** block above (carry look ahead adder, based on HAYES p.54)

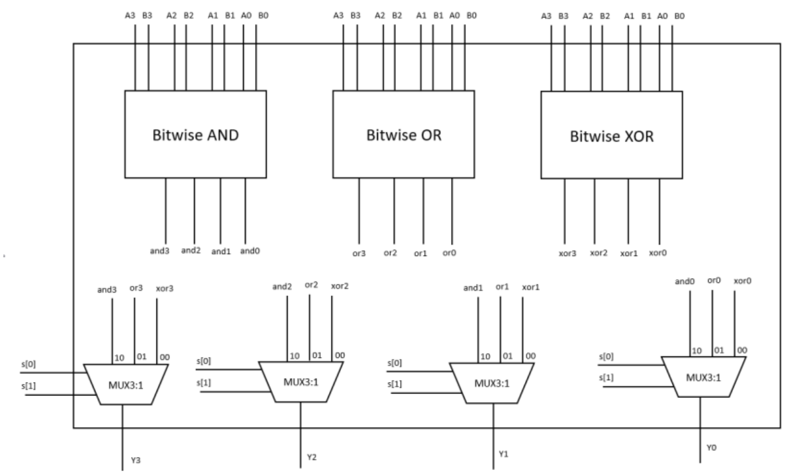
NOTE: since not specified otherwise, we remove the carry-out logic.



Logic gate	count
INV	0
AND2	7
AND3	2
AND4	1
OR2	5
OR3	1
OR4	1
XOR2	4
XOR3	4
DFF	0
MUX2:1	0
MUX3:1	0
MUX4:1	0

and_or_xor

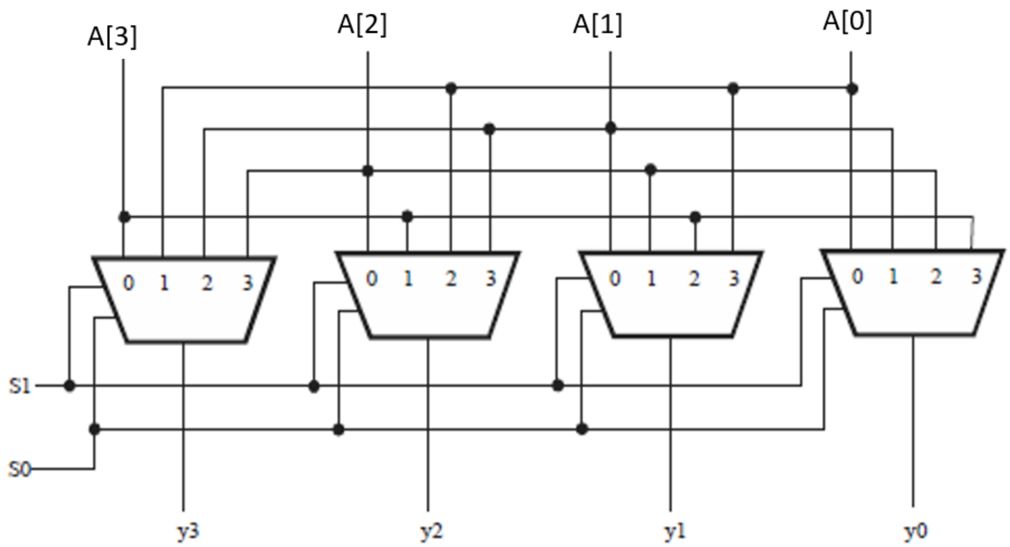
OP[1:0]	Function
00	XOR
01	OR
10	AND



Logic gate	count
INV	0
AND2	4
AND3	0
AND4	0
OR2	4
OR3	0
OR4	0
XOR2	4
XOR3	0
DFF	0
MUX2:1	0
MUX3:1	4
MUX4:1	0

barrel_shift

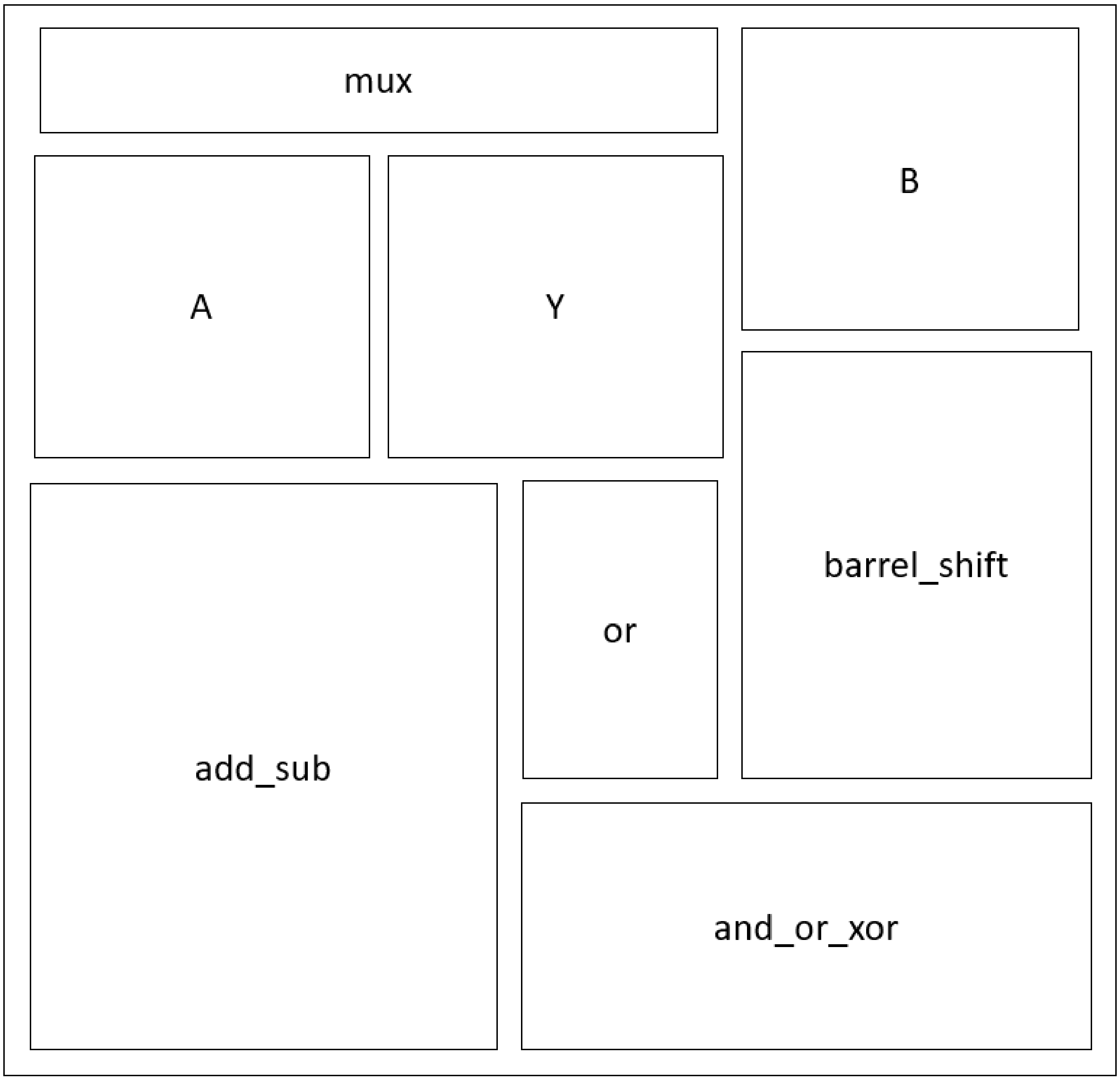
NOTE: we need to shift by 1,2,3 or 4. Shifting by 4 is equal to shifting by 0



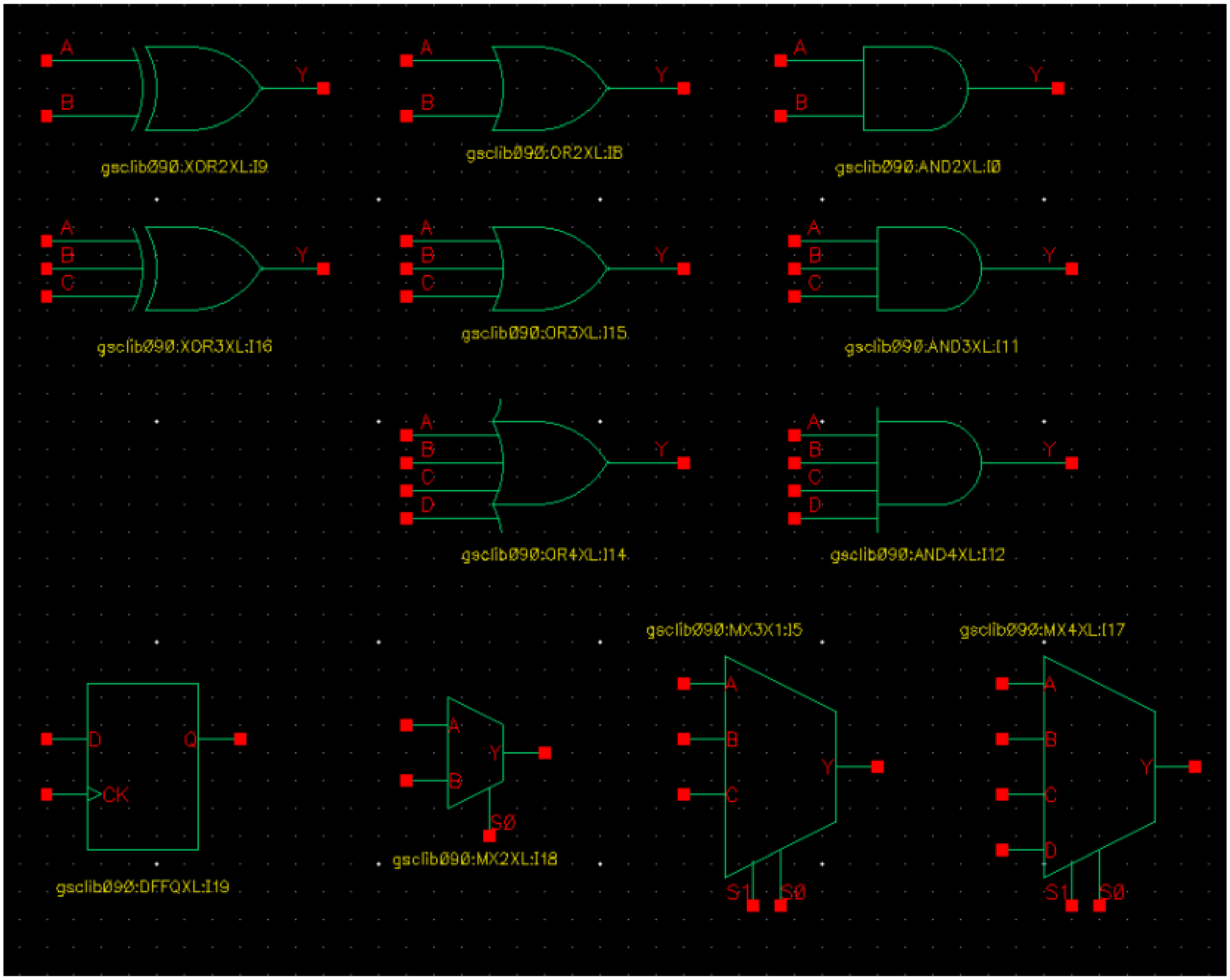
Logic gate	count
INV	0
AND2	0
AND3	0
AND4	0
OR2	0
OR3	0
OR4	0
XOR2	0
XOR3	0
DFF	0
MUX2:1	0
MUX3:1	0
MUX4:1	4

Floor plan

- Registers are close together to minimize delays between them
- Square ALU allows minimizing delays between all blocks



Logic gates that will be used



Total logic gates count:

gate	top sublogic	add_sub	and_or_xor	barrel_shift	A	B	Y	total	gate hight (um)	gate width (um)	gate area (um^2)	accumlated gates area
AND2	0	7	4	0	0	0	0	11	3.09	2.34	7.2306	79.5366
AND3	0	2	0	0	0	0	0	2	3.09	2.92	9.0228	18.0456
AND4	0	1	0	0	0	0	0	1	3.09	3.21	9.9189	9.9189
OR2	0	5	4	0	0	0	0	9	3.09	2.34	7.2306	65.0754
OR3	4	1	0	0	0	0	0	5	3.09	2.92	9.0228	45.114
OR4	0	1	0	0	0	0	0	1	3.09	3.21	9.9189	9.9189
XOR2	0	4	4	0	0	0	0	8	3.09	3.79	11.7111	93.6888
XOR3	0	4	0	0	0	0	0	4	3.09	9.3	28.737	114.948
DFF	0	0	0	0	4	4	4	12	3.09	6.69	20.6721	248.0652
MUX2:1	4	0	0	0	0	0	0	4	3.09	3.5	10.815	43.26
MUX3:1	0	0	4	0	0	0	0	4	3.09	5.53	17.0877	68.3508
MUX4:1	0	0	0	4	0	0	0	4	3.09	7.56	23.3604	93.4416
total	8	25	16	4	4	4	4	65	-	-	-	889.3638
accumulated area	79.3512	295.4658	173.04	93.4416	82.6884	82.6884	82.6884					
with headspace	119.0268	443.1987	259.56	140.1624	124.0326	124.0326	124.0326				alu4 total area	1334.0457

Estimated ALU4 area: 1334 um^2 = 1.33 mm^2