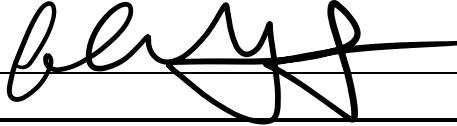


ECE 3544: Digital Design I
Project 2: Modeling the Timing of a Device

Student Name: Colin Grundey

Honor Code Pledge: I have neither given nor received unauthorized assistance on this assignment.



Grading: The design project will be graded on a 100 point basis, as shown below:

Manner of Presentation (30 points)

- _____ Completed cover sheet included with report (5 points)
- _____ Organization: Clear, concise presentation of content; Use of appropriate, well-organized sections (15 points)
- _____ Mechanics: Spelling and grammar (10 points)

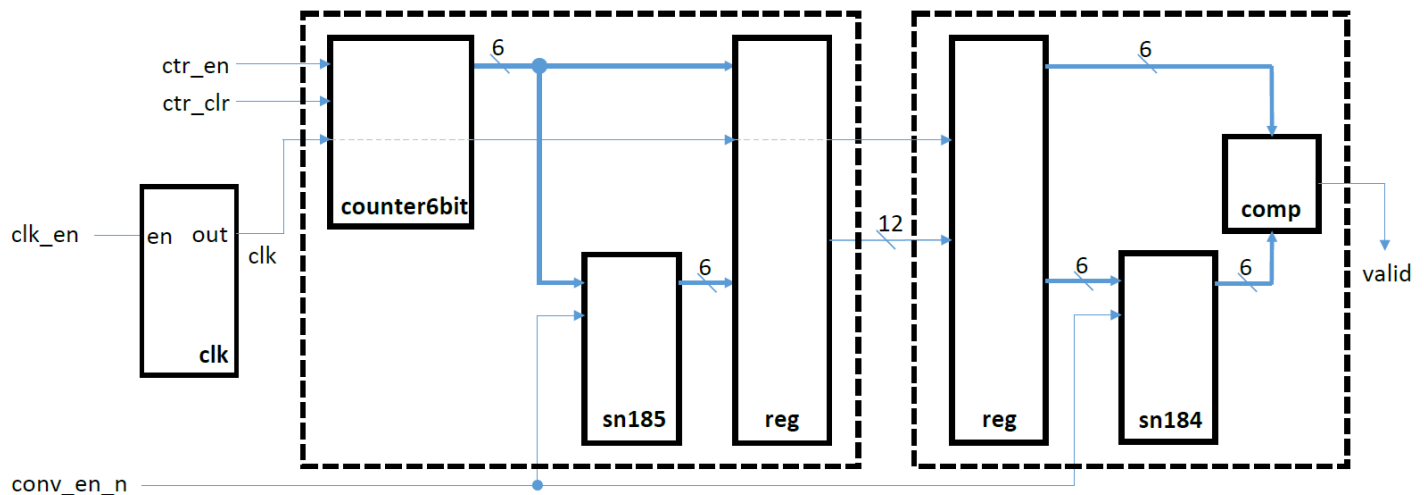
Technical Merit (70 points)

- _____ General discussion: *Did you describe the objectives in your own words? Did you discuss your conclusions and the lessons you learned from the assignment?* (5 points)
- _____ Design discussion: *Did you discuss your design approach, and the design decisions that you made as a part of implementing your modules?* (10 points)
- _____ Timing analysis discussion: *Did you determine the minimum clock period that allows correct operation of the system?* (5 points)
- _____ Testing discussion: *What was your approach to formulating your test benches? How did you verify the correctness of the modules you designed?* (10 points)
- _____ Supporting figures: *Waveforms showing the correct operation of the various modules, Waveforms demonstrating valid and invalid behavior of the system.* (20 points)
- _____ Supporting files: *Do the modules pass any tests applied by the grading staff? Modules whose declarations do not conform to the requirements of the project specification cannot be tested, and will receive no credit.* (20 points)

===== **Project Grade**

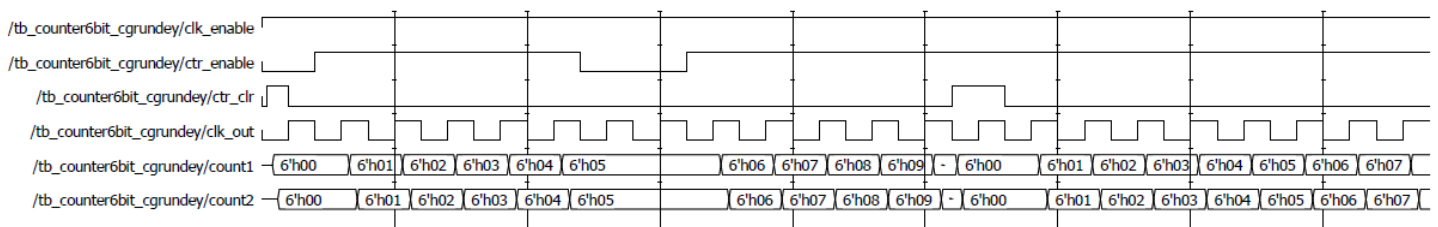
Objective

Project 2 describes several hardware components to model in Verilog that will later be used in a transmit-receive system. Each component is tested to ensure its success with test bench files that cycle through possible inputs to produce outputs. This first module is a 6-bit counter that has delays and increments and outputs on a positive clock edge. The next modules are two 6-bit converters. One converter, sn184, converts a 6-bit BCD number to a 6-bit binary number. The other, sn185, converts a 6-bit binary number to a 6-bit BCD number. Each have the same propagation delay characteristics. A test bench using a clock, counter, and both converters fully tests the modules. The spec also requires the implementation of a 12-bit register. The register writes the input to its output on a positive clock edge. There are no propagation delays in this module per the project spec. Lastly, there are two modules called transmit and receive that are supposed to simulate a data transmission. The counter module is used to produce inputs to the system, the registers are the transport mechanism, and converters are used as a form of error checking. After checking each module's functionality, this system should work and demonstrate their usefulness in circuits. The system diagram from the spec is shown below.



Problem 2: 6-bit Counter

After studying the provided 4-bit counter implementation, I converted the output to be a 6-bit binary number. I kept the delays the same and the logic, but the maximum value for a 6-bit number is 63 so I increased that from the 4-bit counter's max value of 15. The waveform result shows that the enable and clear control signals work properly. When the enable signal is low, the counter does not increment the count values on a positive clock edge. Also, when the clear signal is high, the count values reset to 0.

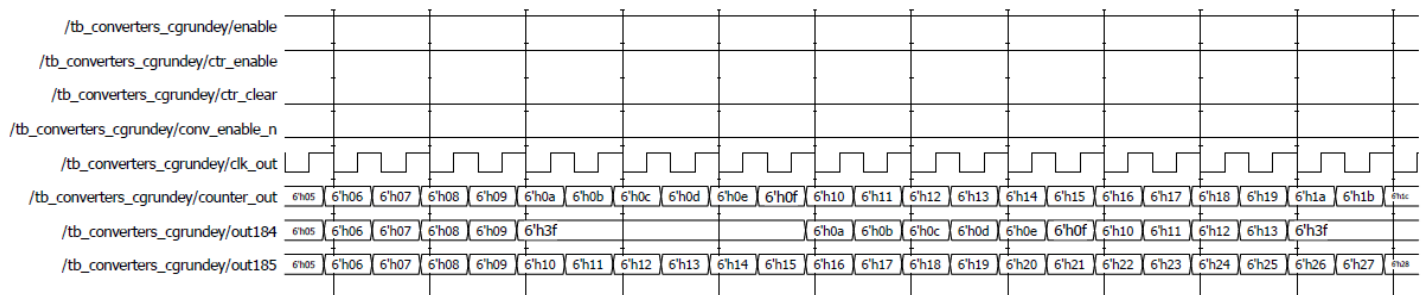
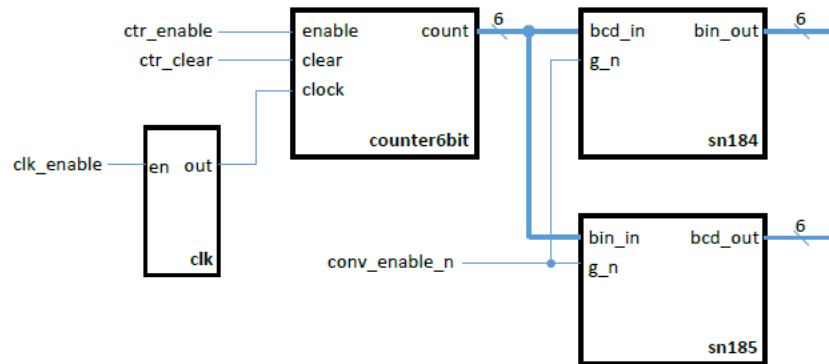


Problem 3: Converters (BCD \leftrightarrow Binary)

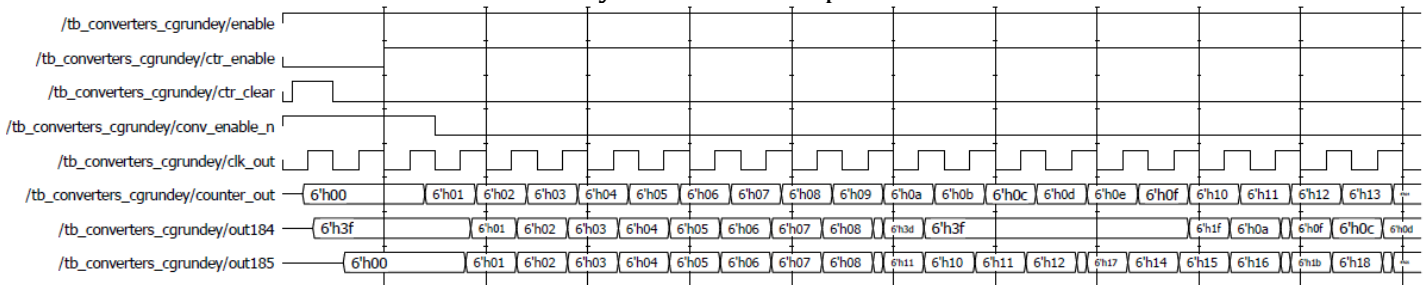
The datasheets for the sn184 and sn185 devices show that they perform inverse conversions between binary and BCD. The sn184 converts a 6-bit BCD number to binary while the sn185 converts a 6-bit binary number to BCD. I chose to implement their functionality by using a behavior model for an algorithmic approach. There are a couple paragraphs on the datasheet that explain the algorithm for the conversion. In my always block for both modules, I check the enable signal, which is active-low, and decide whether to output the invalid signal or perform the conversion. An invalid signal will produce a 6-bit value of all 1's. An important situation that I detected in both modules is if the input number can properly be converted. For the sn184, I made sure that the least significant 4 bits were not greater than 9

because digits greater than 9 can't be represented in BCD. Similarly, in my sn185 module, I made sure that the binary input was not greater than 39 because the conversion would not be meaningful.

Next, using the 6-bit counter module and a clock module, I wrote a test-bench to cycle through the possible inputs to ensure successful operation. The diagram from the project 2 specification shows how it should operate and the waveform shows my implementation to be correct. The converters have the invalid 6'h3F value when the inputs are not able to be converted and the inputs that can be converted are done so correctly.

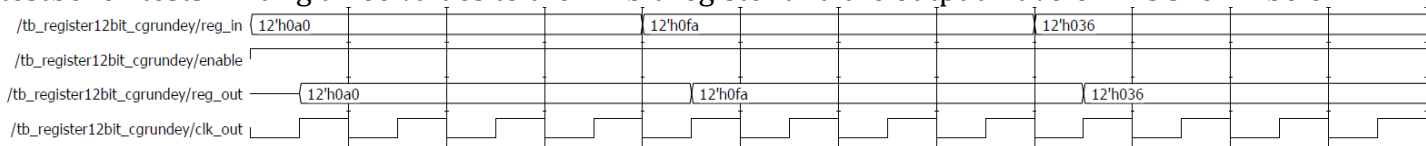


Once I verified my converters with my testbench, I added a specify block with the right propagation delays from the datasheet. I used the MAX values to show the critical path operation of the circuit. The waveform below shows the delayed modules output.



Problem 5: 12-bit Register

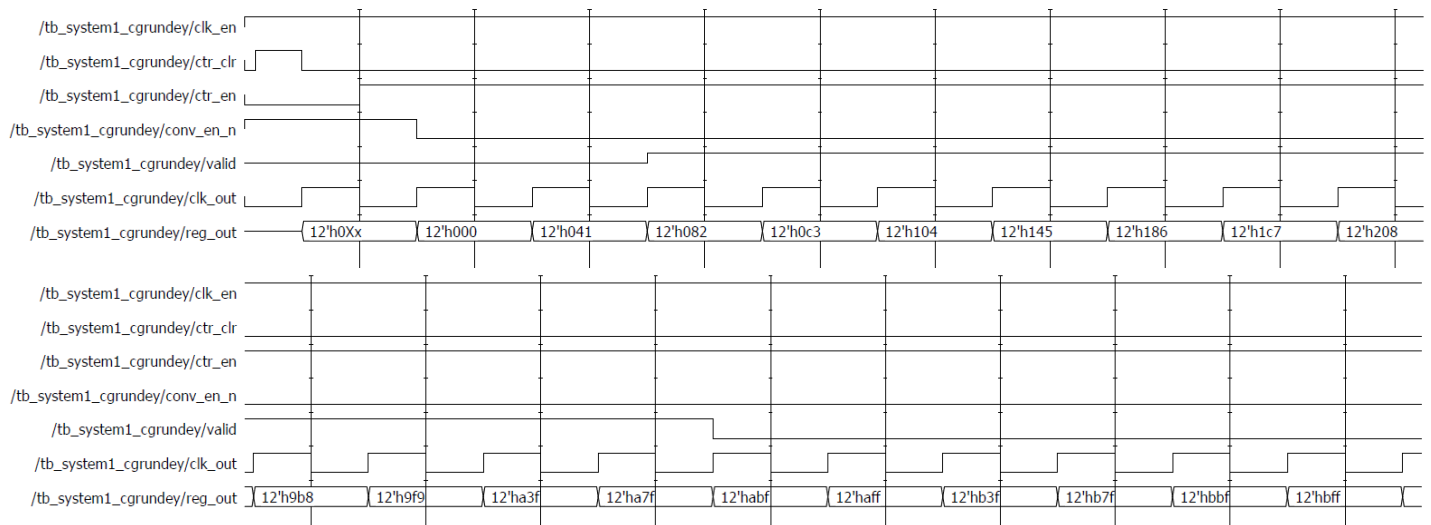
Problem 5 outlines a 12-bit register to be implemented that writes a value on a positive edge of a clock. I used an always block that writes the input to the output on the positive edge of the clock. In order to do this, I had to also name the output as a reg type to retain the value throughout execution. My testbench tests writing three values to the 12-bit register and the output waveform is shown below.



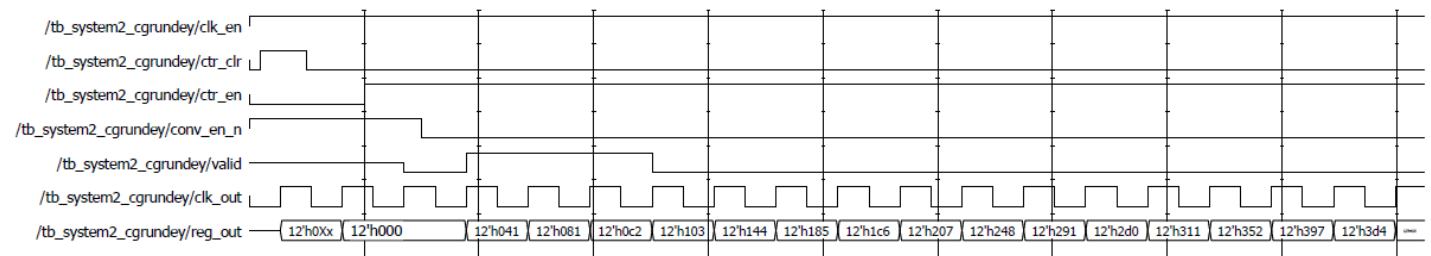
Problem 6: Digital System

The digital system described in problem 6 uses all of the modules created in the previous problems. I began by creating the transmit module with a counter, sn185, and 12-bit register. I tested it in a custom testbench to see if it worked. Then I instantiated a 12-bit register and a sn184 in the receive module and tested its valid output signal to make sure it worked. Finally, I implemented the whole

system in my system1_cgrundey.v file that instantiated the clock, transmit, and receive modules. The clock period seemed to prevent the output from working correctly so I increased it to 100. The system provided the correct outputs, however, the output was delayed 2 clock cycles caused by the delay in the receive module. I had to account for this when observing the output waveforms shown below.



In system 2, a smaller clock period is used to show incorrect operation. I tried a few different period values and found that 55ns was where the system did not function properly. The critical path of the system, due to propagation delays of the modules, causes the circuit to execute fully on a single clock cycle. The waveform for system 2 are shown below.



Conclusion

This project emphasized the importance and difficulty of timing in a synchronous circuit by requiring synchronous and non-synchronous modules, each with specific timing properties, to operate in a larger system together. The 6-bit counter and 12-bit register operated on the positive clock edge while the converters did not use a clock. Propagation delays are used in the converters and delays are used in the counter so this was important to note when designing and analyzing outputs. In addition, all my implementations used a behavioral model which gave me great practice. More specifically, in my converter modules, I used an algorithmic approach in the always block to simplify the code and make it more readable. Using combinational logic would have required more tedious work due to the number of inputs and outputs in the truth table provided in the datasheet. Finally, the system implemented was larger than we have done so far, which forced me to truly understand its operation before observing its outputs. My preparations in my predictions for the outputs were valuable because they helped me debug issues when I found discrepancies in the waveforms.