Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 6, 14:00

Student ID: R10945006

Student Name: 温皆循

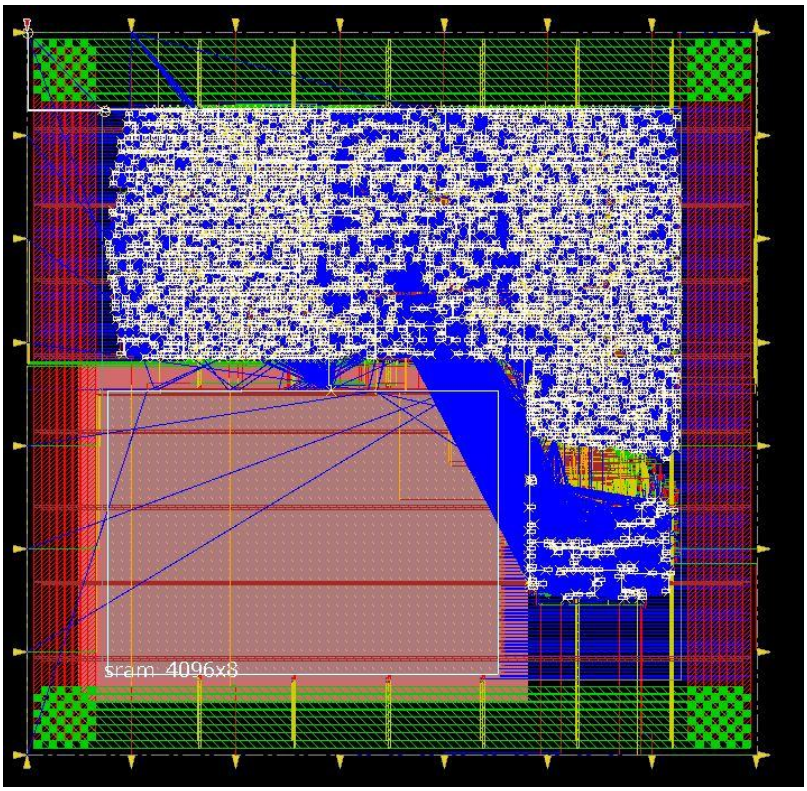
APR Results

1. Fill in the blanks below.

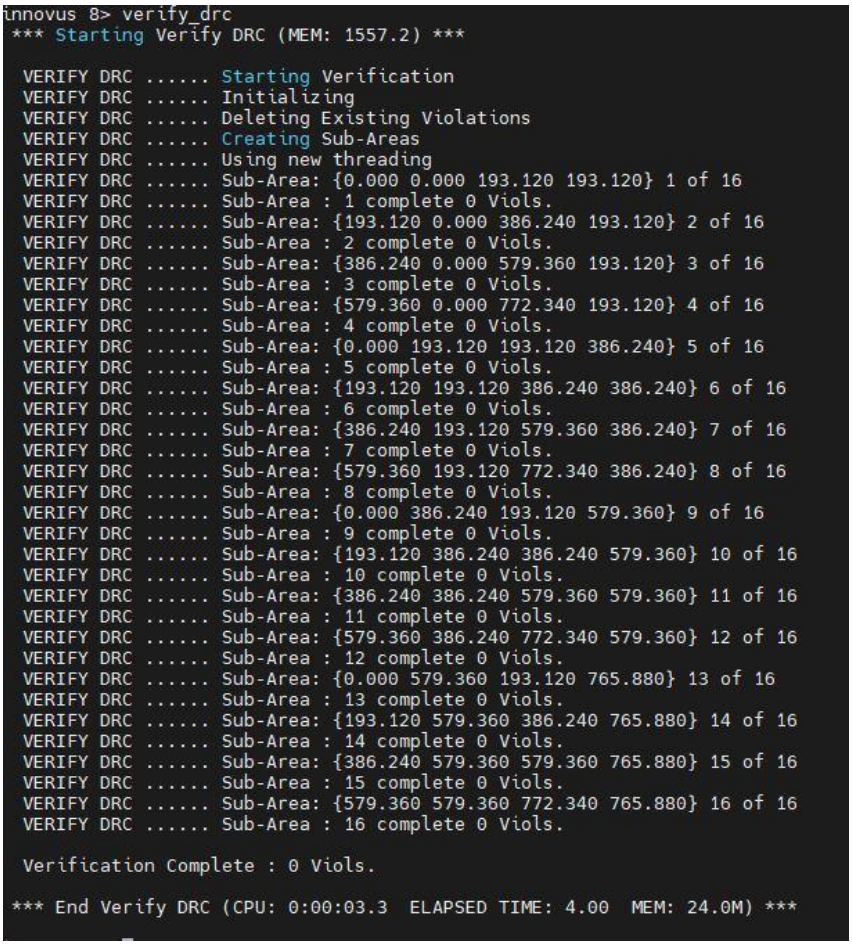
Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	NA
	Core Area (um^2)	591519.76 μm
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	15 ns
Follow your design in HW3? (If not, write down the student ID of the designer)		YES

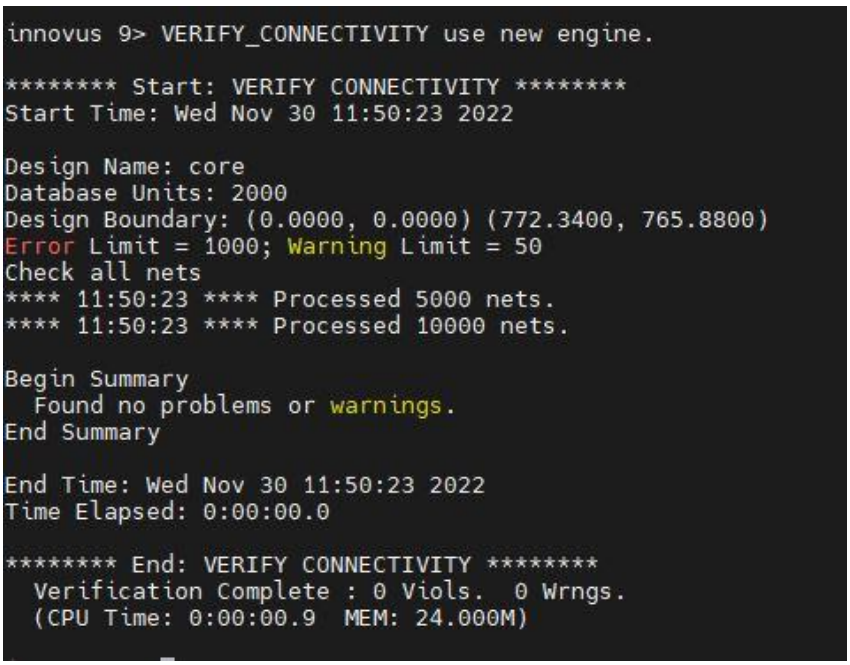
Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result, and show the routing result in the layout (10%).

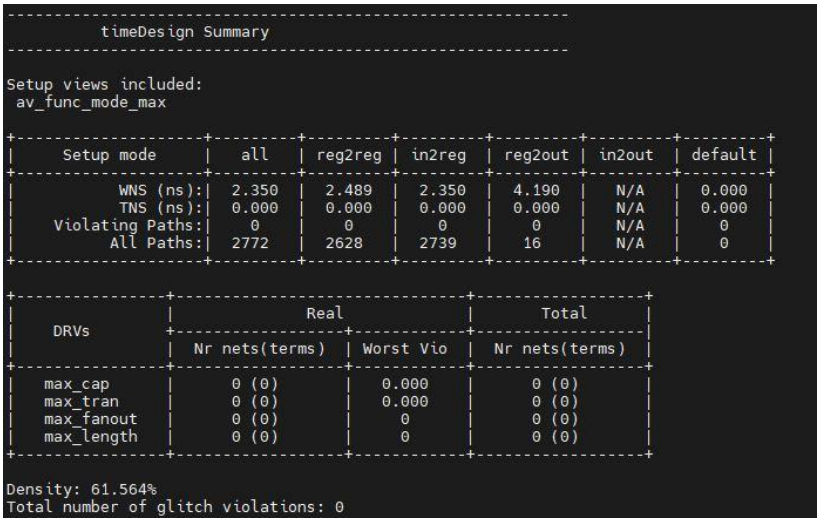


2. Attach the snapshot of DRC and LVS checking after routing. (5%)

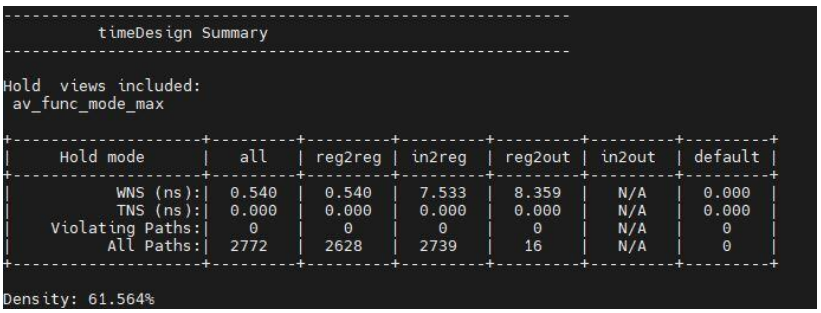




3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)



```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  2.350  |  2.489  |  2.350  |  4.190  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2772   |  2628   |  2739   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 61.564%
Total number of glitch violations: 0
```



```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.540  |  0.540  |  7.533  |  8.359  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2772   |  2628   |  2739   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 61.564%
```

4. Show the critical path after post-route optimization. What is the path type? (5%)
   (The slack of the critical path should match the smallest slack in the timing report)

   4.1 Setup time: in2reg, 2.350

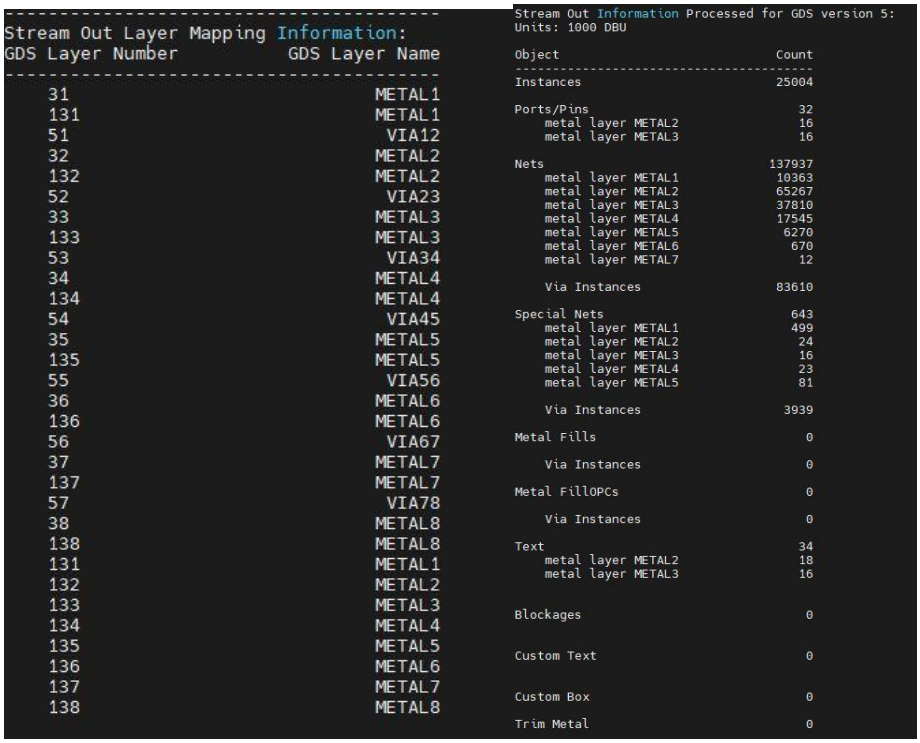
```
Path 1: MET Setup Check with Pin map_0_15_reg_19__11_/CK
Endpoint:   map_0_15_reg_19__11_/D (v) checked with  leading edge of 'i_clk'
Beginpoint: i_in_data[0]          (^) triggered by  leading edge of 'i_clk'
Path Groups: {in2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.541
- Setup                         0.221
+ Phase Shift                  15.000
+ CPPR Adjustment               0.000
= Required Time                15.320
- Arrival Time                 12.970
= Slack Time                    2.350
    Clock Rise Edge                     0.000
    + Input Delay                       7.500
    + Network Insertion Delay           0.500
    = Beginpoint Arrival Time           8.000
    Timing Path:
    +-----------------------------------------------------------------------------------+
    |          Pin          | Edge |     Net     |   Cell    | Delay | Arrival | Required |
    |                       |      |             |           |       |  Time   |   Time   |
    |-----------------------+------+-------------+-----------+-------+---------+----------|
    | i_in_data[0]          | ^    | i_in_data[0] |           |       |   8.000 |   10.350 |
    | U3975/A               | ^    | i_in_data[0] | NAND2X1   | 0.013 |   8.013 |   10.362 |
    | U3975/Y               | v    | n4545       | NAND2X1   | 0.074 |   8.087 |   10.437 |
    | U3739/A1              | v    | n4545       | OAI21XL   | 0.000 |   8.087 |   10.437 |
    | U3739/Y               | ^    | n4551       | OAI21XL   | 0.332 |   8.419 |   10.769 |
    | U4184/A0              | ^    | n4551       | AOI21X1   | 0.000 |   8.419 |   10.769 |
    | U4184/Y               | v    | n4423       | AOI21X1   | 0.172 |   8.592 |   10.941 |
    | U4167/A0              | v    | n4423       | OAI21XL   | 0.000 |   8.592 |   10.941 |
    | U4167/Y               | ^    | n4437       | OAI21XL   | 0.341 |   8.933 |   11.282 |
    | U4940/A0              | ^    | n4437       | AOI21X1   | 0.000 |   8.933 |   11.282 |
    | U4940/Y               | v    | n4455       | AOI21X1   | 0.169 |   9.102 |   11.451 |
    | U4336/A0              | v    | n4455       | OAI21XL   | 0.000 |   9.102 |   11.451 |
    | U4336/Y               | ^    | n4279       | OAI21XL   | 0.348 |   9.450 |   11.799 |
    | U3706/A0              | ^    | n4279       | AOI21X1   | 0.000 |   9.450 |   11.799 |
    | U3706/Y               | v    | n4340       | AOI21X1   | 0.182 |   9.632 |   11.982 |
    | U3917/A0              | v    | n4340       | OAI21XL   | 0.000 |   9.632 |   11.982 |
    | U3917/Y               | ^    | n4320       | OAI21XL   | 0.317 |   9.949 |   12.298 |
    | U4134/A               | ^    | n4320       | NAND2X1   | 0.000 |   9.949 |   12.298 |
    | U4134/Y               | v    | n4243       | NAND2X1   | 0.141 |  10.090 |   12.440 |
    | U4731/A               | v    | n4243       | NOR2X1    | 0.000 |  10.090 |   12.440 |
    | U4731/Y               | ^    | n4239       | NOR2X1    | 0.160 |  10.250 |   12.600 |
    | U4034/A               | ^    | n4239       | NAND2X1   | 0.000 |  10.250 |   12.600 |
    | U4034/Y               | v    | n4124       | NAND2X1   | 0.107 |  10.358 |   12.707 |
    | U6033/A               | v    | n4124       | XOR2X1    | 0.000 |  10.358 |   12.707 |
    | U6033/Y               | v    | n4120       | XOR2X1    | 0.159 |  10.516 |   12.866 |
    | U3672/A               | v    | n4120       | CLKAND2X6 | 0.000 |  10.516 |   12.866 |
    | U3672/Y               | v    | n7692       | CLKAND2X6 | 0.512 |  11.028 |   13.378 |
    | U4018/A               | v    | n7692       | INVX6     | 0.004 |  11.032 |   13.382 |
    | U4018/Y               | ^    | n3434       | INVX6     | 0.568 |  11.600 |   13.950 |
    | FE_OFC17_n3434/A      | ^    | n3434       | CLKBUFX6  | 0.001 |  11.601 |   13.951 |
    | FE_OFC17_n3434/Y      | ^    | FE_OFN17_n3434 | CLKBUFX6 | 0.574 |  12.175 |   14.524 |
    | U6214/B               | ^    | FE_OFN17_n3434 | NAND2XL | 0.023 |  12.198 |   14.548 |
    | U6214/Y               | v    | n7928       | NAND2XL   | 0.346 |  12.544 |   14.894 |
    | U9386/B1              | v    | n7928       | OA22X1    | 0.000 |  12.544 |   14.894 |
    | U9386/Y               | v    | n2711       | OA22X1    | 0.426 |  12.970 |   15.320 |
    | map_0_15_reg_19__11_/D | v   | n2711       | DFFQX1    | 0.000 |  12.970 |   15.320 |
    +-----------------------------------------------------------------------------------+
```

```
Clock Rise Edge                     0.000
= Beginpoint Arrival Time           0.000
Other End Path:
+-----------------------------------------------------------------------------------+
|          Pin          | Edge |     Net     |   Cell    | Delay | Arrival | Required |
|                       |      |             |           |       |  Time   |   Time   |
|-----------------------+------+-------------+-----------+-------+---------+----------|
| i_clk                 | ^    | i_clk       |           |       |   0.000 |   -2.350 |
| CTS_cdb_BUF_i_clk_G0_L1_1/A | ^ | i_clk       | CLKBUFX12 | 0.001 |   0.001 |   -2.349 |
| CTS_cdb_BUF_i_clk_G0_L1_1/Y | ^ | CTS_122     | CLKBUFX12 | 0.111 |   0.112 |   -2.238 |
| CTS_ccl_a_BUF_i_clk_G0_L2_2/A | ^ | CTS_122     | CLKBUFX16 | 0.002 |   0.114 |   -2.236 |
| CTS_ccl_a_BUF_i_clk_G0_L2_2/Y | ^ | CTS_121     | CLKBUFX16 | 0.160 |   0.274 |   -2.076 |
| CTS_ccl_a_BUF_i_clk_G0_L3_26/A | ^ | CTS_121     | CLKBUFX12 | 0.033 |   0.307 |   -2.042 |
| CTS_ccl_a_BUF_i_clk_G0_L3_26/Y | ^ | CTS_119     | CLKBUFX12 | 0.229 |   0.536 |   -1.814 |
| map_0_15_reg_19__11_/CK | ^ | CTS_119     | DFFQX1    | 0.005 |   0.541 |   -1.808 |
+-----------------------------------------------------------------------------------+
```

   4.2 Hold time: reg2reg, 0.540

```
Path 1: MET Hold Check with Pin current_out_count_reg_9_/CK
Endpoint:   current_out_count_reg_9_/D (v) checked with  leading edge of 'i_
clk'
Beginpoint: current_out_count_reg_9_/QN (^) triggered by  leading edge of 'i_
clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.498
+ Hold                         -0.013
+ Phase Shift                   0.000
- CPPR Adjustment               0.000
= Required Time                 0.485
  Arrival Time                  1.026
  Slack Time                    0.540
    Clock Rise Edge                     0.000
    = Beginpoint Arrival Time           0.000
    Timing Path:
    +-----------------------------------------------------------------------------------+
    |          Pin          | Edge |     Net     |   Cell    | Delay | Arrival | Required |
    |                       |      |             |           |       |  Time   |   Time   |
    |-----------------------+------+-------------+-----------+-------+---------+----------|
    | i_clk                 | ^    | i_clk       |           |       |   0.000 |   -0.540 |
    | CTS_cdb_BUF_i_clk_G0_L1_1/A | ^ | i_clk       | CLKBUFX12 | 0.001 |   0.001 |   -0.539 |
    | CTS_cdb_BUF_i_clk_G0_L1_1/Y | ^ | CTS_122     | CLKBUFX12 | 0.111 |   0.112 |   -0.429 |
    | CTS_ccl_a_BUF_i_clk_G0_L2_2/A | ^ | CTS_122     | CLKBUFX16 | 0.002 |   0.114 |   -0.427 |
    | CTS_ccl_a_BUF_i_clk_G0_L2_2/Y | ^ | CTS_121     | CLKBUFX16 | 0.160 |   0.274 |   -0.267 |
    | CTS_ccl_a_BUF_i_clk_G0_L3_15/A | ^ | CTS_121     | CLKBUFX12 | 0.033 |   0.307 |   -0.234 |
    | CTS_ccl_a_BUF_i_clk_G0_L3_15/Y | ^ | CTS_108     | CLKBUFX12 | 0.236 |   0.543 |    0.002 |
    | current_out_count_reg_9_/CK | ^ | CTS_108     | DFFRX1    | 0.002 |   0.545 |    0.004 |
    | current_out_count_reg_9_/QN | ^ | n8367       | DFFRX1    | 0.375 |   0.920 |    0.380 |
    | U7596/B1              | ^    | n8367       | OAI32XL   | 0.000 |   0.920 |    0.380 |
    | U7596/Y               | v    | n3295       | OAI32XL   | 0.106 |   1.026 |    0.485 |
    | current_out_count_reg_9_/D | v | n3295       | DFFRX1    | 0.000 |   1.026 |    0.485 |
    +-----------------------------------------------------------------------------------+
    Clock Rise Edge                     0.000
    + Source Insertion Delay           -0.047
    = Beginpoint Arrival Time          -0.047
    Other End Path:
    +-----------------------------------------------------------------------------------+
    |          Pin          | Edge |     Net     |   Cell    | Delay | Arrival | Required |
    |                       |      |             |           |       |  Time   |   Time   |
    |-----------------------+------+-------------+-----------+-------+---------+----------|
    | i_clk                 | ^    | i_clk       |           |       |  -0.047 |    0.494 |
    | CTS_cdb_BUF_i_clk_G0_L1_1/A | ^ | i_clk       | CLKBUFX12 | 0.001 |  -0.046 |    0.495 |
    | CTS_cdb_BUF_i_clk_G0_L1_1/Y | ^ | CTS_122     | CLKBUFX12 | 0.111 |   0.065 |    0.606 |
    | CTS_ccl_a_BUF_i_clk_G0_L2_2/A | ^ | CTS_122     | CLKBUFX16 | 0.002 |   0.067 |    0.608 |
    | CTS_ccl_a_BUF_i_clk_G0_L2_2/Y | ^ | CTS_121     | CLKBUFX16 | 0.160 |   0.227 |    0.768 |
    | CTS_ccl_a_BUF_i_clk_G0_L3_15/A | ^ | CTS_121     | CLKBUFX12 | 0.033 |   0.260 |    0.801 |
    | CTS_ccl_a_BUF_i_clk_G0_L3_15/Y | ^ | CTS_108     | CLKBUFX12 | 0.236 |   0.496 |    1.037 |
    | current_out_count_reg_9_/CK | ^ | CTS_108     | DFFRX1    | 0.002 |   0.498 |    1.039 |
    +-----------------------------------------------------------------------------------+
```

5. Attach the snapshot of GDS stream out messages. (10%)



```
----------------------------------------
Stream Out Layer Mapping Information:
GDS Layer Number          GDS Layer Name
----------------------------------------
    31                            METAL1
    131                           METAL1
    51                             VIA12
    32                            METAL2
    132                           METAL2
    52                             VIA23
    33                            METAL3
    133                           METAL3
    53                             VIA34
    34                            METAL4
    134                           METAL4
    54                             VIA45
    35                            METAL5
    135                           METAL5
    55                             VIA56
    36                            METAL6
    136                           METAL6
    56                             VIA67
    37                            METAL7
    137                           METAL7
    57                             VIA78
    38                            METAL8
    138                           METAL8
    131                           METAL1
    132                           METAL2
    133                           METAL3
    134                           METAL4
    135                           METAL5
    136                           METAL6
    137                           METAL7
    138                           METAL8
```

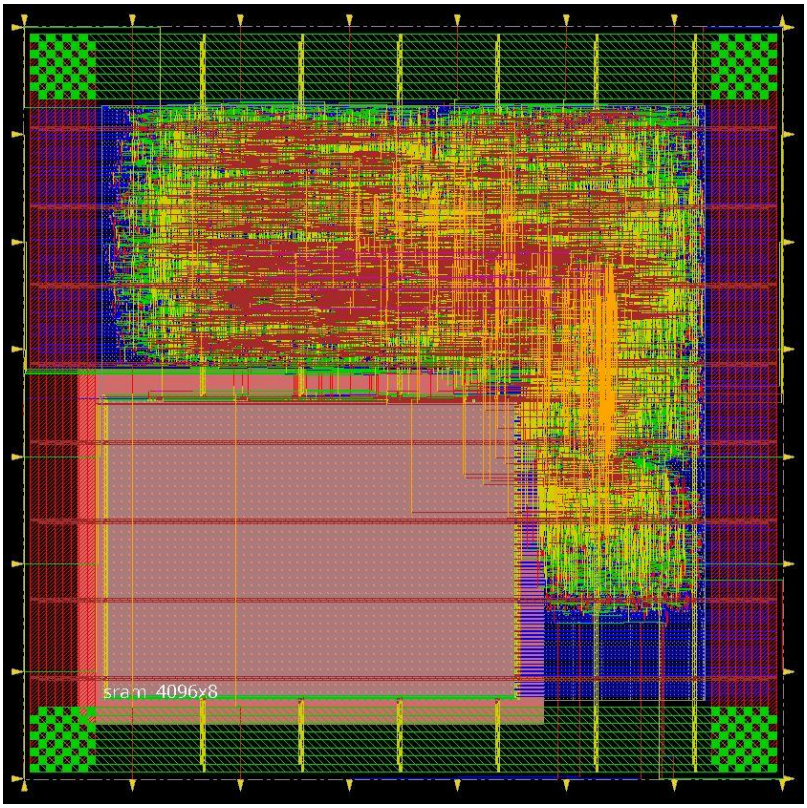
```
Stream Out Information Processed for GDS version 5:
Units: 1000 DBU

Object                             Count
----------------------------------------
Instances                          25004

Ports/Pins                            32
    metal layer METAL2                16
    metal layer METAL3                16

Nets                              137937
    metal layer METAL1                10363
    metal layer METAL2                65267
    metal layer METAL3                37810
    metal layer METAL4                17545
    metal layer METAL5                6270
    metal layer METAL6                670
    metal layer METAL7                12

    Via Instances                 83610

Special Nets                          643
    metal layer METAL1                499
    metal layer METAL2                24
    metal layer METAL3                16
    metal layer METAL4                23
    metal layer METAL5                81

    Via Instances                 3939

Metal Fills                           0

    Via Instances                     0

Metal FillOPCs                        0

    Via Instances                     0

Text                                  34
    metal layer METAL2                18
    metal layer METAL3                16


Blockages                             0


Custom Text                           0


Custom Box                            0

Trim Metal                            0
```

```
Merging with GDS libraries
Scanning GDS file gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file gds/sram_4096x8.gds to register cell name ......
Scanning GDS file gds/tpz013g3_v1.1.gds to register cell name ......
Merging GDS file gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file gds/sram_4096x8.gds ......
        ****** Merge file: gds/sram_4096x8.gds has version number: 5.
        ****** Merge file: gds/sram_4096x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file gds/tpz013g3_v1.1.gds ......
        ****** Merge file: gds/tpz013g3_v1.1.gds has version number: 5.
        ****** Merge file: gds/tpz013g3_v1.1.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
************************ Analyze Floorplan *************************
    Die Area(um^2)              : 591519.76
    Core Area(um^2)             : 370515.26
    Chip Density (Counting Std Cells and MACROs and IOs): 57.897%
    Core Density (Counting Std Cells and MACROs): 92.431%
    Average utilization         : 100.000%
    Number of instance(s)       : 25004
    Number of Macro(s)          : 1
    Number of IO Pin(s)         : 32
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

正方形的 floorplan，io 接口等距分布，由於我使用 4096x8 的 SRAM，面積雖較大，但由於只有一顆，故選擇放在角落的部分，留給整體線路較完整的範圍，若放在中間，可能會導致接線較長，需要繞較多次。