Computer-Aided VLSI System Design
Final Report

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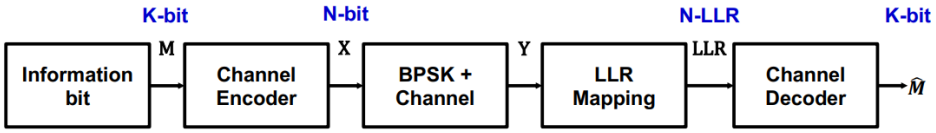
Outline

1 架構設計

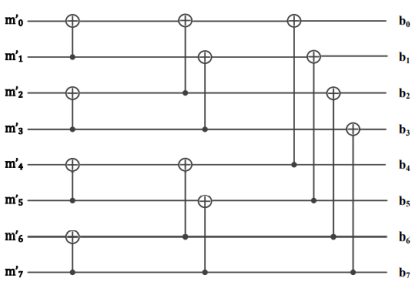
1.1 題目敘述

這次題目是實作 Polar-decoder，目標是希望能將編碼(Polar encode)後的訊號解碼成原始訊號。整體編碼的過程如下:



首先根據原始訊號長度(K)、編碼長度(N)以及各通道的信賴度(Reliability)，將原始訊號插入在信賴度較高的 K 個通道中，其餘則插入 0 也稱為 Frozen channel。

爾後乘上一個 G matrix (Generator matrix)，再取二的餘數(mod 2)，即可完成基本的 Channel encode。乘上 G matrix 是代表各通道的加總結果。如下圖所示:可將其視為一矩陣相乘結果。



$$[b_0 \quad b_1 \quad \cdots \quad b_N] = \overrightarrow{m'}_{1\times N} G_N$$

$$G_8 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

隨後進行 BPSK 的相位偏移，可以根據我們調整的 SNR 以及高斯雜訊標準差的比值來產生不同的E_N，代表我們在傳送 1 bit 時所需的能量。如下圖所示:

最後為避免出現的結果振福相差過大，我們會取 log，稱為 LLR Generation，

$$x_j = \begin{cases} -\sqrt{\frac{2\mathrm{RE_b}}{\mathrm{N_0}}} = -\sqrt{RE_b} = -\sqrt{E_N} & , b_j = 0 \\ \sqrt{\frac{2\mathrm{RE_b}}{\mathrm{N_0}}} = \sqrt{RE_b} = \sqrt{E_N} & , b_j = 1 \end{cases} \quad , \forall j$$

是使用簡化後的方式，如下圖所示:

$$LR(y_j) = \frac{f(y|0)}{f(y|1)} = \frac{\exp\left(-\frac{1}{N_0}\left(y-\left(-\sqrt{\frac{2RE_b}{N_0}}\right)\right)^2\right)}{\exp\left(-\frac{1}{N_0}\left(y-\left(\sqrt{\frac{2RE_b}{N_0}}\right)\right)^2\right)} = \exp\left(-\frac{1}{N_0}\left(4y\sqrt{\frac{2RE_b}{N_0}}\right)\right) = \exp(-2y\sqrt{RE_b})$$

$$LLR(y_j) = \ln(\exp(-2y\sqrt{RE_b})) = -2y\sqrt{RE_b} = -2y\sqrt{E_N}$$

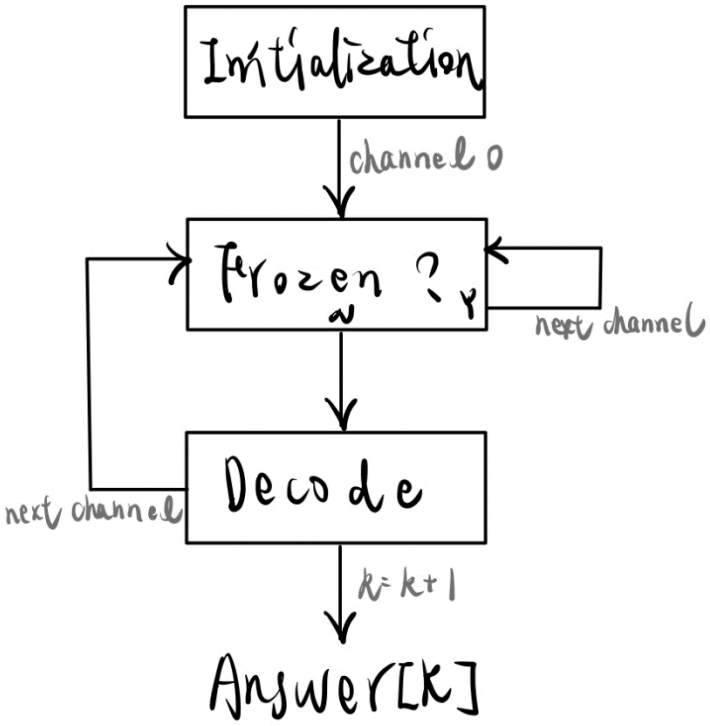
因此，這些 LLR 就是我們編碼後的結果，要依靠我們設計出的 polar decoder 來將其正確的解碼出來。

1.2 演算法

我們使用最簡單的 SC decoder 來完成這次的 final project。

演算法設計如下:

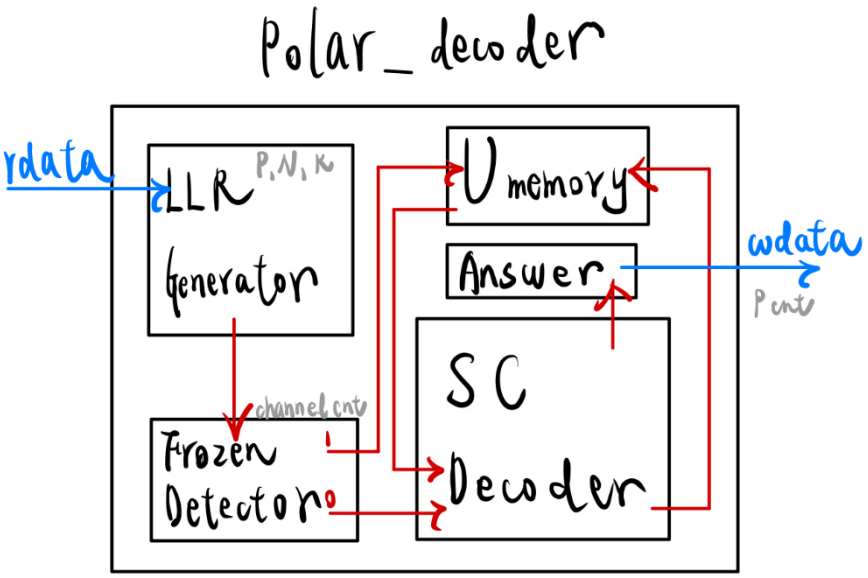
- 將所有 channel 初始化為 0
- 根據 N、K、channel index 及 Reliability 來決定是否為 frozen
- 藉由觀察 channel 的 bit 來知道做 f 或 g 的順序及次數
- 由上往下直到解出該 channel，並繼續解下一個
- 若該 channel 為 frozen，則跳過解下一個
- 直到所有 channel 解出則停止



Decoder 演算法流程

1.3 硬體架構

整體架構圖如下:

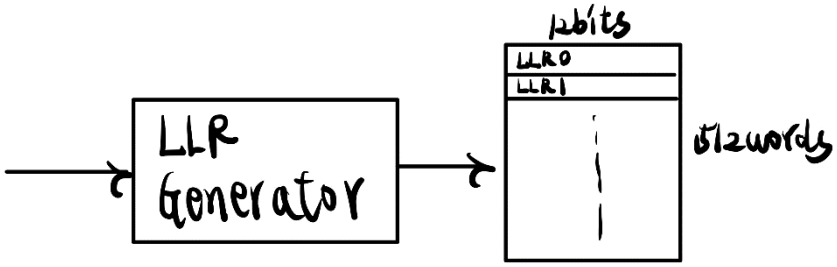


Decoder 硬體架構圖

細節說明:

- LLR Generator

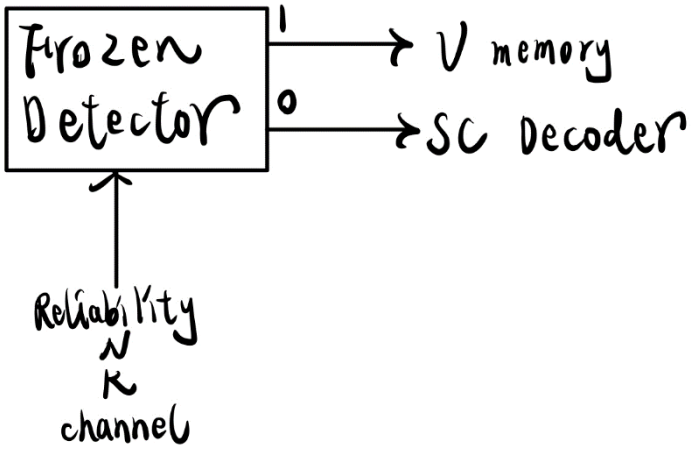
讀到 LLR 資訊後，將之排列為 12 bits, 512 words 的形式，由上自下分別為 LLR0~LLR511，方便後續進行解碼。



LLR generator

- Frozen Detector

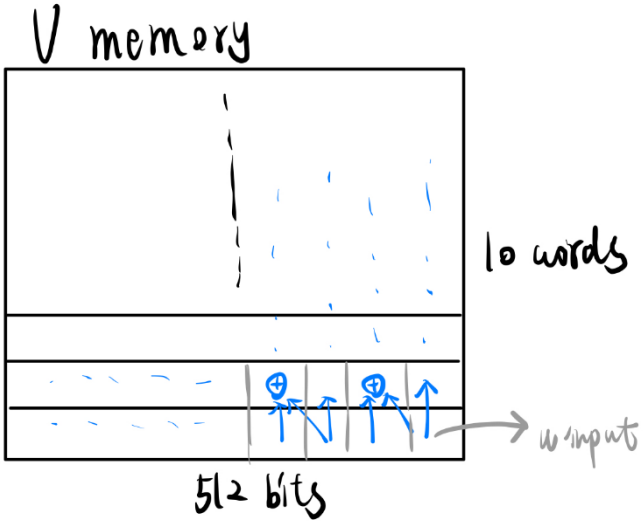
會根據目前要解的 channel (從零開始)、Reliability、N 以及 K，來判斷此通道是否為 frozen，若是，則將零輸入進 U memory；反之則送入 decoder 進行解碼。



Frozen detector

- U Memory

目的是將所有 u 值依照解碼的程度進行安排，會將最新算出的 u 根據 channel 放入最底層，同時往上更新所有 u 值，連接方式是根據位置決定為直接連接或是兩兩做 XOR，這樣再後續若需要進行 g function 的運算，可以直接取得相對應的 u 值。

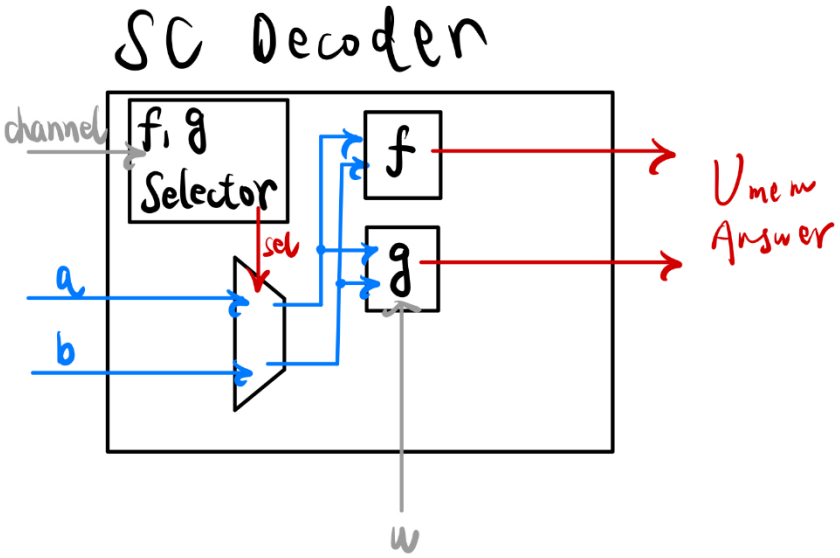


U memory

- SC Decoder

我們採用一個 cycle 只解一個 f 或 g，因此若 N 為 512，則第一次需要做 256 次的 f 或 g，可藉由 channel 的 bit 數來判斷，做完相對應的次數，就繼續向下解剩餘的 128、64、32……直到最後一個 u 被解出，並將之輸入 U memory 最底層。

且為避免在進行 f 及 g 運算時會有 overflow 的問題，我們將要運算的資料以 20 signed bit 儲存，應該足以應對 worst-case 的情形 (累加最多次的 g，且每次都 overflow)。



SC decoder

- Answer

若該 channel 非 frozen，我們會進行 decoder，並將結果放入 answer 中 (位置由 0 到 K)，不足 140 bits 則會在前面補零，最後根據目前解第幾個 packet 輸出答案。

2 優化處理

2.1 時間及面積

在時間的優化上面，原本我們打算一次算完全部的 f 或 g，就是把 SC decoder 的部分展開做 256 次，在 RTL 模擬上面時間確實有大幅下降，但在後續合成的部分，可能因為電路有許多重複的模塊，導致整體面積過大，合成了 15 個小時也和不出結果。

後來我們決定一次只做一個 f 或 g，因此之前需要重複的部分只需一個即可，這樣一來整體面積有大幅下降，但換來的是運算時間的增加，因此在 area、time 的 trade-off 上，我們決定犧牲運算時間換取較小的面積，方便後續合成及 APR 的進行。

差異表格如下: (但前版本沒跑完合成故以大概面積比較，時間以 BASE 比較)

	256 times/ cycle	1 times/cycle
Time (ns)	389400	5722780
Area (um^2)	~17000000	1145353
合成時間	>15 hrs	< 1hr

2.2 功率

原本想加入 clock-gating 來降低功耗，但會有難以處理的 timing 問題，因此我們決定不使用 clock-gating。

3 結果及討論

3.1 MATLAB 演算法驗證

隨機產生 10000 筆數據，總共的 BER 約為 0.0016，因此我們認為此編碼及解碼的演算法準確率符合標準，進而使用來產生 full pattern 以及解碼器 Verilog 的撰寫。

3.2 Timing & area report

合成完後整體面積大約在 1145352um^2，且在 critical path 的地方也有符合 slack 小於零。

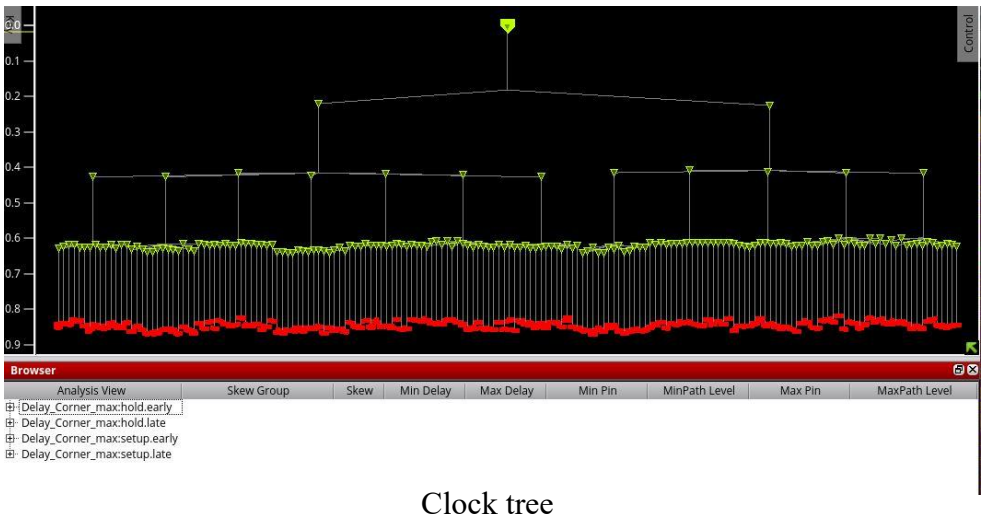
```
****************************************
Report : area
Design : polar_decoder
Version: R-2020.09-SP5
Date   : Mon Dec 19 22:03:02 2022
****************************************

Information: Updating design information... (UID
Warning: Design 'polar_decoder' contains 1 high-
Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_I

Number of ports:                          946
Number of nets:                         79599
Number of cells:                        72585
Number of combinational cells:          55274
Number of sequential cells:             17283
Number of macros/black boxes:               0
Number of buf/inv:                      14006
Number of references:                     259

Combinational area:             556793.034860
Buf/Inv area:                   115508.070199
Noncombinational area:          588559.862581
Macro/Black Box area:                0.000000
Net Interconnect area:        10896582.085968

Total cell area:               1145352.897441
Total area:                   12041934.983409
```

Area report

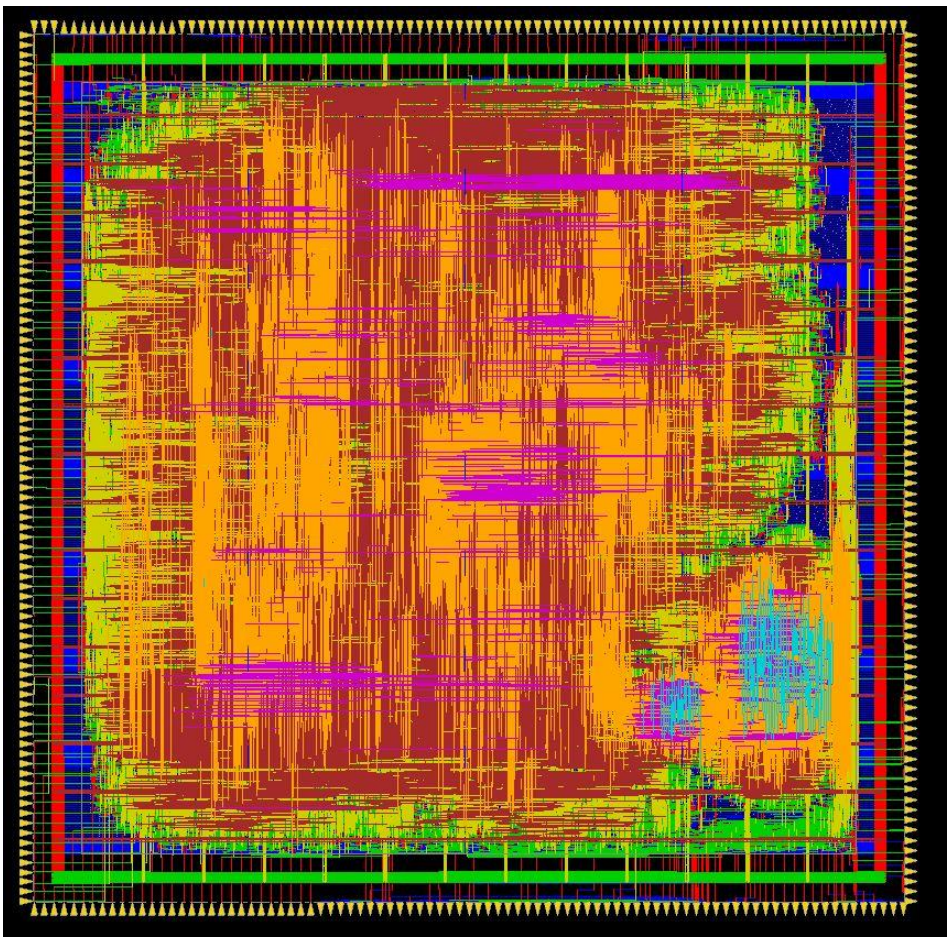
```
  Operating Conditions: slow   Library: slow
  Wire Load Model Mode: top

    Startpoint: current_depth_reg[0]
                (rising edge-triggered flip-flop clocked by clk)
    Endpoint: LLR_tmp_reg[193][9]
              (rising edge-triggered flip-flop clocked by clk)
    Path Group: clk
    Path Type: max


clock clk (rise edge)                          10.00      10.00
clock network delay (ideal)                     0.00      10.00
clock uncertainty                              -0.10       9.90
LLR_tmp_reg[193][9]/CK (DFFRX1)                 0.00       9.90 r
library setup time                             -0.31       9.59
data required time                                         9.59
-----------------------------------------------------------------
data required time                                         9.59
data arrival time                                         -9.59
-----------------------------------------------------------------
slack (MET)                                                0.00
```

Time report

3.3 Route



Clock tree



Route result

3.4 Violation

可由以下報告看出在 APR 階段皆未有任何 violation

```
VERIFY DRC ...... Sub-Area : 60 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {728.960 1275.680 911.200 1437.460} 61 of 64
VERIFY DRC ...... Sub-Area : 61 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {911.200 1275.680 1093.440 1437.460} 62 of 64
VERIFY DRC ...... Sub-Area : 62 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {1093.440 1275.680 1275.680 1437.460} 63 of 64
VERIFY DRC ...... Sub-Area : 63 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {1275.680 1275.680 1441.640 1437.460} 64 of 64
VERIFY DRC ...... Sub-Area : 64 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:47.2  ELAPSED TIME: 48.00  MEM: 2.0M) ***
```

DRC

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue Dec 20 07:59:37 2022

Design Name: polar_decoder
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1441.6400, 1437.4600)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 07:59:41 **** Processed 5000 nets.
**** 07:59:41 **** Processed 10000 nets.
**** 07:59:42 **** Processed 15000 nets.
**** 07:59:42 **** Processed 20000 nets.
**** 07:59:42 **** Processed 25000 nets.
**** 07:59:43 **** Processed 30000 nets.
**** 07:59:43 **** Processed 35000 nets.
**** 07:59:44 **** Processed 40000 nets.
**** 07:59:44 **** Processed 45000 nets.
**** 07:59:44 **** Processed 50000 nets.
**** 07:59:45 **** Processed 55000 nets.
**** 07:59:45 **** Processed 60000 nets.
**** 07:59:46 **** Processed 65000 nets.
**** 07:59:47 **** Processed 70000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Dec 20 07:59:51 2022
Time Elapsed: 0:00:14.0
```

LVS

```
******* START VERIFY ANTENNA ********
Report File: polar_decoder.antenna.rpt
LEF Macro File: polar_decoder.antenna.lef
5000 nets processed: 0 violations
10000 nets processed: 0 violations
15000 nets processed: 0 violations
20000 nets processed: 0 violations
25000 nets processed: 0 violations
30000 nets processed: 0 violations
35000 nets processed: 0 violations
40000 nets processed: 0 violations
45000 nets processed: 0 violations
50000 nets processed: 0 violations
55000 nets processed: 0 violations
60000 nets processed: 0 violations
65000 nets processed: 0 violations
70000 nets processed: 0 violations
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:16.0  MEM: 0.000M)
```

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.294  |  0.294  |  6.303  |  7.700  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|         All Paths:|  34715  |  17283  |  23452  |   158   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+---------------+-------------------------------+------------------+
|               |              Real             |       Total      |
|    DRVs       +------------------+------------+------------------|
|               |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+---------------+------------------+------------+------------------+
|   max_cap     |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran    |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout  |      0 (0)       |     0      |      0 (0)       |
|   max_length  |      0 (0)       |     0      |      0 (0)       |
+---------------+------------------+------------+------------------+

Density: 63.291%
Total number of glitch violations: 0
------------------------------------------------------------
```

Setup timing report

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  1.371  |  1.371  |  1.396  |  2.542  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|         All Paths:|  34715  |  17283  |  23452  |   158   |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 63.291%
------------------------------------------------------------
```

Hold timing report

3.5 Critical path

- Setup: 0.294 (reg2reg)

```
#####################################################################
#  Generated by:      Cadence Innovus 17.11-s080_1
#  OS:                Linux x86_64(Host ID cad33)
#  Generated on:      Tue Dec 20 07:51:47 2022
#  Design:            polar_decoder
#  Command:           timeDesign -postRoute -pathReports -drvReports -slackReports -numPaths 50 -prefix polar_
#####################################################################
Path 1: MET Setup Check with Pin LLR_tmp_reg_199__19_/CK
Endpoint:   LLR_tmp_reg_199__19_/D (^) checked with  leading edge of 'clk'
Beginpoint: j_reg_5_/Q             (v) triggered by  leading edge of 'clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.858
- Setup                         0.259
+ Phase Shift                  10.000
+ CPPR Adjustment               0.000
= Required Time                10.599
- Arrival Time                 10.305
= Slack Time                    0.294
     Clock Rise Edge                     0.000
     + Drive Adjustment                  0.059
     + Source Insertion Delay           -0.912
     = Beginpoint Arrival Time          -0.853
```

add_0_root_add_2343_ni/U1_1_2/A	v	N103706	ADDHX2	0.000	6.193	6.487
add_0_root_add_2343_ni/U1_1_2/CO	v	add_0_root_add_2343_ni/carry[3]	ADDHX2	0.215	6.408	6.702
add_0_root_add_2343_ni/U1_1_3/B	v	add_0_root_add_2343_ni/carry[3]	ADDHX2	0.000	6.408	6.702
add_0_root_add_2343_ni/U1_1_3/CO	v	add_0_root_add_2343_ni/carry[4]	ADDHX2	0.191	6.599	6.893
add_0_root_add_2343_ni/U1_1_4/B	v	add_0_root_add_2343_ni/carry[4]	ADDHX4	0.000	6.599	6.893
add_0_root_add_2343_ni/U1_1_4/CO	v	add_0_root_add_2343_ni/carry[5]	ADDHX4	0.154	6.753	7.047
add_0_root_add_2343_ni/U1_1_5/B	v	add_0_root_add_2343_ni/carry[5]	ADDHX4	0.000	6.753	7.047
add_0_root_add_2343_ni/U1_1_5/CO	v	add_0_root_add_2343_ni/carry[6]	ADDHX4	0.143	6.897	7.190
add_0_root_add_2343_ni/U1_1_6/B	v	add_0_root_add_2343_ni/carry[6]	ADDHX4	0.000	6.897	7.191
add_0_root_add_2343_ni/U1_1_6/CO	v	add_0_root_add_2343_ni/carry[7]	ADDHX4	0.147	7.043	7.337
add_0_root_add_2343_ni/U1_1_7/B	v	add_0_root_add_2343_ni/carry[7]	ADDHX4	0.000	7.043	7.337
add_0_root_add_2343_ni/U1_1_7/CO	v	add_0_root_add_2343_ni/carry[8]	ADDHX4	0.144	7.188	7.482
add_0_root_add_2343_ni/U1_1_8/B	v	add_0_root_add_2343_ni/carry[8]	ADDHX4	0.000	7.188	7.482
add_0_root_add_2343_ni/U1_1_8/CO	v	add_0_root_add_2343_ni/carry[9]	ADDHX4	0.141	7.328	7.622
add_0_root_add_2343_ni/U1_1_9/B	v	add_0_root_add_2343_ni/carry[9]	ADDHX4	0.000	7.328	7.622
add_0_root_add_2343_ni/U1_1_9/CO	v	add_0_root_add_2343_ni/carry[10]	ADDHX4	0.141	7.469	7.763
add_0_root_add_2343_ni/U1_1_10/B	v	add_0_root_add_2343_ni/carry[10]	ADDHX4	0.000	7.469	7.763
add_0_root_add_2343_ni/U1_1_10/CO	v	add_0_root_add_2343_ni/carry[11]	ADDHX4	0.143	7.612	7.906
add_0_root_add_2343_ni/U1_1_11/B	v	add_0_root_add_2343_ni/carry[11]	ADDHX4	0.000	7.612	7.906
add_0_root_add_2343_ni/U1_1_11/CO	v	add_0_root_add_2343_ni/carry[12]	ADDHX4	0.146	7.758	8.052
add_0_root_add_2343_ni/U1_1_12/B	v	add_0_root_add_2343_ni/carry[12]	ADDHX4	0.000	7.759	8.053
add_0_root_add_2343_ni/U1_1_12/CO	v	add_0_root_add_2343_ni/carry[13]	ADDHX4	0.142	7.901	8.195
add_0_root_add_2343_ni/U1_1_13/B	v	add_0_root_add_2343_ni/carry[13]	ADDHX4	0.000	7.901	8.195
add_0_root_add_2343_ni/U1_1_13/CO	v	add_0_root_add_2343_ni/carry[14]	ADDHX4	0.142	8.043	8.337
add_0_root_add_2343_ni/U1_1_14/B	v	add_0_root_add_2343_ni/carry[14]	ADDHX4	0.000	8.043	8.337
add_0_root_add_2343_ni/U1_1_14/CO	v	add_0_root_add_2343_ni/carry[15]	ADDHX4	0.145	8.188	8.482
add_0_root_add_2343_ni/U1_1_15/B	v	add_0_root_add_2343_ni/carry[15]	ADDHX4	0.000	8.188	8.482
add_0_root_add_2343_ni/U1_1_15/CO	v	add_0_root_add_2343_ni/carry[16]	ADDHX4	0.132	8.320	8.614
add_0_root_add_2343_ni/U1_1_16/B	v	add_0_root_add_2343_ni/carry[16]	ADDHX2	0.000	8.320	8.614
add_0_root_add_2343_ni/U1_1_16/CO	v	add_0_root_add_2343_ni/carry[17]	ADDHX2	0.168	8.487	8.781
add_0_root_add_2343_ni/U1_1_17/B	v	add_0_root_add_2343_ni/carry[17]	CMPR22X2	0.000	8.487	8.781
add_0_root_add_2343_ni/U1_1_17/CO	v	add_0_root_add_2343_ni/carry[18]	CMPR22X2	0.184	8.671	8.965
add_0_root_add_2343_ni/U1_1_18/B	v	add_0_root_add_2343_ni/carry[18]	ADDHX2	0.000	8.671	8.965
add_0_root_add_2343_ni/U1_1_18/CO	v	add_0_root_add_2343_ni/carry[19]	ADDHX2	0.152	8.823	9.117
add_0_root_add_2343_ni/U1/A	v	add_0_root_add_2343_ni/carry[19]	XOR2X1	0.000	8.823	9.117
add_0_root_add_2343_ni/U1/Y	^	N103728	XOR2X1	0.151	8.974	9.268
U38068/C0	^	N103728	AOI222X2	0.000	8.974	9.268
U38068/Y	v	n9303	AOI222X2	0.194	9.168	9.462
U38067/A0N	v	n9303	OAI2BB1X4	0.000	9.168	9.462
U38067/Y	v	n989	OAI2BB1X4	0.208	9.375	9.669
FE_OFC485_n989/A	v	n989	CLKBUFX20	0.000	9.376	9.669
FE_OFC485_n989/Y	v	FE_OFN485_n989	CLKBUFX20	0.208	9.584	9.878
FE_OCPC2940_FE_OFN485_n989/A	v	FE_OFN485_n989	BUFX20	0.015	9.599	9.893
FE_OCPC2940_FE_OFN485_n989/Y	v	FE_OCPN2940_FE_OFN485_n989	BUFX20	0.152	9.752	10.045
FE_OFC488_n989/A	v	FE_OCPN2940_FE_OFN485_n989	BUFX12	0.002	9.753	10.047
FE_OFC488_n989/Y	v	FE_OFN488_n989	BUFX12	0.189	9.942	10.236
U37952/B1	v	FE_OFN488_n989	OAI221XL	0.005	9.947	10.241
U37952/Y	^	n33837	OAI221XL	0.358	10.305	10.599
LLR_tmp_reg_199__19_/D	^	n33837	DFFRX1	0.000	10.305	10.599

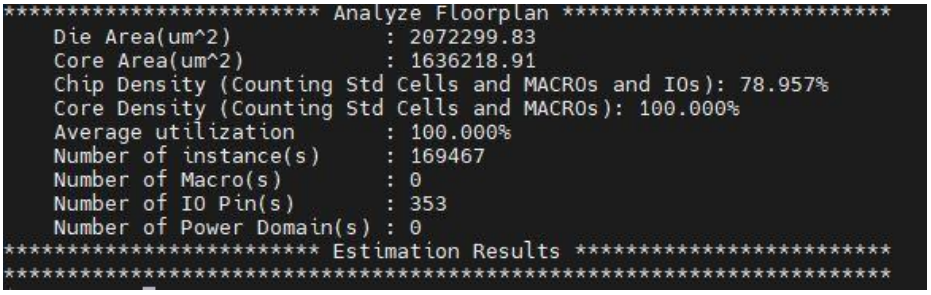
Timing Path:

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk			-0.853	-0.559
CTS_ccl_BUF_clk_G0_L1_1/A	^	clk	CLKBUFX12	0.004	-0.850	-0.556
CTS_ccl_BUF_clk_G0_L1_1/Y	^	CTS_758	CLKBUFX12	0.169	-0.680	-0.386
CTS_ccl_BUF_clk_G0_L2_2/A	^	CTS_758	CLKBUFX16	0.036	-0.645	-0.351
CTS_ccl_BUF_clk_G0_L2_2/Y	^	CTS_757	CLKBUFX16	0.176	-0.468	-0.175
CTS_ccl_a_BUF_clk_G0_L3_11/A	^	CTS_757	CLKBUFX16	0.000	-0.468	-0.174
CTS_ccl_a_BUF_clk_G0_L3_11/Y	^	CTS_741	CLKBUFX16	0.197	-0.271	0.023
CTS_ccl_a_BUF_clk_G0_L4_156/A	^	CTS_741	CLKBUFX16	0.003	-0.268	0.026
CTS_ccl_a_BUF_clk_G0_L4_156/Y	^	CTS_736	CLKBUFX16	0.208	-0.059	0.235
j_reg_5_/CK	^	CTS_736	DFFRX2	0.002	-0.057	0.237
j_reg_5_/Q	v	N1812	DFFRX2	0.789	0.732	1.026
U76739/B	v	N1812	NOR2X1	0.000	0.733	1.027
U76739/Y	^	n57888	NOR2X1	0.719	1.452	1.746
U32634/B	^	n57888	AND2X4	0.000	1.452	1.746
U32634/Y	^	net627490	AND2X4	0.538	1.990	2.284
FE_OFC2759_net627490/A	^	net627490	CLKINVX3	0.006	1.996	2.290
FE_OFC2759_net627490/Y	v	FE_OFN642630_net627490	CLKINVX3	0.591	2.587	2.881
U81692/B0	v	FE_OFN642630_net627490	AOI21X2	0.005	2.592	2.886
U81692/Y	^	n63614	AOI21X2	1.657	4.249	4.543
U81693/D	^	n63614	NOR4X1	0.000	4.249	4.543
U81693/Y	v	n63618	NOR4X1	0.232	4.480	4.774
FE_OFC2070_n63618/A	v	n63618	BUFX4	0.000	4.480	4.774
FE_OFC2070_n63618/Y	v	FE_OFN2070_n63618	BUFX4	0.283	4.764	5.058
U45321/D	v	FE_OFN2070_n63618	NAND4X4	0.003	4.766	5.060
U45321/Y	^	n63890	NAND4X4	0.258	5.024	5.318
U47120/A0	^	n63890	OAI33X2	0.004	5.029	5.323
U47120/Y	v	N103420	OAI33X2	0.171	5.200	5.494
FE_OFC2078_N103420/A	v	N103420	BUFX12	0.000	5.200	5.494
FE_OFC2078_N103420/Y	v	FE_OFN2078_N103420	BUFX12	0.221	5.421	5.715
FE_DBTC101_N103420/A	v	FE_OFN2078_N103420	INVX6	0.002	5.422	5.716
FE_DBTC101_N103420/Y	^	FE_DBTN101_N103420	INVX6	0.182	5.604	5.898
U45791/B1	^	FE_DBTN101_N103420	AO22X1	0.002	5.606	5.900
U45791/Y	^	N103570	AO22X1	0.407	6.013	6.307
U45322/A	^	N103570	CLKINVX1	0.000	6.013	6.307
U45322/Y	v	N103706	CLKINVX1	0.180	6.193	6.487

- Hold :1.371 (reg2reg)

```
#####################################################################
#  Generated by:      Cadence Innovus 17.11-s080_1
#  OS:                Linux x86_64(Host ID cad33)
#  Generated on:      Tue Dec 20 07:55:07 2022
#  Design:            polar_decoder
#  Command:           timeDesign -postRoute -hold -pathReports -slackReports -numPaths 50 -prefix polar_
#####################################################################
Path 1: MET Hold Check with Pin P_reg_5_/CK
Endpoint:   P_reg_5_/D  (v) checked with  leading edge of 'clk'
Beginpoint: P_reg_5_/QN (^) triggered by  leading edge of 'clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time        -0.057
+ Hold                        -0.014
+ Phase Shift                  0.000
- CPPR Adjustment              0.000
= Required Time               -0.071
 Arrival Time                  1.299
 Slack Time                    1.371
    Clock Rise Edge                     0.000
    + Drive Adjustment                  0.059
    = Beginpoint Arrival Time           0.059
    Timing Path:
    +-------------------------------------------------------------------------------+
    |           Pin           | Edge |   Net   |   Cell    | Delay | Arrival | Required |
    |                         |      |         |           |       |  Time   |   Time   |
    |-------------------------+------+---------+-----------+-------+---------+----------|
    | clk                     | ^    | clk     |           |       |   0.059 |   -1.312 |
    | CTS_ccl_BUF_clk_G0_L1_1/A   | ^    | clk     | CLKBUFX12 | 0.004 |   0.063 |   -1.308 |
    | CTS_ccl_BUF_clk_G0_L1_1/Y   | ^    | CTS_758 | CLKBUFX12 | 0.169 |   0.232 |   -1.139 |
    | CTS_ccl_BUF_clk_G0_L2_1/A   | ^    | CTS_758 | CLKBUFX20 | 0.032 |   0.264 |   -1.107 |
    | CTS_ccl_BUF_clk_G0_L2_1/Y   | ^    | CTS_678 | CLKBUFX20 | 0.187 |   0.451 |   -0.920 |
    | CTS_ccl_a_BUF_clk_G0_L3_7/A | ^    | CTS_678 | CLKBUFX20 | 0.010 |   0.461 |   -0.910 |
    | CTS_ccl_a_BUF_clk_G0_L3_7/Y | ^    | CTS_677 | CLKBUFX20 | 0.184 |   0.645 |   -0.726 |
    | CTS_ccl_a_BUF_clk_G0_L4_88/A | ^    | CTS_677 | CLKBUFX16 | 0.010 |   0.655 |   -0.716 |
    | CTS_ccl_a_BUF_clk_G0_L4_88/Y | ^    | CTS_663 | CLKBUFX16 | 0.199 |   0.854 |   -0.517 |
    | P_reg_5_/CK             | ^    | CTS_663 | DFFRX1    | 0.002 |   0.855 |   -0.515 |
    | P_reg_5_/QN             | ^    | n10682  | DFFRX1    | 0.367 |   1.222 |   -0.149 |
    | U76561/A0               | ^    | n10682  | OAI22XL   | 0.000 |   1.222 |   -0.149 |
    | U76561/Y                | v    | n44644  | OAI22XL   | 0.077 |   1.299 |   -0.071 |
    | P_reg_5_/D              | v    | n44644  | DFFRX1    | 0.000 |   1.299 |   -0.071 |
    +-------------------------------------------------------------------------------+
    Clock Rise Edge                     0.000
    + Drive Adjustment                  0.059
    + Source Insertion Delay           -0.912
    = Beginpoint Arrival Time          -0.853
```

3.6 Post-area


********** Analyze Floorplan **********
Die Area(um^2) : 2072299.83
Core Area(um^2) : 1636218.91
Chip Density (Counting Std Cells and MACROs and IOs): 78.957%
Core Density (Counting Std Cells and MACROs): 100.000%
Average utilization : 100.000%
Number of instance(s) : 169467
Number of Macro(s) : 0
Number of IO Pin(s) : 353
Number of Power Domain(s) : 0
********** Estimation Results **********
****