Computer-Aided VLSI System Design
Homework 4 Report

Due Tuesday, Nov. 22, 14:00

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Questions and Discussion

1. Fill in the blanks

Physical category		
Design Stage	Description	Value
Gate-level Simulation	Cycle time for Gate-level Simulation (ex. 10ns)	10 ns
	Area for Synthesis (ex. 50000μm^2)	83547 μm^2
	Gate-level Simulation Time for f1	6934.5 ns
	Gate-level Simulation Time for f2	6934.5 ns
	Gate-level Simulation Time for f3	6934.5 ns
	Gate-level Simulation Time for f4	6925.5 ns
	Gate-level Simulation Time for f5	6934.5 ns
	Gate-level Simulation Time for f6	6925.5 ns
	Gate-level Simulation Time for f7	6925.5 ns

2. Specify the methods you adopted for low-power design. (10pts)
   i. 共用 register (減少 register 數量)
   ii. 使用 clock gating 減少 clock 變動量