CH32V007/M007 Datasheet

V1.7

Overview

CH32V007 is an industrial-grade general-purpose microcontroller designed based on QingKe RISC-V core, supporting 48MHz system frequency, 1-wire SDI. CH32V007 has a built-in 12-bit ADC, with a sampling rate of up to 3Msps; it has a built-in high-voltage swing-rate OPA, supporting 3-channel polling, and supporting 1- or 2-resistor current-sampling scheme; it has a built-in 2-group voltage comparator CMP, supports overcurrent protection and 3-channel polling comparator positioning; provides 7-channel DMA controller, 8-channel Touch-key, multi-group timer, 2-channel USART, I2C, SPI and other peripheral resources; can be used for inductive positioning, ADC sampling or comparator non-inductive positioning, 1-resistor or 2-resistor sampling of the motor program.

CH32M007K8U7 and CH32M007G8R6 is equivalent to CH32V007 plus CH283, with built-in 48V three-phase dual-N pre-driver and bootstrap diode and high-voltage LDO. CH32M007E8 is equivalent to CH32V007 plus CH282, with built-in 24V three-phase P+N pre-driver and high-voltage LDO.

Features

- **Core**
  - QingKe 32-bit RISC-V core, RV32EmC instruction set
  - Fast programmable interrupt controller + hardware interrupt stack
  - Support 2-level interrupt nesting
  - Support system main frequency 48MHz
- **Memory**
  - 8KB volatile data storage area SRAM
  - 62KB program memory CodeFlash
  - 256B system non-volatile configuration information storage area
  - 256B user-defined memory
- **Power management and low-power consumption**
  - CH32V007 supports rated 2.5~5V power supply
  - CH32M007K8U7/G8R6 supports rated 6~48V power supply.
  - CH32M007E8 supports rated 6~24V power supply.
  - Low-power mode: Sleep, Standby
- **3-phase half-bridge driver:**
  - CH32M007K8U7/G8R6 built-in 48V dual-N pre-driver and diode
  - CH32M007E8 Built-in 24V three-phase P+N pre-driver
  - Built-in dead-time control to prevent the high side and low side power tubes from going straight through
  - Built-in undervoltage protection
- **Clock & Reset**
  - Built-in factory-trimmed 24MHz RC oscillator
  - Built-in 128KHz RC oscillator
  - High-speed external 3~25MHz oscillator
  - Built-in system clock monitoring (SCM) module
  - Power on/down reset, programmable voltage detector
- **Security features: Chip unique ID**
- **7-channel general-purpose DMA controller**
  - 7 channels, support ring buffer
  - Support TIMx/ADC /USART/I2C/SPI
- **OPA/PGA/CMP:**
  - Multiple input channels, selectable multi-step gain
  - 2 output channels, optional ADC pins
  - Support 3-channel polling, supports single or dual resistor scheme.
  - Support high-speed mode to increase slew rate

- 2-group analog voltage comparator CMP:
  - General-purpose CMP, 3 input channels, supports 3 CMP polling to detect positioning and output to peripherals or I/Os
  - Streamlined CMP, internally cascaded to OPA outputs
- **12-bit ADC**
  - Analog input range: V_{SS}~V_{DD}
  - 8 external signals + 3 internal signals
  - Support 3M sampling rate
- **8-channel touch-key channel detection**
- **Multiple timers**
  - 16-bit advanced-control timer, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 16-bit general-purpose timer, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
  - 16-bit compact timer for auxiliary motor applications
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 32-bit counter
- **2 set of USART**
  - Support LIN
- **I2C interface**
- **SPI interface**
- **GPIO port**
  - 4 sets of GPIO ports, 31 I/O ports
  - Mapping 1 external interrupt
- **Debug mode: 1-wire or 2-wire serial debug interface**
- **Package: QFN, QSOP**

Model	Flash	RAM	GPIO	ADTM	GPTM	Watchdog	GPIO	Three-phase pre-drive		ADC	Touch-key button	OPA	OPA Polling	CMP	Serial port	I2C	SPI	Package form
								Voltage	Structure									
CH32M007E8R6	62K	8K	15	1	1	1	2	24V	P+N	7+2	7-channel	1	3-channel	2	2	1	1	QSOP24
CH32M007E8U6	62K	8K	16	1	1	1	2	24V	P+N	7+2	7-channel	1	3-channel	2	2	1	1	QFN26C3
CH32M007G8R6	62K	8K	12	1	1	1	2	48V	N+N	7+2	7-channel	1	3-channel	2	2	1	1	QSOP28
CH32M007K8U7	62K	8K	17	1	1	1	2	48V	N+N	7+2	7-channel	1	3-channel	2	2	1	1	QFN32
CH32V007E8R6	62K	8K	22	1	1	1	2	-	-	8+2	8-channel	1	3-channel	2	2	1	1	QSOP24
CH32V007K8U6	62K	8K	31	1	1	1	2	-	-	8+2	8-channel	1	3-channel	2	2	1	1	QFN32

Chapter 1 Specification Information

1.1 System Structure

The microcontroller is based on the RISC-V instruction set design, its architecture will be QingKe microprocessor core, arbitration unit, DMA module, SRAM storage and other components through multiple buses to achieve interaction. The design integrates a general-purpose DMA controller to reduce the burden on the CPU, improve access efficiency. Multi-level clock management mechanism is applied to reduce the power consumption of peripherals, while both data protection mechanisms, automatic clock switching protection and other measures to increase system stability. The following diagram shows the overall architecture.

Figure 1-1-1 CH32V007 system block diagram

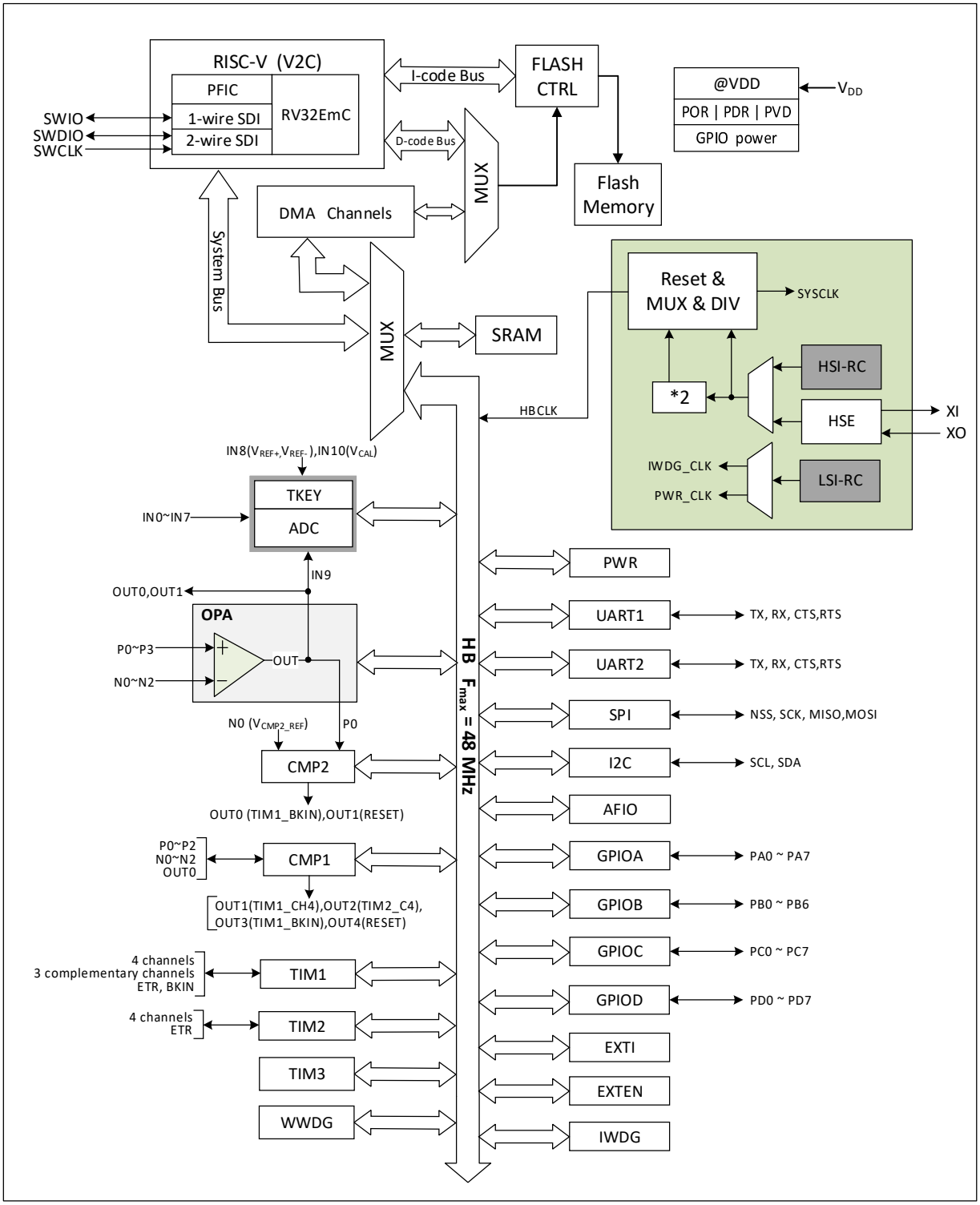


Figure 1-1-2 CH32M007K8U7 and CH32M007G8R6 system block diagram

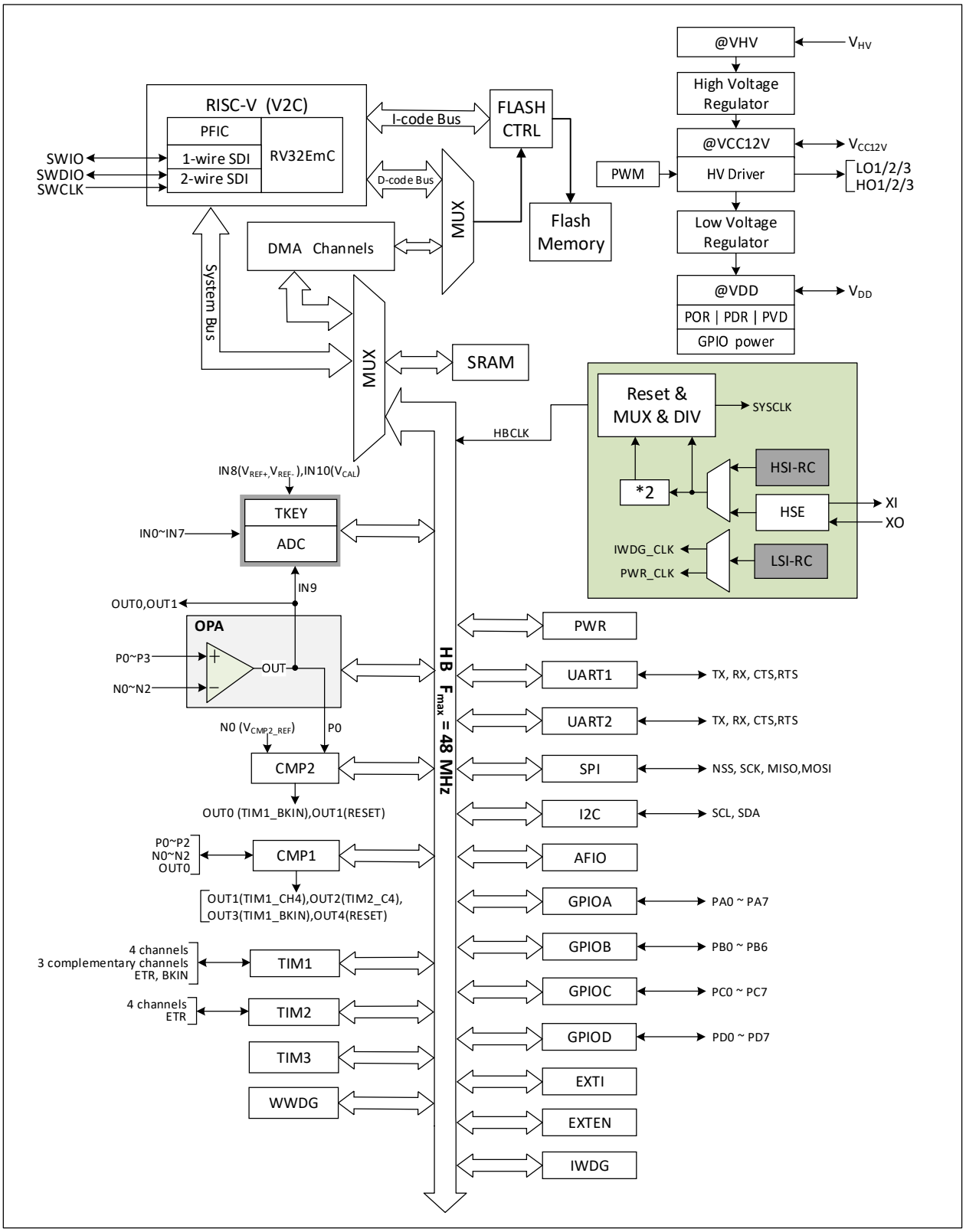


Figure 1-1-3 CH32M007E8U6 system block diagram

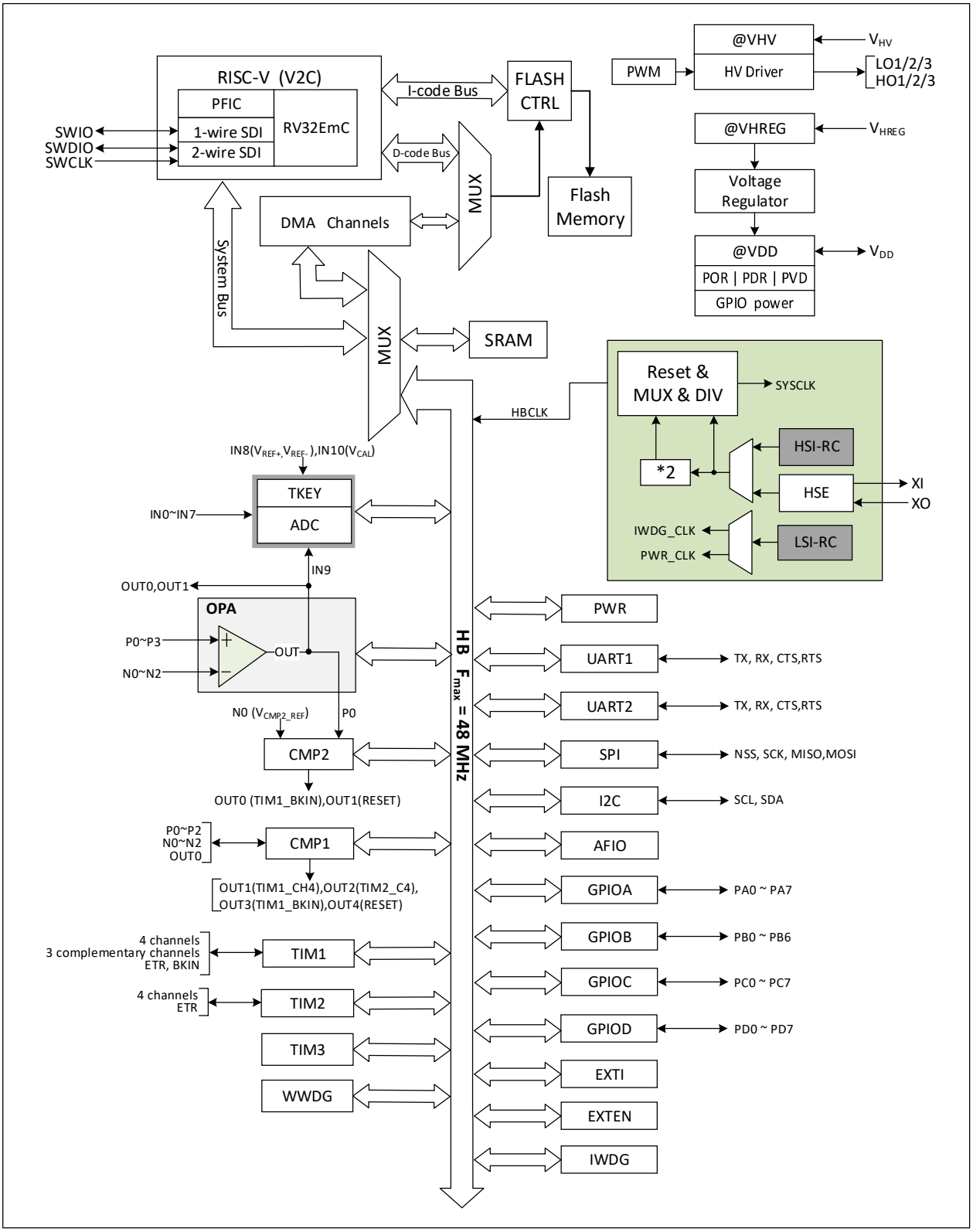
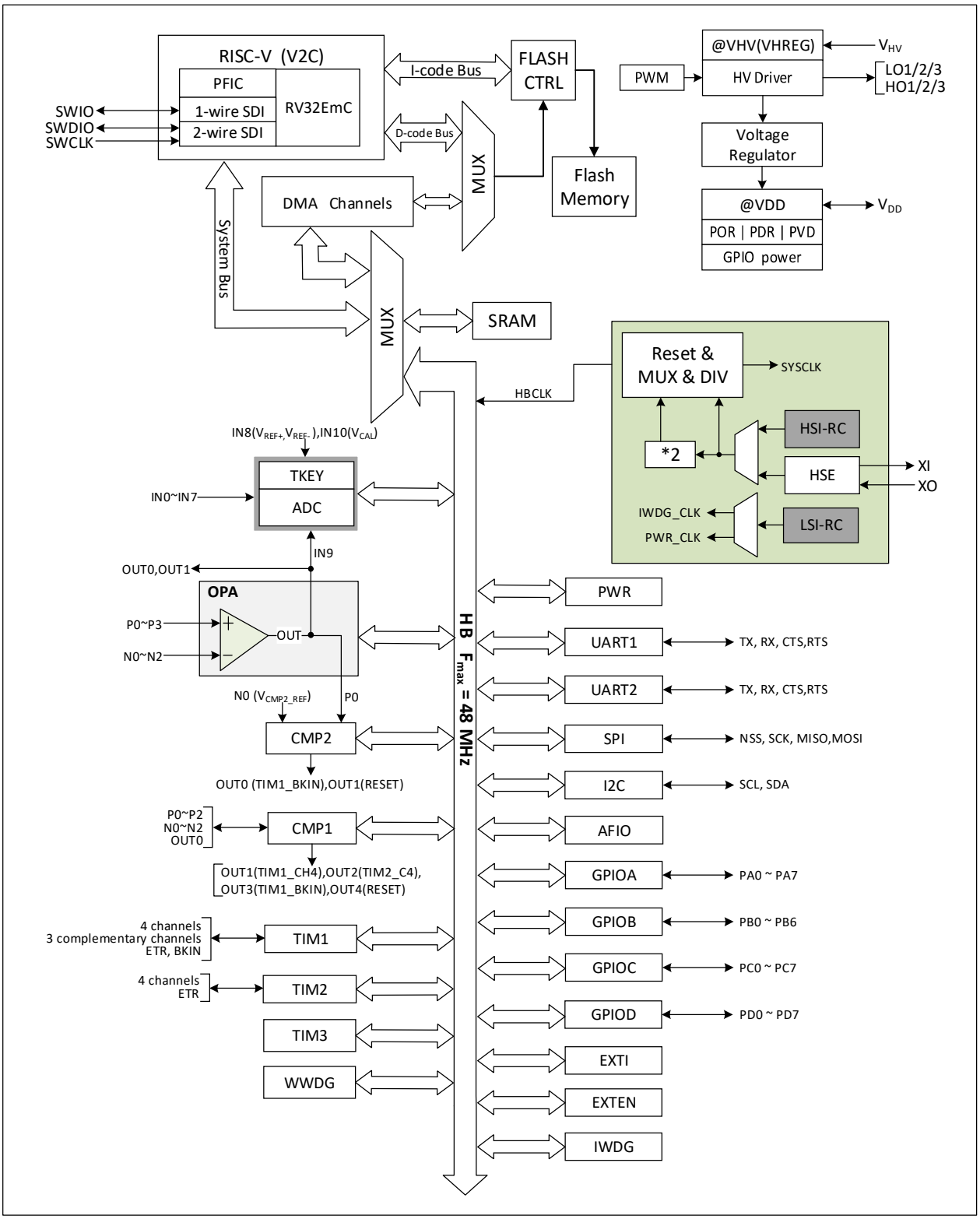
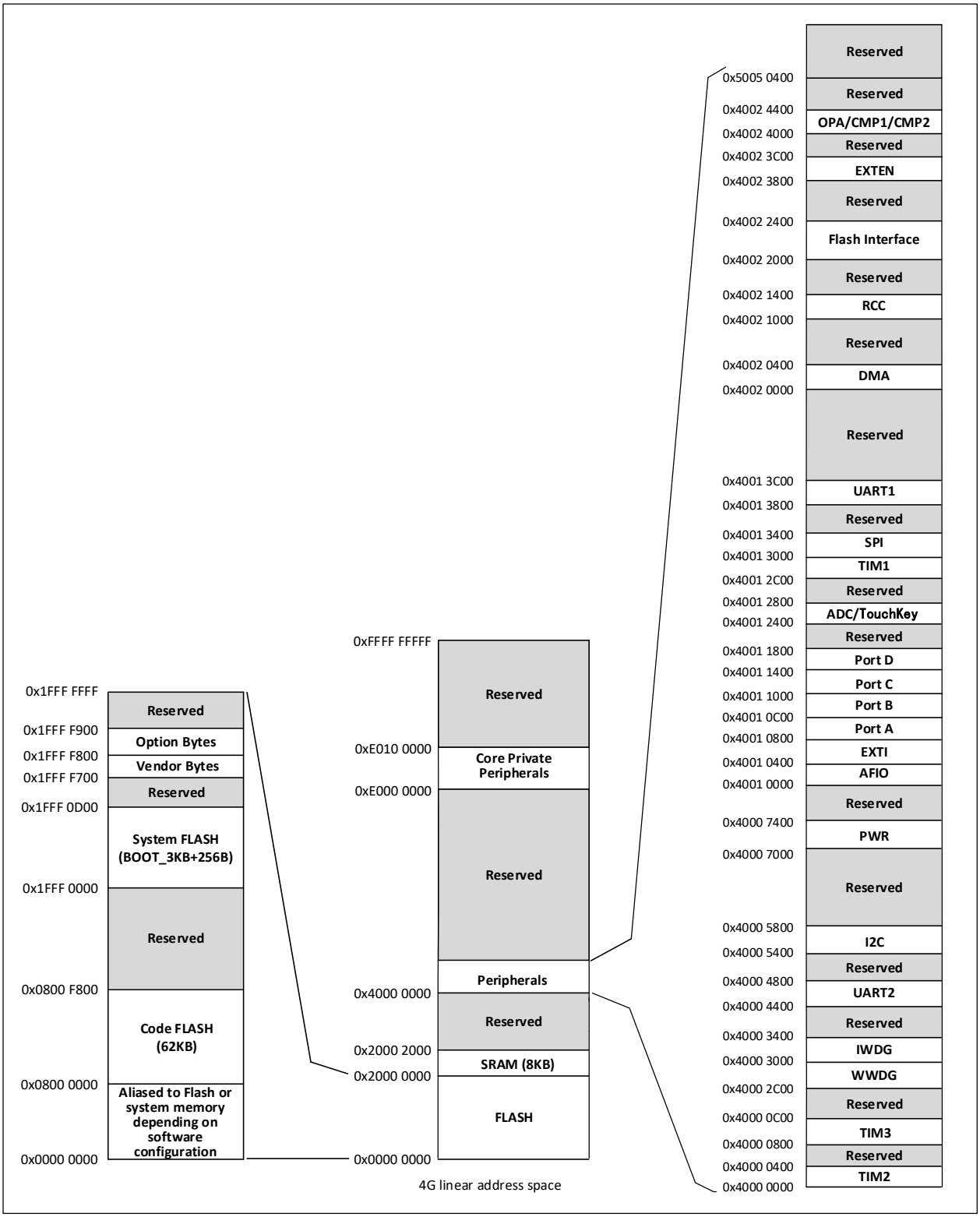


Figure 1-1-4 CH32M007E8R6 system block diagram



1.2 Memory Map

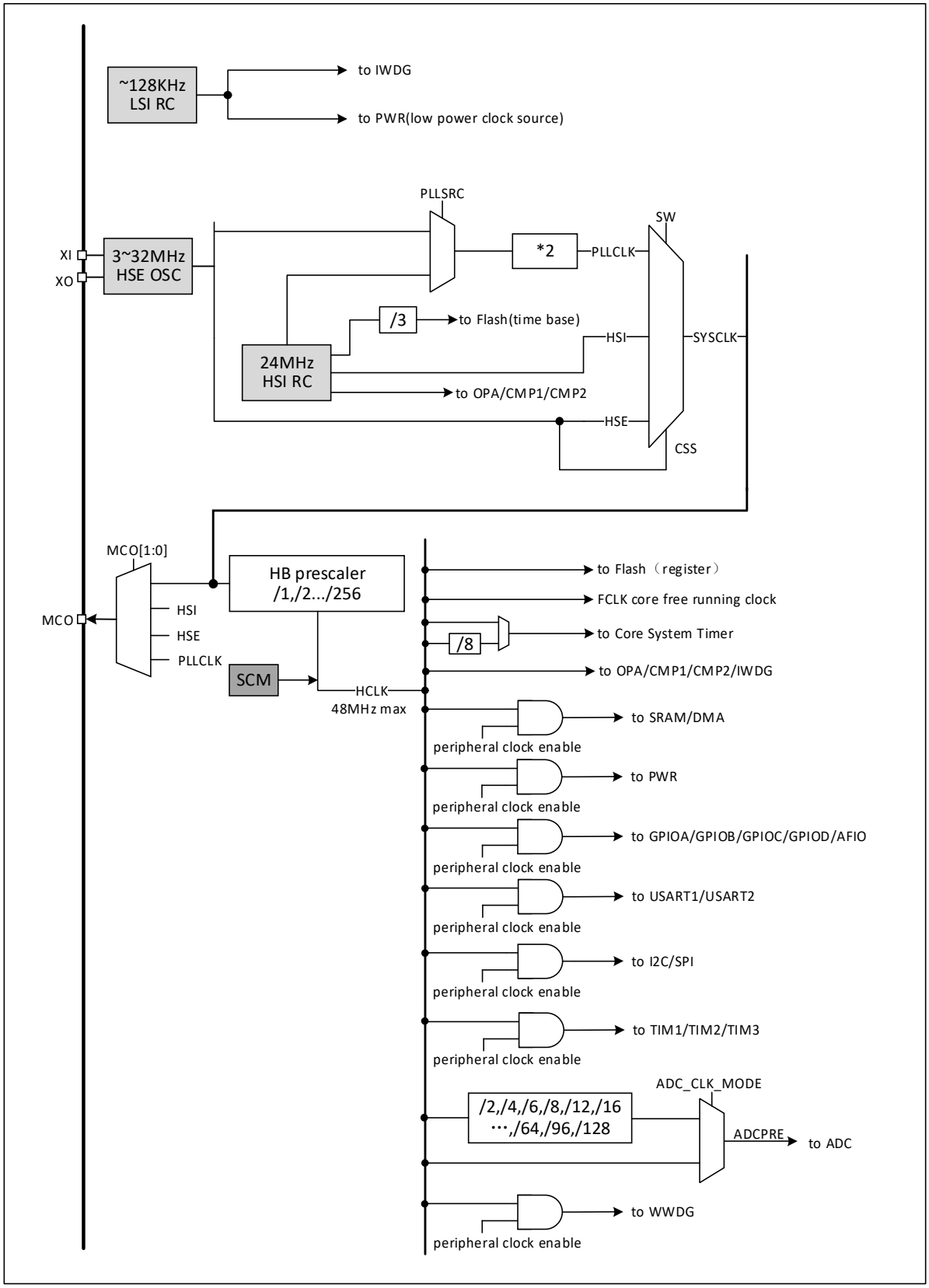
Figure 1-2 Memory address map



1.3 Clock Tree

3 sets of clock sources are introduced into the system: Internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI) and external high-frequency oscillator (HSE). Among them, the low-frequency clock source provides a clock reference for the IWDG, and the high-frequency clock source is directly or indirectly output as the system bus clock (SYSCLK) through a 2x multiplier, and the system clock is then provided by the pre-scaler for the HB domain peripheral control clock and sampling or interface output clock. Part of the module working need to be provided by PLL clock directly.

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V2A Processor

RISC-V2C supports RISC-V instruction set EmC[1] subset. The processor is internally managed in a modular fashion and contains units such as a programmable fast interrupt controller (PFIC), extended instruction support, and so on. The bus is connected to external unit modules to enable interaction between external function modules and the core.

QingKe processor with its minimalist instruction set, a variety of operating modes, modular customization and expansion features can be flexibly applied to different scenarios MCU design, such as small area low-power embedded scenarios.

- Support machine and user privileged modes
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- Support 1-wire /2-wire serial debug interface (SDI)
- Custom extension instructions

Note: 1. The "m" extension in EmC implements the multiplication subset of the M extension.

1.4.2 On-chip Memory

Built-in 8K-byte SRAM area, which is used to store data, which is lost after power loss.

Built-in 62K-byte program flash memory area (Code FLASH), that is, the user area, is used for users' applications and constant data storage.

Built-in 3328-byte system storage area (System FLASH), that is, BOOT area, is used for system boot program storage (factory-solidified bootloader). This region can be used for the user area together with the aforementioned 62K-byte region via the WCH-LinkUtility tool. For details, refer to the relevant EVT.

Built-in 256-byte system non-volatile configuration information storage area, used for manufacturer configuration word storage, solidified before leaving the factory, users can not be modified.

Built-in 256-byte user-defined information store for user option byte storage.

1.4.3 Power Supply Scheme

(1) CH32V007

V_{DD} = 2.0 ~ 5.5V: Supplies power to the I/O pins as well as the internal regulator; When using ADC, V_{DD} should be no less than 2.4V.

(2) CH32M007K8U7 and CH32M007G8R6

CH32M007K8U7 and CH32M007G8R6 has a built-in three-phase double N pre-driver, which supports the gate driving of six N-type MOSFET power tubes in a 3-phase brushless DC motor below 48V.

V_{HV}: It supplies power to the internal high-voltage regulator, and the internal high-voltage regulator generates grid driving power at V_{CC12V} pin (this voltage error is large). For applications below 16V, V_{HV} should be shorted to V_{CC12V}, which is equivalent to turning off the internal high voltage regulator. For applications with high V_{HV}

voltage, it is suggested to divide the voltage in series resistance at the V_{HV} pin according to the load current to reduce the chip heating. When fully loaded, the voltage difference with V_{CC12} is over 8V, and if the voltage difference is small, the heating is less but the loading capacity is weak.

V_{CC12V}: It supplies power to the output terminal of the internal high-voltage regulator, the low-side driver and the internal low-voltage regulator. The internal low-voltage regulator generates a rated voltage of 5V at the V_{DD} pin, and an external MLCC capacitor with a capacity of at least 4.7uF is required, and 10uF is recommended. For the application of V_{CC12} below 7V, it is suggested to add an external high-speed low-drop Schottky diode to increase VB voltage.

V_{DD}: For the power supply terminal of the internal low-voltage regulator and the I/O pin, an external MLCC capacitor with a capacity of at least 4.7uF is required, and 10uF is recommended.

(3) CH32M007E8

CH32M007E8 has a built-in three-phase P+N pre-driver, which supports the grid driving of three pairs of N-type and P-type MOSFET power tubes in a three-phase brushless DC motor below 24V.

For CH32M007E8U6 chip:

V_{HV}: For the power supply terminal of the gate driver, a capacitor of at least 3.3uF should be externally connected, and 10uF is recommended.

V_{HREG}: For the power supply terminal of the internal voltage regulator, power must be supplied, and V_{HV} can be directly connected. It is suggested to divide the voltage between V_{HV} and V_{HREG} in series according to the load current to reduce the chip heating, and the voltage difference with V_{DD} should be over 2V at full load.

V_{DD}: For the output terminal of the internal voltage regulator and the power supply terminal of the I/O pin, an external MLCC capacitor with a capacity of at least 4.7uF is required, and 10uF is recommended.

For CH32M007E8R6 chip:

V_{HV}: For the power supply terminal of the gate driver and the power supply terminal of the internal voltage regulator, at least 3.3uF capacitor should be externally connected, and 10uF is recommended.

V_{DD}: For the output terminal of the internal voltage regulator and the power supply terminal of the I/O pin, an external MLCC capacitor with a capacity of at least 4.7uF is required, and 10uF is recommended.

1.4.4 Power Supply Monitor

The chip integrates a power-on reset (POR)/power-off reset (PDR) circuit, which is always in a working state to ensure that the system works when the power supply is not less than 2.0V; when the V_{HV} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without the need to use an external reset circuit.

In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software, to compare the magnitude of the voltage supplied by V_{DD} with the set threshold V_{PVD}. Turning on the corresponding edge interrupt of the PVD allows you to receive an interrupt notification when V_{DD} falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for $V_{POR/PDR}$ and V_{PVD} values.

1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are two modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.

1.4.6 Low-power Mode

The system supports 2 low-power modes, which can achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Standby mode (STANDBY)

A peripheral clock control mechanism is combined with the SLEEPDEEP of the core and allows the voltage regulator to operate in a lower power state. The high-frequency clock (HSI/HSE/PLL) domain is turned off, SRAM and register contents are maintained, and I/O pin states are maintained. The system can continue to run after this mode wakes up, with HSI as the default system clock.

Exit conditions: Any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 31 external I/O ports, automatic wake-up, etc.

1.4.7 Programmable Fast Interrupt Controller (PFIC)

The chip has a built-in Programmable Fast Interrupt Controller (PFIC) that supports up to 255 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. Currently the chip manages 4 core private interrupts and 25 peripheral interrupt management, with other interrupt sources reserved. the PFIC registers are all accessible in both user and machine privileged modes.

- 2 individually maskable interrupts
- Provide one non-maskable interrupt NMI
- Support Hardware Prologue/Epilogue (HPE) without instruction overhead
- Provide 2 Vector Table Free (VTF) for faster access to interrupt service routines
- Vector table support address or instruction mode
- Interrupt nesting depth can be configured up to 2 levels
- Support interrupt tail linking

1.4.8 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 10 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can detect clock cycles with pulse widths less than the internal HB. Up to 31 general-purpose I/O ports are optionally connected to the same external interrupt line.

1.4.9 General-purpose DMA Controller

The system has built-in general-purpose DMA controller, manages 7 channels, flexibly handles high-speed data transmission from memory to memory, peripheral to memory and memory to peripheral devices, and supports ring buffer mode. Each channel has special hardware DMA request logic, which supports one or more peripheral access requests to memory. Access priority, transmission length, source address and destination address of transmission can be configured.

DMA for the main peripherals include: general / advanced timer TIMx, ADC, USART, I2C, SPI.

Note: DMA and CPU access the system SRAM after arbitration by the arbitrator.

1.4.10 Clock and Boot

The system clock source HSI is on by default. After no clock is configured or reset, the RC oscillator of the internal 24MHz is used as the default CPU clock, and then the external 3~25MHz clock or PLL clock can be selected. When clock safe mode is turned on, if HSE is used as the system clock (directly or indirectly), if an external clock failure is detected, the system clock will automatically switch to the internal RC oscillator, while HSE and PLL will automatically turn off; for low-power mode with clock off, the system will also automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

In addition, in order to improve the reliability of the system, System Clock Monitor (SCM) module is added. When the enable bit is turned on, if the system clock fails, a brake signal will be generated to the advanced timer TIM1, and the system clock failure interrupt flag will be set. If the enable is interrupted in advance, the interrupt will be entered.

1.4.11 Analog-to-digital Converter (ADC) and Touch-key

The chip has a built-in 12-bit ADC that provides up to 8 external channels and 2 internal channels for sampling at sampling rates up to 3Msps, providing programmable channel sampling time for single, continuous, scan or intermittent conversion. The analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring the channel signal voltage, and when the voltage exceeds a set threshold, the system can be configured to generate a reset and protect the system.

The internal channel of ADC is ADC_IN8~ADC_IN9. The internal reference voltage V_{REF} is connected to the IN8 input channel; the OPA internal output channel is connected to the IN9 input channel for converting the output of the OPA into digital values.

Touch-key capacitance detection unit, which provides up to 8 detection channels and multiplexes the external channels of ADC module. The detection results are converted into output results by ADC module, and the touch button status is recognized by touch detection algorithm subroutine library or user software.

1.4.12 Timer and Watchdog

- Advanced-control Timer (TIM1)

The advanced-control timer is a 16-bit automatic load increment / decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc.

Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer (TIM2)

The general-purpose timer is a 16-bit auto-load add/subtract counter with a programmable 16-bit prescaler and 4 independent channels, each of which supports input capture, output comparison, PWM generation and monopulse mode output. By alternate channels 3 and 4, channels 1 and 2 also have complementary PWM output with dead-time insertion. In addition, it can work with the advanced-control timer TIM1 through the timer linking function to provide synchronization or event linking functions. In debug mode, counters can be frozen and any general-purpose timer can be used to generate PWM output.

- Streamlined Timer (TIM3)

The streamlined timer is a 16-bit auto-loading increment/decrement counter that supports four independent comparison channels with output comparison. It is used in conjunction with other functions by generating signals inside the chip, mainly for auxiliary motor applications. Can work with advanced timer TIM1 through timer link function, can generate specific frequency pulse with TIM1, provide synchronization or event link function. The counter can be frozen in debug mode.

- Independent Watchdog (IWDG)

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 128KHz; the LSI is independent of the master clock and can operate in standby mode. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

- Window Watchdog (WWDG)

Window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- SysTick Timer (SysTick)

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, and can also be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.13 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The chip provides 2 sets of USART. Support full-duplex asynchronous serial communication and half-duplex single-wire communication, also support LIN (Local Internet), compatible with IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation, but also support multiprocessor

communication. It adopts fractional baud rate generator system and supports continuous communication of DMA operation.

1.4.14 Serial Peripheral Interface (SPI)

The chip provides a serial peripheral SPI interface, which supports master or slave operation and dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit choice, reliable communication hardware CRC generation / check, support DMA operation continuous communication.

1.4.15 I2C Bus

The chip provides an I2C bus interface, which can work in multi-host mode or slave mode, and complete all I2C bus specific timing, protocol, arbitration and so on. Both standard and fast communication speeds are supported.

The I2C interface provides 7-bit or 10-bit addressing and supports double-slave address addressing in 7-bit slave mode. Built-in hardware CRC generator / verifier.

1.4.16 General-purpose Input and Output (GPIO)

The system provides 4 sets of GPIO ports (PA0~PA7, PB0~PB6, PC0~PC7, PD0~PD7) with a total of 31 GPIO pins. Most pins can be configured by software to output (push-pull or open-drain), input (with or without pull-up or pull-down), or alternate peripheral function ports.

When PA1 and PA2 are crystal pins, i.e., PA1PA2_RM = 1, PA1 and PA2 cannot be used for GPIO functions.

All GPIO pins support controllable pull-up and pull-down resistors. When PC5 is used as reset pins, the pull-up resistor is turned on and the pull-down resistor is turned off by default.

All GPIO pins are shared with digital or analog alternate peripherals. All GPIO pins have a large current drive capability. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.

The power supply of all the I/O pins in the system is provided by the V_{DD}. By changing the V_{DD} power supply, the output level of the I/O pin will be changed to adapt to the external communication interface level. Please refer to the pin description for the specific pin.

1.4.17 Op Amp/Comparator (OPA)

The chip has a set of operational amplifier (OPA) built in, which can also be used as a voltage comparator. Its input can be selected by changing the configuration, including the amplification of programmable gain operational amplifier (PGA). The P terminal supports 3-channel polling and single-resistance or double-resistance current sampling scheme. Its output can be selected by changing the configuration of two output pins. In addition, there is an internal output channel directly connected to the internal channel IN9 of ADC, which supports amplifying external analog small signals into ADC to realize small-signal ADC conversion. OPA supports high-speed mode, and the slew rate can be improved by setting high-speed mode.

1.4.18 Voltage Comparator (CMP)

- Universal voltage comparator (CMP1)

Rail-to-rail universal voltage comparator supports optional hysteresis characteristics, 3-channel timed polling input at P-terminal, and 3-channel comparator polling detection for non-inductive positioning. Its voltage comparison result OUT0 is output by GPIO, while other voltage comparison results (OUT1~OUT4) are directly sent to peripherals from inside, releasing the control of I/O for other purposes. Among them, OUT1 and OUT2 directly access the CH4 input channels of TIM1 and TIM2 inside the chip to realize the trigger; OUT3 is connected to the BKIN channel of TIM1 internally, as the brake source of TIM1, which can be applied to the overcurrent protection of double resistance scheme; OUT4 will reset the system when the internal output is high.

- Streamlined comparator (CMP2)

The P-terminal of the dedicated simplified voltage comparator and the output channel of OPA are directly cascaded in the chip, which can be used for overcurrent protection of single resistance scheme. Its N terminal is directly connected with the reference voltage VCMP2_REF of CMP2 inside the chip, and VCMP2_REF can be selected with multiple values; Its voltage comparison result, OUT0, is directly connected to the BKIN channel of TIM1 inside the chip as the brake source of TIM1. OUT1 will reset the system when the internal output is high.

1.4.19 Gate Driver

CH32M007 is a special MCU for motor, which integrates three independent half-bridge drivers. Each half-bridge includes high-side and low-side level shift circuits and high-side and low-side output drive circuits. Among them, each half-bridge of CH32M007K8U7 and CH32M007G8R6 chip also includes bootstrap diode, which supports the gate drive of six N-type MOSFET power tubes. Only one capacitor is needed to store the bootstrap power supply externally, and the gate drive voltage depends on VCC12V. CH32M007E8 chip supports three pairs of gate drivers of P+N MOSFET power tubes.

The three independent half-bridges integrated by CH32M007 can form a three-phase half-bridge for grid drive of three-phase brushless DC motor. Among them, CH32M007K8U7 and CH32M007G8R6 chip is mainly used to drive the gates of six N-channel MOSFET power tubes in three-phase motors below 48V; The CH32M007E8 chip is mainly used to drive the gates of three pairs of N-channel and P-channel MOSFET power tubes in three-phase motors below 24V.

The three-phase half-bridge of CH32M007 is controlled by six PWM signals generated by the advanced timer TIM1, and the dead time of PWM is adjustable, which supports direct braking control of overcurrent protection. In use, TIM1_RM = 0100 should be set to map the pins of TIM1, and the low-side gate drivers LO1/LO2/LO3 are controlled by PA0, PA2 and PD0 of CH32V007 respectively, and the high-side gate drivers HO1/HO2/HO3 are controlled by PA3, PB0 and PB1 of CH32V007 respectively.

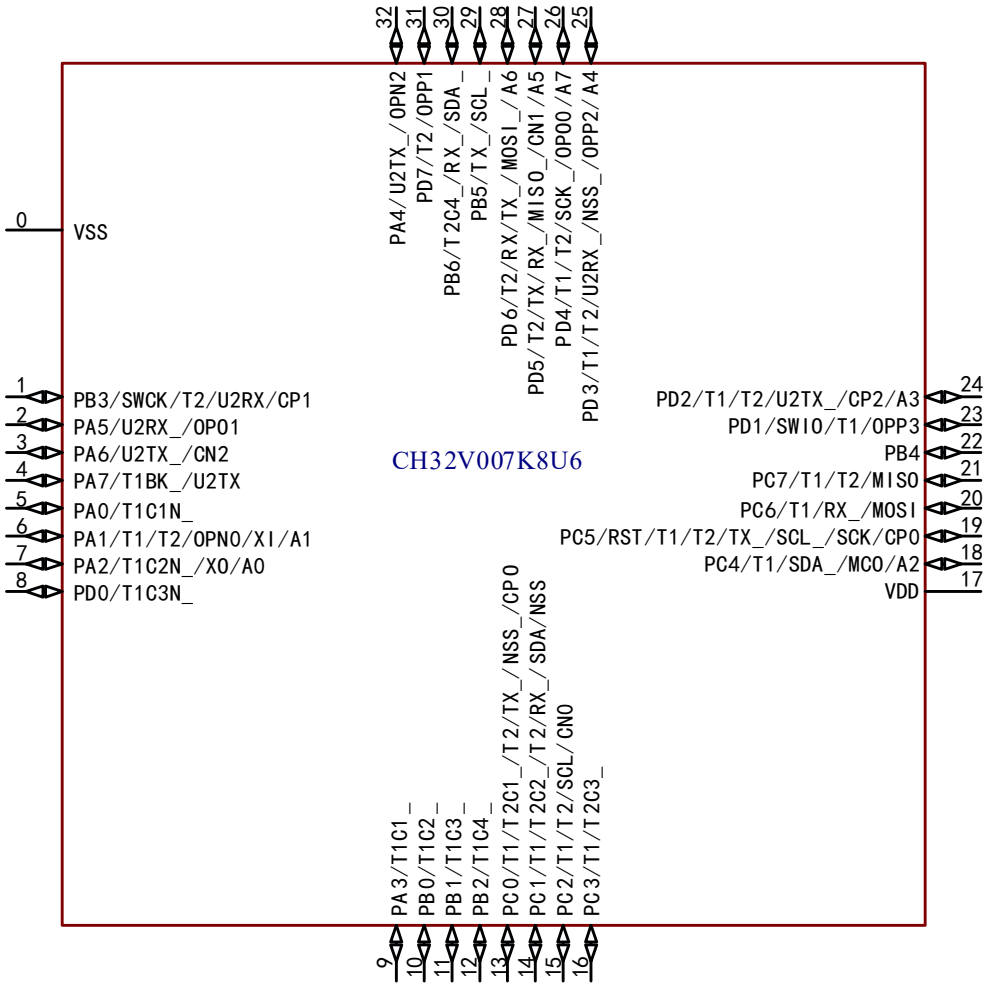
1.4.20 1-wire Serial Debug Interface (SDI)

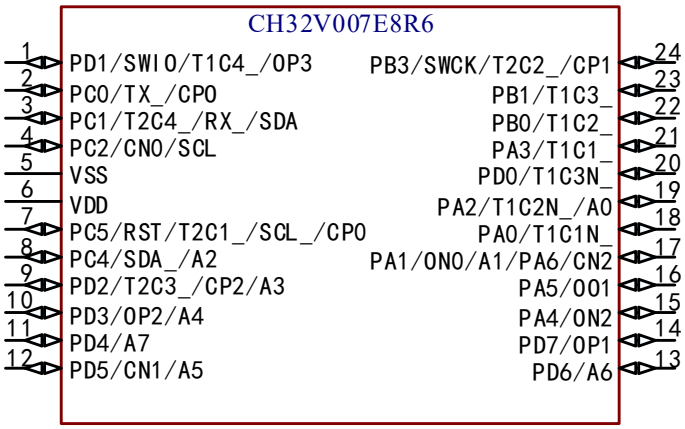
The core comes with a 1-wire SDI Serial Debug Interface and a 2-wire SDI Serial Debug Interface. The system supports both 1- and 2-wire debugging modes; among them, 1-wire debugging is the default debugging mode, which corresponds to the SWIO pin (Single Wire Input Output), while 2-wire debugging corresponds to the SWDIO and SWCLK pins, which can be used to increase the speed of downloading. The default debugging interface pins are turned on after system power-on or reset, and the SDI can be turned off as needed after the main program is run, and the HSI clock must be turned on when using the 1-wire emulation debugging interface.

Chapter 2 Pinouts and Pin Definition

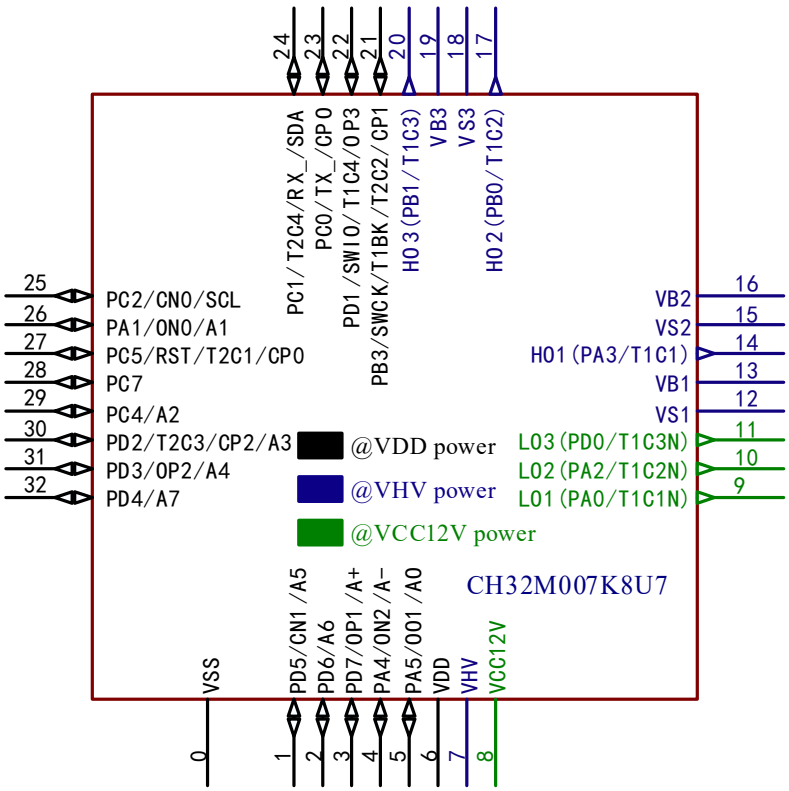
2.1 Pinouts

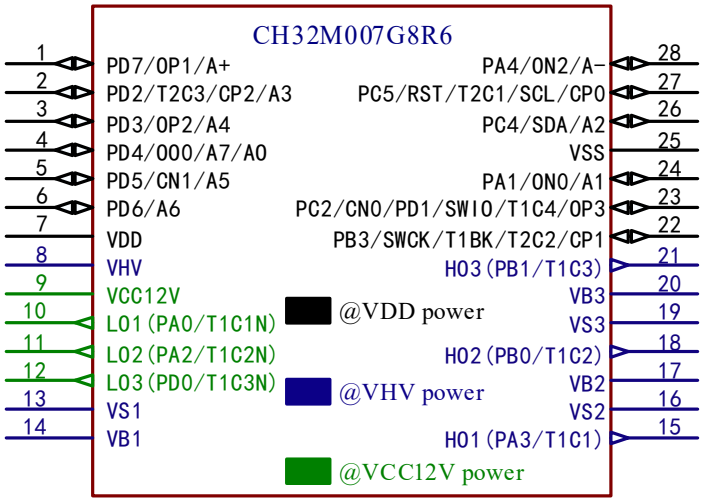
2.1.1 CH32V007 Pinouts

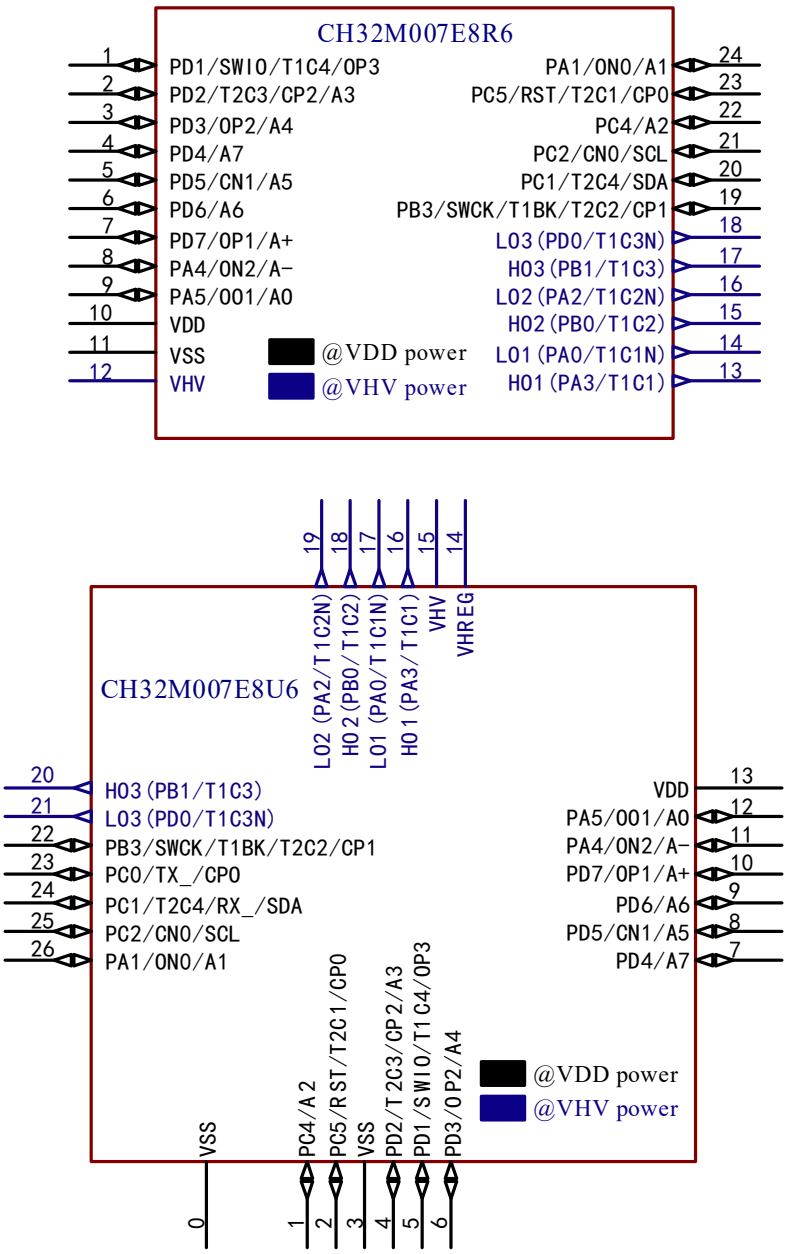




2.1.2 CH32M007 Pinouts







Note: The multiplexed functions in the pin diagram are abbreviated.

Example: A: ADC_ (A1: ADC_IN1, AET: ADC_RETR, AET2: ADC_IETR)

T1: TIM1_ (T1C1: TIM1_CH1、T1C1N: TIM1_CH1N, T1BK: TIM1_BKIN)

T2: TIM2_ (T2C1: TIM2_CH1_ETR, T2C2: TIM2_CH2)

RX: USART1_RX

TX: USART1_TX

U2: USART2_ (U2RX:USART2_RX, U2TX:USART2_TX)

O: OPA_ (OPP3 or OP3: OPA_P3, OPNO or ON0: OPA_NO, OPO1 or OO1: OPA_OUT1)

C: CMP1_ (CP2:CMP1_P2, CN2: CMP1_N2, CPO: CMP1_OUT0)

SDA: I2C_SDA

SCL: I2C_SCL

SCK: SPI_SCK
NSS: SPI_NSS
MISO: SPI_MISO
MOSI: SPI_MOSI
SWIO: SWIO/SWDIO
SWCK: SWCLK

2.2 Pin Definitions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-1 CH32V007 Pin definitions

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
V007E8R6	V007K8U6					
5	0	V_{SS}	P	V_{SS}		
24	1	PB3	I/O/A	PB3	USART2_RX/SWCLK/ CMP1_P1	TIM1_BKIN_4/TIM1_BKIN_5/ TIM2_CH2_2/USART1_TX_5/ USART1_RX_4/USART2_RTS_1/ USART2_RTS_6/I2C_SCL_4/ SPI_MISO_2
16	2	PA5	I/O/A	PA5	USART2_RTS/OPA_OUT1	USART1_RTS_4/USART1_RTS_5/ USART2_RX_1/USART2_RX_6
17	3	PA6(3)	I/O/A	PA6	CMP1_N2	USART2_TX_6
-	4	PA7	I/O	PA7	USART2_TX	TIM1_BKIN_6/USART2_CTS_1/ USART2_CTS_6
18	5	PA0	I/O	PA0		TIM1_CH1_9/TIM1_CH1N_4/ TIM1_CH1N_5/TIM1_CH1N_6/ TIM2_CH1_ETR_5/USART1_TX_8/ USART1_TX_9/USART2_CTS_2/ USART2_CTS_3
17	6	PA1(3)	I/O/A	PA1	ADC_IN1/TIM1_CH2/ OPA_N0	XI/TIM1_CH2_1/TIM1_CH2_9/ TIM2_CH2_5/TIM2_CH2_6/ USART1_RX_8/USART2_RTS_2/ USART2_RTS_3/USART2_RTS_4/

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
V007E8R6	V007K8U6					
						USART2_RTS_5/SPI_SCK_5
19	7	PA2	I/O/A	PA2	ADC_IN0/TIM1_CH2N/ OPA_P0	XO/TIM1_CH3_9/TIM1_CH2N_1/ TIM1_CH2N_4/TIM1_CH2N_5/ TIM1_CH2N_6/TIM2_CH3_5/ TIM2_CH3_6/TIM2_CH3_7/ USART2_TX_2/SPI_MOSI_5/ ADC_IETR_1
20	8	PD0	I/O/A	PD0	TIM1_CH1N/OPA_N1	TIM1_CH1N_1/TIM1_CH3N_4/ TIM1_CH3N_5/TIM1_CH3N_6/ USART1_TX_2/I2C_SDA_1
21	9	PA3	I/O	PA3		TIM1_CH1_4/TIM1_CH1_5/ TIM1_CH1_6/TIM1_CH4_9/ TIM1_CH1N_8/TIM2_CH4_5/ TIM2_CH4_6/TIM2_CH4_7/ USART2_RX_2
22	10	PB0	I/O	PB0		TIM1_CH2_4/TIM1_CH2_5/ TIM1_CH2_6/TIM1_CH2N_8/ USART2_TX_4/SPI_NSS_3/
23	11	PB1	I/O	PB1		TIM1_CH3_4/TIM1_CH3_6/ TIM1_CH3N_8/TIM2_CH1_ETR_6/ USART2_RX_4/SPI_SCK_3
-	12	PB2	I/O	PB2		TIM1_CH4_6/TIM1_BKIN_7/ TIM1_BKIN_8/TIM1_BKIN_9/ SPI_MISO_3
2	13	PC0	I/O/A	PC0	TIM2_CH3/CMP1_OUT0	TIM1_CH3_2/TIM1_CH1N_7/

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
V007E8R6	V007K8U6					
						TIM1_CH1N_9/TIM2_CH1_ETR_4/ TIM2_CH3_1/USART1_TX_3/ SPI_NSS_1/SPI_MOSI_3
3	14	PC1	I/O	PC1	I2C_SDA/SPI_NSS	TIM1_CH2N_7/TIM1_CH2N_9/ TIM1_BKIN_2/TIM1_BKIN_3/ TIM2_CH1_ETR_1/ TIM2_CH1_ETR_3/TIM2_CH2_4/ TIM2_CH4_2/USART1_RX_3/ SPI_NSS_5
4	15	PC2	I/O/A	PC2	TIM1_BKIN/USART1_RTS/ I2C_SCL/CMP1_N0	TIM1_CH3N_7/TIM1_CH3N_9/ USART1_RTS_2/TIM1_BKIN_1/ TIM1_ETR_3/ADC_RETR_1
-	16	PC3	I/O	PC3	TIM1_CH3	TIM1_CH3_1/TIM1_CH3_5/ TIM1_CH1N_2/TIM1_CH1N_3/ TIM2_CH3_4/USART1_CTS_2
6	17	V_{DD}	P			
8	18	PC4	I/O/A	PC4	ADC_IN2/TIM1_CH4/MCO	TIM1_CH1_3/TIM1_CH1_7 TIM1_CH1_8/TIM1_CH4_1 TIM1_CH2N_2/USART1_RX_9 USART2_TX_5/I2C_SDA_2 SPI_NSS_2/SPI_NSS_6
7	19	PC5	I/O/A	PC5	TIM1_ETR/SPI_SCK/ CMP1_P0/RST	TIM1_CH2_7/TIM1_CH2_8/ TIM1_CH3_3/TIM1_ETR_2/ TIM2_CH1_ETR_2/USART1_TX_6/ I2C_SCL_2/SPI_SCK_1

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
V007E8R6	V007K8U6					
-	20	PC6	I/O	PC6	SPI_MOSI	TIM1_CH1_2/TIM1_CH3_7/ TIM1_CH3_8/TIM1_CH3N_3/ USART1_RX_6/USART1_CTS_1/ USART1_CTS_3/SPI_MOSI_1
-	21	PC7	I/O	PC7	SPI_MISO	TIM1_CH2_2/TIM1_CH2_3/ TIM1_CH4_7/TIM1_CH4_8/ TIM2_CH2_3/USART1_CTS_6/ USART1_CTS_7/USART1_RTS_1/ USART1_RTS_3/SPI_MISO_1/ SPI_MISO_6
-	22	PB4	I/O	PB4		TIM1_ETR_7/TIM1_ETR_8/ TIM1_ETR_9/USART1_RTS_6/ USART1_RTS_7/SPI_MOSI_6
1	23	PD1	I/O/A	PD1	TIM1_CH3N/SWIO/ SWDIO/OPA_P3/ ADC_IETR	TIM1_CH4_4/TIM1_CH4_5/ TIM1_CH3N_1/TIM1_CH3N_2/ USART1_TX_4/USART1_RX_2/ USART1_RX_5/USART2_RX_5/ I2C_SCL_1/I2C_SDA_4
9	24	PD2	I/O/A	PD2	ADC_IN3/TIM1_CH1/ CMP1_P2	TIM1_CH1_1/TIM1_CH2N_3/ TIM2_CH3_2/USART1_CTS_8/ USART2_TX_3/SPI_SCK_2
10	25	PD3	I/O/A	PD3	ADC_IN4/TIM2_CH2/ USART1_CTS/OPA_P2/ ADC_RETR	TIM1_CH4_2/TIM2_CH1_ETR_7/ TIM2_CH2_1/USART1_RTS_8/ USART2_RX_3/SPI_NSS_4/ SPI_MOSI_2

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
V007E8R6	V007K8U6					
11	26	PD4	I/O/A	PD4	ADC_IN7/TIM2_CH1_ETR/ OPA_OUT0	TIM1_CH4_3/TIM1_ETR_1/ TIM1_ETR_4/TIM1_ETR_5/ TIM1_ETR_6/TIM2_CH2_7/ USART1_RTS_9/SPI_SCK_4
12	27	PD5	I/O/A	PD5	ADC_IN5/USART1_TX/ CMP1_N1	TIM2_CH4_3/USART1_RX_1/ USART1_CTS_9/SPI_MISO_4
13	28	PD6	I/O/A	PD6	ADC_IN6/USART1_RX	TIM2_CH3_3/USART1_TX_1/ SPI_MOSI_4
-	29	PB5	I/O	PB5		USART1_TX_7/I2C_SCL_3/ SPI_SCK_6/SPI_MISO_5
-	30	PB6	I/O	PB6		TIM2_CH4_4/USART1_RX_7/ USART2_CTS_4/I2C_SDA_3
14	31	PD7	I/O/A	PD7	TIM2_CH4/OPA_P1	TIM2_CH4_1/USART1_CTS_4/ USART1_CTS_5
15	32	PA4	I/O/A	PA4	USART2_CTS/OPA_N2	USART2_TX_1/USART2_CTS_5

Table 2-2 CH32M007 Pin definitions

Pin No.				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
M007E8R6	M007E8U6	M007K8U7	M007G8R6					
-	0	0	-	V_{SS}	P	V_{SS}		
7	10	3	1	PD7(4)(5)	I/O/A	PD7(4)(5)	TIM2_CH4/OPA_P1	TIM2_CH4_1/USART1_CTS_4/ USART1_CTS_5
2	4	30	2	PD2	I/O/A	PD2	ADC_IN3/TIM1_CH1/	TIM1_CH1_1/TIM1_CH2N_3/

Pin No.				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
M007E8R6	M007E8U6	M007K8U7	M007G8R6					
							CMP1_P2	TIM2_CH3_2/USART1_CTS_8/ USART2_TX_3/SPI_SCK_2
3	6	31	3	PD3	I/O/A	PD3	ADC_IN4/TIM2_CH2/ USART1_CTS/OPA_P2/ ADC_RETR	TIM1_CH4_2/TIM2_CH2_1/ TIM2_CH1_ETR_7/ USART1_RTS_8/USART2_RX_3/ SPI_NSS_4/SPI_MOSI_2
4	7	32	4	PD4(4)	I/O/A	PD4(4)	ADC_IN7/ TIM2_CH1_ETR/ OPA_OUT0	TIM1_CH4_3/TIM1_ETR_1/ TIM1_ETR_4/TIM1_ETR_5/ TIM1_ETR_6/TIM2_CH2_7/ USART1_RTS_9/SPI_SCK_4
5	8	1	5	PD5	I/O/A	PD5	ADC_IN5/USART1_TX/ CMP1_N1	TIM2_CH4_3/USART1_RX_1/ USART1_CTS_9/SPI_MISO_4
6	9	2	6	PD6	I/O/A	PD6	ADC_IN6/USART1_RX	TIM2_CH3_3/USART1_TX_1/ SPI_MOSI_4
10	13	6	7	V_{DD}	P	V_{DD}		
-	14	-	-	V_{HREG}	P	V_{HREG}		
12	15	7	8	V_{HV}	P	V_{HV}		
-	-	8	9	V_{CC12V}	P	V_{CC12V}		
14	17	9	10	LO1 (PA0)	O	LO1		
16	19	10	11	LO2 (PA2)	O	LO2		
18	21	11	12	LO3 (PD0)	O	LO3		
-	-	12	13	V_{S1}	P	V_{S1}		

Pin No.				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
M007E8R6	M007E8U6	M007K8U7	M007G8R6					
-	-	13	14	V_{B1}	P	V_{B1}		
13	16	14	15	HO1 (PA3)	O	HO1		
-	-	15	16	V_{S2}	P	V_{S2}		
-	-	16	17	V_{B2}	P	V_{B2}		
15	18	17	18	HO2 (PB0)	O	HO2		
-	-	18	19	V_{S3}	P	V_{S3}		
-	-	19	20	V_{B3}	P	V_{B3}		
17	20	20	21	HO3 (PB1)	O	HO3		
19	22	21	22	PB3	I/O/A	PB3	USART2_RX/SWCLK/ CMP1_P1	TIM1_BKIN_4/TIM1_BKIN_5/ TIM2_CH2_2/USART1_TX_5/ USART1_RX_4/USART2_RTS_1/ USART2_RTS_6/I2C_SCL_4/ SPI_MISO_2
21	25	25	23	PC2(6)	I/O/A	PC2(6)	TIM1_BKIN/ USART1_RTS/ I2C_SCL/CMP1_N0	TIM1_CH3N_7/TIM1_CH3N_9/ USART1_RTS_2/TIM1_BKIN_1/ TIM1_ETR_3/ADC_RETR_1
1	5	22		PD1(6)	I/O/A	PD1(6)	TIM1_CH3N/SWIO/ SWDIO/OPA_P3/ ADC_IETR	TIM1_CH4_4/TIM1_CH4_5/ TIM1_CH3N_1/TIM1_CH3N_2/ USART1_TX_4/USART1_RX_2/ USART1_RX_5/USART2_RX_5/ I2C_SCL_1/I2C_SDA_4
24	26	26	24	PA1	I/O/A	PA1	ADC_IN1/TIM1_CH2/	XI/TIM1_CH2_1/TIM1_CH2_9/

Pin No.				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
M007E8R6	M007E8U6	M007K8U7	M007G8R6					
							OPA_N0	TIM2_CH2_5/TIM2_CH2_6/ USART1_RX_8/USART2_RTS_2/ USART2_RTS_3/USART2_RTS_ 4/ USART2_RTS_5/SPI_SCK_5
11	3		25	V_{SS}	P	V_{SS}		
22	1	29	26	PC4	I/O/A	PC4	MCO/ADC_IN2/TIM1_C H4	TIM1_CH1_3/TIM1_CH1_7/ TIM1_CH1_8/TIM1_CH4_1/ TIM1_CH2N_2/USART1_RX_9/ USART2_TX_5/I2C_SDA_2/ SPI_NSS_2/SPI_NSS_6/
23	2	27	27	PC5	I/O/A	PC5	TIM1_ETR/SPI_SCK/ CMP1_P0/RST	TIM1_CH2_7/TIM1_CH2_8/ TIM1_CH3_3/TIM1_ETR_2/ TIM2_CH1_ETR_2/USART1_TX _6/ I2C_SCL_2/SPI_SCK_1
-	-	28	-	PC7	I/O	PC7	SPI_MISO	TIM1_CH2_2/TIM1_CH2_3/ TIM1_CH4_7/TIM1_CH4_8/ TIM2_CH2_3/USART1_CTS_6/ USART1_CTS_7/USART1_RTS_ 1/ USART1_RTS_3/SPI_MISO_1/ SPI_MISO_6
8	11	4	28	PA4(4)(5)	I/O/A	PA4(4)(5)	USART2_CTS/OPA_N2	USART2_TX_1/USART2_CTS_5
9	12	5	-	PA5(5)	I/O/A	PA5(5)	USART2_RTS/OPA_OU	USART1_RTS_4/USART1_RTS_

Pin No.				Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
M007E8R6	M007E8U6	M007K8U7	M007G8R6					
							T1	5/ USART2_RX_1/USART2_RX_6
-	23	23	-	PC0	I/O/A	PC0	TIM2_CH3/CMP1_OUT 0	TIM1_CH3_2/TIM1_CH1N_7/ TIM1_CH1N_9/ TIM2_CH1_ETR_4/ TIM2_CH3_1/USART1_TX_3/ SPI_NSS_1/SPI_MOSI_3
20	24	24	-	PC1	I/O	PC1	I2C_SDA/SPI_NSS	TIM1_CH2N_7/TIM1_CH2N_9/ TIM1_BKIN_2/TIM1_BKIN_3/ TIM2_CH1_ETR_1/ TIM2_CH1_ETR_3/TIM2_CH2_4 / TIM2_CH4_2/USART1_RX_3/ SPI_NSS_5

Note 1: Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output.

A = Analog signal input or output; P = Power supply.

Note 2: The underlined value of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example: TIM1_BKIN_4 indicates that the corresponding bit configuration of the AFIO register is 100b.

Note 4: For the CH32M007K8U7 and CH32M007G8R6 chip, pin PD7 is usually selected as the positive input to the OPA, pin PA4 is selected as the negative input to the OPA, and pin PD4 is selected as the output of the OPA.

Note 5: For CH32M007E8 chip, usually select PD7 pin as the positive input of the OPA, PA4 pin as the negative input of the OPA, and PA5 pin as the output of the OPA.

Note 6: For the CH32M007G8R6 chip, the PC2 and PD1 pins are shorted inside the chip to prevent both IOs from being configured as output functions.

Table 2-3 CH32M007K8U7 and CH32M007G8R6 proprietary pin description

Pin name	Pin description

V_{CC12V}	The power input of the internal low-side driver and the output of the high-voltage regulator need to be externally connected with an MLCC capacitor with a capacity of at least 4.7uF, and 10uF is recommended.
V_{HV}	Power input of internal high voltage regulator.
V_{DD}	The output of the internal low-voltage regulator needs an external MLCC capacitor with a capacity of at least 4.7uF, and 10uF is recommended.
LO1,LO2,LO3	The output of the internal low-side gate driver is used to drive the gate of N-type MOSFET.
HO1,HO2,HO3	The output of the internal high-side gate driver is used to drive the gate of N-type MOSFET.
V_{S1},V_{S2},V_{S3}	Floating ground of internal high-side gate driver.
V_{B1},V_{B2},V_{B3}	For the bootstrap power supply of the internal high-side gate driver, it is suggested to externally connect the capacitance of 1uF～4.7uF to their respective floating ground VS.

Table 2-4 CH32M007E8U6 proprietary pin description

Pin name	Pin description
V_{HV}	The main power input and the power input of the gate driver need to be externally connected with a capacitor of at least 3.3uF, and 10uF is recommended.
V_{HREG}	The power input of the internal voltage regulator must supply power, generally through a resistor or directly connected to V_{HV}.
V_{DD}	The output of the internal voltage regulator needs an external MLCC capacitor with a capacity of at least 4.7uF, and 10uF is recommended.
LO1,LO2,LO3	The output of the internal low-side gate driver is used to drive the gate of N-type MOSFET.
HO1,HO2,HO3	The output of the internal high-side gate driver is used to drive the gate of the P-type MOSFET.

Table 2-5 CH32M007E8R6 proprietary pin description

Pin name	Pin description
V_{HV}	The main power input and the power input of the gate driver need to be externally connected with a capacitor of at least 3.3uF, and 10uF is recommended.
V_{DD}	The output of the internal voltage regulator needs an external MLCC capacitor with a capacity of at least 4.7uF, and 10uF is recommended.
LO1,LO2,LO3	The output of the internal low-side gate driver is used to drive the gate of N-type MOSFET.
HO1,HO2,HO3	The output of the internal high-side gate driver is used to drive the gate of the P-type MOSFET.

2.3 Pin Alternate Functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-6 Pin alternate and remapping functions

Alternate / Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI	OPA	CMP
PA0		TIM1_CH1_9 TIM1_CH1N_4 TIM1_CH1N_5 TIM1_CH1N_6	TIM2_CH1_ETR_5	USART1_TX_8 USART1_TX_9 USART2_CTS_2 USART2_CTS_3					
PA1	ADC_IN1	TIM1_CH2 TIM1_CH2_1 TIM1_CH2_9	TIM2_CH2_5 TIM2_CH2_6	USART1_RX_8 USART2_RTS_2 USART2_RTS_3 USART2_RTS_4 USART2_RTS_5	XI		SPI_SCK_5	OPA_N0	
PA2	ADC_IN0 ADC_IETR_1	TIM1_CH3_9 TIM1_CH2N TIM1_CH2N_1 TIM1_CH2N_4 TIM1_CH2N_5 TIM1_CH2N_6	TIM2_CH3_5 TIM2_CH3_6 TIM2_CH3_7	USART2_TX_2	XO		SPI_MOSI_5	OPA_P0	
PA3		TIM1_CH1_4 TIM1_CH1_5 TIM1_CH1_6 TIM1_CH4_9 TIM1_CH1N_8	TIM2_CH4_5 TIM2_CH4_6 TIM2_CH4_7	USART2_RX_2					
PA4				USART2_TX_1 USART2_CTS USART2_CTS_5				OPA_N2	
PA5				USART1_RTS_4 USART1_RTS_5 USART2_RX_1 USART2_RX_6 USART2_RTS				OPA_OUT1	
PA6				USART2_TX_6					CMP1_N2
PA7		TIM1_BKIN_6		USART2_TX USART2_CTS_1 USART2_CTS_6					
PB0		TIM1_CH2_4 TIM1_CH2_5 TIM1_CH2_6		USART2_TX_4			SPI_NSS_3		

Alternate Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI	OPA	CMP
		TIM1_CH2N_8							
PB1		TIM1_CH3_4 TIM1_CH3_6 TIM1_CH3N_8	TIM2_CH1_ETR_6	USART2_RX_4			SPI_SCK_3		
PB2		TIM1_CH4_6 TIM1_BKIN_7 TIM1_BKIN_8 TIM1_BKIN_9					SPI_MISO_3		
PB3		TIM1_BKIN_4 TIM1_BKIN_5	TIM2_CH2_2	USART1_TX_5 USART1_RX_4 USART2_RX USART2_RTS_1 USART2_RTS_6	SWCLK	I2C_SCL_4	SPI_MISO_2		CMP1_P1
PB4		TIM1_ETR_7 TIM1_ETR_8 TIM1_ETR_9		USART1_RTS_6 USART1_RTS_7			SPI_MOSI_6		
PB5				USART1_TX_7		I2C_SCL_3	SPI_SCK_6 SPI_MISO_5		
PB6			TIM2_CH4_4	USART1_RX_7 USART2_CTS_4		I2C_SDA_3			
PC0		TIM1_CH3_2 TIM1_CH1N_7 TIM1_CH1N_9	TIM2_CH1_ETR_4 TIM2_CH3 TIM2_CH3_1	USART1_TX_3			SPI_NSS_1 SPI_MOSI_3		CMP1_OUT0
PC1		TIM1_CH2N_7 TIM1_CH2N_9 TIM1_BKIN_2 TIM1_BKIN_3	TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 TIM2_CH2_4 TIM2_CH4_2	USART1_RX_3		I2C_SDA	SPI_NSS SPI_NSS_5		
PC2	ADC_RETR_1	TIM1_CH3N_7 TIM1_CH3N_9 TIM1_BKIN TIM1_BKIN_1 TIM1_ETR_3		USART1_RTS USART1_RTS_2		I2C_SCL			CMP1_N0
PC3		TIM1_CH3 TIM1_CH3_1 TIM1_CH3_5 TIM1_CH1N_2 TIM1_CH1N_3	TIM2_CH3_4	USART1_CTS_2					
PC4	ADC_IN2	TIM1_CH1_3 TIM1_CH1_7 TIM1_CH1_8 TIM1_CH4 TIM1_CH4_1 TIM1_CH2N_2		USART1_RX_9 USART2_TX_5	MCO	I2C_SDA_2	SPI_NSS_2 SPI_NSS_6		
PC5		TIM1_CH2_7	TIM2_CH1_ETR_	USART1_TX_6	RST	I2C_SCL_2	SPI_SCK		CMP1_P0

Alternate Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI	OPA	CMP
		TIM1_CH2_8 TIM1_CH3_3 TIM1_ETR TIM1_ETR_2	2				SPI_SCK_1		
PC6		TIM1_CH1_2 TIM1_CH3_7 TIM1_CH3_8 TIM1_CH3N_3		USART1_RX_6 USART1_CTS_1 USART1_CTS_3			SPI_MOSI SPI_MOSI_1		
PC7		TIM1_CH2_2 TIM1_CH2_3 TIM1_CH4_7 TIM1_CH4_8	TIM2_CH2_3	USART1_CTS_6 USART1_CTS_7 USART1_RTS_1 USART1_RTS_3			SPI_MISO SPI_MISO_1 SPI_MISO_6		
PD0		TIM1_CH1N TIM1_CH1N_1 TIM1_CH3N_4 TIM1_CH3N_5 TIM1_CH3N_6		USART1_TX_2		I2C_SDA_1		OPA_N1	
PD1	ADC_IETR	TIM1_CH4_4 TIM1_CH4_5 TIM1_CH3N TIM1_CH3N_1 TIM1_CH3N_2		USART1_TX_4 USART1_RX_2 USART1_RX_5 USART2_RX_5	SWIO SWDIO	I2C_SCL_1 I2C_SDA_4		OPA_P3	
PD2	ADC_IN3	TIM1_CH1 TIM1_CH1_1 TIM1_CH2N_3	TIM2_CH3_2	USART1_CTS_8 USART2_TX_3			SPI_SCK_2		CMP1_P2
PD3	ADC_IN4 ADC_RETR	TIM1_CH4_2	TIM2_CH1_ETR_7 TIM2_CH2 TIM2_CH2_1	USART1_CTS USART1_RTS_8 USART2_RX_3			SPI_NSS_4 SPI_MOSI_2	OPA_P2	
PD4	ADC_IN7	TIM1_CH4_3 TIM1_ETR_1 TIM1_ETR_4 TIM1_ETR_5 TIM1_ETR_6	TIM2_CH1_ETR TIM2_CH2_7	USART1_RTS_9			SPI_SCK_4	OPA_OUT0	
PD5	ADC_IN5		TIM2_CH4_3	USART1_TX USART1_RX_1 USART1_CTS_9			SPI_MISO_4		CMP1_N1
PD6	ADC_IN6		TIM2_CH3_3	USART1_TX_1 USART1_RX			SPI_MOSI_4		
PD7			TIM2_CH4 TIM2_CH4_1	USART1_CTS_4 USART1_CTS_5				OPA_P1	

Chapter 3 Electrical Characteristics

3.1 Test Condition

Unless otherwise specified and marked, all voltages are based on V_{SS}.

All minimum and maximum values will be guaranteed under the worst environmental temperature, power supply voltage and clock frequency conditions.

The typical value of CH32V007 is based on the ambient temperature of 25℃ and V_{DD} = 3.3V or 5V.

The typical value of CH32M007K8U7 and CH32M007G8R6 is based on the ambient temperature of 25℃, power supply V_{HV} = 24V, generate V_{CC12V} = 12V and V_{DD} = 5V.

The typical value of CH32M007E8U6 is based on the ambient temperature of 25℃, power supply V_{HV} = 15V and V_{HREG} = 7V, generate V_{DD} = 5V.

The typical value of CH32M007E8R6 is based on the ambient temperature of 25℃, power supply V_{HV} = 15V, generate V_{DD} = 5V.

The data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested in the production line. On the basis of comprehensive evaluation, the minimum and maximum values are obtained by statistics after sample testing. Unless otherwise specified as measured values, the characteristic parameters shall be guaranteed by comprehensive evaluation or design.

Power supply scheme (Resistors are optional in the figure, which are used to share the voltage drop and reduce the chip heating):

Figure 3-1-1 CH32V007 typical circuit for conventional power supply

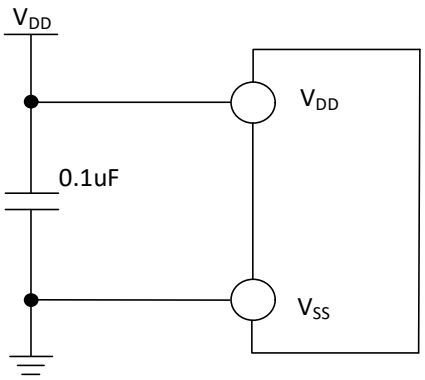


Figure 3-1-2 CH32M007K8U7 and CH32M007G8R6 typical circuit for conventional power supply

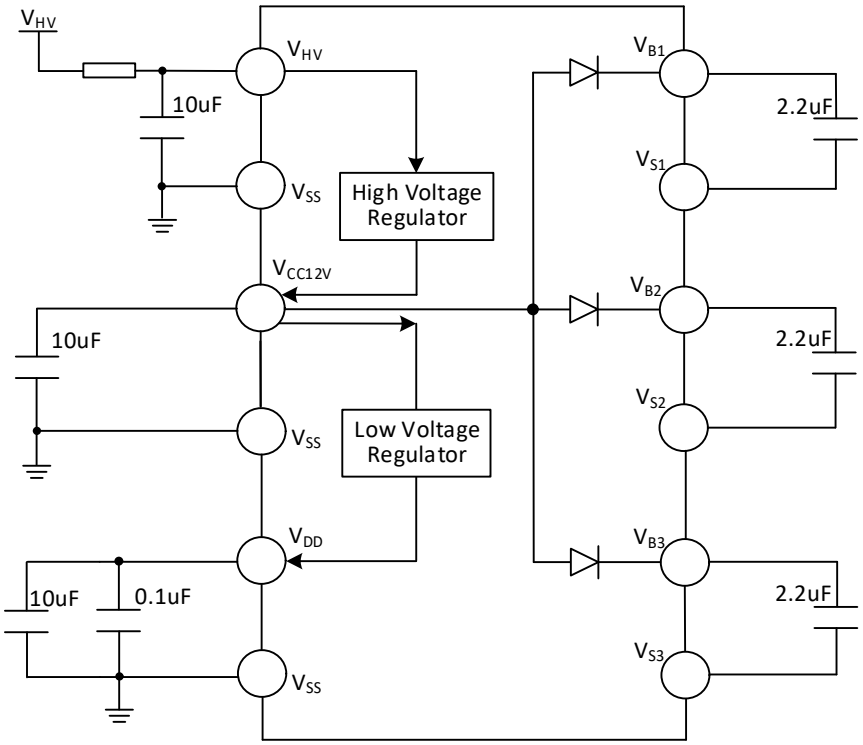


Figure 3-1-3 CH32M007E8U6 typical circuit for conventional power supply

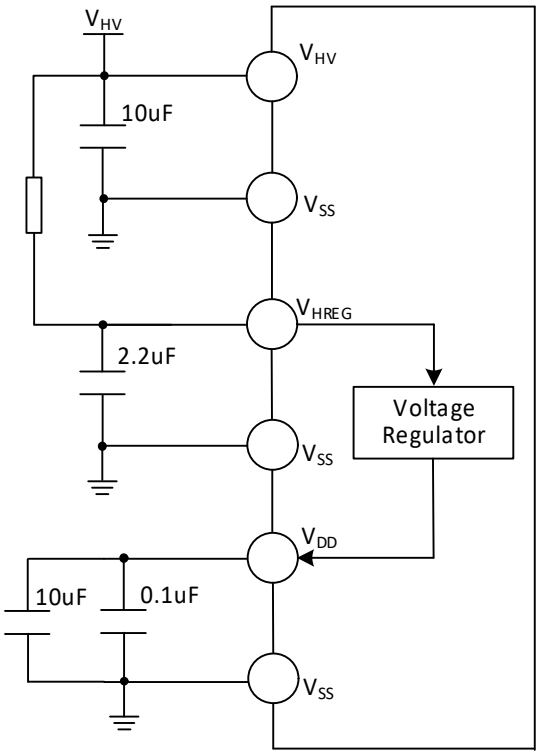
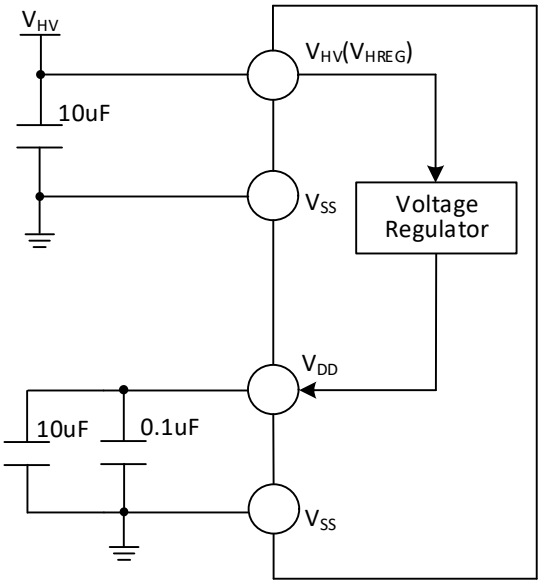


Figure 3-1-4 CH32M007E8R6 typical circuit for conventional power supply



3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description		Min.	Max.	Unit
T_A	Ambient temperature during operation	Exclude CH32M007K8U7	-40	85	℃
		CH32M007K8U7	-40	105	℃
T_S	Ambient temperature during storage		-40	125	℃
V_{DD}	External main supply voltage (V_{DD})	CH32V007	-0.3	5.5	V
	Output voltage of internal low-voltage regulator	CH32M007K8U7 CH32M007G8R6	-0.3	5.5	V
	Output voltage of internal voltage regulator	CH32M007E8	-0.3	5.5	V
V_{HV}	Input power supply voltage of internal high voltage regulator	CH32M007K8U7 CH32M007G8R6	-0.4	56	V
	Power supply voltage of high voltage power supply and gate driver	CH32M007E8	-0.4	28	V
V_{CC12V}	Power supply voltage of low-side driver and	CH32M007K8U7	-0.4	18	V

	low-voltage regulator	CH32M007G8R6			
V_{HREG}	Input power supply voltage of internal voltage regulator	CH32M007E8U6	-0.4	28	V
V_{IN}	Input voltage on the I/O pin		V_{SS}-0.3	V_{DD}+0.3	V
V_B	High-side bootstrap supply voltage	CH32M007K8U7 CH32M007G8R6	-0.4	63	V
V_{BPEAK}	High-side bootstrap 1% duty cycle pulse voltage		-0.4	67	V
V_S	High-side floating ground voltage		-1.5	52	V
V_{SPEAK}	High-side suspended 1% duty cycle pulse voltage		-4.0	56	V
V_{B_S}	Voltage difference between high-side bootstrap power supply and floating ground		-0.4	17	V
V_{HO}	Output voltage of high-side driver	CH32M007K8U7 CH32M007G8R6	V_S-0.4	V_B+0.4	V
		CH32M007E8	-0.4	V_{HV}+0.4	V
V_{LO}	Output voltage of low-side driver	CH32M007K8U7 CH32M007G8R6	-0.4	V_{CC12V}+ 0.4	V
		CH32M007E8	-0.4	V_{HV}+0.4	V
dV_S/dt	Slew rate of floating ground voltage VS	CH32M007K8U7 CH32M007G8R6		20	V/nS
$\|\Delta V_{DD\_x}\|$	Variations between different main power supply pins	CH32V007		50	mV
$\|\Delta V_{SS\_x}\|$	Variations between different ground pins			50	mV
$V_{ESDIO(HBM)}$	Electrostatic discharge voltage (HBM) of ordinary I/O pin		4K		V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (HBM) of dedicated pin.	CH32M007	2K		V
I_{AVVHV}	V_{HV} pin continuous input current			50	mA
$I_{AVVCC12V}$	V_{CC12}V pin continuous input current	CH32M007K8U7		50	mA

I_{PEAKVB}	V_B built-in diode 1% duty cycle pulse output current	CH32M007G8R6		100	mA
I_{AVVB}	V_B built-in diode continuous output current			10	mA
I_{VDD}	Total current of all V_{DD} main power pins	CH32V007		100	mA
I_{VSS}	Total current of all V_{SS} common ground pins			200	mA
I_{IO}	Sink current on any I/O and control pin			30	mA
	Output current on any I/O and control pin			-30	
$I_{INJ(PIN)}$	XI pin of HSE			+/-4	
	Injected current on other pins			+/-4	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins			+/-20	

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2-1 General operating conditions

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
F_{HCLK} Or F_{SYS}	Internal system bus frequency Or microprocessor main frequency					48	MHz
V_{DD}	Standard operating voltage		ADC not used	2.0		5.5	V
			ADC used	2.4		5.5	
T_A	Ambient temperature	Exclude CH32M007K8U7		-40		85	℃
		CH32M007K8U7		-40		105	℃
T_J	Junction temperature range	Exclude CH32M007K8U7		-40		105	℃
		CH32M007K8U7		-40		105	℃

Table 3-2-2 Other power supply operating conditions (only for CH32M007K8U7 and CH32M007G8R6 chip)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

V_{HV}	Input power supply voltage of internal high voltage regulator	Enable high voltage regulator		18	20~48	50	V
		V_{HV} short to V_{CC12V}		6		17	V
V_{HVREG}	Internal high voltage regulator V_{CC12V} pin output voltage			10	12	13	V
I_{HVREG}	Load current of internal high voltage regulator (including internal bootstrap)		Attention to heat dissipation			30	mA
V_{CC12V}	Input power supply voltage of low-side driver and internal low-voltage regulator			6	12	17	V
V_{DD}	Output voltage of internal low-voltage regulator			4.9	5	5.1	V
I_{DD}	Load current of internal low-voltage regulator (including all loads such as ordinary I/O and MCU core)		Attention to heat dissipation			20	mA
V_S	High-side floating ground voltage			-1.2		50	V
V_B	High-side bootstrap supply voltage			V_{CC12V} -1.2	V_{CC12V}+ V_S	62	V
V_{B_S}	Voltage difference between high-side bootstrap power supply V_B and floating ground V_S			5.5	V_{CC12V}-1	16	V

Table 3-2-3 Other power supply operating conditions (only for CH32M007E8U6 chip)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HV}	Power supply voltage of gate driver		6	6~24	26	V
V_{HREG}	Input power supply voltage of internal voltage regulator		6	7	26	V
V_{DD}	Output voltage of internal voltage regulator		4.9	5	5.1	V
I_{DD}	Load current of internal voltage regulator	Attention to			30	mA

	(including all loads such as ordinary I/O and MCU core)	heat dissipation				

Table 3-2-4 Other power supply operating conditions (only for CH32M007E8R6 chip)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HV}	Supply voltage of internal voltage regulator and gate driver		6	6~24	26	V
V_{DD}	Output voltage of internal voltage regulator		4.9	5	5.1	V
I_{DD}	Load current of internal voltage regulator (including all loads such as ordinary I/O and MCU core)	Attention to heat dissipation			30	mA

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rising rate		0.1	∞	us/V
	V_{DD} falling rate		40	∞	
t_{VHV}	V_{HV} rising rate		0.2	∞	us/V
	V_{HV} falling rate		20	∞	
t_{VCC12V}	V_{CC12V} rising rate		0.2	∞	us/V
	V_{CC12V} falling rate		20	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}	Programmable Voltage Detector level selection	PLS[1:0] = 00 Rising edge		1.86		V
		PLS[1:0] = 00 Falling edge		1.85		
		PLS[1:0] = 01 Rising edge		2.22		V
		PLS[1:0] = 01 Falling edge		2.21		
		PLS[1:0] = 10 Rising edge		2.42		V

		PLS[1:0] = 10 Falling edge		2.4		
		PLS[1:0] = 11 Rising edge		2.64		V
		PLS[1:0] = 11 Falling edge		2.59		
$V_{PVDhyst}$	PVD hysteresis		5	20	60	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.7	1.85	2.0	V
		Falling edge	1.6	1.75	1.9	V
$V_{PDRhyst}$	PDR hysteresis		60	100	150	mV
$t_{RSTTEMPO}$	Power-on reset	RST_MODE[1:0] = 11		2		ms
	Other reset			300		us

Note: 1. Normal temperature test value.

2. The built-in gate driver of CH32M007 supports undervoltage protection. Refer to Table 3-28 for specific voltages.

3.3.3 Embedded Reference Voltage

Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40℃~85℃	1.18	1.2	1.22	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	Slow sampling is recommended.	3		240	$1/f_{ADC}$

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2-1 CH32V007 current consumption measurement

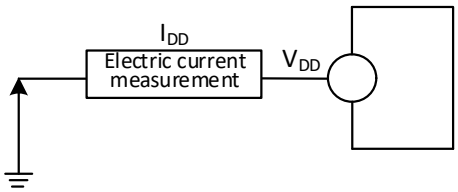


Figure 3-2-2 CH32M007K8U7 and CH32M007G8R6 current consumption measurement

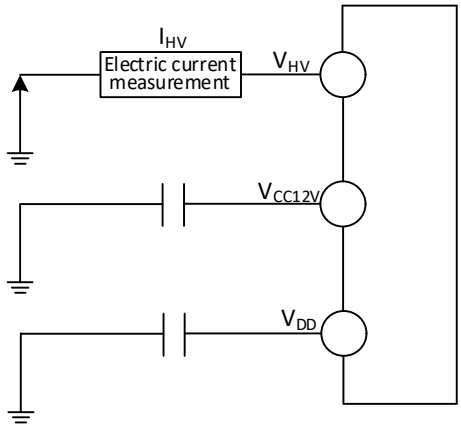


Figure 3-2-3 CH32M007E8U6 current consumption measurement

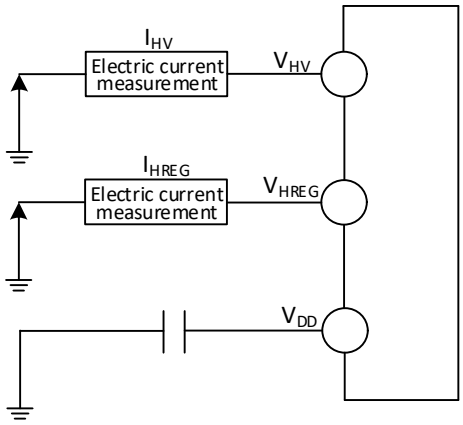
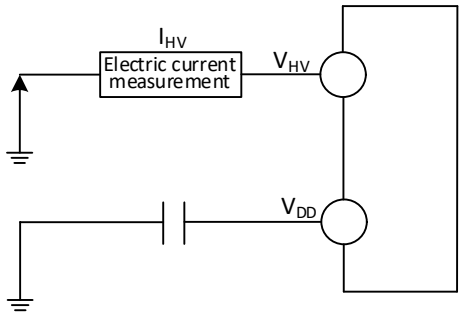


Figure 3-2-4 CH32M007E8R6 current consumption measurement



The CH32V007 is in the following conditions:

In the case of room temperature V_{DD} = 3.3V or 5V, during the test: all I/O ports are configured with pull-down input, HSI = 24MHz (calibrated), and the bit LDO_MODE of register PWR_CTLR is 10. Enable or disable the power consumption of all peripheral clocks.

The CH32M007 is in the following conditions:

CH32M007K8U7 and CH32M007G8R6: room temperature V_{HV} = 24V, V_{CC12V} = 12V, V_{DD} = 5V case, when tested: all I/O ports configured with pull-up inputs, HSI = 24M (calibrated), bit LDO_MODE of register PWR_CTLR = 10. enables or disables power consumption for all peripheral clocks.

CH32M007E8U6: Normal temperature V_{HV} = 15V, V_{HREG} = 7V, V_{DD} = 5V case, when tested: all I/O ports are configured with pull-up inputs, HSI = 24M (calibrated), bit LDO_MODE of register PWR_CTLR = 10. enable or disable power consumption for all peripheral clocks.

CH32M007E8R6: at room temperature with V_{HV} = 15V, V_{DD} = 5V, when tested: all I/O ports configured with pull-up inputs, HSI = 24M (calibrated), register PWR_CTLR bit LDO_MODE = 10. enables or disables power consumption for all peripheral clocks.

Table 3-6 Typical current consumption in Run mode, data processing code runs from the internal Flash

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	Runs on the high-speed external clock (HSE) (HSE_SI = 00, HSE_LP = 1)	X	F_{HCLK} = 48MHz	4.4	3.5	mA
				F_{HCLK} = 24MHz	3.3	2.8	
				F_{HCLK} = 16MHz	2.8	2.5	
				F_{HCLK} = 8MHz	2.5	2.4	
				F_{HCLK} = 750KHz	1.7	1.7	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	3.7	2.8	
				F_{HCLK} = 24MHz	2.5	2.0	
				F_{HCLK} = 16MHz	2.1	1.7	
				F_{HCLK} = 8MHz	1.8	1.6	
				F_{HCLK} =	0.9	0.9	

				750KHz			
			1	F_{HCLK} = 40KHz	0.6	0.6	

Note: The above are the measured parameters of CH32V007.

Table 3-7 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	Runs on the high-speed external clock (HSE) (HSE_SI = 00, HSE_LP = 1)	X	F_{HCLK} = 48MHz	3.0	2.1	mA
				F_{HCLK} = 24MHz	2.3	1.8	
				F_{HCLK} = 16MHz	2.1	1.8	
				F_{HCLK} = 8MHz	1.8	1.7	
				F_{HCLK} = 750KHz	1.6	1.6	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	2.2	1.3	
				F_{HCLK} = 24MHz	1.5	1.0	
				F_{HCLK} = 16MHz	1.3	1.0	
				F_{HCLK} = 8MHz	1.1	0.9	
				F_{HCLK} = 750KHz	0.9	0.9	
			1	F_{HCLK} = 40KHz	0.6	0.6	

Note: The above are the measured parameters of CH32V007.

Table 3-8 Typical current consumption in Standby mode

Symbol	Parameter	Condition			Typ.	Unit
		Independent watchdog	LSI	V_{DD}		
I_{DD}	Supply current in Standby mode	Enable	Enable	3.3V	10.7	uA
				5V	11.6	
		Disable	Disable	3.3V	10.2	
				5V	11.1	
		Disable	Enable	3.3V	10.7	
				5V	11.6	

Note: The above are the measured parameters of CH32V007.

Table 3-9-1 Other typical current consumption (Increased CH32M007K8U7 and CH32M007G8R6 compared to CH32V007)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_Q(1)(2)	V_{CC12V} and V_{HV} combined quiescent current (high voltage regulator enabled)	V_{CC12V} = V_{HV} = 6V		105		uA
		V_{CC12V} = V_{HV} = 15V		115		uA
		V_{HV} = 24V, V_{CC12}V to capacitor		135		uA
		V_{HV} = 48V, V_{CC12V} to capacitor		185		uA

Note: 1. The above are measured parameters.

2. At this time, it is necessary to set the pre-drive signal in CH32M007K8U7 and CH32M007G8R6 at a low level.

3. If you need more low-power consumption, the available independent CH283 chip and only to the V_{CC12V} power supply, V_{HV}/V_{CCREG} suspended, without its internal high-voltage and low-voltage regulator, you can save another 30uA.

Table 3-9-2 Other typical current consumption (Increased CH32M007E8U6 compared to CH32V007)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_Q(1)(2)	V_{HV} and V_{HREG} combined quiescent current	V_{HV} = V_{HREG} = 6V		41		uA
		V_{HV} = V_{HREG} = 11.5V		52		uA
		V_{HV} = V_{HREG} = 12.5V		97		uA

		V_{HV} = V_{HREG} = 24V		130		uA

Note: 1. The above are measured parameters.

2. At this time, it is necessary to set the pre-drive signal in CH32M007E8U6 at a low level.

Table 3-9-2 Other typical current consumption (Increased CH32M007E8R6 compared to CH32V007)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_Q(1)(2)	V_{HV} quiescent current	V_{HV} = 6V		41		uA
		V_{HV} = 11.5V		52		uA
		V_{HV} = 12.5V		97		uA
		V_{HV} = 24V		130		uA

Note: 1. The above are measured parameters.

2. At this time, it is necessary to set the pre-drive signal in CH32M007E8R6 at a low level.

3.3.5 External Clock Source Characteristics

Table 3-10 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		3	24	32	MHz
V_{HSEH}(1)	XI input pin high-level voltage		0.8V_{DD}		V_{DD}	V
V_{HSEL}(1)	XI input pin low-level voltage		0		0.2V_{DD}	V
$C_{in(HSE)}$	XI input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle		40	50	60	%
I_L	XI input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

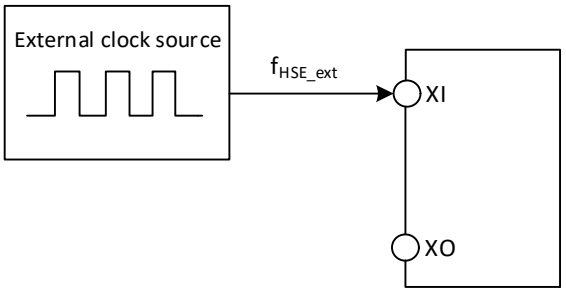


Table 3-11 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{XI}	Resonator frequency		3	24	32	MHz
R_F	Feedback resistor (no external)			250		kΩ
C_{LOAD}	Recommended load capacitance and corresponding crystal series impedance R_S	R_S = 60Ω(1)		20		pF
I_{HSE}	HSE drive current	HSE_LP = 0, 20p load		1.6		mA
		HSE_LP = 1, 20p load		0.8		
g_m	Oscillator transconductance	Startup		21		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable		1.5(2)		ms

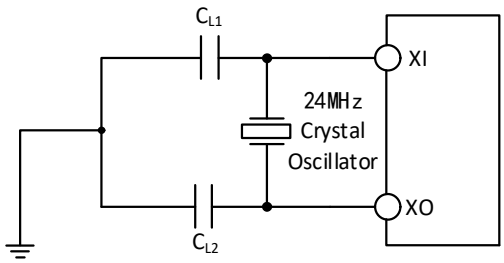
Note: 1. 25M crystal ESR is recommended not more than 80Ω, less than 25m can be appropriately relaxed.

2. Startup time refers to the time difference between when HSEON is turned on and when HSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally C_{L1} = C_{L2}.

Figure 3-4 Typical circuit of external 24M crystal



3.3.6 Internal Clock Source Characteristics

Table 3-12 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)	HSI_LP = 0		24		MHz
		HSI_LP = 1	30	42	58	KHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	HSI_LP = 0, TA = -10℃~70℃	-2.0		2.0	%

		HSI_LP = 0, TA = -40℃~85℃	-3.0		3.0	%
$t_{SU(HSI)}$(1)	HSI oscillator startup stabilization time			3	8	us
$I_{DD(HSI)}$	HSI oscillator power consumption	HSI_LP = 0		200		uA
		HSI_LP = 1		8.5		

Note: 1. Register RCC_CTLR HSION is set to 1 and wait for HSIRDY to be set to 1.

Table 3-13 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		90	128	172	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$(1)	LSI oscillator startup stabilization time			30	100	us
$I_{DD(LSI)}$(1)	LSI oscillator power consumption			550		nA

Note: 1. Register RCC_CTLR LSION is set to 1 and wait for LSIRDY to be set to 1.

3.3.7 Wakeup Time from Low-power Mode

Table 3-14 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	Use HSI RC clock to wakeup	10	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up	250	us

Note: The above are measured parameters.

3.3.8 Memory Characteristics

Table 3-15 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (256 bytes) program time			1.5	2.0	ms
t_{erase_page}	Page (256 bytes) erase time			2.5	3.0	ms

t_{erase_sec}	Sector (1K bytes) erase time			2.7	3.3	ms

Table 3-16 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase and write times	T_A = 25℃	300K			Times
		T_A = 70℃	100K			Times
t_{RET}	Data retention period	T_A = 25℃	20			Years
		T_A = 70℃	10			Years

3.3.9 I/O Port Characteristics

Table 3-17 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.3*V_{DD}+0.7		V_{DD}	V
V_{IL}	Standard I/O pin, input low-level voltage		0		0.15*V_{DD}+0.3	V
V_{hys}	Schmitt trigger voltage hysteresis		150			mV
I_{lkg}	Input leakage current				1	uA
R_{PU}	Pull-up equivalent resistance		35	45	55	kΩ
R_{PD}	Pull-down equivalent resistance		35	45	55	kΩ
C_{IO}	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-18 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, 8 pins input current	TTL port, I_{IO} = +8mA		0.4	V
V_{OH}	Output high level, 8 pin output current	2.7V< V_{DD} <5.5V	V_{DD}-0.4		

V_{OL}	Output low level, 8 pins input current	CMOS port, I_{IO} = +8mA		0.4	V
V_{OH}	Output high level, 8 pin output current	2.7V< V_{DD} <5.5V	2.3		
V_{OL}	Output low level, 8 pins input current	I_{IO} = +20mA		1.3	V
V_{OH}	Output high level, 8 pin output current	2.7V< V_{DD} <5.5V	V_{DD}-1.3		

Note: The sum of current must not exceed the absolute maximum rating given in Section 3.2 of the table if more than one I/O pin is driven at the same time in the above conditions. When multiple I/O pins are driven at the same time, the current on the power supply/ground wire point is very large, which will cause the voltage drop so that the voltage of the internal I/O cannot reach the power supply voltage in the meter, resulting in the drive current less than the nominal value.

Table 3-19 Input/output AC characteristics

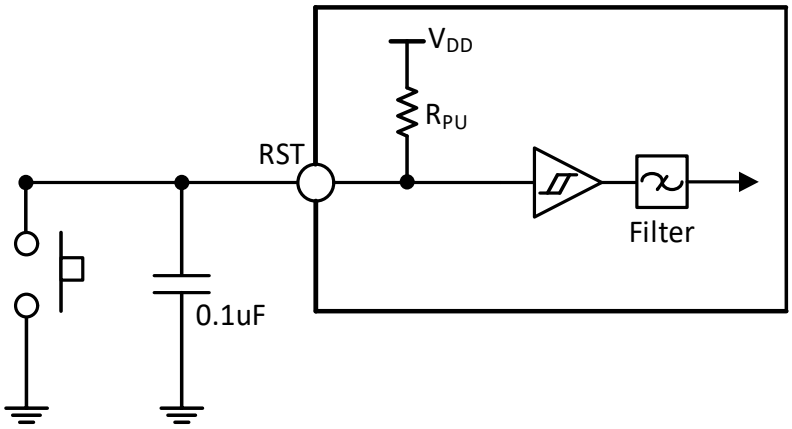
Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{max(IO)out}$	Maximum frequency	CL = 50pF, V_{DD} = 2.7-5.5V		30	MHz
$t_{f(IO)out}$	Output high to low fall time	CL = 50pF, V_{DD} = 2.7-5.5V		10	ns
$t_{r(IO)out}$	Output low to high rise time	CL = 50pF, V_{DD} = 2.7-5.5V		10	ns
t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

Note: Above parameters are guaranteed by design.

3.3.10 NRST Pin Characteristics

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin



Note: The capacitor in the figure is optional and can be used to filter out key jitter.

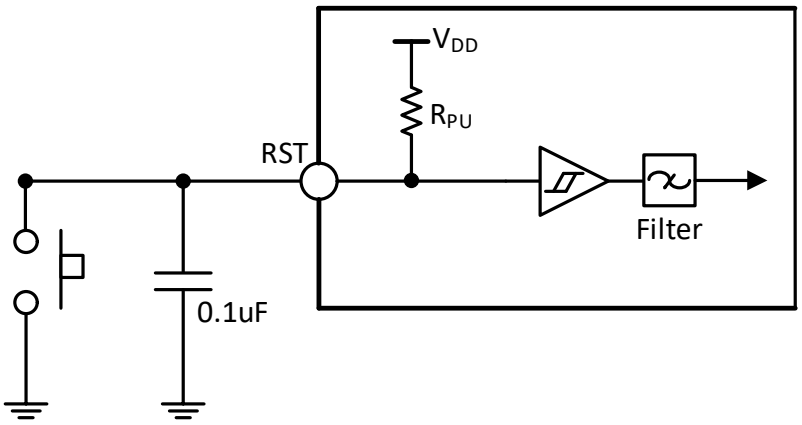
Table 3-20 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

$V_{IH(RST)}$	RST input high-level voltage		0.3*V_{DD}+0.7		V_{DD}	V
$V_{IL(RST)}$	RST input low-level voltage		0		0.15*V_{DD}+0.3	V
$V_{hys(RST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}	Pull-up equivalent resistance		35	45	55	kΩ
$V_{F(RST)}$	RST input can be filtered pulse width				100	ns
$V_{NF(RST)}$	RST input cannot be filtered pulse width		300			ns

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin



Note: The capacitance in the figure is optional and can be used to filter out key jitter.

3.3.11 TIM Timer Characteristics

Table 3-21 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	MHz
R_{esTIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock cycle when the		1	65536	$t_{TIMxCLK}$

	internal clock is selected	$f_{TIMxCLK}$ = 48MHz	0.0208	1363	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		1363	us

3.3.12 I2C Interface Characteristics

Figure 3-6 I2C bus timing diagram

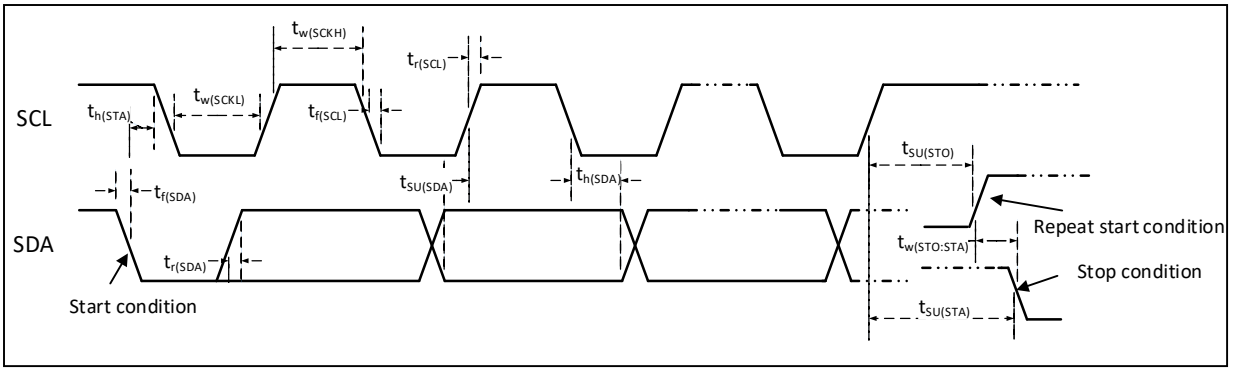


Table 3-22 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low-level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high-level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.13 SPI Interface Characteristics

Figure 3-7 SPI timing diagram in Master mode

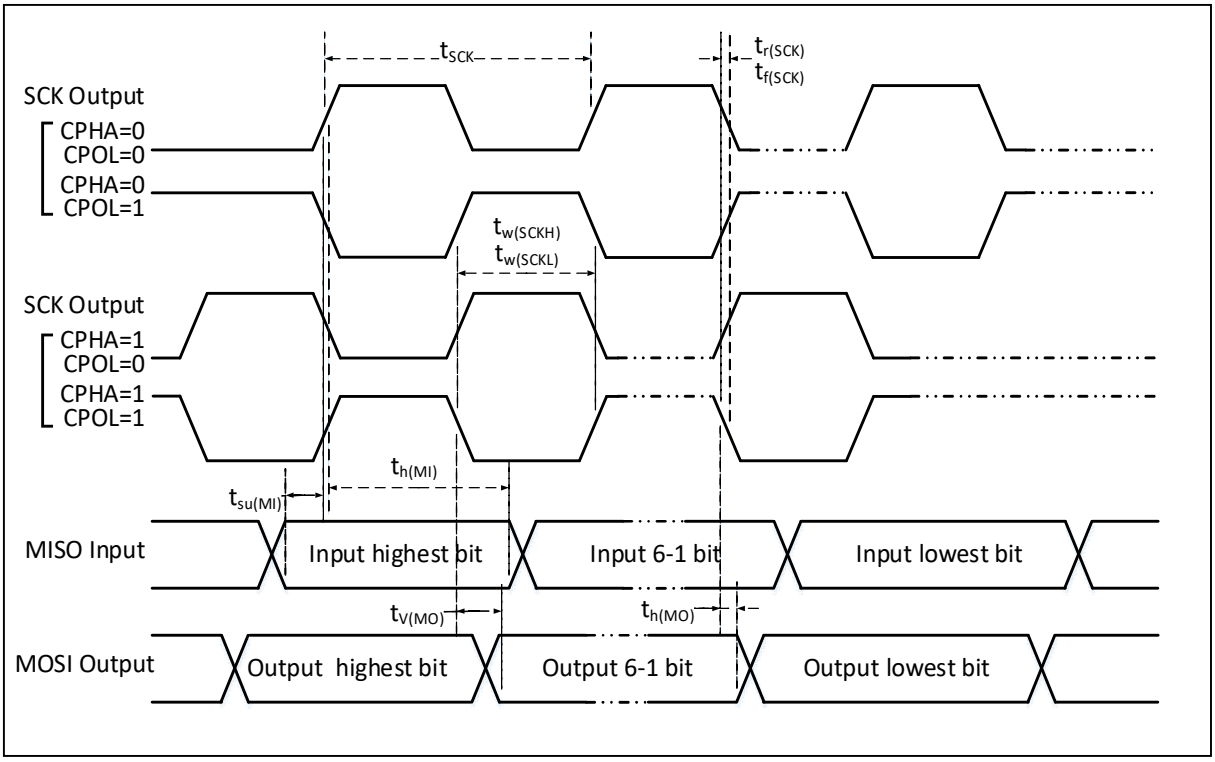


Figure 3-8-1 SPI timing diagram in Slave mode (CPHA=0, CPOL=0)

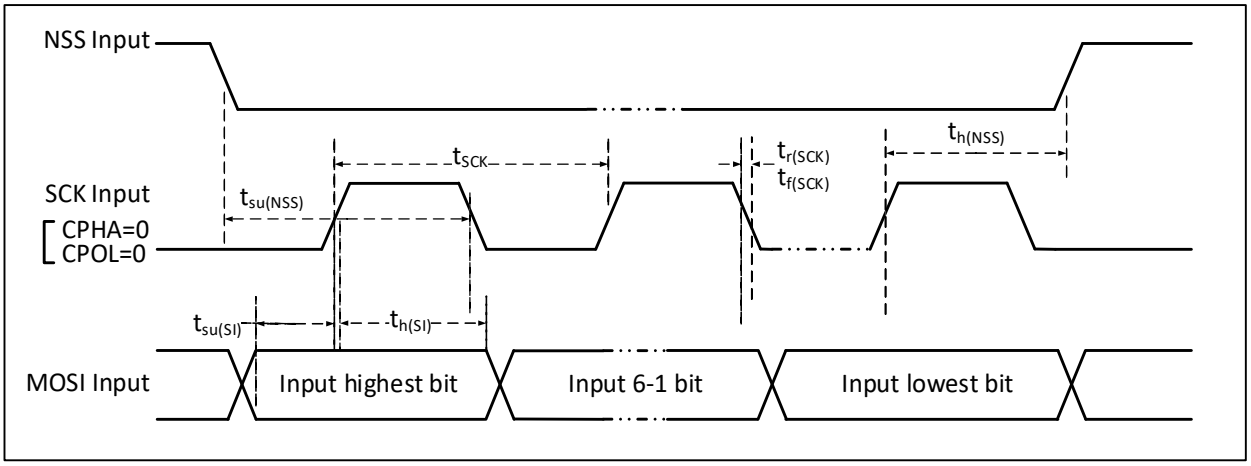


Figure 3-8-2 SPI timing diagram in Slave mode (CPHA=0, CPOL=1)

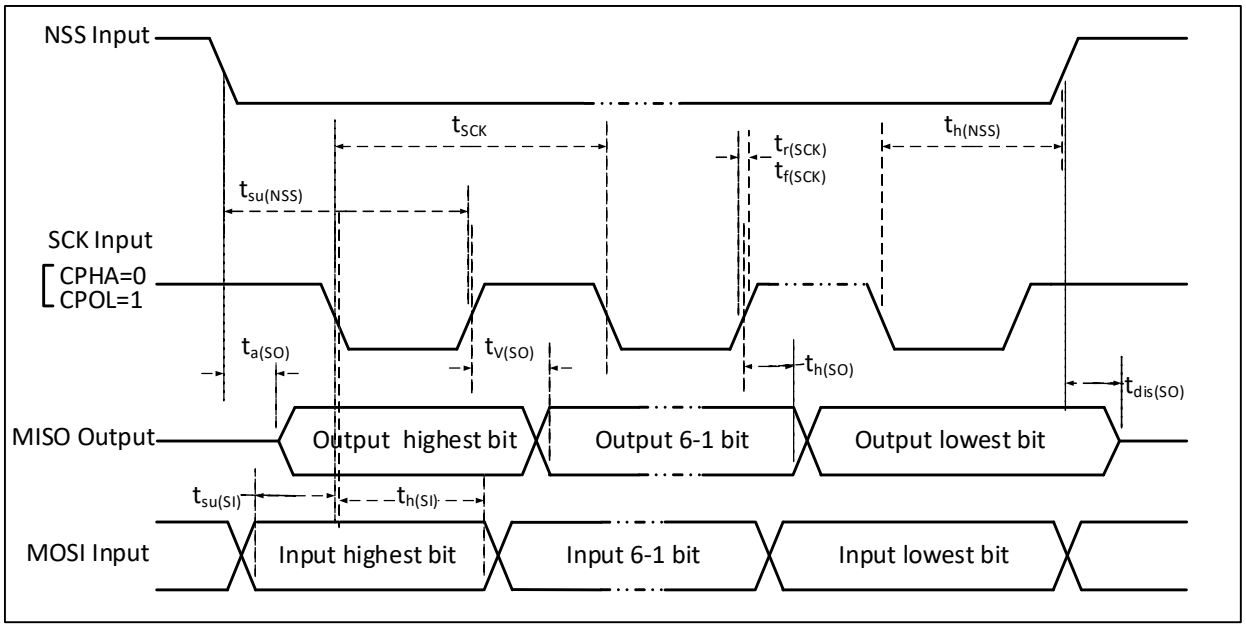


Figure 3-9-1 SPI timing diagram in Slave mode (CPHA = 1, CPOL=0)

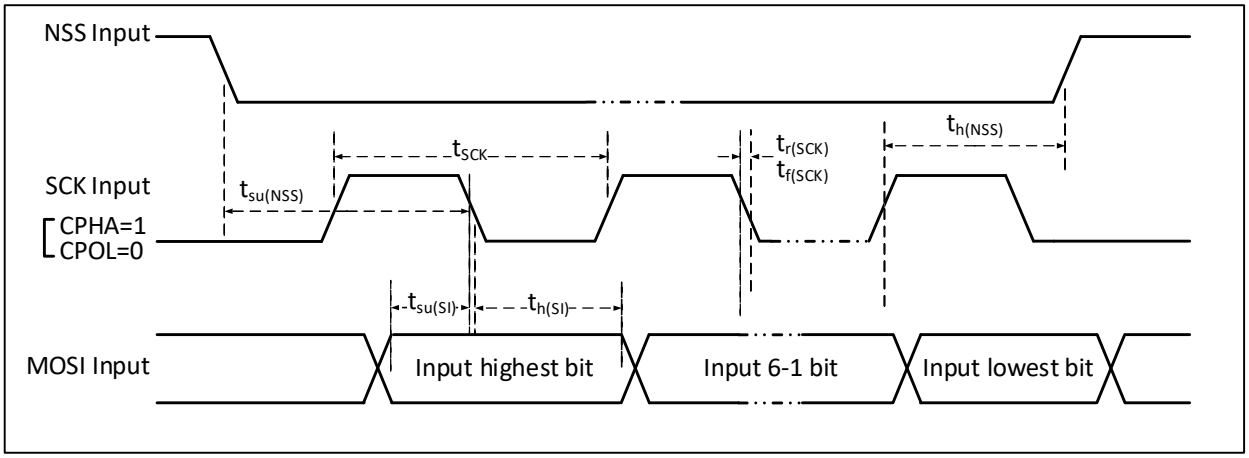


Figure 3-9-2 SPI timing diagram in Slave mode (CPHA = 1, CPOL=1)

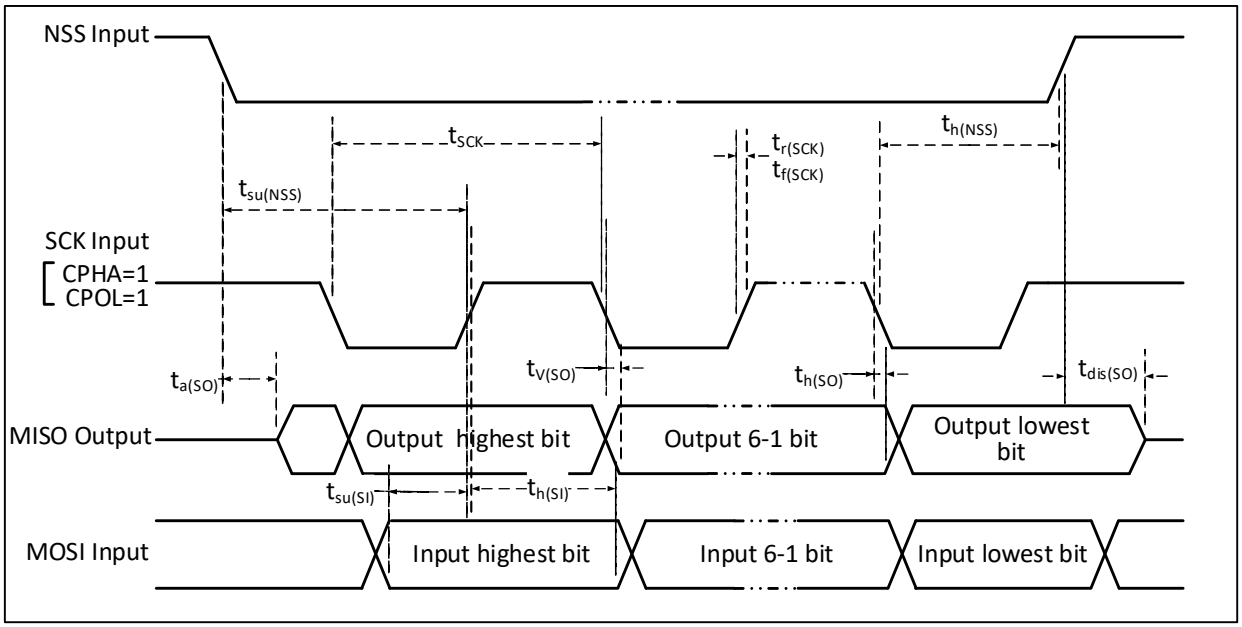


Table 3-23 SPI interface characteristics

Symbol	Parameter	Condition		Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode			24	MHz
		Slave mode			24	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF			10	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode		$2t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode		$2t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{HCLK} = 24MHz，Prescaler factor = 4		70	97	ns
$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	15		ns
			HSRXEN = 1	15-0.5t_{SCK}		
$t_{SU(SI)}$		Slave mode				ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	-4		ns
			HSRXEN = 1	0.5t_{SCK}-4		
$t_{h(SI)}$		Slave mode				ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{HCLK} = 20MHz		0	1t_{HCLK}	ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			15	ns

$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	6		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

3.3.14 12-bit ADC Characteristics

Table 3-24 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	$f_S \leq 1MHz$	2.4		5.5	V
		$f_S > 1MHz$	4.5		5.5	V
I_{DDA}	ADC supply current (Without buffer)	$f_S = 3MHz$		1.34		mA
		$f_S = 1MHz$		0.42		mA
I_{BUF}	ADC buffer own current	ADC_LP = 0		0.68		mA
		ADC_LP = 1		0.13		mA
f_{ADC}	ADC clock frequency			16	48	MHz
f_S	Sampling rate		0.06		3	MHz
f_{TRIG}	External trigger frequency	$f_{ADC} = 16MHz$			900	KHz
		$f_{ADC} = 48MHz$			2.7	MHz
					18	$1/f_{ADC}$
V_{AIN}	Switching voltage range		0		V_{DD}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1.5	kΩ
C_{ADC}	Internal sample and hold capacitance			4		pF
t_{CAL}	Calibration time	$f_{ADC} = 16MHz$			6.25	us
					100	$1/f_{ADC}$
t_{Iat}	Injection trigger conversion delay	$f_{ADC} = 16MHz$			0.125	us
		$f_{ADC} = 48MHz$			0.042	us
					2	$1/f_{ADC}$
t_{Iatr}	Conventional trigger conversion	$f_{ADC} = 16MHz$			0.125	us

	delay	f_{ADC} = 48MHz			0.042	us
					2	$1/f_{ADC}$
t_s	Sampling time	f_{ADC} = 16MHz	0.218		14.97	us
			3.5		239.5	$1/f_{ADC}$
		f_{ADC} = 48MHz	0.073		0.739	us
			3.5		35.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16MHz	1		15.75	us
			16		252	$1/f_{ADC}$
		f_{ADC} = 48MHz	0.33		1	us
			16		48	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N = 12 (represents a 12-bit resolution).

Table 3-25-1 Maximum R_{AIN} when f_{ADC} = 16MHz

T_S(Cycle)	t_S(us)	Maximum R_{AIN}(kΩ)
3.5	0.22	4
7.5	0.47	10
13.5	0.84	20
28.5	1.78	45
41.5	2.59	65
55.5	3.47	/
71.5	4.47	/
239.5	14.97	/

Table 3-25-2 Maximum R_{AIN} (High-speed) when f_{ADC} = 48MHz

T_S(Cycle)	t_S(us)	Maximum R_{AIN}(kΩ)

3.5	0.073	1.5
7.5	0.16	3
11.5	0.24	5
19.5	0.41	9
35.5	0.74	17
55.5	1.16	28
71.5	1.49	37
239.5	4.99	/

Table 3-26 ADC error (f_{ADC} = 16MHz, ADC_LP = 1, R_{AIN} < 10kΩ, V_{DD} = 5V)

Symbol	Parameter	Condition	Typ.	Max.	Unit
ET	Total error	$0 \le V_{AIN} < V_{DD}/2$	±3.5		LSB
		$0 \le V_{AIN} < V_{DD}$	±6		
ED	Differential nonlinear error	$0 \le V_{AIN} < V_{DD}/2$	±3.5		
		$0 \le V_{AIN} < V_{DD}$	±6		
EL	Differential nonlinear error	$0 \le V_{AIN} < V_{DD}/2$	±2.5		
		$0 \le V_{AIN} < V_{DD}$	±5		

Note: Above parameters are guaranteed by design.

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-10 ADC typical connection diagram

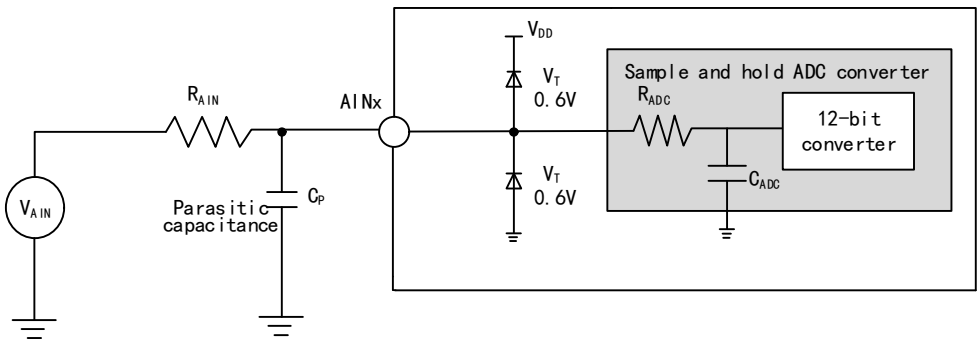
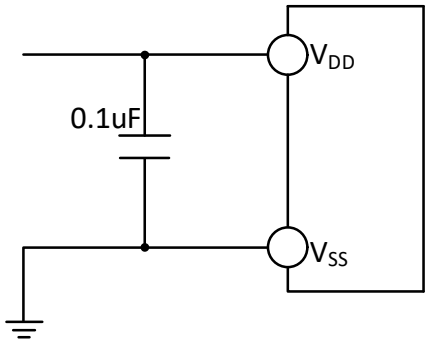


Figure 3-11 Analog power supply and decoupling circuit reference



3.3.15 OPA Characteristics

Table 3-27-1 OPA Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	No less than 2.5V is recommended	2.0	5	5.5	V
V_{CMIR}	Common mode input voltage		0		V_{DD}	V
$V_{IOFFSET}$	Input offset voltage			±3	±12	mV
I_{LOAD}	Drive current	R_{LOAD} = 4kΩ			1.4	mA
I_{LOAD_PGA}	PGA mode drive current				500	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		420		uA
CMRR(1)	Common mode rejection ratio	@1kHz		96		dB
PSRR(1)	Power supply rejection ratio	@1kHz		82		dB
Av(1)	Open loop gain	C_{LOAD} = 5pF		110		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 5pF		12		MHz
P_M(1)	Phase margin	C_{LOAD} = 5pF		75		°
S_R(1)	Slew rate limited	C_{LOAD} = 5pF		10		V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up,	Input V_{DD}/2, C_{LOAD} = 50pF, R_{LOAD} =			1	us

	0.1%	4kΩ				
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 4kΩ	V_{DD}-160			mV
		R_{LOAD} = 20kΩ	V_{DD}-35			
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 4kΩ			25	mV
		R_{LOAD} = 20kΩ			5	
PGA Gain(1)	PGADIF = 1 mode in phase	Gain = 4/8/16	-3		3	%
	Internal in-phase PGA	Gain = 4, V_{INP} < (V_{DD}/3)	-1		1	%
		Gain = 8, V_{INP} < (V_{DD}/7)	-1		1	%
		Gain = 16, V_{INP} < (V_{DD}/15)	-1		1	%
		Gain = 32, V_{INP} < (V_{DD}/31)	-1		1	%
V_B	Output DC bias voltage in PGA mode	VBEN = 1, VBSEL = 0		V_{DD}/2		V
		VBEN = 1, VBSEL = 1		V_{DD}/4		V
Delta R	Absolute value change of resistance		-15		15	%
eN(1)	Equivalent input noise	R_{LOAD} = 4kΩ@1kHz		100		nV/ sqrt(Hz)
		R_{LOAD} = 20kΩ@1KHz		60		

Note: 1. Design parameters are guaranteed.

2. The load current limits the saturated output voltage.

Table 3-27-2 OPA characteristics (High-speed mode)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7	5	5.5	V
V_{CMIR}	Common mode input voltage		0		V_{DD}	V
$V_{IOFFSET}$	Input offset voltage			±3	±12	mV
I_{LOAD}	Drive current	R_{LOAD} = 4kΩ			1.4	mA
I_{LOAD_PGA}	PGA mode drive current				500	uA

$I_{DDOPAMP}$	Current consumption	No load, static mode		1.6		mA
CMRR(1)	Common mode rejection ratio	@1kHz		96		dB
PSRR(1)	Power supply rejection ratio	@1kHz		82		dB
Av(1)	Open loop gain	C_{LOAD} = 5pF		115		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 5pF		64		MHz
P_M(1)	Phase margin	C_{LOAD} = 5pF		72		°
S_R(1)	Slew rate limited	C_{LOAD} = 5pF		36		V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up, 0.1%	Input V_{DD}/2, C_{LOAD} = 50pF, R_{LOAD} = 4kΩ			1	us
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				20	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 4kΩ	V_{DD}-160			mV
		R_{LOAD} = 20kΩ	V_{DD}-35			
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 4kΩ			25	mV
		R_{LOAD} = 20kΩ			5	
PGA Gain(1)	PGADIF = 1 mode in phase	Gain = 4/8/16	-3		3	%
	Internal in-phase PGA	Gain = 4, V_{INP} < (V_{DD}/3)	-1		1	%
		Gain = 8, V_{INP} < (V_{DD}/7)	-1		1	%
		Gain = 16, V_{INP} < (V_{DD}/15)	-1		1	%
		Gain = 32, V_{INP} < (V_{DD}/31)	-1		1	%
V_B	Output DC bias voltage in PGA mode	VBEN = 1, VBSEL = 0		V_{DD}/2		V
		VBEN = 1, VBSEL		V_{DD}/4		V

		= 1				
eN(1)	Equivalent input noise	RLOAD = 4kΩ@1kHz		100		nV/ sqrt(Hz)
		RLOAD = 20kΩ@1KHz		60		

Note: 1. Design parameters are guaranteed.

2. The load current limits the saturated output voltage.

3.3.16 CMP Characteristics

Table 3-28-1 CMP1 Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	No less than 2.5V is recommended.	2.0	5	5.5	V
V_{CMIR}	Common mode input voltage		0		V_{DD}	V
$V_{IOFFSET}$(1)	Input offset voltage			±3	±15	mV
$I_{DDOPAMP}$	Drive current			80		uA
V_{hys}	Hysteresis voltage			±24		mV
t_D(1)	Comparator delay, V_{INP} varies from (VINN-100mV) to (VINN+100mV).	$0 \le V_{INN} \le V_{DD}$		16	50	ns

Note: 1. Design parameters are guaranteed.

Table 3-28-2 CMP2 Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	No less than 2.5V is recommended.	2.0	5	5.5	V
V_{CMIR}	Common mode input voltage		0.9		V_{DD}	V
$V_{IOFFSET}$(1)	Input offset voltage			±3.3	±16	mV
$I_{DDOPAMP}$	Drive current			35		uA
V_{hys}	Hysteresis voltage			20	60	mV
t_D(1)	Comparator delay, V_{INP} varies	$0 \le V_{INN} \le V_{DD}$	2.0	5	5.5	ns

	from (VINN-100mV) to (VINN+100mV).					

Note: 1. Design parameters are guaranteed.

3.3.17 Internal Gate Driver Characteristics (only for CH32M007 chip)

Table 3-29-1 Internal gate driver characteristics (only for CH32M007K8U7 and CH32M007 chip)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC12UV}	Gate driver VCC12V undervoltage protection voltage		5.1	5.8	6.4	V
$V_{OH(LO)}$	LO high-level output voltage (relative to V_{CC12V})	I_{SOURCE} = 20mA		-250	-400	mV
$V_{OH(HO)}$	HO high-level output voltage (relative to V_B)	I_{SOURCE} = 20mA		-250	-400	mV
$V_{OL(LO)}$	LO low-level output voltage	I_{SINK} = 20mA		70	120	mV
$V_{OL(HO)}$	HO low-level output voltage (relative V_S)	I_{SINK} = 20mA		70	120	mV
$I_{OH(LO/HO)}$	LO/HO high-level output short-circuit pulse current	V_{CC12V}= 15V	320	530		mA
		V_{CC12V}= 12V	230	400		
$I_{OL(LO/HO)}$	LO/HO low-level output short-circuit pulse current	V_{CC12V}= 15V	650	1000		mA
		V_{CC12V}= 12V	480	770		

Table 3-29-2 Internal gate driver characteristics (only for CH32M007E8 chip)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HVUVR}	Gate driver V_{HV} undervoltage protection turn-on voltage		4.8	5.2	5.7	V
V_{HVUVF}	Gate driver V_{HV} undervoltage protection turn-off voltage		4.4	4.9	5.3	V
V_{HVUVS}	Gate driver V_{HV} undervoltage protection hysteresis voltage		0.1	0.3	0.6	V
V_{OHL}	LO high level output voltage	I_{SOURCE} = 20mA	9.5	11.5	14	V

V_{OHH}	HO high level output voltage (relative to V_{HV})	I_{SOURCE} = 20mA		-170	-280	mV
V_{OLL}	Lol low level output voltage	I_{SINK} = 20mA		105	180	mV
V_{OLH}	HO low level output voltage (relative to V_{HV})	I_{SINK} = 20mA	-14	-11.5	-9.5	V
I_{OH}	Short-circuit pulse current when LO drives high level (used to turn on N-type power tube)	V_{HV} = 15V	100	140		mA
		V_{HV} = 7V	80	115		
	Short-circuit pulse current when HO drives high level (used to quickly turn off P-type power tube)	V_{HV} = 15V	500	720		mA
		V_{HV} = 7V	160	230		
I_{OL}	Short-circuit pulse current when LO drives low level (used to quickly turn off N-type power tube)	V_{HV} = 15V	420	600		mA
		V_{HV} = 7V	140	200		
	Short-circuit pulse current when HO drives low level (used to turn on P-type power tube)	V_{HV} = 15V	105	150		mA
		V_{HV} = 7V	85	120		

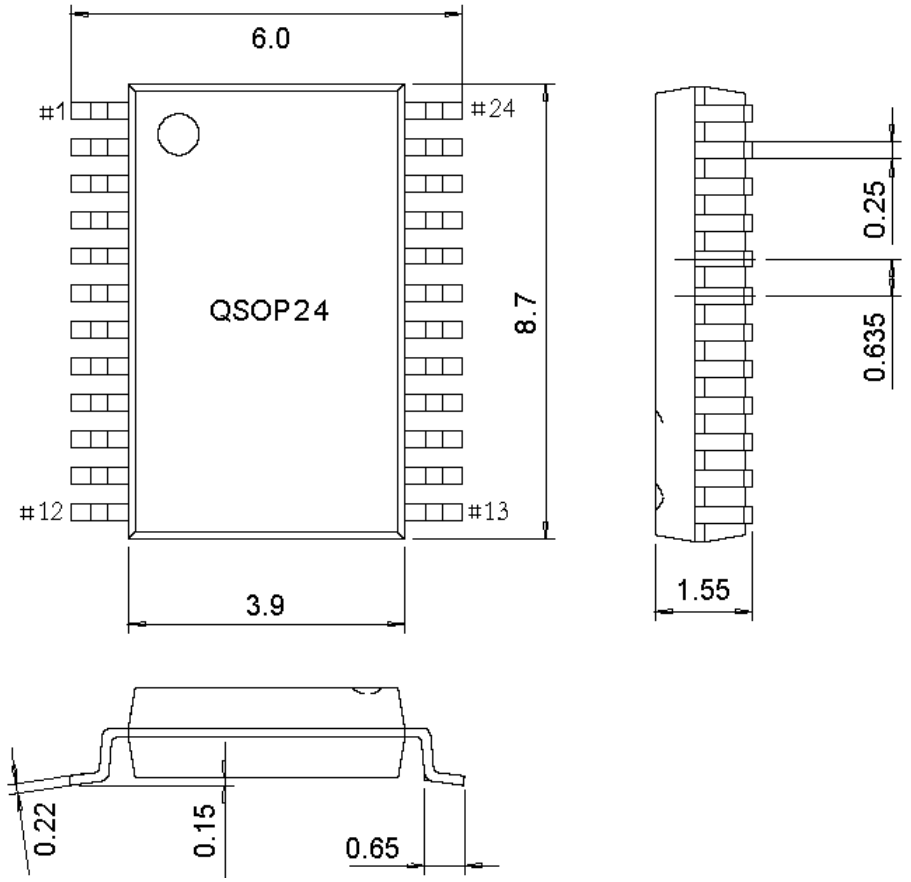
Chapter 4 Package and Ordering Information

Packages

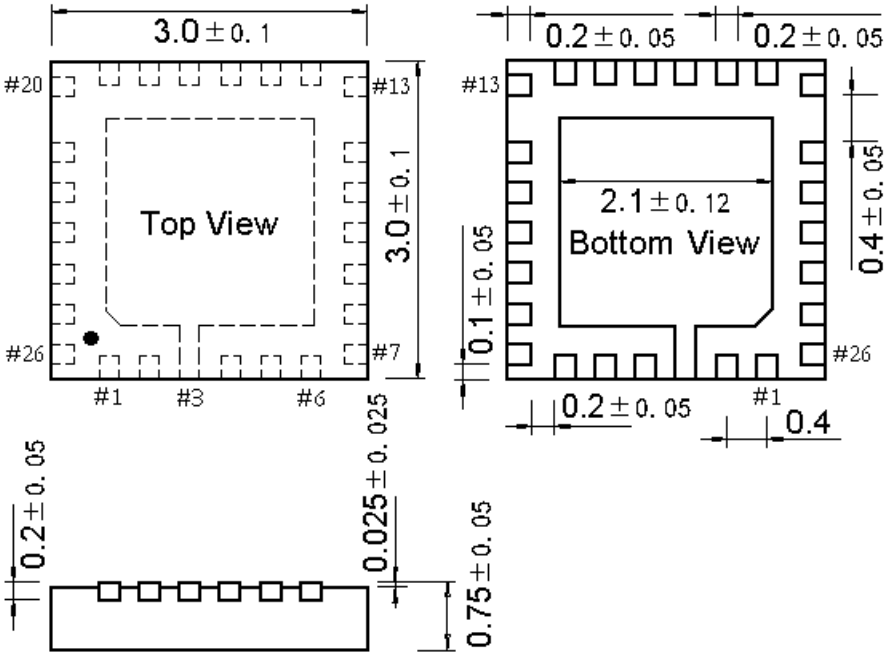
Package Form	Body Size	Pin Pitch		Package Description	Order Model
QSOP24	3.9*8.7mm	0.635mm	25.0mil	Quarter-sized Outline Package	CH32M007E8R6
QFN26C3	3*3mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32M007E8U6
QSOP28	3.9*9.9mm	0.635mm	25.0mil	Quarter-sized Outline Package	CH32M007G8R6
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32M007K8U7
QSOP24	3.9*8.7mm	0.635mm	25.0mil	Quarter-sized Outline Package	CH32V007E8R6
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32V007K8U6

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

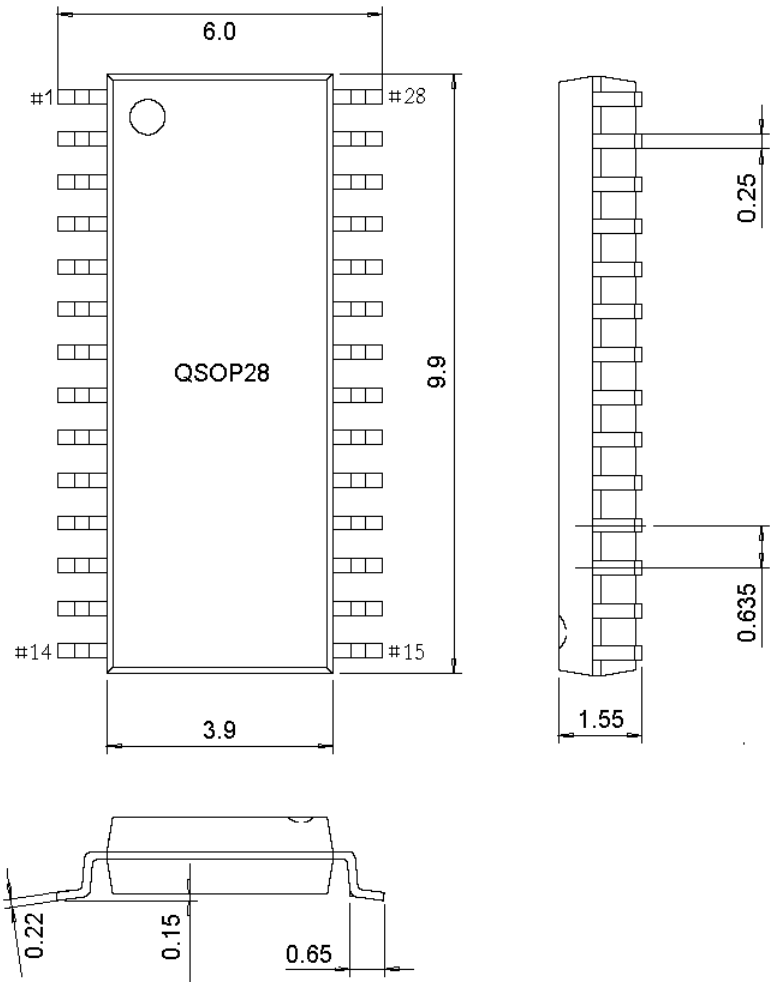
4.1 QSOP24 Package



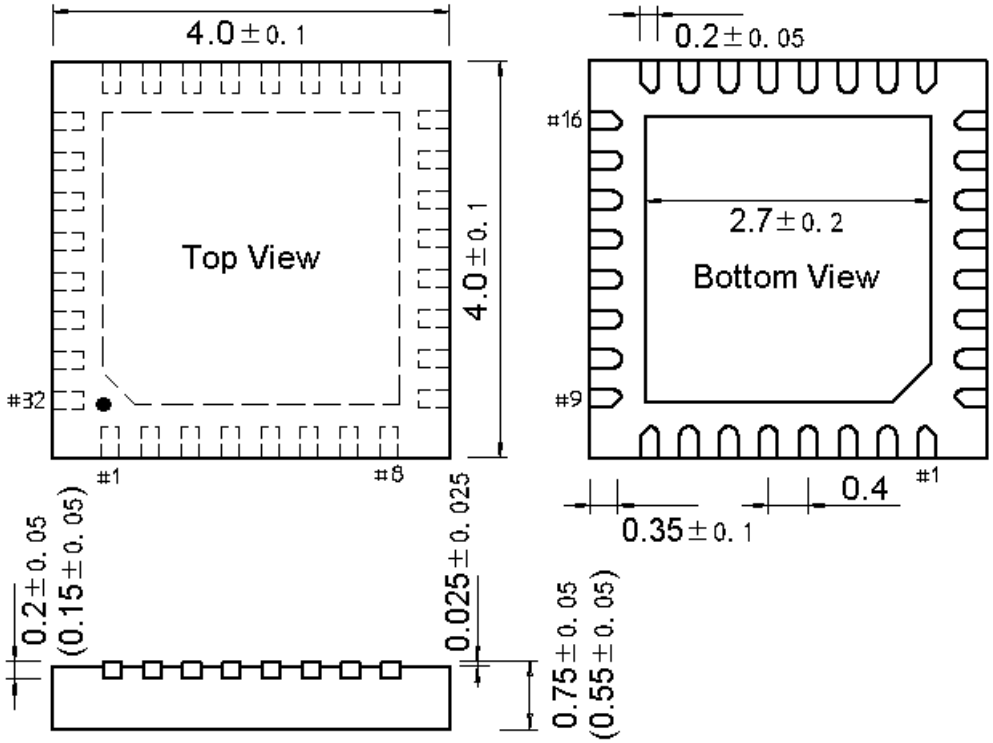
4.2 QFN26C3 Package



4.3 QSOP28 Package



4.4 QFN32 Package



Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Device family

F = Arm core, general-purpose MCU

V = QingKe RISC-V core, general-purpose MCU

L = QingKe RISC-V core, low-power MCU

X = QingKe RISC-V core, dedicated or special peripherals MCU

M = QingKe RISC-V core, built-in pre-drive motor MCU

Product type (*) + product subseries (*)

Product type	Product subseries
0 = QingKe V2/V4 core, Super value version, system frequency <=48M	02 = 16K Flash memory super value general-purpose 03 = 16K Flash basic general-purpose, OPA 05 = 32K Flash enhanced general-purpose, OPA, dual serial port 06 = 64K Flash versatile, OPA, dual serial port, TKey 07 = Basic motor application, OPA+CMP 35 = Connection, USB, USB PD/Type-C 33 = Connection, USB
1 = M3/QingKe V3/V4 core, Basic version, system frequency<=96M 2 = M3/QingKe V4 non-floating-point core, Enhanced, system frequency <=144M	03 = Connection, USB 05 = Connection, USB HS, SDIO, CAN 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 17 = Interconnected, USB HS, CAN, Ethernet (built-in PHY), SDIO, FSMC

3 = QingKe V4F floating-point core, Enhanced, system frequency <=144M	

Pin number

J = 8 pins	D = 12 pins	A = 16 pins	F = 20 pins	E = 24 pins
G = 28 pins	K = 32 pins	T = 36 pins	C = 48 pins	R = 64 pins
W = 68 pins	V = 100 pins	Z = 144 pins		

Flash memory size

4 = 16K Flash memory	6 = 32K Flash memory	7 = 48K Flash memory
8 = 64K Flash memory	B = 128K Flash memory	C = 256K Flash memory

Package

T = LQFP	U = QFN	R = QSOP	P = TSSOP	M = SOP

Temperature range

6 = -40°C~85°C	7 = -40°C~105°C
3 = -40°C~125°C	D = -40°C~150°C