SSC8629G
High-Integrated Car Camera SoC Processor

Preliminary Product Brief Version 0.2

REVISION HISTORY

Revision No.	Description	Date
0.1	• Initial release	10/29/2019
0.2	• Updated ambient operating temperature range	12/20/2019

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1. CHIP OVERVIEW

The SSC8629G products are highly integrated multimedia System-on-Chip (SoC) products for high-resolution intelligent video recording applications like Car camera.

The chip includes a 32-bit dual-core RISC processor, advanced Image Signal Processor (ISP), high performance MJPEG/H.264/H.265 video encoder (up to 4K 30fps), Deep Learning Accelerator (DLA), Intelligent Video Engine (IVE), as well as high speed I/O interfaces like MIPI, and Ethernet.

Advanced low-power, low-voltage architecture and optimized design flow are implemented to fulfill long time usage applications. Hardwired AES/DES/3DES cipher engines are integrated to support secure boot, authentication, and video/audio stream encryption in security system.

The SSC8629G, powered by SigmaStar Technology, comes with a complete hardware platform and software SDK, allowing customers to speed up "Time-to-Market."

2. BLOCK DIAGRAM

Figure 2-1 shows the major functional blocks of SSC8629G chip.

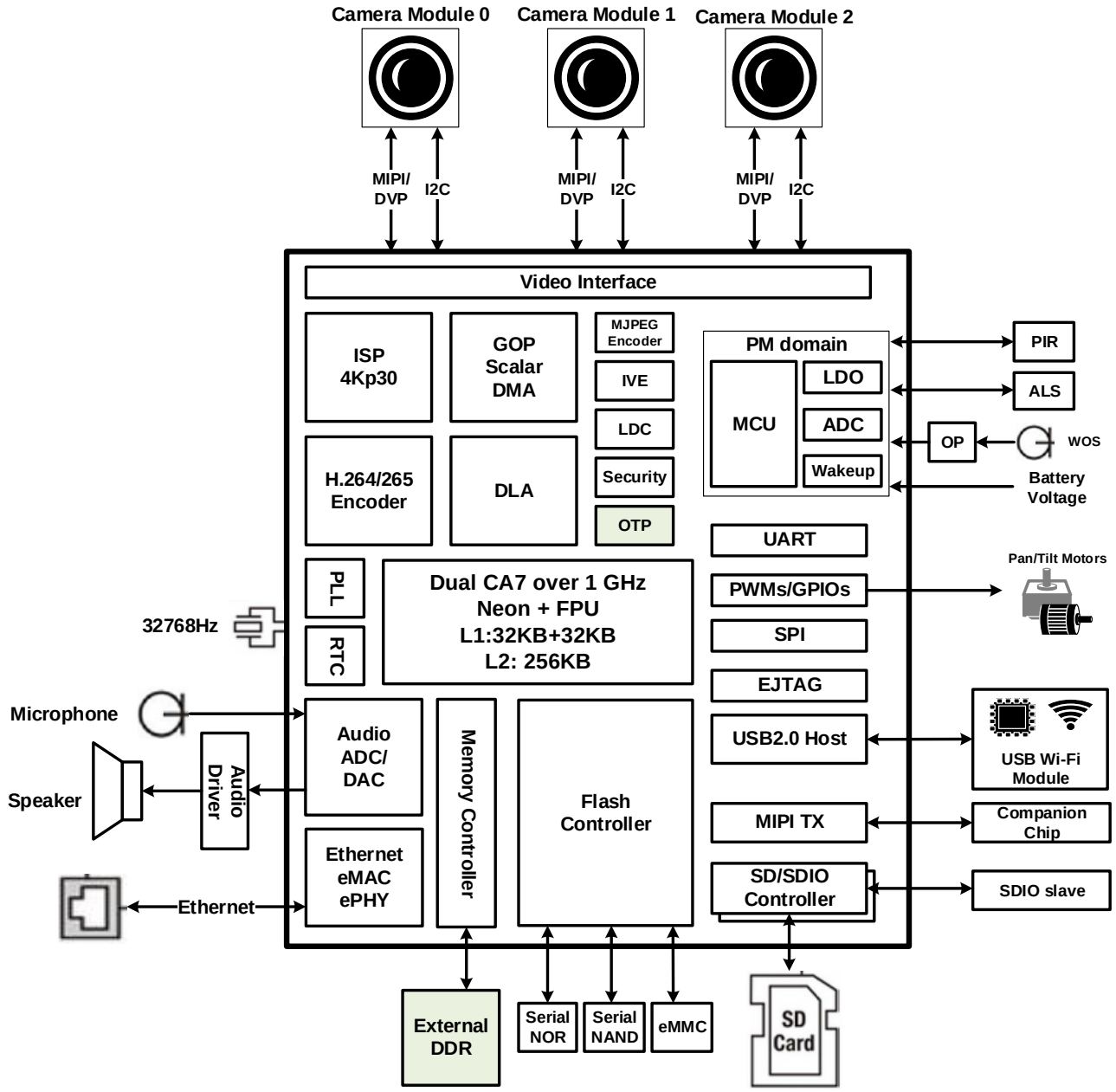


Figure 2-1: SSC8629G Block Diagram

3. FEATURES

- High Performance Processor Core
  - ARM Cortex-A7 Dual Core
  - Clock rate over 1GHz
  - Neon and FPU
  - Memory Management Unit for Linux support
  - DMA Engine
- Image/Video Processor
  - Supports 8/10/12-bit parallel interface for raw data input
  - Supports MIPI interface with 2/4 data lanes and 1 clock lane
  - Supports max. three MIPI interfaces
  - Supports sensor interface with both parallel and MIPI
  - Supports 8/10-bit CCIR656 interface
  - Supports max. 4K (3840x2160) pixels video recording and image snapshot
  - Bad pixel compensation
  - Temporal-domain Noise Reduction (3DNR)
  - Bayer domain Spatial-domain Noise Reduction (2DNR)
  - Bayer domain filter to remove purple false color in highlight regions
  - Optical black correction
  - Lens shading compensation
  - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
  - CFA color interpolation
  - Color correction
  - Gamma correction
  - Video stabilization
  - High Dynamic Range (HDR) with two exposure frames and de-ghost function
  - Frame buffer data compression and de-compression to save memory bandwidth
  - Wide Dynamic Range (WDR) with local tone mapping
  - Flip, Mirror, and Rotation with 90 or 270 degree
  - Lens distortion correction (LDC/FishEye)
  - Rolling shutter compensation
  - Fully programmable multi-function scaling engines
- Advanced Color Engine
  - Luma gain/offset adjustment
  - Supports 2D peaking with user definition filter
  - Horizontal noise masking
  - Direct Luma Correction (DLC)
  - Black/White Level Extension (BLE/WLE)
  - IHC/ICC/IBC for chroma adjustment
  - Histogram statistics
  - Spatial domain IIR filter to reduce noise
- H.265/HEVC
  - Supports H.265/HEVC main profile
  - Supported Prediction Unit (PU) size: 32x32, 16x16, 8x8
  - Supported Transform Unit (TU) size: 32x32 to 4x4
  - Search range [H: +/-128, V: +/-64]
  - Supports up to quarter-pixel
  - Supports frame level and MB level rate control
  - Supports ROI encoding with custom QP map
  - Supports max. 4K with 30 fps encoding
- H.264 Encoder
  - Supports H.264 baseline, constrained baseline, main, and high profile
  - Supports 16x16, 8x8 and 4x4 block sizes
  - Search range [H: +/-64, V: +/-32]
  - Supports up to quarter-pixel
  - Supports frame level and MB level rate control
  - Supports ROI encoding with custom QP map
  - Supports max. 4K with 30 fps encoding

- JPEG Encoder
  - Supports JPEG baseline encoding
  - Supports YUV422 or YUV420 formats
  - Supports max. 4K with 30 fps encoding
  - Supports real-time mode and frame encode mode
- Video Encoding Performance
  - Supports 4K + FHD + D1 30 fps H.265/HEVC encoding
  - Supports 4K + FHD + D1 30 fps H.264 encoding
  - Supports MJPEG up to 4K 30 fps encoding
- Deep Learning Accelerator
  - Pure hardwired accelerator
  - Supports various video analysis functions like FD/FR, human detection, MD/OD, object tracking, etc.
- Audio Processor
  - One stereo ADC for microphone input
  - Two stereo DMIC inputs
  - One stereo DAC for lineout
  - Supports 8K/16K/32KHz/48KHz sampling rate audio recording
  - Digital and analog gain adjustment
  - I2S digital audio input and output with TDM up to 8-ch input and 2-ch output
- NOR/NAND Flash Interface
  - Compliant with standard, dual and quad SPI Flash memory components
  - High speed clock/data rate up to 108MHz
- SD Card/eMMC Interface
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode
  - Supports eMMC 4.3 interface
- SDIO 2.0 Interface
  - Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode
- USB Interface
  - One USB 2.0 configurable host or device
    - Host mode supports EHCI specification
    - Device mode supports 4 endpoints
  - Supports suspend/hibernation/wake-up power saving mode
- DRAM Memory
  - Supports external dual 16-bit DDR2 or DDR3/DDR3L or single 32-bit LPDDR2 interface with 1~8Gb size
- Connectivity
  - Supports MIPI TX CSI2 up to FHD@30fps RGB/YUV/Generic 8-bit format
  - Built-in 10/100M Ethernet MAC and Ethernet PHY
  - USB 2.0 Host Controller could be used for USB Wi-Fi Dongle or Module
  - SDIO 2.0 Host Controller could be used for SDIO Wi-Fi module
  - Supports Wake-on-LAN (WOL)
- Security Engines
  - Supports AES/DES/3DES/RSA/SHA-I/SHA-256
  - Supports secure booting
- Real Time Clock (RTC)
  - Built-in RTC working with 32.768 KHz crystal
  - Alarm interrupt for wakeup
  - Tick time interrupt (millisecond)
  - Built-in regulator
  - Supports low leakage RTC-mode for long battery application
- Power Management Unit (PM)
  - Built-in LDO to provide both 0.9V and 1.8V power sources
  - Built-in RC FRO to generate clock source
  - Supports multiple GPIOs for power control and RTC events
  - Supports PIR (Passive Infrared Sensor) interface
  - Supports ALS (Ambient Light Sensor) interface
  - Supports WOS (Wake on Sound) function
  - Supports 1.8V serial flash interface for MCP under low power application

- Peripherals
  - Dedicated GPIOs for system control
  - Supports max. 11 PWM outputs
  - Three generic UARTs and one fast UART with flow control
  - Three generic timers and one watchdog timer
  - Two SPI masters
  - Four I2C Masters
  - Built-in SAR ADC with 4-channel analog inputs for different kinds of applications
  - Supports internal temperature sensor
- Operating Voltage Range
  - Core: 0.9V
  - I/O: 1.8 ~ 3.3V
  - DRAM: 1.5V (DDR3) or 1.35V (DDR3L) or 1.2V (LPDDR2)
  - Power Consumption: TBD
- Package
  - BGA with 307 pins, 13mm x 13mm, ball pitch 0.65mm, ball size 0.35mm

4. PACKAGE DESCRIPTION

4.1. Ball Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A		SD0_CMD	SD0_D0	SD0_CDZ		XTAL_OUT	GND	SR1_IO10	SR1_IO08	SR1_IO06	SR1_IO04	SR1_IO02	SR0_IO10	SR0_IO08	SR0_IO06	SR0_IO04	SR0_IO02	SR0_IO00		A
B	SD0_D2	SD0_D3	SD0_CLK	SD0_D1	SPI_CZ	SE_XTAL_OUT	XTAL_IN	SR1_IO11	SR1_IO09	SR1_IO07	SR1_IO05	SR1_IO03	SR0_IO11	SR0_IO09	SR0_IO07	SR0_IO05	SR0_IO03	SR0_IO01	SR0_IO17	B
C	ETH_RN	ETH_RP	GND	SPI_CK	SD0_GPIO0	GND	GND	GND	GPIO12	GPIO11		SR1_IO19	SR1_IO18	GND		SR1_IO00	SR1_IO12	SR0_IO15	SR0_IO16	C
D		ETH_TN	ETH_TP	SPI_DO	SPI_DI	GND	GND		GPIO13	GPIO10		SR1_IO16	SR1_IO15	GND		SR1_IO01	SR0_IO14	SR0_IO18	SR0_IO19	D
E		GND	USB2_DM	I2S0_MCLK	SPI_WPZ	GND			GPIO14	GPIO9	AVDD_XTAL	SR1_IO17	SR1_IO14		AVDD1P2_MIPI		SR0_IO12	FUART_CTS	SR0_IO13	E
F	GND	USB2_DP	GND	I2S0_WCK	SPI_HLD		VDD	VDDP_0	GPIO15	GPIO8	GND		SR1_IO13	GND		VDDP_2A	FUART_RTS	FUART_RX		F
G	AUD_VAG	AUD_VRM_DAC	AUD_VRM_ADC	I2S0_DI	I2S0_BCK	AVDD_ETH	VDD	VDD	GND	GND	GND		GND	AVDDL_MIPI		VDDP_2B	FUART_TX	AVSS_XTAL_RTC		G
H		AUD_MICIN0	AUD_MICCM0	I2S0_DO	I2C0_SCL	GND		VDD	VDD	VDD	VDD	VDD	VDD	VDD		VDDP_1	XTAL_OUT_32K	XTAL_IN_32K	AVDD_RTC	H
J		AUD_MICIN1	AUD_MICCM1	ETH_LED0	I2C0_SDA	GND		VDD	VDD	VDD	VDD	VDD	VDD	GND	GND	GND	RESET	RTC_IO0		J
K	AUD_LINEOUT_L0	GND	AUD_LINEOUT_R0	GND	ETH_LED1	GND	AVDD3P3_USB	AVDD_USB	VDD	VDD	VDD	VDD	GND	GND	GND		RTC_IO2	RTC_IO1		K
L		GND	GND			AVDD_AUD	AVDD_PLL	DVDD_DDR_RX		GND	GND	GND	GND		GND		RTC_IO5	RTC_IO4	SAR_GPIO3	L
M		PAD_IO[73]	PAD_IO[72]	PAD_IO[62]	GND	GND	VDDIO_DATA	VDDIO_DATA		DVDD_DDR		GND	GND		AVDD_NODIE	DVDD_NODIE	SAR_GPIO2	SAR_GPIO0	SAR_GPIO1	M
N	GND	PAD_IO[69]	PAD_IO[71]	PAD_IO[60]	PAD_IO[57]		VDDIO_DATA	VDDIO_DATA	GND	VDDIO_MCLK	VDDIO_CMD	VDDIO_CMD	GND		GND	AVDD1P8_SPI	PM_SPI_HLD	PM_SPI_DO		N
P	PAD_IO[65]	PAD_IO[64]	PAD_IO[67]	PAD_IO[58]	PAD_IO[52]		GND	GND	GND			GND	GND	GND			PM_SPI_WPZ	PM_SPI_DI		P
R	PAD_IO[70]	PAD_IO[68]	PAD_IO[61]	PAD_IO[55]	PAD_IO[53]	GND	GND	PAD_IO[33]	PAD_IO[30]	PAD_IO[40]	PAD_IO[36]	PAD_IO[34]	GND	GND	GND	PM_GPIO7	PM_SPI_CK	PM_SPI_CZ	PM_GPIO8	R
T	PAD_IO[63]	PAD_IO[66]	GND	PAD_IO[59]	PAD_IO[56]	PAD_IO[54]	PAD_IO[37]	PAD_IO[38]	PAD_IO[39]	PAD_IO[31]	PAD_IO[35]	PAD_IO[32]	PAD_IO[28]	PAD_IO[29]	PAD_IO[1]	GND	PM_GPIO1	PM_GPIO5	PM_GPIO6	T
U	PAD_IO[47]	PAD_IO[46]	PAD_IO[45]	GND	PAD_IO[48]	PAD_IO[19]	PAD_IO[26]	GND	PAD_IO[18]	PAD_IO[14]	GND	PAD_IO[11]	PAD_IO[9]	GND	PAD_IO[0]	PM_UART_RX	PM_I2CM_SCL	PM_GPIO3	PM_GPIO4	U
V	PAD_IO[51]	PAD_IO[49]	PAD_IO[41]	PAD_IO[44]	PAD_IO[23]	PAD_IO[21]	PAD_IO[20]	PAD_IO[17]	PAD_IO[13]	PAD_IO[12]	PAD_IO[10]	PAD_IO[8]	PAD_IO[4]	PAD_IO[3]	PAD_IO[24]	PM_UART_TX	PM_UART_TX1	PM_GPIO0	PM_GPIO2	V
W		PAD_IO[50]	PAD_IO[43]	PAD_IO[42]		PAD_IO[27]	PAD_IO[22]		PAD_IO[16]	PAD_IO[15]		PAD_IO[6]	PAD_IO[7]	PAD_IO[5]	PAD_IO[2]		PM_UART_RX1	PM_I2CM_SDA		W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

4.2. Signal Description

Signal Name	Signal Type	Function	Pin Location
System Reset Interface			
RESET	I	System Reset (Active High)	J17
Debug UART Interface			
PM_UART_RX	I	Debug UART Receive Data Input with Pull Up Resistor / Slave I2C Serial Clock	U16
PM_UART_TX	O	Debug UART Transmit Data Output with Pull Up Resistor / Slave I2C Serial Data	V16
PM_UART_RX1	I	PM_UART1 Receive Data Input with Pull Up Resistor in Power Manage group domain	W17
PM_UART_TX1	O	PM_UART1 Transmit Data Output with Pull Up Resistor in Power Manage group domain	V17
System Interface			
XTAL_IN	I	24MHz Crystal Input	B7
XTAL_OUT	O	24MHz Crystal Output	A6
XTAL_IN_32K	I	32.768KHz Crystal Input	H18
XTAL_OUT_32K	O	32.768KHz Crystal Output	H17
SE_XTAL_OUT	O	24MHz Clock Output	B6
8051 SPI Flash Interface			
PM_SPI_CZ	O	SPI Flash Chip Select (Active Low)	R18
PM_SPI_CK	O	SPI Flash Clock	R17
PM_SPI_DI	O	SPI Flash Serial Data To Device (MOSI)	P18
PM_SPI_DO	I	SPI Flash Serial Data From Device (MISO)	N18
PM_SPI_WPZ	O	SPI Flash Write Protect	P17
PM_SPI_HLD	O	SPI Flash Hold	N17
GPIO Interface			
GPIO8	I/O	General Purpose Input/Output 8	F10
GPIO9	I/O	General Purpose Input/Output 9	E10
GPIO10	I/O	General Purpose Input/Output 10	D10
GPIO11	I/O	General Purpose Input/Output 11	C10
GPIO12	I/O	General Purpose Input/Output 12	C9
GPIO13	I/O	General Purpose Input/Output 13	D9
GPIO14	I/O	General Purpose Input/Output 14	E9

Signal Name	Signal Type	Function	Pin Location
GPIO15	I/O	General Purpose Input/Output 15	F9
PM GPIO Interface			
PM_GPIO0	I/O	Power Manage Group General Purpose Input/Output 0	V18
PM_GPIO1	I/O	Power Manage Group General Purpose Input/Output 1	T17
PM_GPIO2	I/O	Power Manage Group General Purpose Input/Output 2	V19
PM_GPIO3	I/O	Power Manage Group General Purpose Input/Output 3	U18
PM_GPIO4	I/O	Power Manage Group General Purpose Input/Output 4	U19
PM_GPIO5	I/O	Power Manage Group General Purpose Input/Output 5	T18
PM_GPIO6	I/O	Power Manage Group General Purpose Input/Output 6	T19
PM_GPIO7	I/O	Power Manage Group General Purpose Input/Output 7	R16
PM_GPIO8	I/O	Power Manage Group General Purpose Input/Output 8	R19
SAR ADC Interface			
SAR_GPIO0	I	General Purpose Input/Output or Muxed to SARADC Input Channel 0	M18
SAR_GPIO1	I	General Purpose Input/Output or Muxed to SARADC Input Channel 1	M19
SAR_GPIO2	I	General Purpose Input/Output or Muxed to SARADC Input Channel 2	M17
SAR_GPIO3	I	General Purpose Input/Output or Muxed to SARADC Input Channel 3	L19
CA7 SPI Flash Interface			
SPI_CZ	O	Master SPI Chip Select (Active Low)	B5
SPI_CK	O	Master SPI Serial Clock	C4
SPI_DI	I/O	Master SPI Serial Data To Device (MOSI) / SDIO0 - 4x IO mode	D5
SPI_DO	I/O	Master SPI Serial Data From Device (MISO) / SDIO1 - 4x IO mode	D4
SPI_WPZ	I/O	Master SPI Write Protect (Active Low) / SDIO2 - 4x IO mode	E5
SPI_HLD	I/O	Master SPI Hold input (Active Low) / SDIO3 - 4x IO mode	F5
I2S Interface			
I2S0_MCLK	O	I2S Master Clock	E4
I2S0_BCK	O	I2S Bit Clock	G5
I2S0_WCK	O	I2S Word Clock	F4

Signal Name	Signal Type	Function	Pin Location
I2S0_DI	I	I2S Data Input	G4
I2S0_DO	O	I2S Data Output	H4
Master I2C Interface			
I2C0_SCL	O	Non-PM Domain I2C 0 Master I2C Clock	H5
I2C0_SDA	I	Non-PM Domain I2C 0 Master I2C Data	J5
PM_I2CM_SCL	O	PM Domain I2C Master I2C Clock	U17
PM_I2CM_SDA	I	PM Domain I2C Master I2C Data	W18
Fast UART Interface			
FUART_RX	I	Fast UART Receive Data Input	F18
FUART_TX	O	Fast UART Transmit Data Output	G17
FUART_CTS	I	Fast UART Clear to Send	E18
FUART_RTS	O	Fast UART Request to Send	F17
Image Sensor Interface			
SR0_IO00	I/O	Sensor General Purpose Input/Output 0	A18
SR0_IO01	I/O	Sensor General Purpose Input/Output 1	B18
SR0_IO02	I/O	Sensor General Purpose Input/Output 2	A17
SR0_IO03	I/O	Sensor General Purpose Input/Output 3	B17
SR0_IO04	I/O	Sensor General Purpose Input/Output 4	A16
SR0_IO05	I/O	Sensor General Purpose Input/Output 5	B16
SR0_IO06	I/O	Sensor General Purpose Input/Output 6	A15
SR0_IO07	I/O	Sensor General Purpose Input/Output 7	B15
SR0_IO08	I/O	Sensor General Purpose Input/Output 8	A14
SR0_IO09	I/O	Sensor General Purpose Input/Output 9	B14
SR0_IO10	I/O	Sensor General Purpose Input/Output 10	A13
SR0_IO11	I/O	Sensor General Purpose Input/Output 11	B13
SR0_IO12	I/O	Sensor General Purpose Input/Output 12	E17
SR0_IO13	I/O	Sensor General Purpose Input/Output 13	E19
SR0_IO14	I/O	Sensor General Purpose Input/Output 14	D17
SR0_IO15	I/O	Sensor General Purpose Input/Output 15	C18
SR0_IO16	I/O	Sensor General Purpose Input/Output 16	C19
SR0_IO17	I/O	Sensor General Purpose Input/Output 17	B19
SR0_IO18	I/O	Sensor General Purpose Input/Output 18	D18
SR0_IO19	I/O	Sensor General Purpose Input/Output 19	D19
SR1_IO00	I/O	Sensor General Purpose Input/Output 0 (Group 1)	C16

Signal Name	Signal Type	Function	Pin Location
SR1_IO01	I/O	Sensor General Purpose Input/Output 1 (Group 1)	D16
SR1_IO02	I/O	Sensor General Purpose Input/Output 2 (Group 1)	A12
SR1_IO03	I/O	Sensor General Purpose Input/Output 3 (Group 1)	B12
SR1_IO04	I/O	Sensor General Purpose Input/Output 4 (Group 1)	A11
SR1_IO05	I/O	Sensor General Purpose Input/Output 5 (Group 1)	B11
SR1_IO06	I/O	Sensor General Purpose Input/Output 6 (Group 1)	A10
SR1_IO07	I/O	Sensor General Purpose Input/Output 7 (Group 1)	B10
SR1_IO08	I/O	Sensor General Purpose Input/Output 8 (Group 1)	A9
SR1_IO09	I/O	Sensor General Purpose Input/Output 9 (Group 1)	B9
SR1_IO10	I/O	Sensor General Purpose Input/Output 10 (Group 1)	A8
SR1_IO11	I/O	Sensor General Purpose Input/Output 11 (Group 1)	B8
SR1_IO12	I/O	Sensor General Purpose Input/Output 12 (Group 1)	C17
SR1_IO13	I/O	Sensor General Purpose Input/Output 13 (Group 1)	F13
SR1_IO14	I/O	Sensor General Purpose Input/Output 14 (Group 1)	E13
SR1_IO15	I/O	Sensor General Purpose Input/Output 15 (Group 1)	D13
SR1_IO16	I/O	Sensor General Purpose Input/Output 16 (Group 1)	D12
SR1_IO17	I/O	Sensor General Purpose Input/Output 17 (Group 1)	E12
SR1_IO18	I/O	Sensor General Purpose Input/Output 18 (Group 1)	C13
SR1_IO19	I/O	Sensor General Purpose Input/Output 19 (Group 1)	C12
10/100M Ethernet Interface			
ETH_RN	I	10/100M Ethernet Differential Pair of Receiver Signal Negative	C1
ETH_RP	I	10/100M Ethernet Differential Pair of Receiver Signal Positive	C2
ETH_TN	O	10/100M Ethernet Differential Pair of Transmitter Signal Negative	D2
ETH_TP	O	10/100M Ethernet Differential Pair of Transmitter Signal Positive	D3
ETH_LED0	O	10/100M Ethernet LED0 Control Driven Active When Linked	J4
ETH_LED1	O	10/100M Ethernet LED1 Control Driven Active When Linked in 100 Base-TX and Blinking When Transmitting or Receiving Data	K5
SD 2.0 Card Interface			
SD0_CLK	O	SD 2.0 Clock	B3
SD0_CMD	O	SD 2.0 Command	A2

Signal Name	Signal Type	Function	Pin Location
SD0_D0	I/O	SD 2.0 Data Bus 0	A3
SD0_D1	I/O	SD 2.0 Data Bus 1	B4
SD0_D2	I/O	SD 2.0 Data Bus 2	B1
SD0_D3	I/O	SD 2.0 Data Bus 3	B2
SD0_CDZ	I	Power Manage SD 2.0 Card Detect	A4
SD0_GPIO0	I/O	SD0 General Purpose Input/Output 0	C5
Audio Line Out Interface			
AUD_LINEOUT_L0	O	Audio Left Channel Line Output	K1
AUD_LINEOUT_R0	O	Audio Right Channel Line Output	K3
AUD_VAG	O	Audio Reference Voltage from 1/2 AVDD_AUD	G1
AUD_VRM_ADC	I	Audio Reference Voltage for ADC	G3
AUD_VRM_DAC	I	Audio Reference Voltage for DAC	G2
Analog Microphone Interface			
AUD_MICIN0	I	Audio Left Channel Microphone Positive Input	H2
AUD_MICCM0	I	Audio Left Channel Microphone Negative Input	H3
AUD_MICIN1	I	Audio Right Channel Microphone Positive Input	J2
AUD_MICCM1	I	Audio Right Channel Microphone Negative Input	J3
USB 2.0 Interface			
USB2_DM	I/O	USB 2.0 Differential Pair, Negative	E3
USB2_DP	I/O	USB 2.0 Differential Pair, Positive	F2
Power-on Control/RTC Interface			
RTC_IO0	I	Power-on Control & RTC GPIO0	J18
RTC_IO1	I	Power-on Control & RTC GPIO1	K18
RTC_IO2	I	Power-on Control & RTC GPIO2	K17
RTC_IO4	O	Power-on Control & RTC GPIO4	L18
RTC_IO5	O	Power-on Control & RTC GPIO5	L17
DDR Interface			
PAD_IO[0]	DDR IO	DDR3 DRAM Memory On-Die Termination DDR2 DRAM Memory On-Die Termination LPDDR2 NC	U15
PAD_IO[1]	DDR IO	DRAM Chip Selection 0 Signal	T15
PAD_IO[2]	DDR IO	DRAM Chip Selection 1 Signal	W15
PAD_IO[3]	DDR IO	DDR3 DRAM Memory Reset; Active Low DDR2 NC LPDDR2 NC	V14

Signal Name	Signal Type	Function	Pin Location
PAD_IO[4]	DDR IO	DDR3 DRAM Memory Address [13] DDR2 DRAM Memory Address [12] LPDDR2 NC	V13
PAD_IO[5]	DDR IO	DDR3 Row Address Strobe; Active Low DDR2 NC LPDDR2 NC	W14
PAD_IO[6]	DDR IO	DDR3 DRAM Memory Address [5] DDR2 DRAM Memory Address [9] LPDDR2 NC	W12
PAD_IO[7]	DDR IO	DDR3 DRAM Memory Address [7] DDR2 DRAM Memory Address [14] LPDDR2 NC	W13
PAD_IO[8]	DDR IO	DDR3 DRAM Memory Address [2] DDR2 DRAM Memory Address [3] LPDDR2 NC	V12
PAD_IO[9]	DDR IO	DDR3 DRAM Memory Address [9] DDR2 DRAM Memory Address [7] LPDDR2 NC	U13
PAD_IO[10]	DDR IO	DDR3 DRAM Memory Address [0] DDR2 DRAM Memory Address [10] LPDDR2 DRAM Memory Command/Address [8]	V11
PAD_IO[11]	DDR IO	DDR3 DRAM Memory Address [3] DDR2 DRAM Memory Address [5] LPDDR2 NC	U12
PAD_IO[12]	DDR IO	DDR3 DRAM Memory Bank Address [0] DDR2 DRAM Memory Address [1] LPDDR2 DRAM Memory Command/Address [9]	V10
PAD_IO[13]	DDR IO	DDR3 DRAM Memory Address [12] DDR2 Write Enable; Active Low LPDDR2 DRAM Memory Command/Address [6]	V9
PAD_IO[14]	DDR IO	DDR3 Write Enable; Active Low DDR2 DRAM Memory Bank Address [1] LPDDR2 NC	U10
PAD_IO[15]	DDR IO	DDR3 DRAM Memory Bank Address [2] DDR2 DRAM Memory Bank Address [2] LPDDR2 DRAM Memory Command/Address [7]	W10
PAD_IO[16]	DDR IO	DDR3 Column Address Strobe; Active Low DDR2 DRAM Memory Bank Address [0] LPDDR2 DRAM Memory Command/Address [5]	W9

Signal Name	Signal Type	Function	Pin Location
PAD_IO[17]	DDR IO	DDR3 DRAM Memory Address [14] DDR2 DRAM Memory Address [11] LPDDR2 DRAM Memory Command/Address [2]	V8
PAD_IO[18]	DDR IO	DDR3 DRAM Memory Address [1] DDR2 Column Address Strobe; Active Low LPDDR2 NC	U9
PAD_IO[19]	DDR IO	DDR3 DRAM Memory Address [15] DDR2 DRAM Memory Address [0] LPDDR2 NC	U6
PAD_IO[20]	DDR IO	DDR3 DRAM Memory Address [11] DDR2 DRAM Memory Address [13] LPDDR2 DRAM Memory Command/Address [4]	V7
PAD_IO[21]	DDR IO	DDR3 DRAM Memory Bank Address [1] DDR2 DRAM Memory Address [2] LPDDR2 DRAM Memory Command/Address [1]	V6
PAD_IO[22]	DDR IO	DDR3 DRAM Memory Address [8] DDR2 DRAM Memory Address [8] LPDDR2 DRAM Memory Command/Address [3]	W7
PAD_IO[23]	DDR IO	DDR3 DRAM Memory Address [10] DDR2 Row Address Strobe; Active Low LPDDR2 NC	V5
PAD_IO[24]	DDR IO	DRAM Clock Enable Control Signal	V15
PAD_IO[26]	DDR IO	DDR3 DRAM Memory Address [6] DDR2 DRAM Memory Address [6] LPDDR2 NC	U7
PAD_IO[27]	DDR IO	DDR3 DRAM Memory Address [4] DDR2 DRAM Memory Address [4] LPDDR2 DRAM Memory Command/Address [0]	W6
PAD_IO[28]	DDR IO	DRAM Memory Negative Differential Clock Signal	T13
PAD_IO[29]	DDR IO	DRAM Memory Positive Differential Clock Signal	T14
PAD_IO[30]	DDR IO	DDR3 DRAM Memory Data Bus [15] DDR2 DRAM Memory Data Bus [9] LPDDR2 DRAM Memory Data Bus [6]	R9
PAD_IO[31]	DDR IO	DDR3 DRAM Memory Data Bus [8] DDR2 DRAM Memory Data Bus [10] LPDDR2 DRAM Memory Data Bus [0]	T10
PAD_IO[32]	DDR IO	DDR3 DRAM Memory Data Bus [10] DDR2 DRAM Memory Data Bus [13] LPDDR2 DRAM Memory Data Bus [2]	T12

Signal Name	Signal Type	Function	Pin Location
PAD_IO[33]	DDR IO	DDR3 DRAM Memory Data Bus [11] DDR2 DRAM Memory Data Bus [12] LPDDR2 DRAM Input Data Mask [0]	R8
PAD_IO[34]	DDR IO	DDR3 DRAM Memory Data Bus [14] DDR2 DRAM Memory Data Bus [15] LPDDR2 DRAM Memory Data Bus [4]	R12
PAD_IO[35]	DDR IO	DDR3 DRAM Input Data Mask [1] DDR2 DRAM Memory Data Bus [11] LPDDR2 DRAM Memory Data Bus [1]	T11
PAD_IO[36]	DDR IO	DDR3 DRAM Memory Data Bus [12] DDR2 DRAM Memory Data Bus [8] LPDDR2 DRAM Memory Data Bus [3]	R11
PAD_IO[37]	DDR IO	DDR3 DRAM Memory Data Bus [13] DDR2 DRAM Memory Data Bus [14] LPDDR2 DRAM Memory Data Bus [5]	T7
PAD_IO[38]	DDR IO	DDR3 DRAM Data Strobe Inverse [1] DDR2 DRAM Data Strobe [1] LPDDR2 DRAM Data Strobe Inverse [0]	T8
PAD_IO[39]	DDR IO	DDR3 DRAM Data Strobe [1] DDR2 DRAM Data Strobe Inverse [1] LPDDR2 DRAM Data Strobe [0]	T9
PAD_IO[40]	DDR IO	DDR3 DRAM Memory Data Bus [9] DDR2 DRAM Input Data Mask [1] LPDDR2 DRAM Memory Data Bus [7]	R10
PAD_IO[41]	DDR IO	DDR3 DRAM Memory Data Bus [7] DDR2 DRAM Memory Data Bus [3] LPDDR2 DRAM Memory Data Bus [20]	V3
PAD_IO[42]	DDR IO	DDR3 DRAM Input Data Mask [0] DDR2 DRAM Memory Data Bus [7] LPDDR2 DRAM Memory Data Bus [23]	W4
PAD_IO[43]	DDR IO	DDR3 DRAM Memory Data Bus [5] DDR2 DRAM Memory Data Bus [2] LPDDR2 DRAM Memory Data Bus [16]	W3
PAD_IO[44]	DDR IO	DDR3 DRAM Memory Data Bus [1] DDR2 DRAM Memory Data Bus [0] LPDDR2 DRAM Memory Data Bus [17]	V4
PAD_IO[45]	DDR IO	DDR3 DRAM Memory Data Bus [0] DDR2 DRAM Input Data Mask [0] LPDDR2 DRAM Memory Data Bus [18]	U3

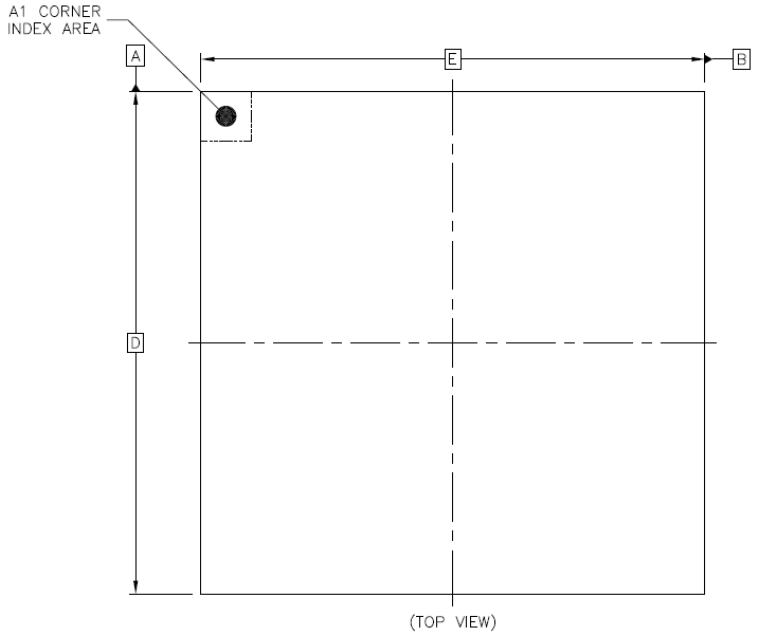
Signal Name	Signal Type	Function	Pin Location
PAD_IO[46]	DDR IO	DDR3 DRAM Memory Data Bus [6] DDR2 DRAM Memory Data Bus [1] LPDDR2 DRAM Memory Data Bus [21]	U2
PAD_IO[47]	DDR IO	DDR3 DRAM Memory Data Bus [4] DDR2 DRAM Memory Data Bus [4] LPDDR2 DRAM Input Data Mask [2]	U1
PAD_IO[48]	DDR IO	DDR3 DRAM Memory Data Bus [3] DDR2 DRAM Memory Data Bus [5] LPDDR2 DRAM Memory Data Bus [19]	U5
PAD_IO[49]	DDR IO	DDR3 DRAM Data Strobe [0] DDR2 DRAM Data Strobe Inverse [0] LPDDR2 DRAM Data Strobe [2]	V2
PAD_IO[50]	DDR IO	DDR3 DRAM Data Strobe Inverse [0] DDR2 DRAM Data Strobe [0] LPDDR2 DRAM Data Strobe Inverse [2]	W2
PAD_IO[51]	DDR IO	DDR3 DRAM Memory Data Bus [2] DDR2 DRAM Memory Data Bus [6] LPDDR2 DRAM Memory Data Bus [22]	V1
PAD_IO[52]	DDR IO	DDR3 DRAM Memory Data Bus [31] DDR2 DRAM Memory Data Bus [28] LPDDR2 DRAM Memory Data Bus [14]	P5
PAD_IO[53]	DDR IO	DDR3 DRAM Data Strobe Inverse [3] DDR2 DRAM Data Strobe [3] LPDDR2 DRAM Data Strobe Inverse [1]	R5
PAD_IO[54]	DDR IO	DDR3 DRAM Data Strobe [3] DDR2 DRAM Data Strobe Inverse [3] LPDDR2 DRAM Data Strobe [1]	T6
PAD_IO[55]	DDR IO	DDR3 DRAM Memory Data Bus [24] DDR2 DRAM Memory Data Bus [26] LPDDR2 DRAM Memory Data Bus [10]	R4
PAD_IO[56]	DDR IO	DDR3 DRAM Memory Data Bus [28] DDR2 DRAM Memory Data Bus [31] LPDDR2 DRAM Input Data Mask [1]	T5
PAD_IO[57]	DDR IO	DDR3 DRAM Memory Data Bus [29] DDR2 DRAM Memory Data Bus [25] LPDDR2 DRAM Memory Data Bus [15]	N5
PAD_IO[58]	DDR IO	DDR3 DRAM Memory Data Bus [25] DDR2 DRAM Memory Data Bus [27] LPDDR2 DRAM Memory Data Bus [9]	P4

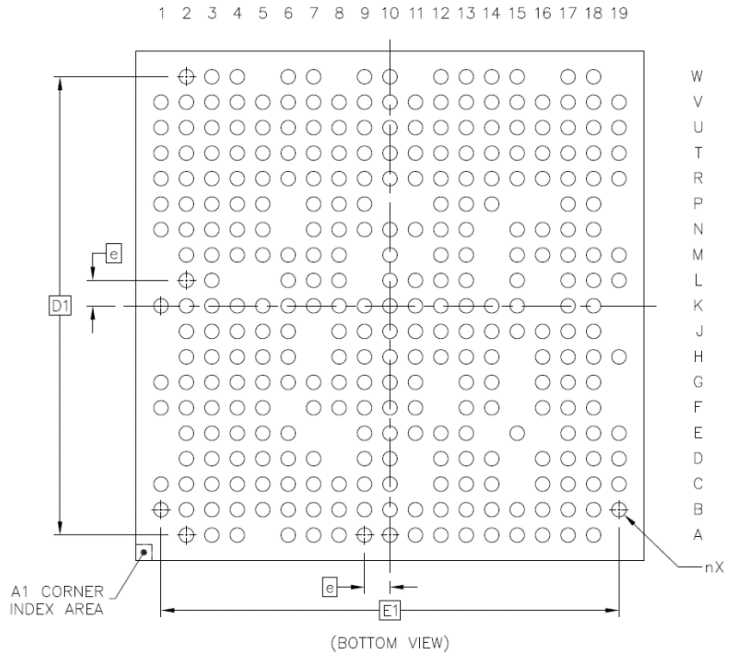
Signal Name	Signal Type	Function	Pin Location
PAD_IO[59]	DDR IO	DDR3 DRAM Memory Data Bus [30] DDR2 DRAM Memory Data Bus [24] LPDDR2 DRAM Memory Data Bus [8]	T4
PAD_IO[60]	DDR IO	DDR3 DRAM Input Data Mask [3] DDR2 DRAM Input Data Mask [3] LPDDR2 DRAM Memory Data Bus [13]	N4
PAD_IO[61]	DDR IO	DDR3 DRAM Memory Data Bus [26] DDR2 DRAM Memory Data Bus [29] LPDDR2 DRAM Memory Data Bus [12]	R3
PAD_IO[62]	DDR IO	DDR3 DRAM Memory Data Bus [27] DDR2 DRAM Memory Data Bus [30] LPDDR2 DRAM Memory Data Bus [11]	M4
PAD_IO[63]	DDR IO	DDR3 DRAM Input Data Mask [2] DDR2 DRAM Memory Data Bus [23] LPDDR2 DRAM Memory Data Bus [26]	T1
PAD_IO[64]	DDR IO	DDR3 DRAM Data Strobe [2] DDR2 DRAM Data Strobe Inverse [2] LPDDR2 DRAM Data Strobe [3]	P2
PAD_IO[65]	DDR IO	DDR3 DRAM Data Strobe Inverse [2] DDR2 DRAM Data Strobe [2] LPDDR2 DRAM Data Strobe Inverse [3]	P1
PAD_IO[66]	DDR IO	DDR3 DRAM Memory Data Bus [19] DDR2 DRAM Memory Data Bus [21] LPDDR2 DRAM Input Data Mask [3]	T2
PAD_IO[67]	DDR IO	DDR3 DRAM Memory Data Bus [23] DDR2 DRAM Memory Data Bus [19] LPDDR2 DRAM Memory Data Bus [31]	P3
PAD_IO[68]	DDR IO	DDR3 DRAM Memory Data Bus [17] DDR2 DRAM Memory Data Bus [16] LPDDR2 DRAM Memory Data Bus [29]	R2
PAD_IO[69]	DDR IO	DDR3 DRAM Memory Data Bus [16] DDR2 DRAM Input Data Mask [2] LPDDR2 DRAM Memory Data Bus [27]	N2
PAD_IO[70]	DDR IO	DDR3 DRAM Memory Data Bus [21] DDR2 DRAM Memory Data Bus [18] LPDDR2 DRAM Memory Data Bus [25]	R1
PAD_IO[71]	DDR IO	DDR3 DRAM Memory Data Bus [18] DDR2 DRAM Memory Data Bus [22] LPDDR2 DRAM Memory Data Bus [30]	N3

Signal Name	Signal Type	Function	Pin Location
PAD_IO[72]	DDR IO	DDR3 DRAM Memory Data Bus [20] DDR2 DRAM Memory Data Bus [20] LPDDR2 DRAM Memory Data Bus [28]	M3
PAD_IO[73]	DDR IO	DDR3 DRAM Memory Data Bus [22] DDR2 DRAM Memory Data Bus [17] LPDDR2 DRAM Memory Data Bus [24]	M2
Power Pins			
VDD	Core Power	Digital Core Power	F7, G7, G8, H8, H9, H10, H11, H12, H13, H14, J8, J9, J10, J11, J12, J13, K9, K10, K11, K12
VDDP_0	3.3V Power	Digital Input/Output Power for Domain 0	F8
VDDP_1	3.3V/1.8V Power	Digital Input/Output Power for Domain 1	H16
VDDP_2A	3.3V/1.8V Power	Digital Input/Output Power for Domain 2A (Sensor IO Group 0 Power)	F16
VDDP_2B	3.3V/1.8V Power	Digital Input/Output Power for Domain 2B (Sensor IO Group 1 Power)	G16
DVDD_DDR_RX	Core Power	Digital Power for DDR RX LDO (0.1uF CAP to GND)	L8
DVDD_DDR	Core Power	Digital Power for DDR TX	M10
VDDIO_DATA	DDR Power	IO Power for DDR Data	M7, M8, N7, N8
VDDIO_MCLK	DDR Power	IO Power for DDR Clock	N10
VDDIO_CMD	DDR Power	IO Power for DDR Command	N11, N12
AVDDL_MIPI	Core Power	Analog LV Power for MIPI RX (could be shared with VDD)	G14
AVDD1P2_MIPI	O	LDO Output for MIPI TX (0.1uF Cap To GND)	E15
AVDD_NODIE	3.3V Power	Analog Power for PM Domain	M15
DVDD_NODIE	O	PM Domain LDO Output (1uF Cap to GND)	M16
AVDD1P8_SPI	O	PM SPI Domain LDO Output (1uF Cap to GND)	N16
	3.3V Power	IO Power for PM Flash Domain Signal	
AVDD_PLL	3.3V Power	Analog Power for PLL	L7
AVDD_XTAL	3.3V Power	Analog Power for XTAL	E11
AVDD_RTC	3.3V Power	Analog Power for RTC	H19
AVDD_USB	3.3V Power	Analog Power for USB	K8
AVDD3P3_USB	3.3V Power	Analog Power for USB2.0	K7

Signal Name	Signal Type	Function	Pin Location
AVDD_ETH	3.3V Power	Analog Power for Ethernet	G6
AVDD_AUD	3.3V Power	Analog Power for Audio	L6
AVSS_XTAL_RTC	GND	Analog Ground for RTC Crystal	G18
GND	GND	Ground	A7, C3, C6, C7, C8, C14, D6, D7, D14, E2, E6, F1, F3, F11, F14, G9, G10, G11, G13, H6, J6, J14, J15, J16, K2, K4, K6, K13, K14, K15, L2, L3, L10, L11, L12, L13, L15, M5, M6, M12, M13, N1, N9, N13, N15, P7, P8, P9, P12, P13, P14, R6, R7, R13, R14, R15, T3, T16, U4, U8, U11, U14

4.3. Mechanical Dimensions





	Symbol	Common Dimensions		
		MIN.	NOR.	MAX.
Total Thickness	A	1.42	1.49	1.56
Stand Off	A1	0.22	0.27	0.32
Body Size	D	13 BSC		
	E	13 BSC		
Ball Diameter		0.35		
Ball Pitch	e	0.65 BSC		
Ball Count	n	307		
Edge Ball Center to Center	D1	11.7 BSC		
	E1	11.7 BSC		

5. ELECTRICAL CHARACTERISTIC

5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
Core Power Supply Voltage	VDD	-0.3		1.26	V
3.3V I/O Supply Voltage	VDDP_0 VDDP_1	-0.3		3.63	V
1.8~3.3V I/O Supply Voltage	VDDP_2A VDDP_2B AVDD1P8_SPI	-0.3		3.63	V
DDR Digital Power Supply Voltage	DVDD_DDR*	-0.3		1.26	V
DDR IO Power Supply Voltage (DDR3/L)	VDDIO_* AVDD*_DRAM	-0.3		1.8	V
DDR IO Power Supply Voltage (LPDDR2)	VDDIO_* AVDD1_DRAM	-0.3 -0.3		1.6 2.3	V V
PM IO Power Supply Voltage	AVDD_NODIE	-0.3		3.63	V
3.3V Analog Power Supply Voltage	AVDD*	-0.3		3.63	V
0.9V Analog Power Supply Voltage	AVDDL*	-0.3		1.26	V
Storage Temperature	T_{STG}	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

5.2. Recommended Operating Conditions

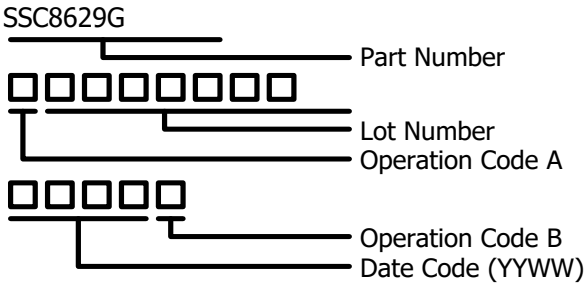
Parameter	Description	Min.	Typ.	Max	Unit
VDD	Digital Core Power	0.825	0.9	1.05	V
VDDP_0	Digital Input/Output Power for Domain 0	2.97	3.3	3.63	V
VDDP_1	Digital Input/Output Power for Domain 1	2.97	3.3	3.63	V
VDDP_2A	Digital Input/Output Power for Domain 2A (Sensor IO Group 0 Power)	2.97	3.3	3.63	V
	Digital Input/Output Power for Domain 2A (Sensor IO Group 0 Power)	1.62	1.8	1.98	V
VDDP_2B	Digital Input/Output Power for Domain 2B (Sensor IO Group 1 Power)	2.97	3.3	3.63	V
	Digital Input/Output Power for Domain 2B (Sensor IO Group 1 Power)	1.62	1.8	1.98	V
DVDD_DDR_RX	Digital Power for DDR RX LDO (0.1uF CAP to GND)	TBD	0.9	TBD	V
DVDD_DDR	Digital Power for DDR TX	TBD	0.9	TBD	V
VDDIO_DATA	(DDR3) IO Power for DDR Data	1.45	1.5	1.55	V
	(DDR3L) IO Power for DDR Data	1.3	1.35	1.45	V
	(LPDDR2) IO Power for DDR Data	1.14	1.2	1.26	V
	(DDR2) IO Power for DDR Data	1.71	1.8	1.89	V
VDDIO_MCLK	(DDR3) IO Power for DDR Clock	1.45	1.5	1.55	V
	(DDR3L) IO Power for DDR Clock	1.3	1.35	1.45	V
	(LPDDR2) IO Power for DDR Clock	1.14	1.2	1.26	V
	(DDR2) IO Power for DDR Clock	1.71	1.8	1.89	V
VDDIO_CMD	(DDR3) IO Power for DDR Command	1.45	1.5	1.55	V
	(DDR3L) IO Power for DDR Command	1.3	1.35	1.45	V
	(LPDDR2) IO Power for DDR Command	1.14	1.2	1.26	V
	(DDR2) IO Power for DDR Command	1.71	1.8	1.89	V
AVDDL_MIPI	Analog LV Power for MIPI RX (could be shared with VDD)	TBD	0.9	TBD	V
AVDD1P2_MIPI	LDO Output for MIPI TX (0.1uF Cap To GND)	TBD	0.9	TBD	V
AVDD_NODIE	Analog Power for PM Domain	2.97	3.3	3.63	V
DVDD_NODIE	PM Domain LDO Output (1uF Cap to GND)	TBD	0.9	TBD	V
AVDD1P8_SPI	PM SPI Domain LDO Output (1uF Cap to GND)	TBD	1.8	TBD	V
	External power supply for 3.3V IO	2.97	3.3	3.63	V
AVDD_PLL	Analog Power for PLL	3.14	3.3	3.46	V

Parameter	Description	Min.	Typ.	Max	Unit
AVDD_XTAL	Analog Power for XTAL	3.14	3.3	3.46	V
AVDD_RTC	Analog Power for RTC	1.6	3	3.6	V
AVDD_POC	Analog Power for POC	1.6	3	3.6	V
AVDD_USB	Analog Power for USB	3.14	3.3	3.46	V
AVDD3P3_USB	Analog Power for USB2.0	3.14	3.3	3.46	V
AVDD_ETH	Analog Power for Ethernet	3.14	3.3	3.46	V
AVDD_AUD	Analog Power for Audio	3.14	3.3	3.46	V
Junction Temperature				125	°C

6. ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
SSC8629G	-40°C to +85°C	BGA	307

6.1. Marking Information



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. SSC8629G comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.