SSW105

Dual-band IEEE802.11a/b/g/n 1T1R Wireless Network Controller with USB/SDIO Interface

Data Sheet Version 1.0

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

REVISION HISTORY

Revision No.	Description	Date
1.0	• Initial release	07/22/2020

1. OVERVIEW

1.1. General Descriptions

The SSW105 is a low-power single chip device with the highest level of integration for the internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54Mbps, as well as 802.11n MCS0~MCS7, HT20/HT40, 800ns and 400ns guard interval.

It includes a dual-band WLAN CMOS efficient power amplifier (PA) and an internal low noise amplifier (LNA). The Radio Frequency Front-end is single-ended bi-directional input and output.

The SSW105 has additional LDOs and DCDC buck convertors that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

While they both provide multiple peripheral interfaces including SPI_ MASTER, UART_DATA, UART_DEBUG, I2C_MASTER, I2S, etc.

The only external clock source needed for SSW105 based designs is a high-speed crystal or oscillator. SSW105AT only supports two reference clocks which are 25MHz and 40MHz. SSW105BT support a variety of reference clocks which include 19.2, 20, 24, 25, 26, 38.4, 40 and 52MHz.

SSW105 series include:

- SSW105AT (USB interface)
- SSW105BT (SDIO interface)

1.2. Block Diagram

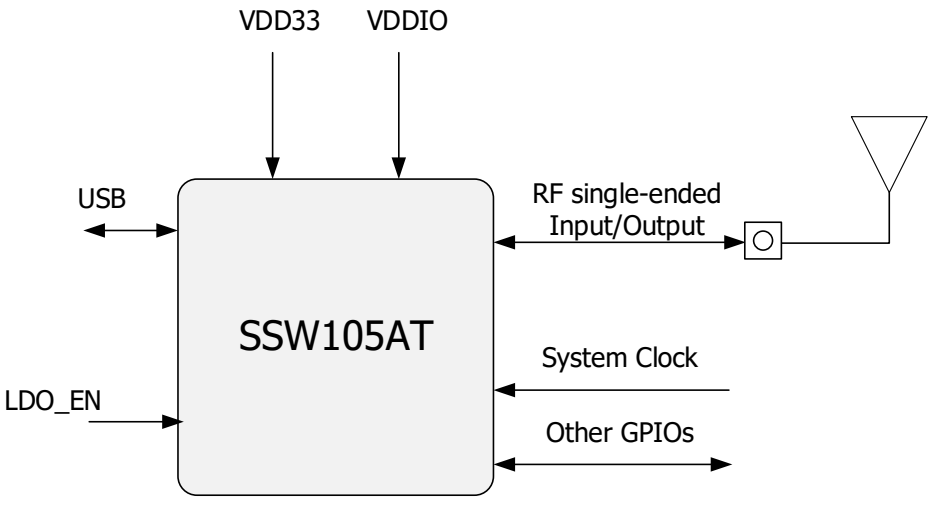


Figure 1-1: SSW105AT System Block Diagram

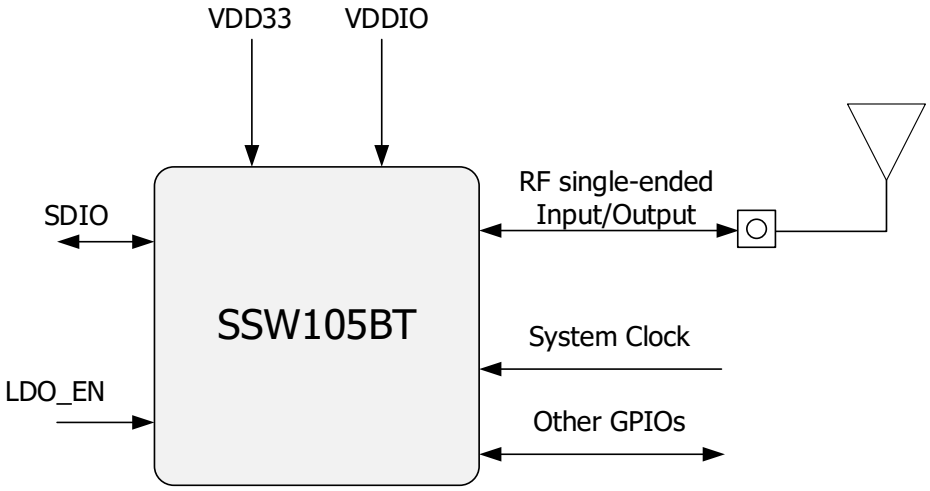


Figure 1-2: SSW105BT System Block Diagram

1.3. SSW105AT/SSW105BT Feature List

- IEEE 802.11 a/b/g/n
- Embedded high-performance 32-bit Andes Technology N10 processor w/ ILM/DLM and I-cache
- Highly integrated RF with CMOS technology
- WLAM MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip
- Integrated PA, LNA
- Support A-MPDU transmit and receive for throughput improvement
- Advanced 1x1 802.11n features:
  - Full / Half Guard Interval
  - Frame Aggregation
  - Space-Time Block Coding (STBC)
  - Greenfield mode
- Supports both 20MHz and 40MHz bandwidth transmission
- QFN-48, 6x6mm^2, 0.4mm pitch
- Security support Hardware Crypto Engine for Advanced Fast Security, Including WEP, TKIP, WPA,WPA2
- Supports STA and AP mode

2. PIN INFORMATION

2.1. Pin Map

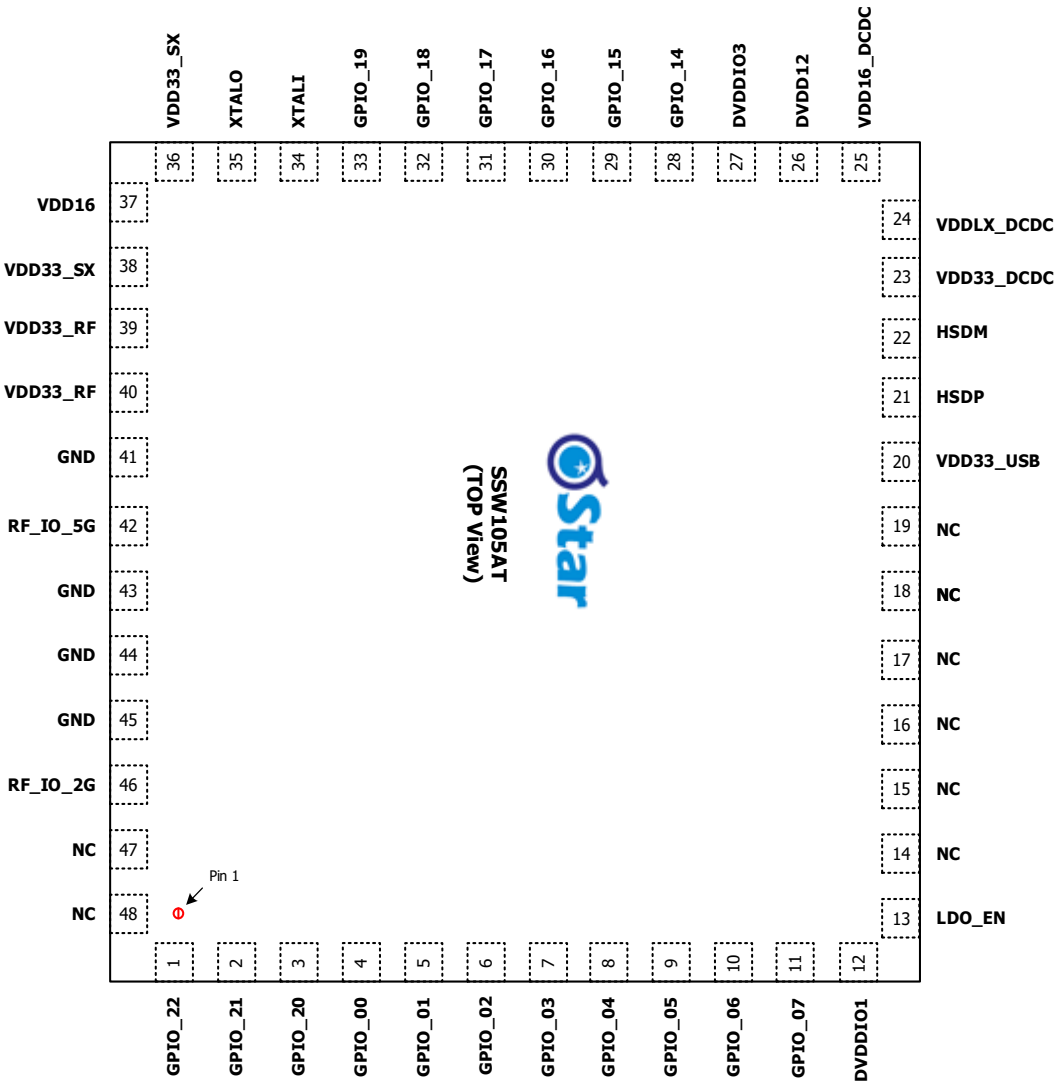


Figure 2-1: SSW105AT QFN Pin Assignment (top view)

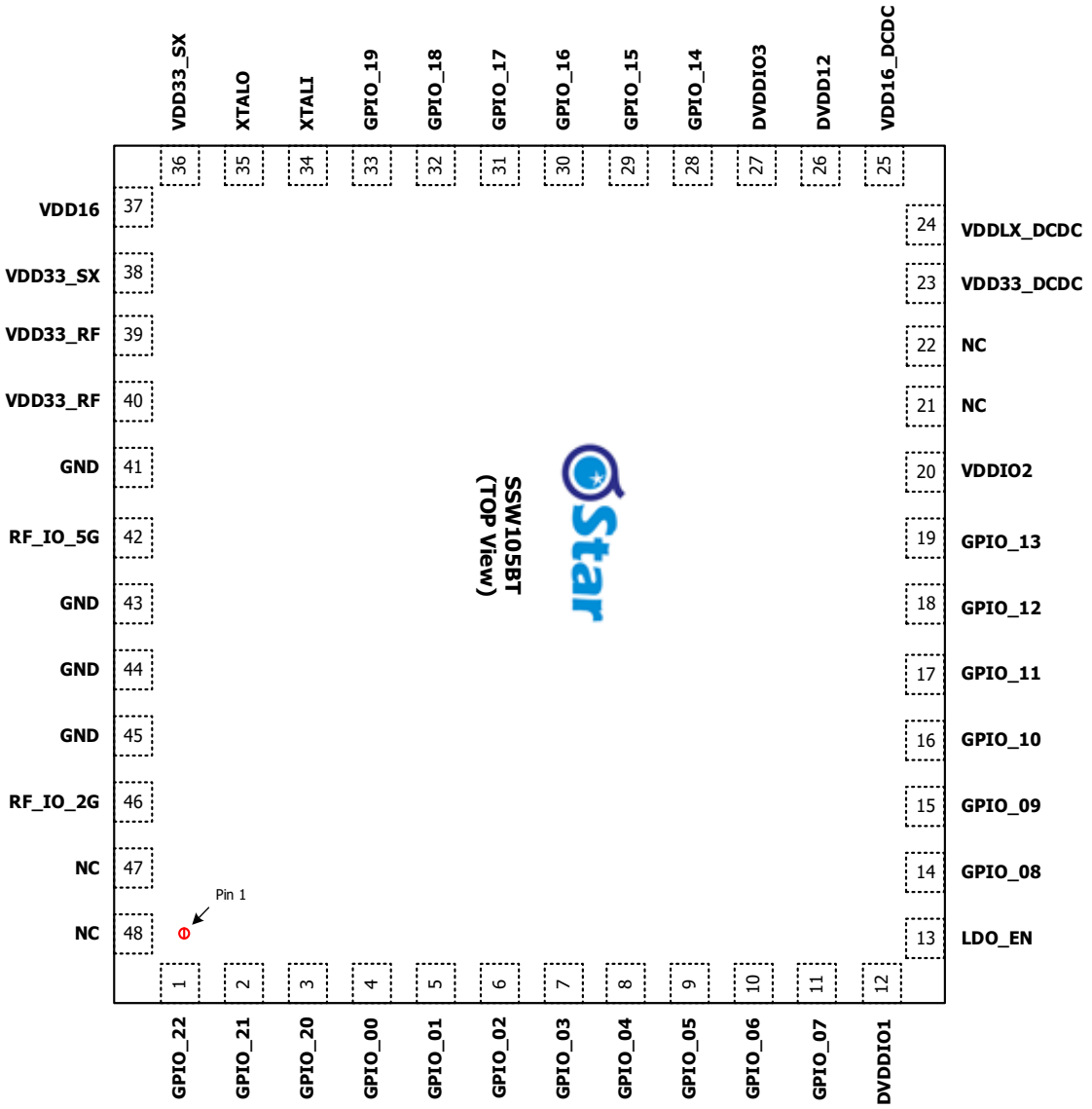


Figure 2-2: SSW105BT QFN Pin Assignment (top view)

2.2. Pin Table

Table 2-1: SSW105 Pin Table

Pin Name	Pin Description	Type	Pin Location
GPIO_22	General Purpose I/O Pins	I/O	1
GPIO_21	General Purpose I/O Pins	I/O	2
GPIO_20	Strapping Purpose I/O Pins	I/O	3
GPIO_00	General Purpose I/O Pins	I/O	4
GPIO_01	General Purpose I/O Pins	I/O	5
GPIO_02	General Purpose I/O Pins	I/O	6

Pin Name	Pin Description	Type	Pin Location
GPIO_03	General Purpose I/O Pins	I/O	7
GPIO_04	General Purpose I/O Pins	I/O	8
GPIO_05	General Purpose I/O Pins	I/O	9
GPIO_06	General Purpose I/O Pins	I/O	10
GPIO_07	Strapping Purpose I/O Pins	I/O	11
DVDD1O1	VIO input for GPIO00~07/GPIO20~22	Power	12
LDO_EN	Reset signal to power down IC	Input	13
GPIO_08	General Purpose I/O Pins(NC pin SSW105BT)	I/O	14
GPIO_09	General Purpose I/O Pins(NC pin SSW105BT)	I/O	15
GPIO_10	General Purpose I/O Pins(NC pin SSW105BT)	I/O	16
GPIO_11	General Purpose I/O Pins(NC pin SSW105BT)	I/O	17
GPIO_12	General Purpose I/O Pins(NC pin SSW105BT)	I/O	18
GPIO_13	General Purpose I/O Pins(NC pin SSW105BT)	I/O	19
DVDD1O2	VIO input for GPIO08~13/HSDP/HSDM	Power	20
HSDP	HSDP (NC pin @ SSW105BT)	I/O	21
HSDM	HSDM (NC pin @ SSW105BT)	I/O	22
VDD33_DCDC	analog 3.3V input for DCDC	Power	23
VDDLX_DCDC	DCDC buck regulator: output to the inductor	Power	24
VDD16_DCDC	DCDC 1.6V	Power	25
DVDD12	Digital 1.2V input	Power	26
DVDDIO3	VIO input for GPIO14~19	Power	27
GPIO14	Strapping Purpose I/O Pins	I/O	28
GPIO15	Strapping Purpose I/O Pins	I/O	29
GPIO16	General Purpose I/O Pins	I/O	30
GPIO17	General Purpose I/O Pins	I/O	31
GPIO18	General Purpose I/O Pins	I/O	32
GPIO19	General Purpose I/O Pins	I/O	33
XTALI	The input of crystal clock reference	Input	34
XTALO	The output of crystal clock reference	Output	35
VDD33_SX	analog 3.3V input	Power	36
VDD16	analog 1.6V input	Power	37
VDD33_SX	analog 3.3V input	Power	38
VDD33_RF	analog 3.3V input	Power	39
VDD33_RF	analog 3.3V input	Power	40
GND	Ground	GND	41
RF_IO_5G	5 GHz RF input & output port	RF I/O	42
GND	Ground	GND	43
GND	Ground	GND	44
GND	Ground	GND	45
RF_IO_2G	2.4 GHz RF input & output port	RF I/O	46
NC	NC Pin	RF I/O	47
NC	NC Pin	NC	48

3. ELECTRICAL CHARACTERISTICS

3.1. Recommended Operating conditions

Table 3-1: Recommended Operating Ratings

Domain (Symbol)	Description	Min	Typ	Max	Unit
VDD16	VDD input for analog 1.6V		1.6		V
VDD33_SX	VDD input for external components I/O control	2.1	3.3	3.46	V
VDD33_RF	VDD input for external components I/O control	2.1	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO2	VDD input for GPIO pins (same level as DVDDIO1)	1.75	3.3	3.46	V
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16_DCDC	VDD input for digital circuit's LDO		1.6		V
VDD33_DCDC	VDD input for DCDC	2.1	3.3	3.46	V
VDD33	VDD input	3.13	3.3	3.46	V
(V_{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
(V_{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
(V_{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.6	1.74	1.89	V
(V_{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.27	1.4	1.56	V
(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option				kΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option				kΩ
(I_{OL})	Low level output current @ V_{OL}(max), 8mA setting	11.9	17.7	23.4	mA

Domain (Symbol)	Description	Min	Typ	Max	Unit
	Low level output current @ V_{OL}(max), 12mA setting	15.8	23.5	31.1	mA
(I_{OH})	High-level output current @ V_{OH}(min), 8mA setting	17.2	34.1	58.8	mA
	High-level output current @ V_{OH}(min), 12mA setting	23.9	47.2	81.5	mA

Note: The voltage of VDDIO is depended on the system I/O voltage.

3.2. Thermal Data

Thermal characteristics without an external heat sink in still air condition

Table 3-2: The thermal characteristics of the SSW105

Symbol	Description	Typ.	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	37.8	°C/W
θ_{JC}	Thermal Resistance θ_{JC} (°C /W) for JEDEC 4L system PCB	TBD	°C/W
Ψ_{Jt}	Thermal Characterization parameter Ψ_{Jt} (°C /W) for JEDEC 4L system PCB	4.13	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes:

- JEDEC 51-7 system FR4 PCB size: 3” x 4.5” (76.2 x 114.3 mm)
- Thermal characteristics without an external heat sink in still air condition

3.3. DC Electrical Specifications

3.3.1. Absolute Maximum Ratings

The absolute maximum ratings in Table 3-3 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect the long-term reliability of the device.

Table 3-3: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
VDD16	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33_RF	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for I/O	-0.3 to 3.6	V
DVDDIO3	VDD input for I/O	-0.3 to 3.6	V

Symbol (domain)	Description	Max Rating	Unit
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16_DCDC	VDD input for digital circuit's LDO	-0.3 to 3.6	V
VDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V
VDD33_USB	VDD input for I/O	-0.3 to 3.6	V

3.3.2. Environmental conditions

The environmental ratings are shown in Table 3-4.

Table 3-4: Environmental Ratings

	Part Number	Value	Units
Operating Temperature(T_A)	SSW105AT	-40 to +85	°C
	SSW105BT	-40 to +85	

The calculated shelf life in a sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high-temperature processes must be handled in the following manner:

a) Mounted within 168-hours of factory conditions < 30 **°C** /60%RH

b) Storage humidity needs to maintained at <10% RH

c) Baking is necessary if customer exposes the component to air over 168 hrs, baking condition: 125°C / 8hrs

3.3.3. Electrostatic Discharge Specifications

This is an ESD sensitive product. Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 3-5: ESD Specifications

Pin Type	Test Condition	ESD Rating	Unit
Human Body Mode (HBM)	refers to MIL-STD-883G Method 3015.7	Pass ±2.5	kV
Charged Device Model(CDM)	JEDEC –500 +500 V specification JESD22-C101, all pins	Pass ±500	V

3.3.4. Power-On Hours(POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under iComm's standard terms and conditions for iComm semiconductor products.

Table 3-6: Power-On Hours

Operation Condition	Part Number	Power-On Hours(POH)(hours)
T_A up to 85**°C** [a]	SSW105AT	87600

Operation Condition	Part Number	Power-On Hours(POH)(hours)
T_A up to 85°C [a]	SSW105BT	

The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

3.4. Requirements to Peripheral Circuits

Table 3-7: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm

Table 3-8: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	1500	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11a/b/g)	26MHz clock at 1kHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10kHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100kHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4/5GHz)	26MHz clock at 1kHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10kHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100kHz offset	–	–	–140	dBc/Hz

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

3.5. RF Performance

3.5.1. RF Performance Diagram

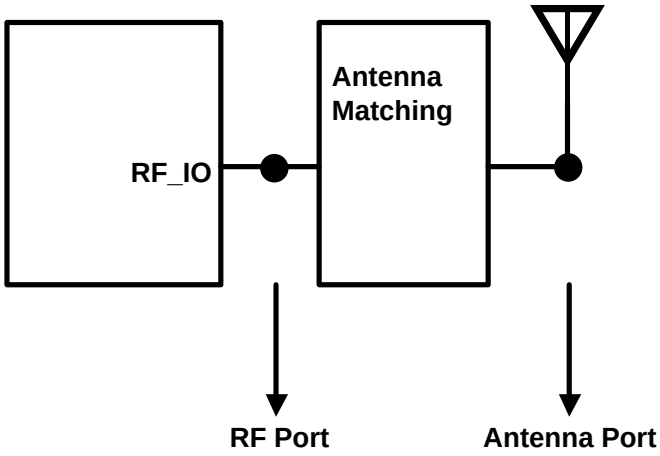


Figure 3-1: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the RF Port unless otherwise specified.

3.5.2. WLAN RF Performance Specifications

Table 3-9: 2.4G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-95.5		dBm
	CCK, 2 Mbps		-93.5		dBm
	CCK, 5.5 Mbps		-91.0		dBm
	CCK, 11 Mbps		-88.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.0		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity (HT20) Greenfield	HT20, MCS0		-91.0		dBm
	HT20, MCS1		-88.0		dBm
	HT20, MCS2		-86.0		dBm

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
800nS GI Non-STBC	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.5		dBm
	HT20, MCS7		-72.5		dBm
RX Adjacent Channel Rejection (CCK)	CCK, 1 Mbps (30 MHz offset)		41		dB
	CCK, 11 Mbps (25 MHz offset)		41		dB
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (25 MHz offset)		39		dB
	OFDM, 54 Mbps (25 MHz offset)		23		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (25 MHz offset)		38		dB
	HT20, MCS7 (25 MHz offset)		21		dB
TX Output Power (with PADPD)	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		16		dBm
	HT20, MCS7		15		dBm

Table 3-10: 5G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		5180	-	5850	MHz
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.0		dBm
	OFDM, 9 Mbps		-89.5		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity Greenfield 800nS GI Non-STBC	HT20, MCS0		-90.0		dBm
	HT20, MCS1		-87.5		dBm
	HT20, MCS2		-85.5		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.0		dBm
	HT20, MCS7		-72.0		dBm
	HT40, MCS0		-87.0		dBm
	HT40, MCS7		-68.5		dBm

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (20 MHz offset)		28		dB
	OFDM, 54 Mbps (20 MHz offset)		19		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (20 MHz offset)		27		dB
	HT20, MCS7 (20 MHz offset)		6		dB
TX Output Power (with PADPD)	OFDM, 54 Mbps		13.5		dBm
	HT20, MCS7		13		dBm
	HT40, MCS7		13		dBm

3.6. Power-on Sequence

Figure 3-2 shows the power-on sequence of the SSW105 from power-up to firmware download, including the initial device power-on reset evoked by the LDO_EN signal. The LDO_EN input level must be kept the same as the VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SSW105 or pulsed low to induce a subsequent reset. After LDO_EN is asserting and the host starts the power-on sequence of the SSW105. From that point, the typical SSW105 power-on sequence is shown below:

1. Within 1.3 milliseconds, the internal power-on reset (POR) will be done. And host could download the firmware code of DPLL setting if the crystal is not the default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, the host could set internal clock to full speed and finish all the downloading of firmware code.

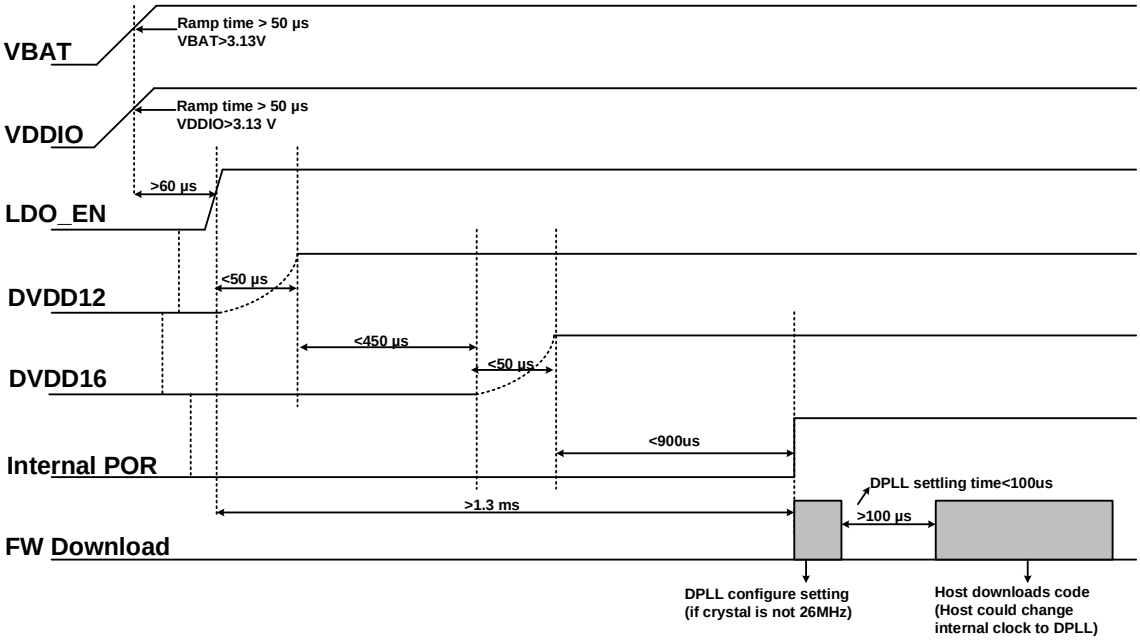


Figure 3-2: Power-on sequence

3.7. Reset Control

The SSW105 LDO_EN pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SSW105 is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SSW105 turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

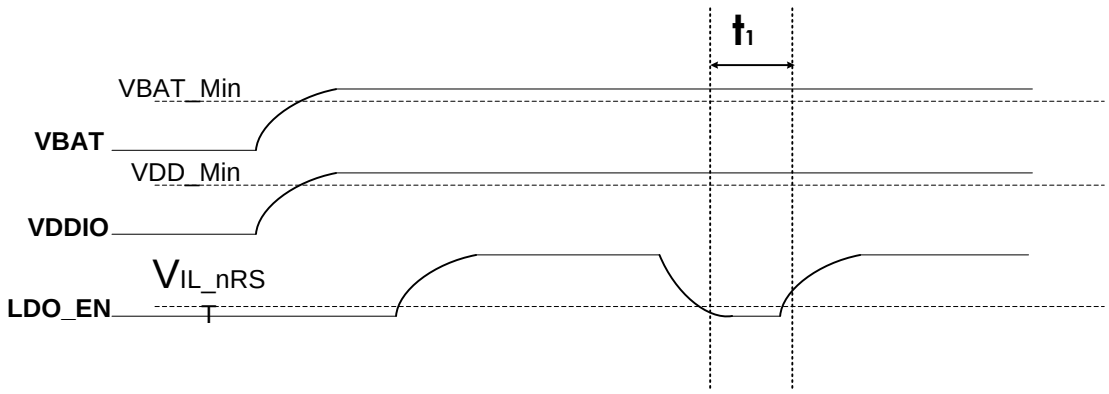


Figure 3-3 : Reset Timing

Table 3-11 : Reset Timing Parameters

Parameters	Description	Min.	Unit
t_1	Duration of LDO_EN signal level < V_{IL}_nRST to reset the chip	30	us

3.8. System Power Consumption

Table 3-12: Power Consumption at DCDC mode (DCDC buck convertor is enabled)

WLAN Operational Modes	Typ.[d]	Unit
OFFa	2	uA
Rx, CCK, 1 Mbps	68	mA
Rx, OFDM, 54 Mbps	68	mA
Rx, HT20, MCS7	68	mA
Rx, HT40, MCS7	75	mA
Rx, 5.18G HT20, MCS7	88	mA
Rx, 5.805G HT20, MCS7	88	mA
Rx, 5.18 G HT40, MCS7	97	mA
Rx, 5.805G HT40, MCS7	97	mA
Tx, CCK, 1 Mbps	307	mA
Tx, OFDM, 54 Mbps@15dBm	256	mA
Tx, HT20, MCS7@15dBm	260	mA

WLAN Operational Modes	Typ.[d]	Unit
Tx, HT40, MCS7@15dBm	260	mA
Tx, 5.18　G HT20, MCS7	310	mA
Tx, 5.805G HT20, MCS7	293	mA

Table 3-13: Power Consumption at LDO mode (DCDC buck convertor is disabled)

WLAN Operational Modes	Typ.[d]	Unit
OFFa	2	uA
Rx, CCK, 1 Mbps	113	mA
Rx, OFDM, 54 Mbps	113	mA
Rx, HT20, MCS7	113	mA
Rx, HT40, MCS7	124	mA
Rx, 5.18G HT20, MCS7	133	mA
Rx, 5.805G HT20, MCS7	133	mA
Rx, 5.18　G HT40, MCS7	142	mA
Rx, 5.805G HT40, MCS7	142	mA
Tx, CCK, 1 Mbps@18dBm	328	mA
Tx, OFDM, 54 Mbps@15dBm	280	mA
Tx, HT20, MCS7@15dBm	283	mA
Tx, HT40, MCS7@15dBm	285	mA
Tx, 5.18　G HT20, MCS7	356	mA
Tx, 5.805G HT20, MCS7	335	mA

a. OFF mode test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V.

b. Intra-beacon Sleep when MCU is turn on.

c. It is used in the applications that require the CPU to be working.

d. Intra-beacon Sleep when MCU is turn off.

e. Conditions: VBAT at 3.3v, VDDIO at 3.3V, 25°C.

4. PERIPHERAL INTERFACE

4.1. GPIO interface

SSW105AT has fifteen GPIO pins(twenty-four GPIO pins@SSW105BT), which can be assigned as different functions by registers setting. When these pins are used as GPIO, they may be assigned as High/Low voltage level input/output and high impedance. When these GPIO pins are used as GPIO input, High/Low input voltage levels on GPIOs can be read by registers to trigger CPU interruption.

4.1.1. Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 2-1 / Figure 2-2 for the SSW105 QFN package pin-out).

The following nomenclature is used for signal names:

Name	Description
NC	No connection should be made to this pin
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name, indicates the negative side of a differential signal

4.1.2. Interface Selection

SSW105 has bootstrap pins to select interface which including debug interface, the host I/O. There are GPIO07, GPIO14, GPIO15, and GPIO20 (see Table 4-1 for detail). The bootstrap pin of GPIO07 decides to switch the debug interface (ICE or SPI DEBUG slave) out to GPIOs (see Table 4-2 for detail). The bootstrap pins of GPIO14 and GPIO15 decode switch the host IO (USB/SDIO) out to GPIOs (see Table 4-3/ Table 4-4 for detail). The bootstrap pin of GPIO20 decides to switch 25MHz or 40MHz clock when using the USB interface.

Table 4-1: The strapping truth table

	Interface mode	Description
GPIO[07]		
0	ICE debug	for ICE debug interface
1	SPI debug	for SPI debug interface (default)
GPIO[15], GPIO[14]		
00	SPIFL-E	SPI flash w/I in-place execution (default)
01	SPIDATA	SPI data mode
10	SDIO	SDIO mode
11	USB	USB mode
GPIO[20]		

	Interface mode	Description
0	USB_XO25M	for USB 25MHz clock (default)
1	USB_XO40M	for USB 40MHz clock

Table 4-2: The strapping pin of GPIO07

GPIO07		Low			High		
Pin No.	Name	I/O	PULL	I/O Function	I/O	PULL	I/O Function
4	GPIO00	I/O	F	TMSC	I/O	F	GPIO00
5	GPIO01	I	F	TCKC	I	F	SPI1_S_CLK
6	GPIO02	I	PU	nSRST	I	PU	SPI1_S_CSN
7	GPIO03	I	F	UART0_RXD	I	F	SPI1_S_MOSI
8	GPIO04	O	F	UART0_TXD	O	F	SPI1_S_MISO

Table 4-3: The strapping pin of GPIO14/15 for SDIO interface

GPIO15/14		2'b10		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**
9	GPIO05	O	F	GPIO05
10	GPIO06	I	F	UART1_RXD
11	GPIO07	O	PU	UART1_TXD
14	GPIO08	I/O	F	SD_D2
15	GPIO09	I	F	SD_D3
16	GPIO10	I/O	F	SD_CMD
17	GPIO11	I/O	F	SD_CLK
18	GPIO12	I/O	F	SD_D0
19	GPIO13	O	F	SD_D1
28	GPIO14	I/O	F	GPIO14
29	GPIO15	O	F	GPIO15
30	GPIO16	I/O	F	GPIO16
31	GPIO17	O	F	GPIO17
32	GPIO18	I/O	F	GPIO18
33	GPIO19	I/O	F	GPIO19
3	GPIO20	I/O	F	WIFI_WAKE_HOST
2	GPIO21	I	F	HOST_WAKE_WIFI
1	GPIO22	I/O	F	WIFI_CLK_REQ

Table 4-4: The strapping pin of GPIO14/15 for USB slave interface

GPIO15/14		2'b11		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**
9	GPIO05	O	F	UART1_RTS

GPIO15/14		2'b11		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**
10	GPIO06	I	F	UART1_RXD
11	GPIO07	O	PU	UART1_TXD
14	GPIO08	O	F	GPIO08
15	GPIO09	I	F	UART1_CTS
16	GPIO10	I	F	GPIO10
17	GPIO11	I	F	GPIO11
18	GPIO12	O	F	GPIO12
19	GPIO13	I	F	GPIO13
28	GPIO14	I/O	F	GPIO14
29	GPIO15	I/O	F	GPIO15
30	GPIO16	I/O	F	GPIO16
31	GPIO17	I/O	F	GPIO17
32	GPIO18	I/O	F	GPIO18
33	GPIO19	I/O	F	GPIO19
3	GPIO20	O	F	WIFI_WAKE_HOST(GPIO20)
2	GPIO21	I	F	HOST_WAKE_WIFI(GPIO21)
1	GPIO22	O	F	WIFI_CLK_REQ(RTC_RDY_V12D)

4.1.3. User Define I/O Function Selection

After bootstrap, the SSW105 also provides a pad multiplex switching from the bootstrap function to selected I/O function by register signals. There is a condition to leave the bootstrap function. That is switching to GPIO first then switching to select I/O function.Table 4-5 shows all I/O functions for each PAD.

Table 4-5: The PAD multiplex for each PAD

Pin No.	Pin Name	Alternate Functions		
4	GPIO00	strapping function		
		I/O	U	GPIO[00]
		O	F	gpo_int
		O	F	PWM0
		O	F	WIFI_TX_SW
5	GPIO01	strapping function		
		I/O	U	GPIO[01]
		O	F	gpo_int
		O	F	PWM1
		O	F	WIFI_RX_SW
6	GPIO02	strapping function		
		I/O	U	GPIO[02]
		O	F	gpo_int
		O	F	PWM2

Pin No.	Pin Name	Alternate Functions		
		O	F	BT_SW
7	GPIO03	strapping function		
		I/O	U	GPIO[03]
		O	F	gpo_int
		O	F	PWM3
		I	F	BT_PRIORITY
		I	F	UART0_RXD
8	GPIO04	strapping function		
		I/O	U	GPIO[04]
		O	F	gpo_int
		O	F	PWM4
		O	F	WLAN_ACTIVE
		O	F	UART0_TXD
9	GPIO05	strapping function		
		I/O	U	GPIO[05]
		O	F	gpo_int
		I/O	F	I2S_BCLK
10	GPIO06	strapping function		
		I/O	U	GPIO[06]
		O	F	gpo_int
		I	F	I2S_DI
11	GPIO07	strapping function		
		I/O	U	GPIO[07]
		O	F	gpo_int
		O	F	I2S_DO
14	GPIO08	strapping function		
		I/O	U	GPIO[08]
		O	F	gpo_int
		I/O	F	I2S_BCLK
		O	L	SPI_M_CLK
15	GPIO09	strapping function		
		I/O	U	GPIO[09]
		O	F	gpo_int
		I/O	F	I2S_LRCLK
16	GPIO10	strapping function		
		I/O	U	GPIO[10]
		O	F	gpo_int
		I	F	I2S_DI
		I	H	SPI_M_MISO
		I/O	H	I2C_M_SDA

Pin No.	Pin Name	Alternate Functions		
17	GPIO11	strapping function		
		I/O	U	GPIO[11]
		O	F	gpo_int
18	GPIO12	strapping function		
		I/O	U	GPIO[12]
		O	F	gpo_int
		O	F	I2S_DO
		O	H	SPI_M_MOSI
		O	H	I2C_M_SCL
19	GPIO13	strapping function		
		I/O	U	GPIO[13]
		O	F	gpo_int
		I/O	F	I2S_LRCLK
		O	H	SPI_M_CS
		O	PU	SPI_PSRAM_CSN
28	GPIO14	strapping function		
		I/O	U	GPIO[14]
		O	F	gpo_int
		I/O	PD	SPI_flash_IO0_DI
29	GPIO15	strapping function		
		I/O	U	GPIO[15]
		O	F	gpo_int
		O	PD	SPI_flash_CLK
30	GPIO16	strapping function		
		I/O	U	GPIO[16]
		O	F	gpo_int
		I/O	PU	SPI_flash_IO3_HD
		O	F	SPI1_S_MISO
31	GPIO17	strapping function		
		I/O	U	GPIO[17]
		O	F	gpo_int
		O	PU	SPI_flash_CSN
32	GPIO18	strapping function		
		I/O	U	GPIO[18]
		O	F	gpo_int
		I/O	PD	SPI_flash_IO1_DO
		I	F	SPI1_S_CSN
33	GPIO19	strapping function		
		I/O	U	GPIO[19]

Pin No.	Pin Name	Alternate Functions		
		O	F	gpo_int
		I/O	PU	SPI_flash_IO2_WP
		I	F	SPI1_S_MOSI
3	GPIO20	strapping function		
		I/O	U	GPIO[20]
		O	F	gpo_int
		O	F	I2S_MCLK
		O	F	I2S_MCLK
		I	F	SPI1_S_CLK
2	GPIO21	strapping function		
		I/O	U	GPIO[21]
		O	F	gpo_int
		O	H	I2C_M_SCL
		I	F	I2C_S_SCL
		O	F	UART0_TXD
Pin No.	Pin Name	Alternate Functions		
1	GPIO22	strapping function		
		I/O	U	GPIO[22]
		O	F	gpo_int
		I/O	H	I2C_M_SDA
		I/O	F	I2C_S_SDA
		I	F	UART0_RXD
		I	F	BT_ACTIVE

5. INTERFACE TIMING SPECIFICATION

5.1. SPI Timing Waveform

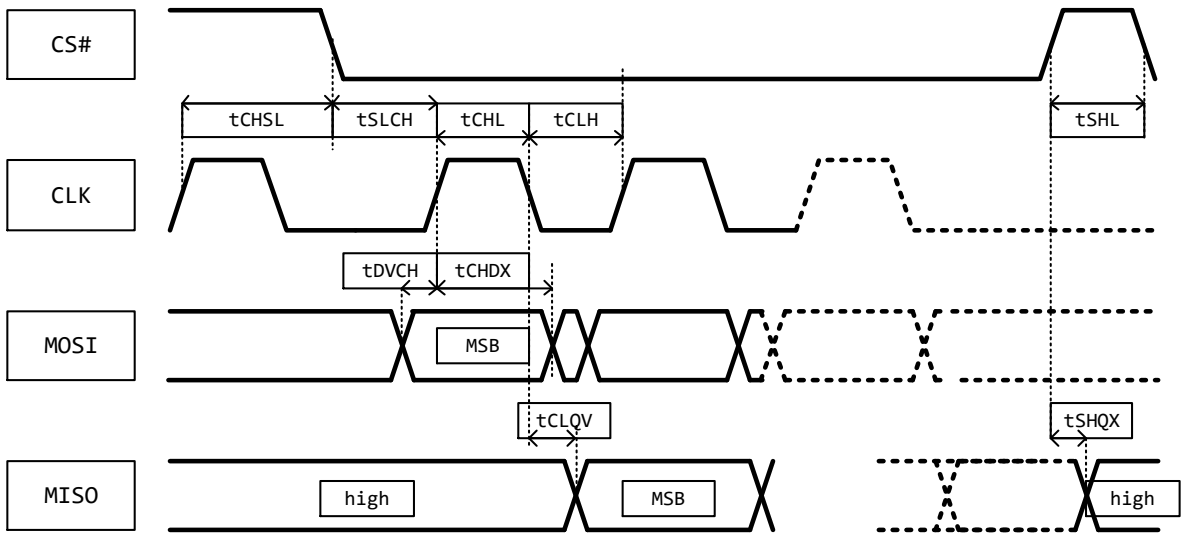


Figure 5-1: SPI Timing Waveform

Table 5-1: SPI Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCHSL	CS# active hold time	10			ns
tSLCH	CS# active setup time	3			ns
tSHL	CS# inactive time	300			ns
tCHL	CLK high time	12.5			ns
tCLH	CLK low time	12.5			ns
tDVCH	Data in (MISO) setup time	3			ns
tCHDX	Data in (MISO) hold time	3			ns
tCLQV	Data output delay			6.5	ns
tSHQX	Data output disable time			6	ns

5.2. SDIO Timing Waveform

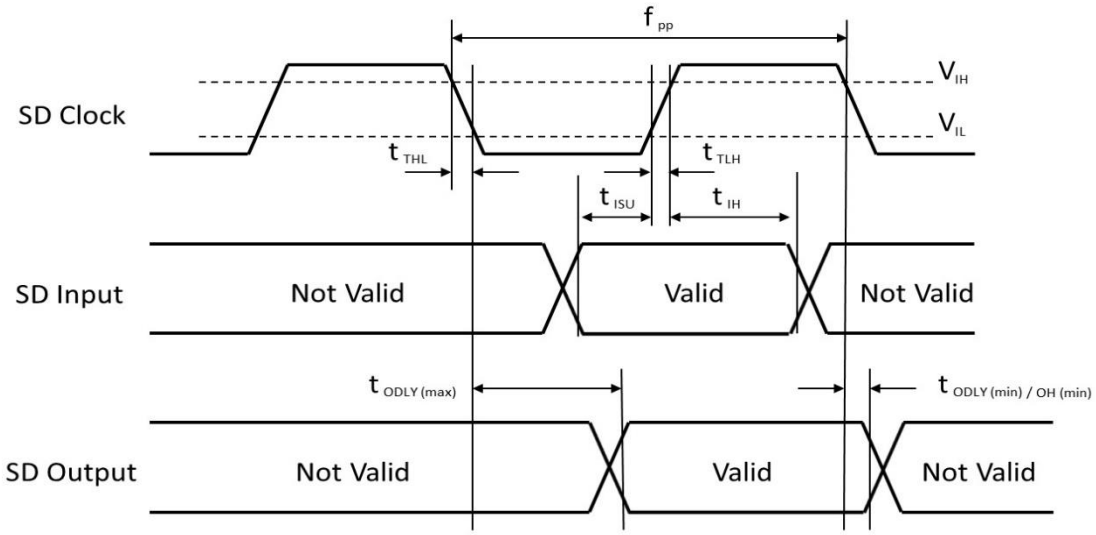


Figure 5-2: SDIO Timing Waveform

Table 5-2: SSW105BT SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock CLK (All values are referred to min(VIH) and max (VIL).					
fpp	Clock frequency Data Transfer Mode	0		50	MHz
tTLH	Clock rise time			3	ns
tTHL	Clock fall time			3	ns
Inputs CMD, DAT (reference to CLK)					
tISU	Input set-up time	6			ns
tIH	Input hold time	2			ns
Outputs CMD, DAT (reference to CLK)					
tODLY	Output Delay time during Data Transfer Mode			14	ns
tOH	Output Hold time	2.5			Ns

5.3. USB Timing Waveform

Table 5-3: SSW105AT USB High-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tHSRLEW	Slew rate of the rising edge	-	-	-	1600	V/usec

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
tHSFLEW	Slew rate of falling edge	-	-	-	1600	V/usec
Driver waveform	-	Specified by eye pattern template in USB2.0 spec.	-	-	-	-
Clock Timings						
THSRDRATE	High-speed data rate		479.76	-	480.24	Mbps
High-Speed Data Timings						
TJ	Data source jitter	Source and receiver jitter specified by the eye pattern template defined in USB2.0 spec.				
RXJT	Receiver jitter tolerance					

Table 5-4: SSW105AT USB Full-Speed Source Electrical Characteristics

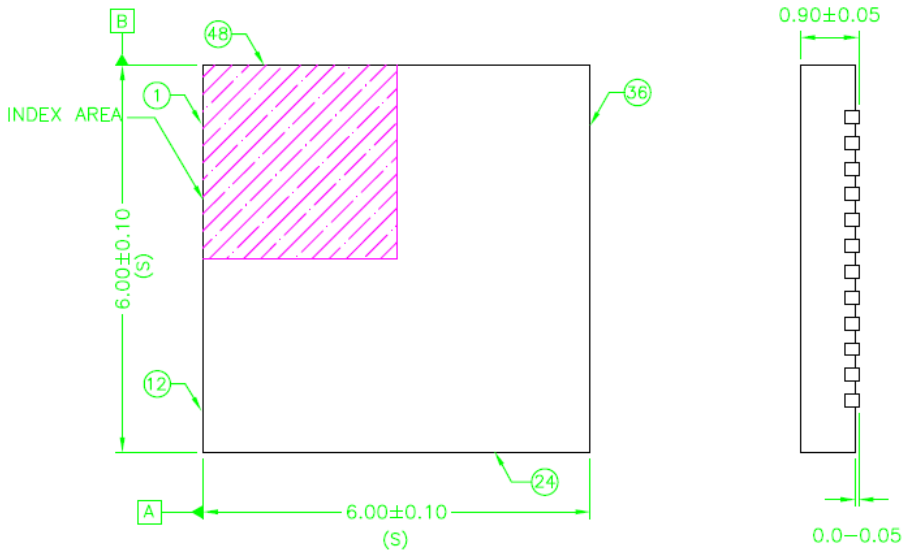
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 50 pF 10% ~ 90% of |VOH – VOL|	4	-	20	ns
tHSFLEW	Fall time	CL = 50 pF 90% ~ 10% of |VOH – VOL|	4	-	20	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	90	-	110	%
Clock Timings						
TFSTXDRATE	Full-speed TX data rate		11.994	-	12.006	Mbps
TFSRXDRATE	Full-speed RX data rate		11.97	-	12.03	Mbps
Full-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-2	-	5	ns
TJR1	Receiver jitter	To next transition	18.5	-	18.5	ns
TJR2	Receiver jitter	For paired transition	-9	-	9	ns
TFEOPT	Source SE0 interval of EOP	-	160	-	175	ns
TFEOPR	Receiver SE0 interval of EOP	-	82	-	-	ns
TFST	Width of SE0 interval during the differential transition	-	-	-	14	ns

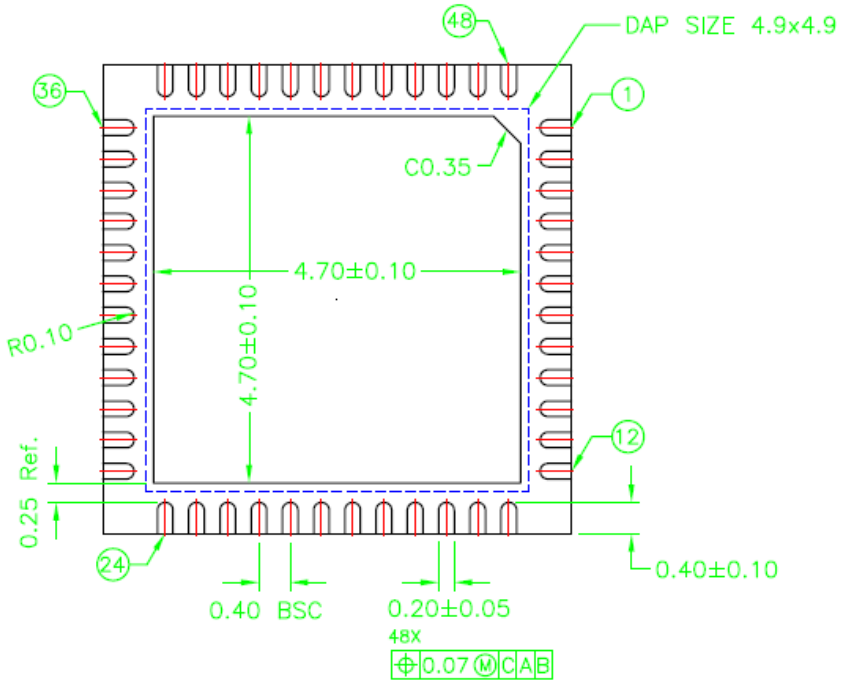
Table 5-5: SSW105AT USB Low-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 200 pF~ 600 pF 10% ~ 90% of |VOH–VOL|	75	-	300	ns
tHSFLEW	Fall time	CL = 200pF ~ 600pF 90% ~ 10% of |VOH–VOL|	75	-	300	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	80	-	125	%
Clock Timings						
TFSTXDRATE	Low-speed TX data rate		1.49925	-	1.50075	Mbps
TFSRXDRATE	Low-speed RX data rate		1.49925	-	1.50075	Mbps
Low-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-40	-	100	ns
TJR1	Receiver jitter	To next transition	-75	-	75	ns
TJR2	Receiver jitter	For paired transition	-45	-	45	ns
TFEOPT	Source SE0 interval of EOP	-	1.25	-	1.5	ns
TFEOPR	Receiver SE0 interval of EOP	-	670	-	-	ns
TFST	Width of SE0 interval during the differential transition	-	-	-	210	ns

6. MECHANICAL DIMENSIONS

6.1. Chip Package Drawing





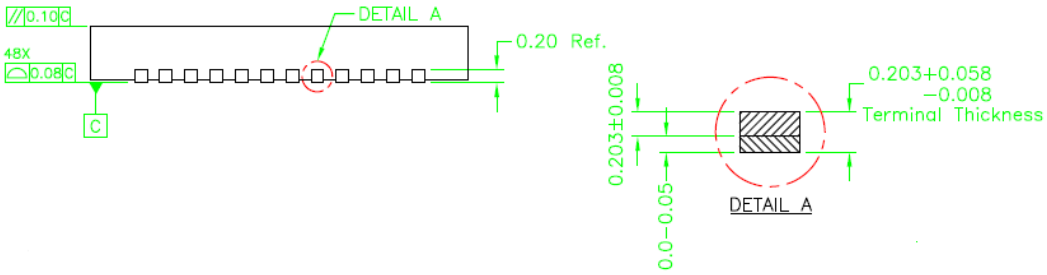


Figure 6-1: SSW105 QFN 6 x 6 mm Package Dimensions

NOTE:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

   COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. L/F STOCK# FR9012 (PPF)

6.2. Package information

6 x 6 mm (body size), 0.4mm pitch QFN-48

Marking format (top view)

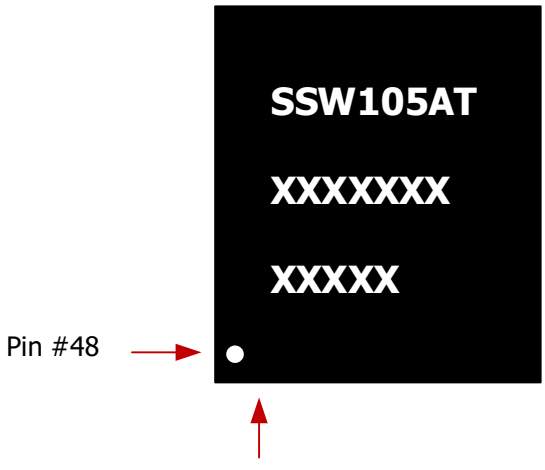


Figure 6-2: Package Information

7. SOLDER REFLOW PROFILE

7.1. Package Peak Reflow Temperature

SSW105AT/SSW105BT is assembled in a lead-free QFN48 package. Since its size is 6*6*0.90 mm3, the volume and thickness are in the category of volume<550mm3 and thickness<1.8mm in Table 4-2 of IPC/JEDEC J-STD-020C. Accordingly, the peak reflow temperature (Tp) is 260℃

7.2. Classification Reflow Profile

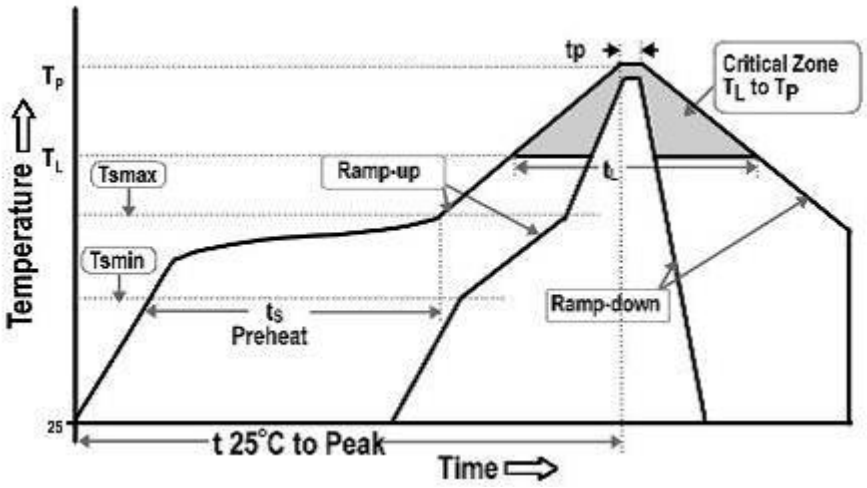


Figure 7-1: Reflow Profile

Table 7-1: Reflow Profile Classify Description

Profile Feature		Specification*
Average ramp-up rate (t_{smax} to t_P)		3℃/second max.
Pre-heat	Minimal temperature (T_{smin})	150℃
	Maximal temperature (T_{smax})	200℃
	Time (t_s)	60~120 seconds
Time maintained above	Temperature (T_L)	217℃
	Time (t_L)	40~60 seconds
Peak/Classification temperature (T_P)		250℃
The time within 5℃ of actual peak temperature (t_P)		10~20 seconds
Ramp-down rate		2.5℃/second max.
Time 25℃ to peak temperature		8 minutes max.

*Note: all temperatures are measured on the top surface of the package.

7.3. Maximum Reflow Times

The maximum reflow times are **three (3)** times. All package reliability tests are performed and passed the tests with a pre-condition procedure that repeats the above reflow profile.