

1. Cache principles
 - a. Cache holds a much smaller subset of RAM's contents
 - b. Terminology
 - i. Memory *block*
 - ii. Cache *line*
 - iii. Cache *tag*
 - iv. Cache *hit*
 - v. Cache *miss*
 - vi. *Eviction*
 - vii. *Dirty*
2. Cache design
 - a. Cache design
 - i. Multiple-level caches
 - ii. Unified or split

b. How to address the cache

c. Cache size

3. Cache address layout

- a. Going to use slightly different terminology than the book
 - i. Same idea, but I find the book's variable names less than intuitive
- b. Terminology
 - i. C

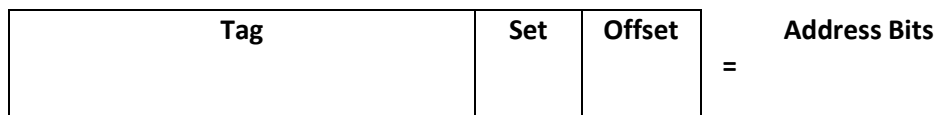
ii. LS

iii. LIC

iv. S

v. W

c. Address layout (in bits)



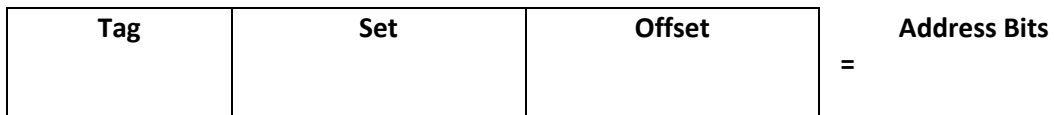
- d. Problems of this type
 - i. Usually given some of the variables above
 - ii. Asked to calculate the rest

4. Cache mapping types

- a. How does an address from main memory map to the cache?
- b. Direct mapped (DM)

i. Example

- 1. 8-byte DM cache with line size of 2, and 4-bit address



ii. Cache mapping example

- 1. Memory values for addresses

- a. 0110 = 0x1B
- b. 0111 = 0x59
- c. 1000 = 0xFE
- d. 1001 = 0x3D
- e. 1110 = 0x0C
- f. 1111 = 0x3A
- g. 1010 = 0x25
- h. 1011 = 0x98

- 2. Assume we pull in values from RAM in same order as above
 - a. What happens when we reach the last two accesses?

| Set Number | Tag | Byte 1 | Byte 2 |
|------------|-----|--------|--------|
| | | | |
| | | | |
| | | | |
| | | | |

c. Fully associative

i. Example

1. Same cache parameters as before, except now a FA cache
2. 8-byte FA cache with line size of 2, and 4-bit address

| Tag | Set | Offset | = | Address Bits |
|-----|-----|--------|---|--------------|
|-----|-----|--------|---|--------------|

ii. Cache mapping example

1. Same memory values for addresses
 - a. 0110 = 0x1B
 - b. 0111 = 0x59
 - c. 1000 = 0xFE
 - d. 1001 = 0x3D
 - e. 1110 = 0x0C
 - f. 1111 = 0x3A
 - g. 1010 = 0x25
 - h. 1011 = 0x98
2. Assume we pull in values from RAM in same order as above

| Line in Cache | Tag | Byte 1 | Byte 2 |
|---------------|-----|--------|--------|
| | | | |
| | | | |
| | | | |
| | | | |

d. Set associative

i. Example

1. Same cache parameters as before, except now a 2-way SA cache
2. 8-byte 2-way SA cache with line size of 2, and 4-bit address

| Tag | Set | Offset | = Address Bits |
|-----|-----|--------|----------------|
|-----|-----|--------|----------------|

ii. Cache mapping example

1. Same memory values for addresses
 - a. 0110 = 0x1B
 - b. 0111 = 0x59
 - c. 1000 = 0xFE
 - d. 1001 = 0x3D
 - e. 1110 = 0x0C
 - f. 1111 = 0x3A
 - g. 1010 = 0x25
 - h. 1011 = 0x98
2. Assume we pull in values from RAM in same order as above

| Set | Line Number | Tag | Byte 1 | Byte 2 |
|-----|-------------|-----|--------|--------|
| 0 | 0 | | | |
| | 1 | | | |
| 1 | 2 | | | |
| | 3 | | | |