THE UNIVERSITY OF KANSAS

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EECS 645 – Computer Architecture

Spring 2023

Homework 03 (MIPS Register File)

Student Name: Student ID:

MIPS Register File

Describe in behavioral VHDL (using 3 concurrent VHDL processes) the MIPS register file shown in Figure 1 that supports 3-operand arithmetic operations with the following interface:

- Generics
  - Register file size/depth (*reg_file_depth* with default value of **23** registers)
  - Register file width (*reg_file_width* with default value of 32 bits)
- Inputs
  - Clock (clk → 1 bit)
  - Asynchronous reset (rst → 1 bit)
  - Register write enable (RegWrite → 1 bit)
    - 1 → enable writing to register file,
    - 0 → disable writing to register file
  - Read Address for first (read) operand (RA1 → $\lceil \log_2(reg\_file\_depth) \rceil$ bits)
  - Read Address for second (read) operand (RA2 → $\lceil \log_2(reg\_file\_depth) \rceil$ bits)
  - Write Address for third (write) operand (WA → $\lceil \log_2(reg\_file\_depth) \rceil$ bits)
  - Write Data for third (write) operand (WD → *reg_file_width* bits)
- Outputs
  - Read Data for first (read) operand (RD1 → *reg_file_width* bits)
  - Read Data for second (read) operand (RD2 → *reg_file_width* bits)

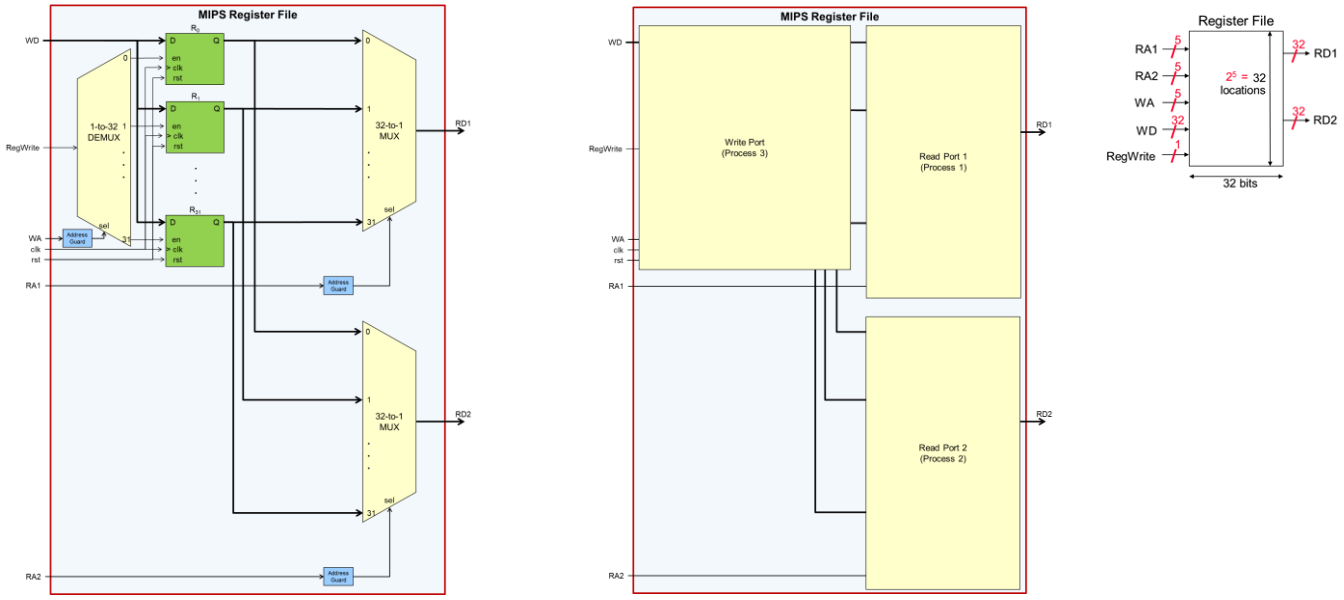

Figure 1. MIPS Register File

In your design:

- **Guard against address-spilling (address-overflow) where addresses could go out of range, e.g., exceeding the register file size/depth.**
- **Guard against unintentional writes to register zero ($0), i.e., $0 is read-only and has always the value 0.**

- In Vivado
  - Create a blank project
  - Add design and simulation source files
  - Run behavioral simulation
  - Your waveform configuration should be identical to the provided waveform snapshot, see Figure 2.
- Steps:
  1) Download the file "HW03_MIPS_RegFile.zip" from Canvas and extract its contents.
  2) Rename the folder "HW03_MIPS_RegFile" to "HW03_MIPS_RegFile_<your last name>", for example "HW03_MIPS_RegFile_El-Araby".
  3) Launch Vivado and create a new project, for example "vivado_project", with the default settings under the following directory "\HW03_MIPS_RegFile_<your last name>" resulting in the following project directory "\HW03_MIPS_RegFile_<your last name>\vivado_project\"
  4) Add to the project the VHDL design and simulation source files from the folders; "\HW03_MIPS_RegFile_<your last name>\design_sources" and "\HW03_MIPS_RegFile_<your last name>\simulation_sources" respectively.
  5) Edit the VHDL file in the folder "\HW03_MIPS_RegFile_<your last name>\design_sources\" according to your design such that it describes the required *MIPS register file*.
  6) Set the simulation time to the proper time, e.g., ***300 ns***, and then launch Vivado Simulator.
  7) Verify the correctness of your design. Your waveform configuration should be identical to the waveform snapshot shown in Figure 2. You may go back to step 5 to correct your code until your design works properly as required.
  8) After you are done, compress the folder "\HW03_MIPS_RegFile_<your last name>" to "HW03_MIPS_RegFile_<your last name>.zip", for example "HW03_MIPS_RegFile_El-Araby.zip" and upload it to Canvas before the due date and time.

Grade Distribution:

- Functional Correctness, i.e., correct source code → 75 / 100
- Proper Setup of Vivado Project → 25 / 100

NOTE:

Homework submission is a "Single Attempt", i.e. carefully review everything that you want to submit before hitting the "submit" button and make sure that you have uploaded all documents you want to submit and have not missed anything.

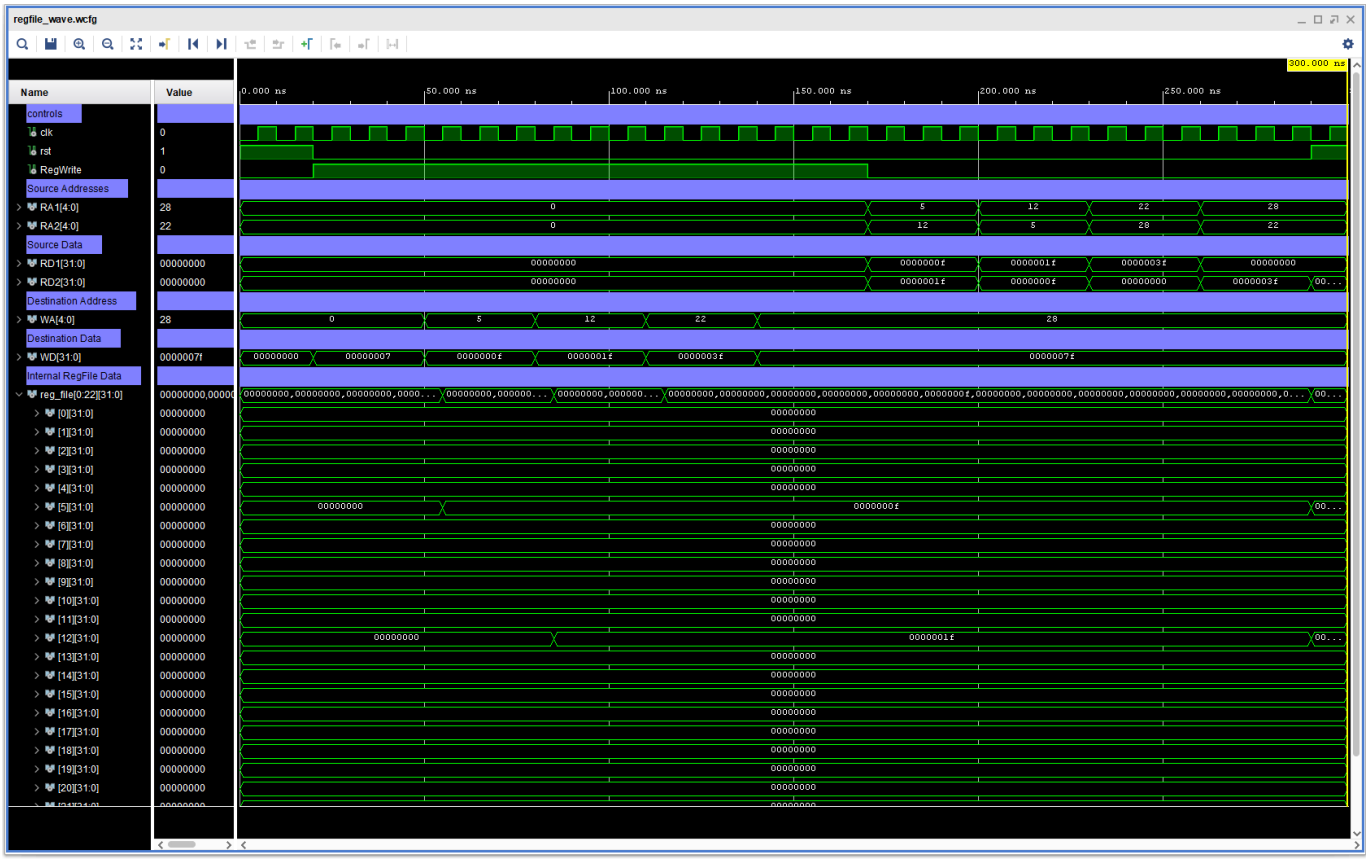

Figure 2. Snapshot of Correct Waveform Configuration