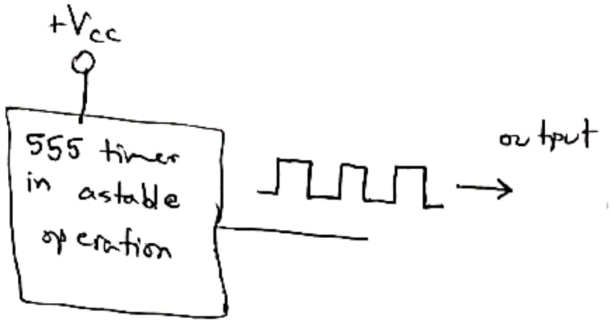
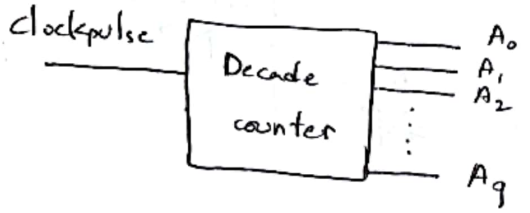
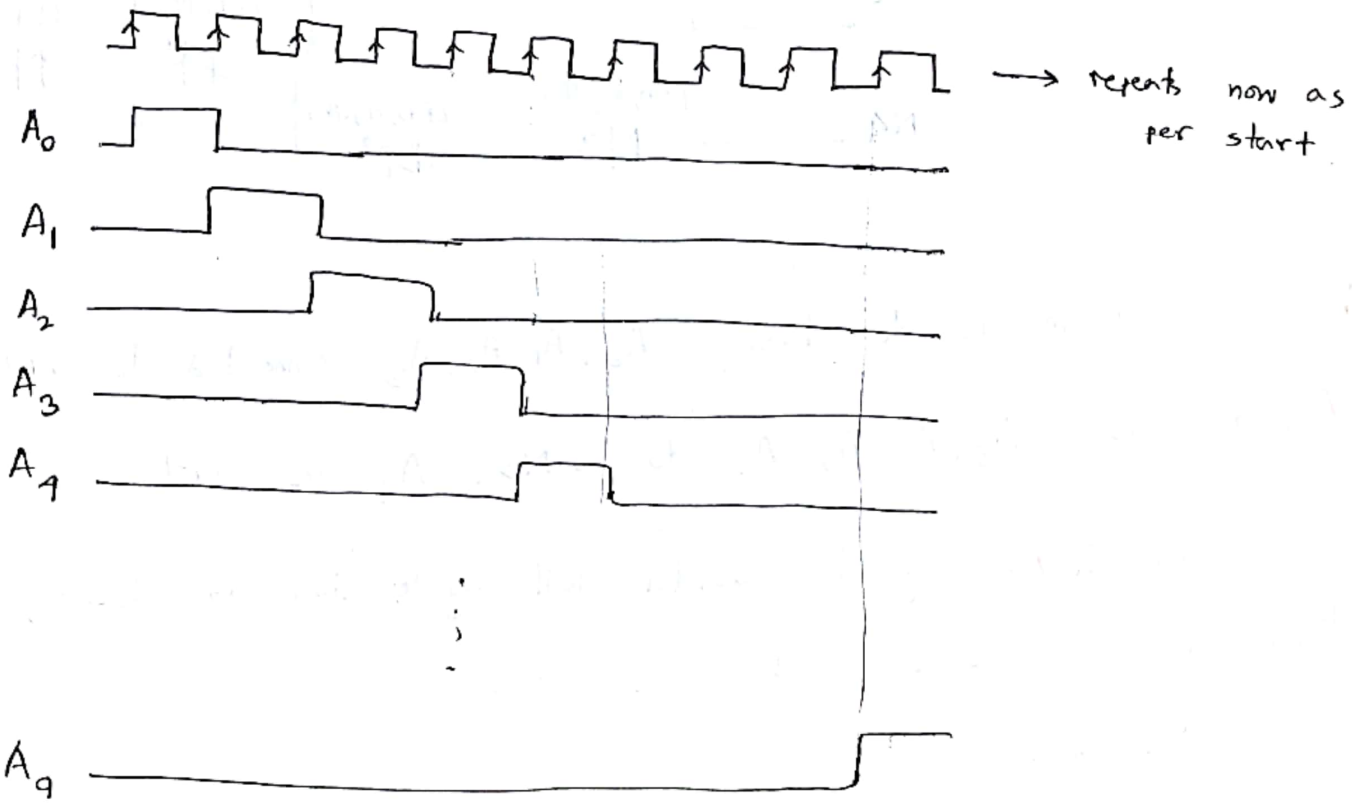
Generating ~~pulse~~ pulse train with 555 timer:



; will be used as clock pulse

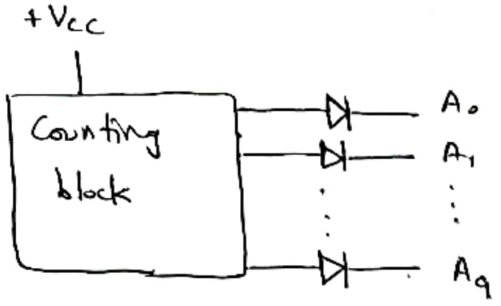
Using decade counter to generate counts from 0 to 9:





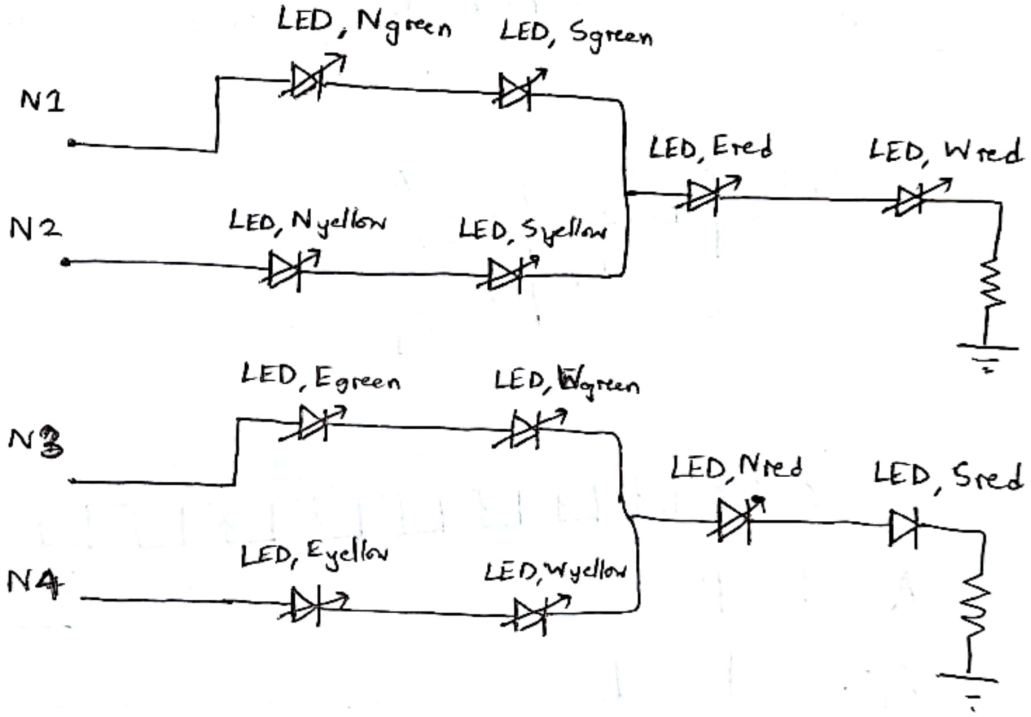
* Initial pulse must be set to reset [details ~~in a website~~ later]

okay, so lets call that a block named 'canting block'-



diodes added.

Now, assume 4 nodes.



Default system is to have A_0, A_1, A_2, A_3 connected to N1. A_4 to N2. A_5, A_6, A_7, A_8 to N3. A_9 to N4.

~~We want to~~ Assuming the counter full cycle time is 100s,

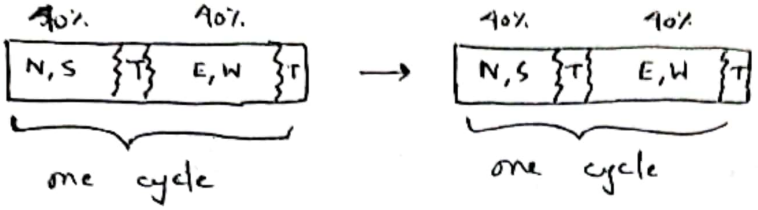
N, S on and E, W off for 40s

10s transition

N, S off and E, W on for 40s

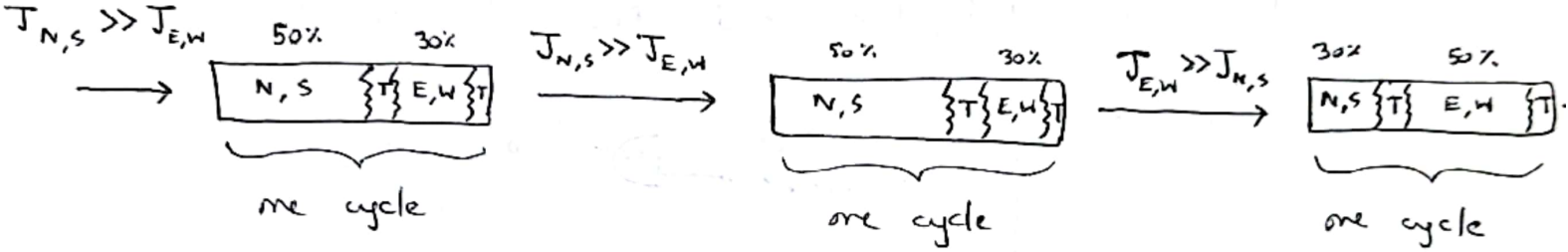
10s transition.

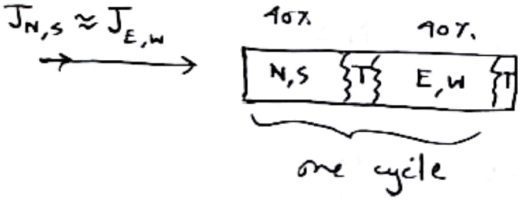
This one cycle of counter allocates 50% time to one lane, and other 50% to the other lane.



T → transition

When one lane has more traffic than another, we want the next cycle to have more time on for that lane. So:



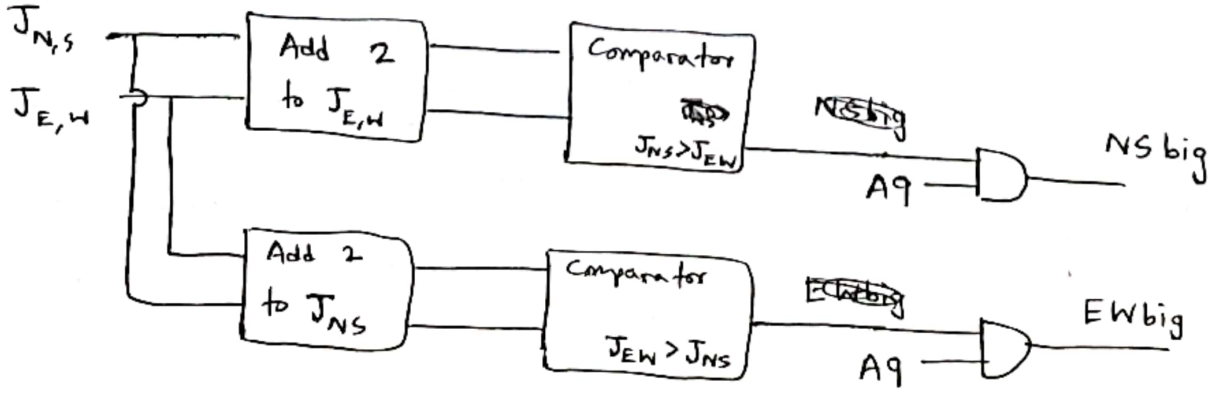


$J_{N,S}$ → traffic in North, South

$J_{E,W}$ → traffic in east, west

How to do this? We use latching switches.

- Basic idea is to have a traffic check when counter is at A9. Using comparators and adders, we can do such. Assume traffic has to be '3' more than other, in order to shift weights.



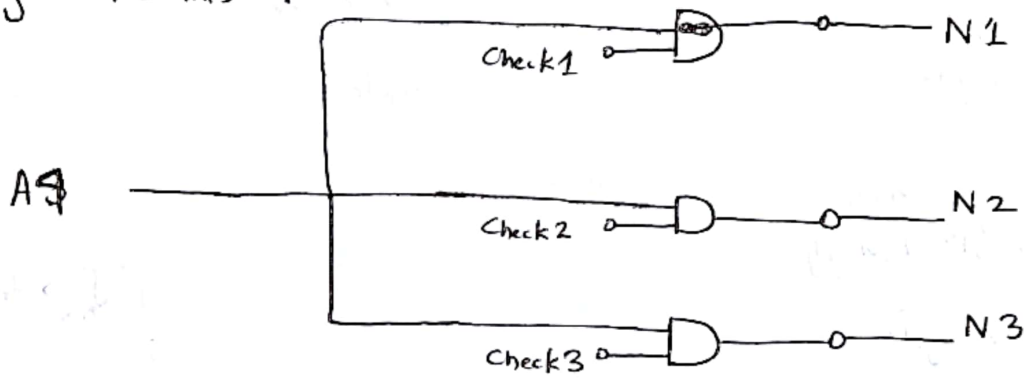
If J_{NS} greater than J_{EW} by 3 or more, 1st circuit output +ve.

" J_{EW} " " " J_{NS} " " " " " , 2nd " " +ve.

Other two outputs of comparator circuit not used.

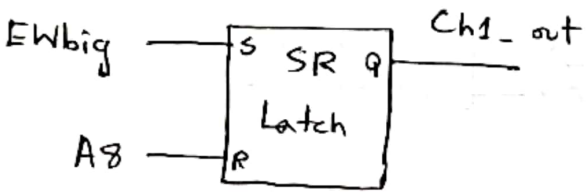
Lets call the 1st circuit output NSbig. And 2nd circuit output EWbig. Comparison is only done on when last digit of counter happens.

Now, let us take A3, A4, A5 and work with connecting them to N1, N2 and N3. It should look something like this :



Check1, Check2, Check3 - what are these? We use latching elements so that they stay on ~~and~~ till the next check. We use SR latches for this.

Check1 circuit :



When EWbig == 5V, Q is 1.

Q stays 1 even when EWbig disappears [only exists for duration of A9]

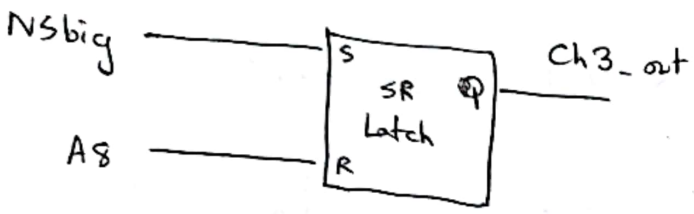
S=1, R=0 → Q=1.

A8 used to reset latch at φ^{th} part of one cycle [A8]

Then, S = 0, R = 1 so that φ = 0 [reset-ted].

Once decision is made during A9 cycle, whether φ = 0 or 1, it stays that way till comter does full revolution to A8, then it resets to 0.

Check3 circuit :



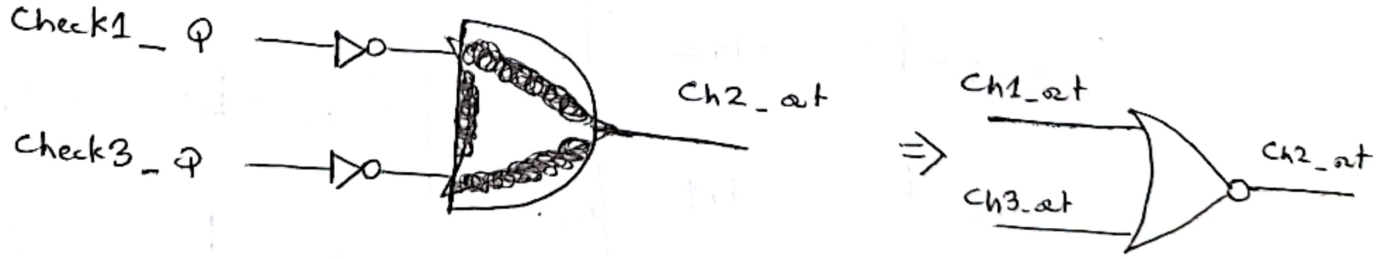
same logic as before.

NSbig == 5V, Q is 1.

The setting is done when A9 is high. Stays ~~high till next~~ that way till next cycle A8.

A8 == high resets latch so that φ = 0.

Check 2 circuit :



Ch1_φ Ch3_φ

This stays on when ~~NSbig~~ and ~~EWbig~~ are both zero.

[When NS traffic and EW traffic has a difference of 2 or less].

~~The same is repea~~ Essentially, during the end of one cycle-

A8 resets all latches, connecting A9 to N2.

A9 checks if NW big ~~is~~ has more dominant traffic or EW. Then connects A1 to N1 or N3 depending on whether ~~NW~~ EW big or NS.

(1) More traffic on NS → A1 — N3

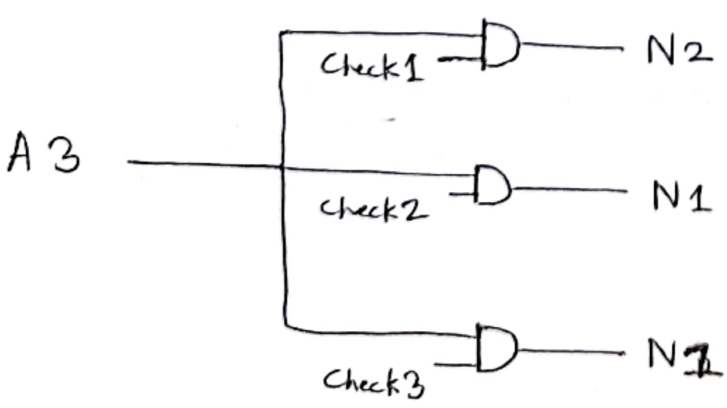
More traffic on EW → A1 — N1

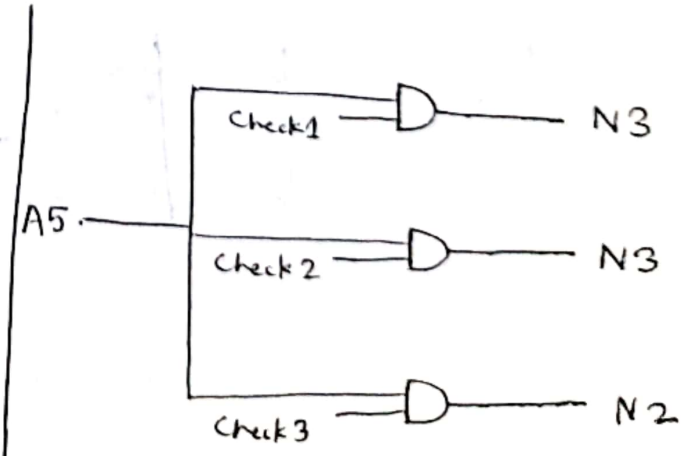
(2) A8 high → A1 — N1 and A1 — N3

A1 — N2

(3) A9 → checks for (1). Then goes to next cycle.

A3 and A5 are treated similarly:





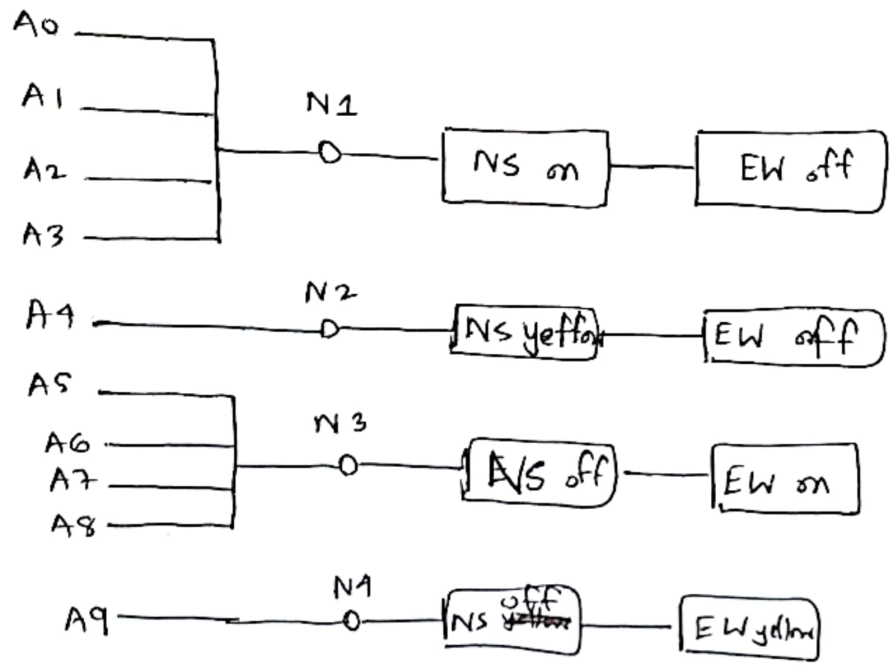
Remember:

Check 1 → EW big Check 3 → NS big

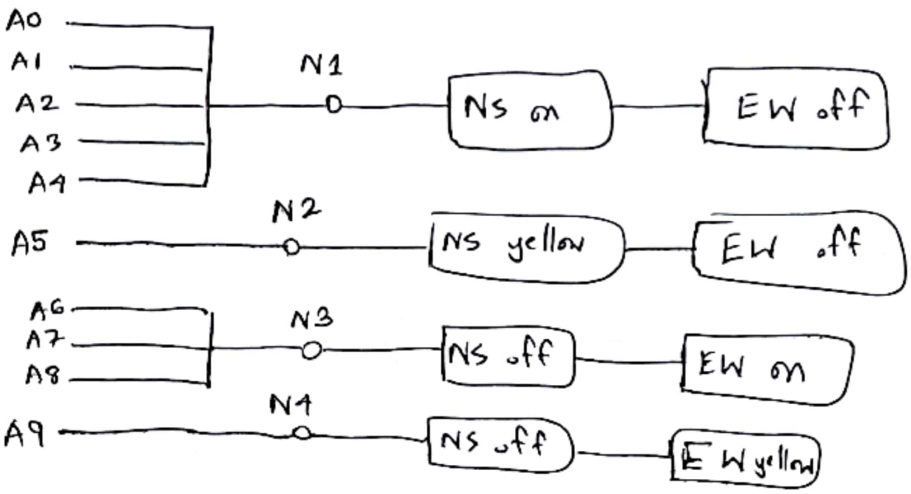
Check 2 → default

The 3 circuits thus made when operating at 3 states are:

Default:



When NS traffick higher than EW:



When EW traffic higher: