

**ROAD TO HIGHER DEFINITION MID-WAVE INFRARED SCENE  
PROJECTORS BY SHRINKING PIXEL PITCH**

by

Miguel Angel Hernandez-Raya

A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Department of Electrical and Computer Engineering

Spring 2020

© 2020 Miguel Angel Hernandez-Raya  
All Rights Reserved

**ROAD TO HIGHER DEFINITION MID-WAVE INFRARED SCENE  
PROJECTORS BY SHRINKING PIXEL PITCH**

by

Miguel Angel Hernandez-Raya

Approved: \_\_\_\_\_

Kenneth Barner, PhD  
Chair of the Department of Electrical and Computer Engineering

Approved: \_\_\_\_\_

Levi T. Thompson, PhD  
Dean of the College of Engineering

Approved: \_\_\_\_\_

Douglas J. Doren, Ph.D.  
Interim Vice Provost for Graduate and Professional Education and  
Dean of the Graduate College

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: \_\_\_\_\_

Fouad Kiamilev, PhD  
Professor in charge of dissertation

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: \_\_\_\_\_

Mark Mirotznik, PhD  
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: \_\_\_\_\_

Steven Hegedus, PhD  
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: \_\_\_\_\_

Jorge Garcia, PhD  
Member of dissertation committee

## **ACKNOWLEDGEMENTS**

## TABLE OF CONTENTS

<b>LIST OF TABLES . . . . .</b>	<b>viii</b>
<b>LIST OF FIGURES . . . . .</b>	<b>ix</b>
<b>ABSTRACT . . . . .</b>	<b>xix</b>
Chapter	
<b>1 INTRODUCTION TO INFRARED SCENE PROJECTORS . . . . .</b>	<b>1</b>
<b>2 BACKGROUND ON IRSP TECHNOLOGIES . . . . .</b>	<b>3</b>
2.1 Resistor Arrays . . . . .	3
2.2 Liquid Crystal Arrays . . . . .	5
2.3 Carbon Nanotubes . . . . .	7
2.4 Light Emitting Diode Arrays . . . . .	7
<b>3 EVOLUTION OF SUPER-LATTICE LIGHT EMITTING DIODE INFRARED PROJECTORS . . . . .</b>	<b>10</b>
3.1 Super Lattice LED System . . . . .	10
3.2 Two Color SLED Array . . . . .	13
3.3 Night Glow LED System . . . . .	16
3.4 High Definition IR LED . . . . .	17
3.5 Road to future IR LED systems . . . . .	18
3.5.1 AERIA . . . . .	18
<b>4 INTRODUCTION TO ADVANCE RIIC TECHNOLOGIES FOR INCREASING DENSITY OF ARRAYS . . . . .</b>	<b>20</b>
4.1 Motivation for ART-IDEA . . . . .	20
4.2 Wafer Yields for RIICs . . . . .	21
4.2.1 Wafer Testing Methodologies . . . . .	22

4.2.2	Results of Wafer testing . . . . .	25
4.2.3	Summary of Yield of RIICs . . . . .	27
<b>5</b>	<b>DESIGN OF THE TEST CHIP . . . . .</b>	<b>33</b>
5.1	Picking the right tools for the job . . . . .	33
5.1.1	N-type laterally diffused high power transistor . . . . .	36
5.1.2	VLSI techniques relevant to the project . . . . .	36
5.2	Base Design is NSLEDS . . . . .	40
5.3	First iteration of the RIIC super pixel with the ONC18 libraries . . . . .	45
5.4	Adaptations for the design of the ART-IDEA super-pixel . . . . .	50
5.5	Final layout 4x4 ART-IDEA super-pixel . . . . .	52
5.5.1	experimental circuits . . . . .	56
5.6	Contact pads and ESD protection . . . . .	58
5.7	Final Test Chip Layout to be Fabricated . . . . .	62
5.8	Packaging . . . . .	64
<b>6</b>	<b>DESIGN OF THE LED DEVICES FOR ART-IDEA . . . . .</b>	<b>65</b>
6.1	Motivation for decreasing the LED size . . . . .	66
6.2	Fabrication of the SLED devices . . . . .	68
6.2.1	Challenges Encountered During SLED Fabrication . . . . .	70
6.3	packaging . . . . .	72
<b>7</b>	<b>RESULTS OF TESTING THE RIIC AND SLED PIXELS . . . . .</b>	<b>74</b>
7.1	RIIC pixels test results . . . . .	74
7.1.1	First test on the 4x4 super-pixel . . . . .	75
7.1.2	characterization of the RIIC pixels . . . . .	77
7.2	SLED pixels test results . . . . .	81
7.3	combined test results . . . . .	86
<b>8</b>	<b>CONSLUSION . . . . .</b>	<b>94</b>
<b>REFERENCES . . . . .</b>		<b>96</b>

## Appendix

<b>A EXPERIMENTAL CIRCUITS SIMULATIONS AND FIGURES</b>	<b>99</b>
<b>B FINAL TEST CHIP LAYOUT CIRCUITS</b>	<b>109</b>
<b>C RIIC SUPER PIXEL PACKAGING</b>	<b>120</b>
<b>D PARTITIONED SVSM - 84-PIN LCC SOCKET</b>	<b>128</b>
<b>E AUXILIARY TEST RESULTS</b>	<b>137</b>
E.1 RIIC Test Chip Auxiliary Results	137
E.2 SLED Auxiliary Test Results	137

## **LIST OF TABLES**

## LIST OF FIGURES

1.1	IRSP developed at the University of Delaware. 1. Scene generator PC, 2. Close Support Electronics (CSE), 3. IR LED emitter array mounted in a Dewar package, 4. FLIR camera . . . . .	1
2.1	Structure of a resistor array for an IRSP . . . . .	4
2.2	Structure of a resistor array for an IRSP . . . . .	6
2.3	Composition of a SLED array hybrid . . . . .	8
2.4	Hybrid after flip chip bonding, and wirebonded to a carrier board . . . . .	8
3.1	Schematic of a single SLEDS pixel . . . . .	10
3.2	SLEDS RIIC layout and a zoomed in single pixel layout . . . . .	11
3.3	Donald duck being displayed on the SLEDS . . . . .	12
3.4	TCSA pixel wavelengths (left), and Stack structure for the TCSA pixel (right) . . . . .	14
3.5	3D representation of a single TCSA pixel . . . . .	14
3.6	TCSA driver circuit with two gears per color . . . . .	15
3.7	The NSLEDS Super Pixel consists of 4 pixels with sharing common anodes . . . . .	16
3.8	In HDILED the super pixel only had one common anode in the middle . . . . .	17
3.9	Architectural overview of the AERIA arrays . . . . .	19
4.1	Moore's Law data collected over 40 years showing the expected behavior . . . . .	21

4.2	Bigger chip size per wafer greatly reduces the yield per wafer . . . . .	22
4.3	Break down of the RIIC chip, each of the quadrants is controlled by the appropriate corners containing all the digital logic. The rest of the perimeter is used to bring in all the high power voltage rails and return paths . . . . .	23
4.4	Custom probe card used to test RIICs on wafers . . . . .	24
4.5	RIIC corners under a microscope . . . . .	26
4.6	Sample curves collected during wafer testing to check if the RIIC chip showed signs of life . . . . .	26
4.7	Example of NSLEDS yield of transistors, candidate for hybridization. Curves represent the current output of the transistors as a function of voltage applied at the gate. . . . .	28
4.8	Pixel maps for all the quadrants of the NSLEDS RIIC shown on figure 4.7, the pixels are mapped one to one to their actual location on the RIIC . . . . .	29
4.9	Example of HDILED yield of transistors, candidate for hybridization. Curves represent the current output of the transistors as a function of voltage applied at the gate. Because of the low yield of such a big chip, parts that had "bad" pixels were considered for hybridization as long as the number was below 1% . . . . .	30
4.10	Pixel maps for all the quadrants of the HDILED RIIC shown on figure 4.9, the pixels are mapped one to one to their actual location on the RIIC . . . . .	31
4.11	cost per part for different RIICs, with the $24\mu\text{m}$ pixel design it is very costly to make a 4+ million pixel projector . . . . .	32
5.1	Comparison between different CMOS technology libraries . . . . .	33
5.2	NLDMOS structure for the 3.3V process . . . . .	35
5.3	IV curves for NLDMOS transistors with different physical sizes . . . . .	35
5.4	VLSI CMOS transistors, NMOS (top) are grown on a p-well, and PMOS (bottom) are grown on a n-well . . . . .	37

5.5	This simulation shows the effect of having a mismatch in mobility of the pull-up and pull-down CMOS logic. Ideally the mobility has to equal on both the PMOS pull-up network or the NMOS pull-up network. However, in some scenarios it might be beneficial to have a faster rise time and a slow fall time, or vice versa. The simulation shown is a DC sweep of the input of an inverter where the size of the NMOS transistor is kept constant at 420nm while the PMOS size varies from 250nm to 2000nm with 11 steps. Since this is the ONC18 Technology the best match for no skew is when the PMOS is around 1400nm . . . . .	38
5.6	Top: Sample shows how to utilized the techniques discussed to maximize area of Series CMOS. Bottom: Same techniques applied to a parallel network of 3 CMOS . . . . .	39
5.7	Simplified version of the NSLEDS pixel design . . . . .	41
5.8	NSLEDS super-pixel top level design diagram . . . . .	41
5.9	Address decoder (left) and gear selector (right) circuits for the NSLEDS super-pixel design . . . . .	42
5.10	Driver circuits for all 4 pixels within a NSLEDS super-pixel and MOUT circuit (bottom right) . . . . .	43
5.11	Final layout of a 2x2 super-pixel using the 3.3V technology library in an area of $48\mu mx48\mu m$ . The memory capacitor (green circle) and the NLDMOS (yellow circle) are the largest components in the layout . . . . .	46
5.12	post PEX simulation of inputs and gate states for a 2x2 super-pixel using the ONC18 3.3V flow process. . . . .	47
5.13	post PEX simulation of the weak gears based on the inputs provided for fig 5.12 for a 2x2 super-pixel using the ONC18 3.3V flow process.	48
5.14	post PEX simulation of the strong gears based on the inputs provided for fig 5.12 for a 2x2 super-pixel using the ONC18 3.3V flow process.	49
5.15	4x4 super-pixel concept to be used on the RIIC and SLED designs of ART-IDEA . . . . .	50
5.16	address decoder for a 4x4 super-pixel . . . . .	51

5.17	address decoder for a 4x4 super-pixel . . . . .	51
5.18	top level cell for the 4x4 super-pixel of ART-IDEA . . . . .	53
5.19	Final Layout for the ART-IDEA 4x4 super-pixel design . . . . .	54
5.20	Post PEX simulation for the 4x4 ART-IDEA super-pixel . . . . .	55
5.21	Final schematic and Layout for the improved driver circuit. This design was based on the simulations performed on Appendix A . . . . .	57
5.22	schematic for the input pads with ESD protecting diodes . . . . .	59
5.23	ESD diode to be connected to VDD_ESD, the diode is interlace with p and ntype fingers and grown on a nwell. The entire diode is also surrounded by a p+ substrate contact for isolation . . . . .	60
5.24	ESD diode to be connected to GND_ESD, the diode is interlace with p and ntype fingers and grown directly on the p-sub. The entire diode is also surrounded by a n+ nwell contact for isolation . . . . .	61
5.25	Top: zoomed in layout of a single IO pad with ESD diodes and signal paths. Bottom: Final chip layout, a total of six circuit layouts are brought out to the pads for wirebonding . . . . .	62
5.26	RIIC chip prototype packaged in a 144 PGA package . . . . .	64
6.1	SLED stack diagram showing all the layers used make a single device. Some of these layer may repeat N times depending on the number of stages the specific device has . . . . .	65
6.2	A SLED stage is composed of an active region and a tunnel junction as shown on figure 6.1. However, it is easier to think of them as single LEDs where the number of LEDs is the number of stages of the stucture . . . . .	66
6.3	Current density (left) and bias voltage versus randiance for different size 16-stage SLED devices . . . . .	67
6.4	Simulations that show the ideal wall angle for the best extraction, this angle would be around 45°. The other is a ray tracing simulation that predicts the path of light with angled sidewalls on the SLED device	67

6.5	Two plots that show the effect of having different number of stages on SLED devices. With higher number of stages the maximum light out from a SLED increases, however, this increases the turn on voltage of the SLED device . . . . .	68
6.6	Mask used for fabricating the SLED devices. The mask is geometrically symmetrical between the four quadrants, each contains different sized messas and partition mesas that help us compare the differences between them . . . . .	69
6.7	$12\mu m$ mini arrays for IAG739 (left) and IAG740(right) . . . . .	71
6.8	SEM for a $24\mu m$ pitch SLED device . . . . .	71
6.9	SEM for a $18\mu m$ pitch SLED device . . . . .	71
6.10	SEM for a $12\mu m$ pitch SLED device . . . . .	72
6.11	SLED part being wired bonded to an 84-pin LCC package . . . . .	73
7.1	PCB used for housing the 144 PGA chips. It brings out all 144 pins to two rows of female jumper connectors. ESD diodes can be installed on the underside of the PCB if the user desires. . . . .	75
7.2	Set up use to test the RIIC chip. (1) control PC, (2) Keithley meter, (3) digilent Explorer board, (4) Tektronix power supply, (5) RIIC chip mounted on break out pcb . . . . .	76
7.3	Lighting up an LED using a single RIIC pixel was the first test done on the 4x4 super-pixel. Left - the weak gear is driving the pixel. Right - the strong gear is driving the pixel . . . . .	77
7.4	100 sweeps of pixel AN and AP using vinn and vinp analog input signals respectevily, the weak gear was more noisy than expected . . . . .	78
7.5	100 sweeps of pixel AN and AP using vinn and vinp analog input signals respectevily. The strong gear worked as expected and matched simulation results . . . . .	78
7.6	100 sweeps of pixel AN and AP at the same time. Since both vinn and vinp ran simultaneously the current double as expected . . . . .	79

7.7	50 sweeps of all 16 pixels at the same time. The weak gear is not as noisy . . . . .	79
7.8	parametric sweep displaying the behavior of both gears with varying Voltage on the LED supply and sweeping vinp . . . . .	80
7.9	A 4x4 mini grid of macro LEDs being dirven by the 4x4 RIIC super pixel . . . . .	80
7.10	Legend for reading SLED plots. Solid lines = single mesas. Broken/dotted lines: Dashed = $12\mu m$ pitch subdivisions, Dash-Dot = $18\mu m$ pitch subdivisions, Dot = $24\mu m$ pitch subdivisions . . . . .	82
7.11	SLED test chip IAG739-A02 radiance vs. voltage . . . . .	83
7.12	SLED test chip IAG739-A04 radiance vs. voltage . . . . .	84
7.13	SLED test chip IAG739-A04 radiance vs. voltage . . . . .	85
7.14	Comprehensive view of SLED devices tested by pixel-pitch, values represent the max radiance observed on data collected at UIowa . . . . .	86
7.15	In order to test the SLED test chips in conjuction with the RIIC test chip, a PLCC86 socket was added to the test set up to hold the SLED test chips, and a FLIR SC6800 camera to caputure the light	87
7.16	Using the RIIC pixel to drive a SLED pixel at different lighth intensities . . . . .	87
7.17	Post-process camera image captured for a $38\mu m^2$ mesa SLED device on test chip IAG739-A02 line 2 using strong gear . . . . .	88
7.18	Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested - $38\mu m^2$ mesa SLED device on test chip IAG739-A02 line 18 using strong gear . . . . .	89
7.19	Post-process camera image captured for a $38\mu m^2$ mesa SLED device on test chip IAG739-A02 line 2 using weak gear . . . . .	90

7.20	Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested - $38\mu\text{m}^2$ mesa SLED device on test chip IAG739-A02 line 18 using weak gear . . . . .	91
7.21	Post-process camera image captured for a $12\mu\text{m}$ pitch SLED device on test chip IAG739-A02 line 2 using strong gear . . . . .	92
7.22	Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested - $12\mu\text{m}$ pitch SLED device on test chip IAG739-A02 line 18 using strong gear . . . . .	93
A.1	cascoding transistors simulation schematic. The three paths are a stand alone NLDMOS transistor, middle path uses a NMOS transistor as resistor, right path uses a pmos . . . . .	100
A.2	For reference, this is the Current vs Voltage curve for the weak gear NLDMOS of the ART-IDEA pixel . . . . .	101
A.3	Varying the width of the NMOS transistor on the cascode circuit did not have a big effect as expected. This is because the larger the width of the device, the wider the channel will be. In other words, there is a bigger highway for electrons to flow. . . . .	102
A.4	Varying the Length of the transistor creates a longer channel on the transistors. As a result the electrons have to travel a longer distance to reach the other side. This increases the impedance of the device decreasing the amount of current that can flow. . . . .	103
A.5	Varying the voltage at the gate ( $V_g$ ) of the MOS transistors puts it in different modes of operation. In the linear region the MOS acts as a resistor and the value of equivalent resistance changes depending on the value of $V_g$ . . . . .	104
A.6	Varying the length of the PMOS transistor yields very high apperent resistance but the threshold voltage for the path increases significantly. For this reason further investigations into using a PMOS device as a resistor were dropped . . . . .	105
A.7	Simulation that shows the effect of the reset line on the drive circuit	106
A.8	Improved driver circuit with a reset line and a cascaded weak gear .	107

A.9	Improved driver circuit layout for the ART-IDEA pixel . . . . .	108
B.1	NLDMOS Drive transistors circuit with the same size as they would have in the 4x4 super-pixel . . . . .	109
B.2	NLDMOS Drive transistors Layout. Top portion is the weak gear and bottom portion is the strong gear . . . . .	110
B.3	Address Decoder circuit and gear selector are combined into one block on the test chip . . . . .	111
B.4	Layout block for the address decoder and gear selector circuit . . .	112
B.5	Circuit schematic for the LED driver. This version has been used on previous RIICs . . . . .	113
B.6	Layout for the driver circuit shown on figure B.5 . . . . .	114
B.7	Circuit Schematic for the enhanced driver circuit. This circuit was derived after many simulations. It contains a pixel level reset line, and a properly sized cascaded weak gear. If it proves to be effective after testing it will be implemented to the main design and replace the current drive circuit . . . . .	115
B.8	This is the layout that corresponds to the driver schematic with a reset line and cascaded weak gear shown in figure ?? . . . . .	116
B.9	This is the top cell schematic for the 4x4 RIIC super-pixel. Inputs are on the left side, and all 16 LED outputs plus the telemetry pin are on the right side . . . . .	117
B.10	Layout for the 4x4 RIIC super-pixel that was submitted for fabrication after passing DRC, LVS and post PEX simulation tests	118
B.11	Top cell for a 2x1 ART-IDEA super-pixels, a total of 32 pixel can be driven with this design . . . . .	119
B.12	Layout of two tiled ART-IDEA super-pixels. This was done to prove that the design is easily scalable . . . . .	119

E.1	Left: IV curves for pixel AN swept 100 times. Right: IV curves for pixel AP swept 100 times. This test prove the addressing scheme worked, as well as the analog inputs <b>vinn</b> and <b>vinp</b> can control the weak gear current output. The LED power source was set to 5V and the load used was a macro LED. Note: All 100 AN curves were collected first with AP off. Then with AN off, the 100 curves on AP were collected. . . . .	138
E.2	Left: IV curves for pixel AN swept 100 times. Right: IV curves for pixel AP swept 100 times. This is the same test as figure E.1 but using the strong gear on the driver . . . . .	138
E.3	Left: IV curves for pixel AN and AP in strong mode. Right: AN and AP IV curves in weak mode. For this test, the LED power source was set to 5V and the load were the macro LED attached to AN and AP outputs on the test chip. In this test, both AN and AP were swept simultanously and as expected the current increased by a factor of 2X	139
E.4	Left: IV curves for all 16 pixels in weak mode. Right: IV curves for all 16 pixels in strong mode. LED power source set to 5V, and as a load 16 macro LEDs attached to each of the pixels in the super-pixel. All pixels were swept at the same time, thus this shows the max current used by the entired super-pixel for both gears . . . . .	139
E.5	IV curves comparing the performance of pixels AN and AP. Relative location within the super-pixel, AN is pixel (0,0) and AP is pixel (0,1). . . . .	140
E.6	IV curves comparing the performance of pixels BN and BP. Relative location within the super-pixel, BN is pixel (1,0) and AP is pixel (1,1). . . . .	140
E.7	IV curves comparing the performance of pixels CN and CP. Relative location within the super-pixel, CN is pixel (2,0) and CP is pixel (2,1). . . . .	141
E.8	IV curves comparing the performance of pixels DN and DP. Relative location within the super-pixel, DN is pixel (3,0) and DP is pixel (3,1). . . . .	141
E.9	IV curves comparing the performance of pixels EN and EP. Relative location within the super-pixel, EN is pixel (0,2) and AP is pixel (0,3). . . . .	142

E.10	IV curves comparing the performance of pixels FN and FP. Relative location within the super-pixel, FN is pixel (1,2) and FP is pixel (1,3). . . . .	142
E.11	IV curves comparing the performance of pixels GN and GP. Relative location within the super-pixel, GN is pixel (2,2) and GP is pixel (2,3). . . . .	143
E.12	IV curves comparing the performance of pixels HN and HP. Relative location within the super-pixel, HN is pixel (3,2) and HP is pixel (3,3). . . . .	143
E.13	Relevant data collected for SLED test chip IAG739-A02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage . . . . .	144
E.14	Relevant data collected for SLED test chip IAG739-A03. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage . . . . .	145
E.15	Relevant data collected for SLED test chip IAG739-A04. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage . . . . .	146
E.16	Relevant data collected for SLED test chip IAG740-A02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage . . . . .	147
E.17	Relevant data collected for SLED test chip IAG739-B02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage . . . . .	148

## ABSTRACT

The role an Infrared scene projector (IRSP) plays in the qualification of infrared (IR) detection systems is to provide realistic simulated scenarios in a lab setting. As IR sensors become ever increasingly more complex, there comes a critical need for projection technologies to provide a means of testing. This method of hardware in the loop (HWIL) implementation reduces the cost and time of development. As a result, research and development (R&D) groups in industry and military have a large interest in IRSP technologies. Going forward, IRSP systems need even higher resolutions while increasing the speed of projection. A new Read-in integrated circuit (RIIC) architecture is necessary to push this technology forward towards the higher resolutions. The new RIIC architecture is 4x smaller and allows for more pixels per surface area than current architectures. Similarly, development of denser light emitting diode (LED) pixels in the mid-wave infrared (MWIR) spectrum was explored. This dissertation discusses the methodologies and results obtained from these new architectures.

# Chapter 1

## INTRODUCTION TO INFRARED SCENE PROJECTORS



**Figure 1.1:** IRSP developed at the University of Delaware. 1. Scene generator PC, 2. Close Support Electronics (CSE), 3. IR LED emitter array mounted in a Dewar package, 4. FLIR camera

The academic, military, medical, and industry have found many uses for Infrared (IR) imaging systems. Such systems have sensors which capture wavelengths of light below that of the visible spectrum. Different types of wavelengths can reveal different information about the environment around us. This is the main concept which has led to the development of many different systems in the IR spectrum. Some examples of systems that interpret IR light include things such as night vision goggles, IR cameras, communication systems, gas detectors, etc..

When dealing with very complex and expensive systems it becomes increasingly important to ensure that the IR components work as designed. Characterizing such components becomes a necessity for quality assurance of the system. This is where IRSps make their entry into the world of system development, IRSps are tools that

aid the test and evaluation of complex IR systems by providing heat signatures needed to stimulate the sensors. More specifically, the Unit Under Test (UUT) uses IRSPs in Hardware in the Loop (HWIL) configuration to test against realistic projected scenarios.

At the University of Delaware we have developed a stable and reliable LED based IRSP that has been used at different labs in HWIL configurations. The current components that make up an IRSP system are shown in figure 1.1. Referring to the figure, a scene generation computer is the high-level interface that provides a graphical user interface (GUI) with all the control functionalities. Furthermore, the scene generation computer preprocesses and bit-packs all imagery to be displayed by the projector. The CSE is the link between the output imagery of the scene generation computer and the display. The CSE contains all the hardware needed to process the data and put it into a format the RIIC component of the display can interpret as an image. The display LED array or hybrid, is housed in a commercial off the shelf (COTS) Dewar that allows us to run the system at 78K. For in house use only and development purposes, we use a FLIR camera during the development of the IRSP.

One of the oldest types of emitters are resistor arrays. The way resistor arrays emit in the IR spectrum is fairly simple. Heat produces a wide range of IR wavelengths, by heating up the component, a small MEMS resistor will produce heat, hence IR light. Honeywell was one of the first companies that made this technology available for commercialization, specifically in the military fields. This was the first type of IR projector that could produce dynamic imagery which made it popular for testing systems equipped with IR detectors. Today there are more technologies that made it into the IR projection world. Such technologies include, light emitting diodes, lasers, liquid crystal display, and carbon nanotube.

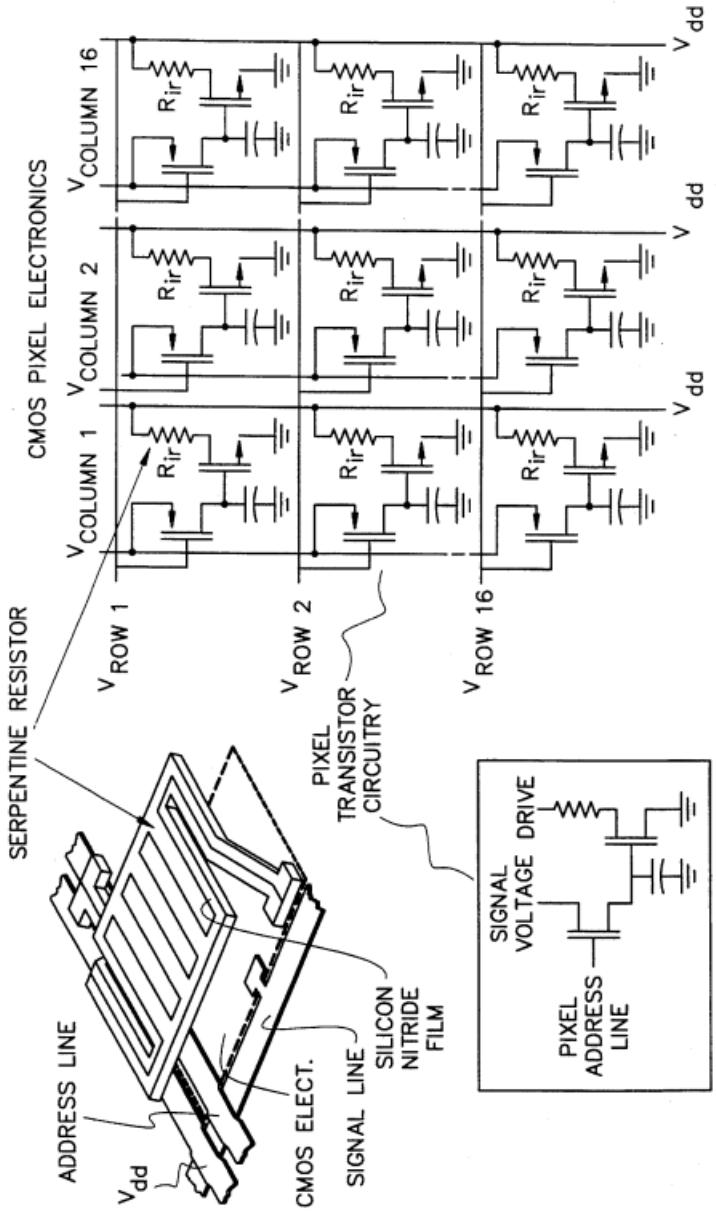
## Chapter 2

### BACKGROUND ON IRSP TECHNOLOGIES

In the IRSP field there is only one technology that has made a name for itself, and it is the resistor array technology. However, there are others who are trying to elbow their way into the top position in the market. This has come as a result of the shortcoming of the resistor array technologies. Some of these technologies include LCD displays, carbon nanotubes and LED arrays. Some are younger than others and each comes with a set of pros and cons. This chapter will briefly go over the different technologies.

#### 2.1 Resistor Arrays

The resistor array technology for IRSP systems is the only one being used commercially. This is due to the fact that it was the very first technology to successfully produce dynamic scenes in the IR spectrum. Honeywell was the company responsible for the discovery, both Barrett E. Cole and Chien J. Han were the inventors according to a patent filed in 1994. The concept for the technology is very simple. An electrical current flows thru a resistor and causes that resistor to heat up, hence IR signatures are generated. A single pixel is composed of a small serpentine resistor, the material used to make it is Silicon Nitride. The entire structure of the resistor is suspended over the pixel driver to avoid transmitting the heat down to the silicon structure of the driver[1]. On figure 2.1 both the physical structure of a resistor pixels, and the schematic for it can be compared side by side. Resistor pixels are grown individually on top of a silicon Read-in Integrated Circuit (RIIC) that uses Complementary Metal Oxide Semiconductor (CMOS)technology. The driver transistor is connected in series with the Serpentine Resistor as controls its flow of current. A second transistor acts as



**Figure 2.1:** Structure of a resistor array for an IRSI 

the address line and signal voltage for the main drive transistor[1]. The emitter array is formed by connecting many of these devices in parallel effectively forming a square grid.

After Santa Barbara IR (SBIR) licensed the technology from Honeywell they

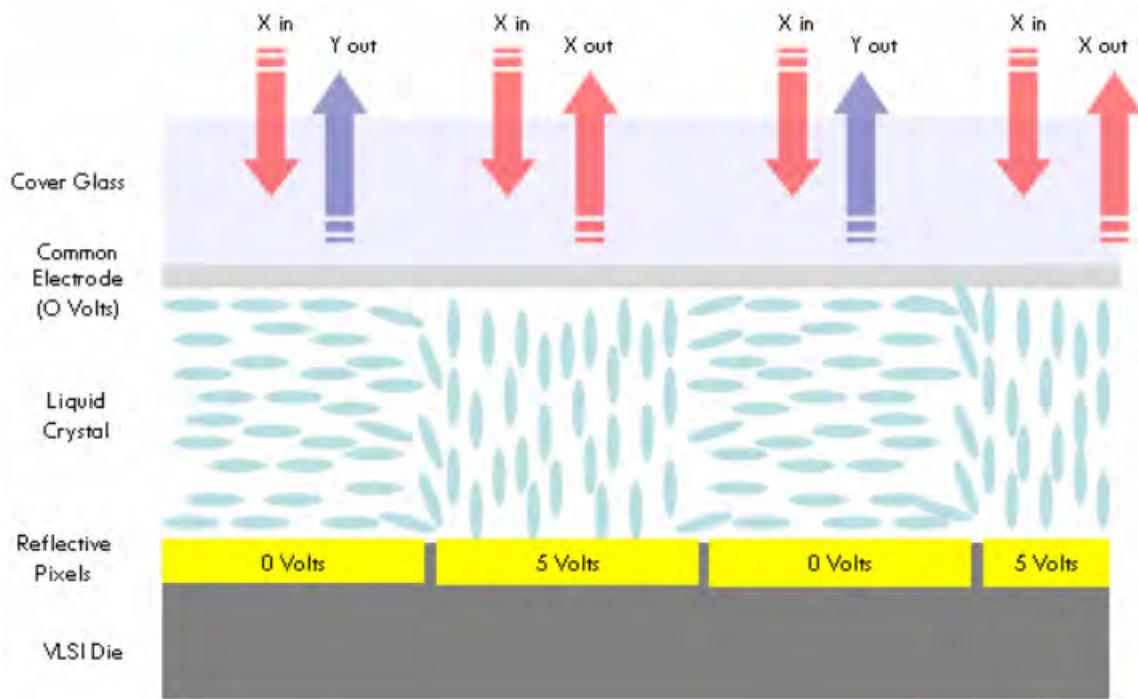
have been the only producers of IRSPs commercially[2]. In 1999 SBIR develop their MIRAGE projector. It was specifically designed for HWIL testing of missile seekers, IR cameras, and other tracking systems. Their first system was a 512x511 array that could produce apparent temperatures 475K. Their newest model is the MIRAGE XL has a resolution of 1024x1024, and an apparent temperature of up to 650K[3].

Resistor arrays proved that projection in IR has a great potential, however, they are on their way out as developing better IRSPs using this approach presents many walls that are very hard for resistor to overcome. Some of these include the physical size of the serpentine resistor can't get any smaller than a 48 micron pitch per pixel. They always have to be run at cryogenic temperatures to avoid damaging itself. Over time the optical properties of the resistors change, and the apparent temperatures are not very high[4, 2, 3].

## 2.2 Liquid Crystal Arrays

Liquid crystal display (LCD) technologies have also made themselves present in the IR projection business. LCD technologies work by having a very high power, broad spectrum back light which provides the illumination. An example of this technology is the BAT IR 4300 projector made by Kent Optronics. The display resolution for the model is 512x512 pixels, they can run 140Hz speed with a resolution of 12 bits[5].

A younger technology in the LCD world is Liquid Crystal on Silicon (LCoS). An LCoS uses the same concept as an LCD with the exemption that the light doesn't initially come in via a backlight, but instead it comes from a front source of illumination, and after being processed by the device, it leaves it as a reflection thru the front of the display. This is better understood by analyzing figure 2.2, X in represents linearly polarized light which travels down the structure. The second layer is a layer of conductive material that is very thin and transparent and acts as a common electrode. The liquid crystal layer is sandwiched between the electrode material and the Silicon die. The silicon die is divided into many pixels, each is plated with metal that provides the



**Figure 2.2:** Structure of a resistor array for an IRSP

medium for changing the angle of the crystals, and acting as a mirror that reflects the incoming light[6].

The LCD displays for IRSP have a big drawback being absorption. LCDs rely on an external source of light in order to produce images, this light is often very bright and good source of heat. While the light travels through the LCD structure absorption starts to happen leading to the display getting hotter. Local heating on a LCD array is overlooked and not very crucial in the visible spectrum, however, in IR if the device gets hot it generates undesirable sources of IR signatures. Other IR technologies are also affected by local heating.

The material that liquid crystals used are usually not the best choice for IR light. And the response of LCoS displays have not reached very fast response times. For IR projection the required thickness of the liquid crystal layer increases, thus reducing the response time of the display. The minimum thickness for an LCoS device is one

quarter of the wavelength[6], as shown in equation (2.1) where  $\lambda$  is the wavelength,  $\Delta n$  the birefringence which is the property of a material that dictates its refractive index dependant on the direction of light and polarization.

$$d = \frac{\lambda}{4\Delta n} \quad (2.1)$$

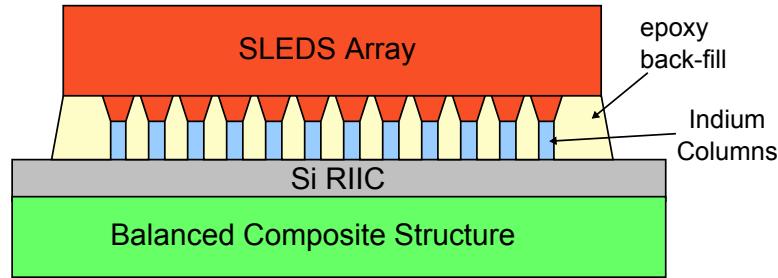
### 2.3 Carbon Nanotubes

A carbon nanotube (CNT) is a form of a very thin carbon graphitic sheet that is rolled up into a needle like tube. The fullerenes used is  $C_{60}$  as this forms the hexagonal lattice needed for a cylindrical shape of the tubes. The whole process is done via arc-discharge evaporation, the structure grows on the negative end of a carbon electrode in an argon filled vessel[7].

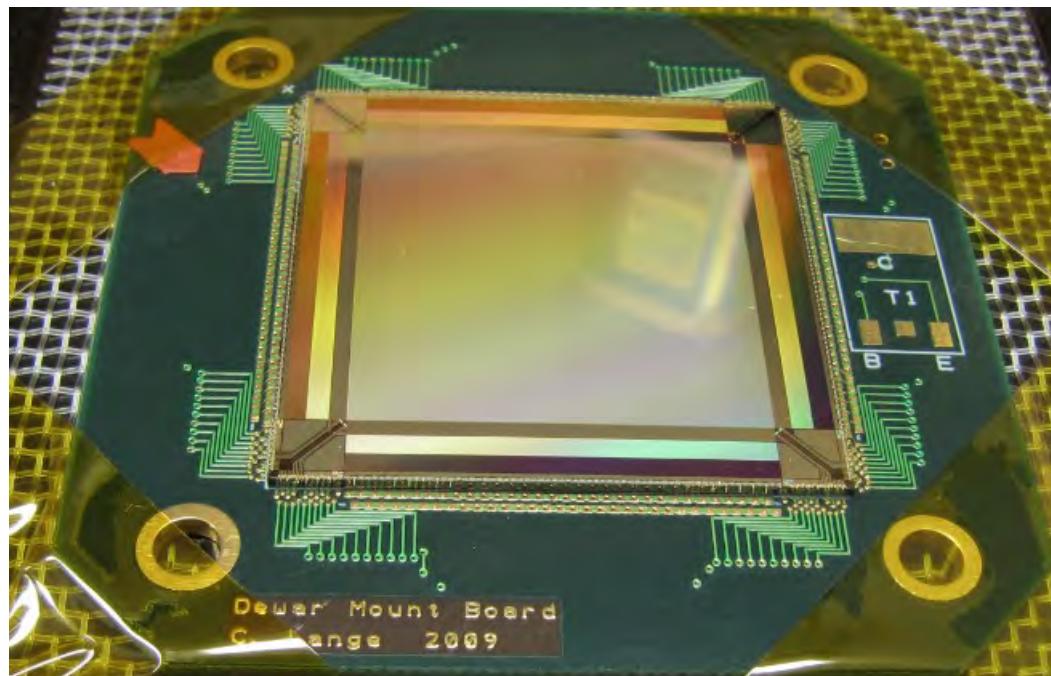
Recently CNT technology has been known have the capability of emitting in the IR spectrum. Different than a LED transistor configuration where the participating carriers are injected into the LED via the source or the drain, single walled semiconducting CTN have claimed they can generate the carriers locally when a single type of carrier, either  $e^-$  or  $h^+$ , is accelerated under a high electromagnetic field[8]. However, the application of this technology is fairly novel in the field of IR projection. The concept has been proven in very small scales and it will take some time before it can be compared to other projection technologies at the same level[7, 8, 9].

### 2.4 Light Emitting Diode Arrays

IRSPs that use LED arrays have been research since 2008, it started as a contribution between the University of Delaware (UD) and the University of Iowa (UI). An IR LED array has two parts to it, the first one being the RIIC, a chip that contains all the electrical pixels that control the radiance output of the LEDs and also provides communication to a system. Second, the super lattice LED (SLED) array, it is grown on a GaSb semiconductor wafer using molecular beam epitaxy[10]. The RIIC and the SLED array are hybridized together using flip chip bonding creating a single part that



**Figure 2.3:** Composition of a SLED array hybrid



**Figure 2.4:** Hybrid after flip chip bonding, and wirebonded to a carrier board

we call the SLEDs hybrid as shown on figure 2.3. Both the RIIC and the SLED array are a mirror image of each other on the side that has the contacts. Indium bumps are placed on the metal contacts for both and then the RIIC and the SLED array are pressed together. The final step is to add epoxy in the remaining gaps in order add an extra reinforcements to the part. 

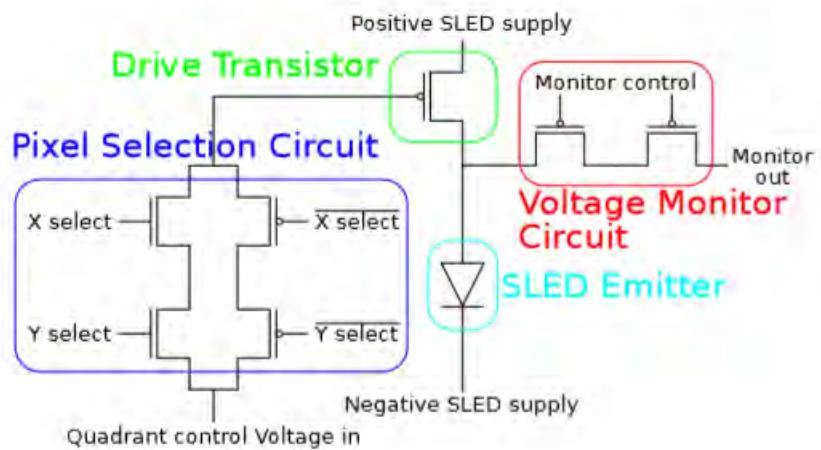
The final physical part is shown on figure 2.4, The emission area of the hybrid is the

inner most circle, this is **were** the SLED array is bonded with the RIIC. It is important to notice that the RIIC is bigger in size than the SLED array. This is because the RIIC also has to interface with the mounting printed circuit board (PCB), thus the extra space around the emission area contain all the pads necessary for wire bonding[[11](#)].

## Chapter 3

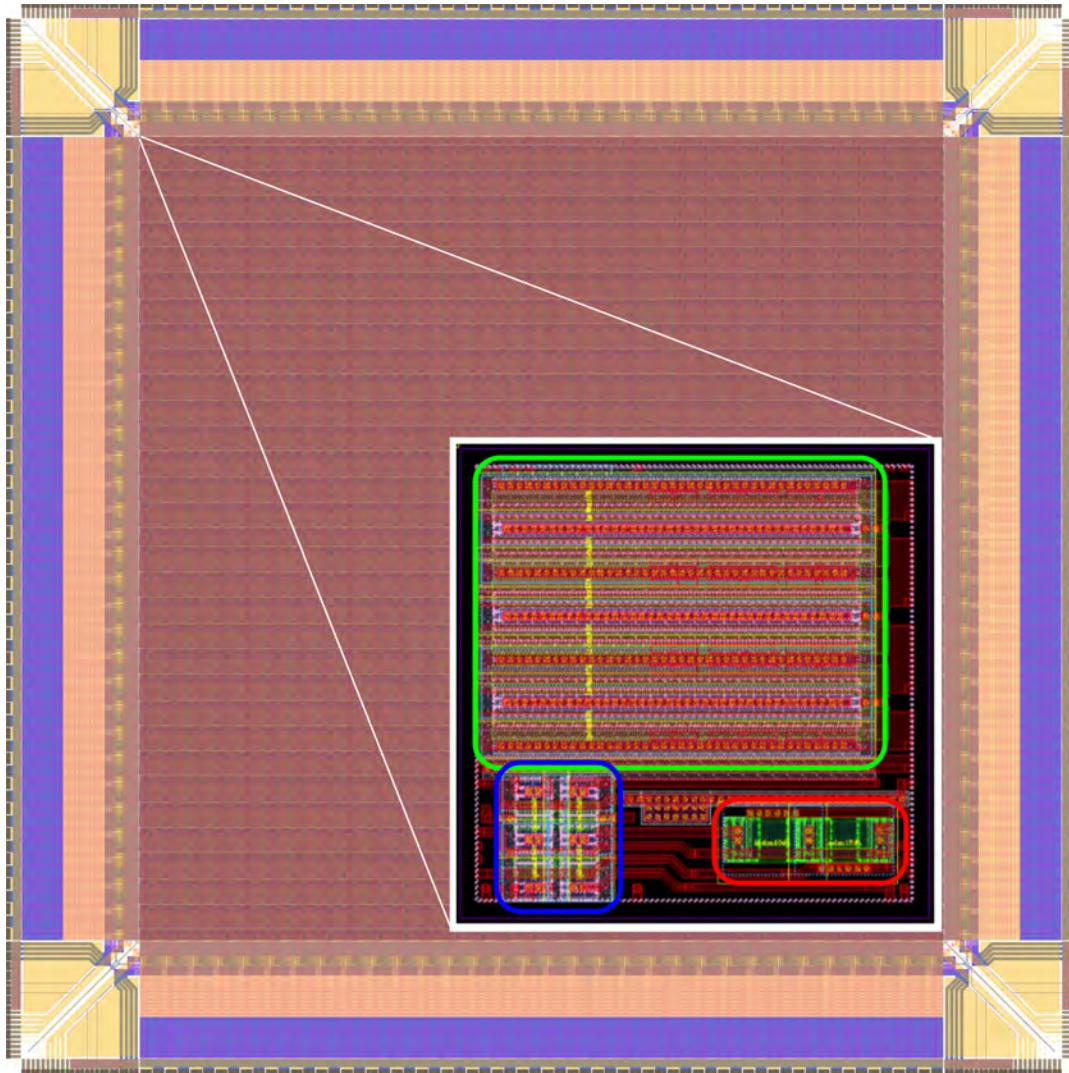
### EVOLUTION OF SUPER-LATTICE LIGHT EMITTING DIODE INFRARED PROJECTORS

#### 3.1 Super Lattice LED System



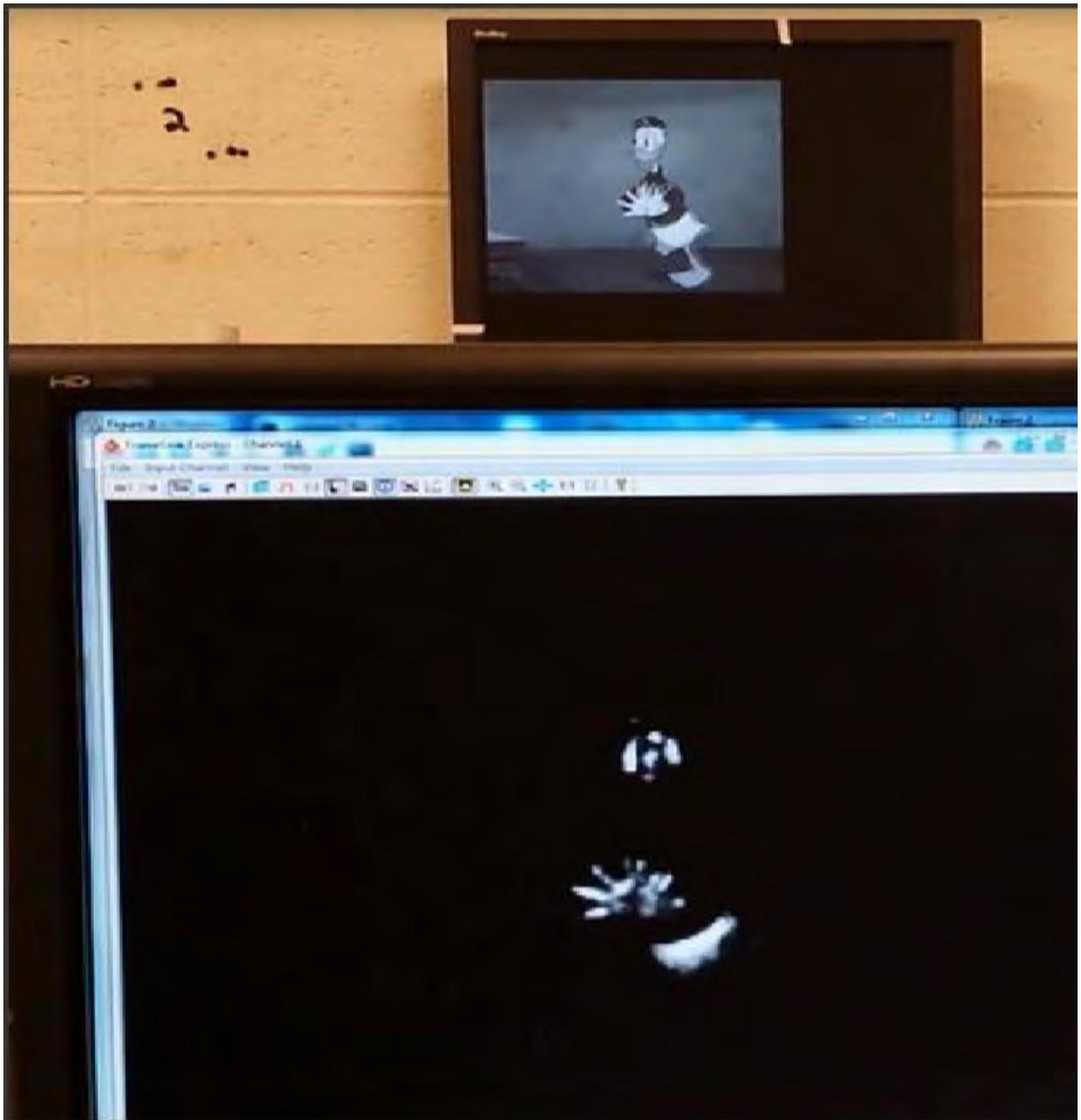
**Figure 3.1:** Schematic of a single SLEDS pixel

In 2014 our team at the University of Delaware made the first successful IRSP system using IR LED technology. The emitter array had a 512x512 resolution with a 48 $\mu$ m pitch. We called our first LED IRSP the Super Lattice LED System (SLEDS), not to be confused with SLEDs, this second form simply signifies the plural form of SLED. The SLEDS, as mentioned in section 2.4, uses the hybrid scheme approach to project light out of the IR LEDs. Figure 3.1 shows the schematic for a single pixel on the SLEDS hybrid array, and figure 3.2 shows the SLEDS RIIC layout, and a zoomed in image of a single RIIC pixel.



**Figure 3.2:** SLEDS RIIC layout and a zoomed in single pixel layout

Each individual pixel on the hybrid array had a dedicated circuit on the RIIC that controlled when the pixel was on or off using a very simple double chain of transmission gates that act as the selection circuit. In a CMOS process a transmission gate is formed when a N-type Metal Oxide Semiconductor (NMOS) transistor is connected in parallel to a P-type Metal Oxide Semiconductor (PMOS) transistor. The gate connections of both transistors are connected to a complementary signal. For example if a signal  $A$  is applied to the gate of the NMOS transistor, then the signal  $\bar{A}$  is applied to



**Figure 3.3:** Donald duck being displayed on the SLEDS

the gate of the PMOS transistor. In simple terms, both MOS transistors will turn off at the same time and turn on at the same time, enabling or disabling the signal that passes thru. The rest of the pixel circuit consist of a Drive transistor, and a Monitor

control. The drive transistor is controlled by the Voltage in signal and provides a path for current to flow to the LED. The monitor control PMOS chain allowed us to verify the pixel was alive by monitoring the voltage going to the LED[11, 12].

To get a better perspective the different pieces of the circuit have been encircled with different colors. The zoomed in layout for a RIIC pixel was also marked with the same colors to make a good comparison between the two. However, the LED is not shown on the layout because it is its own entity on the SLED array.

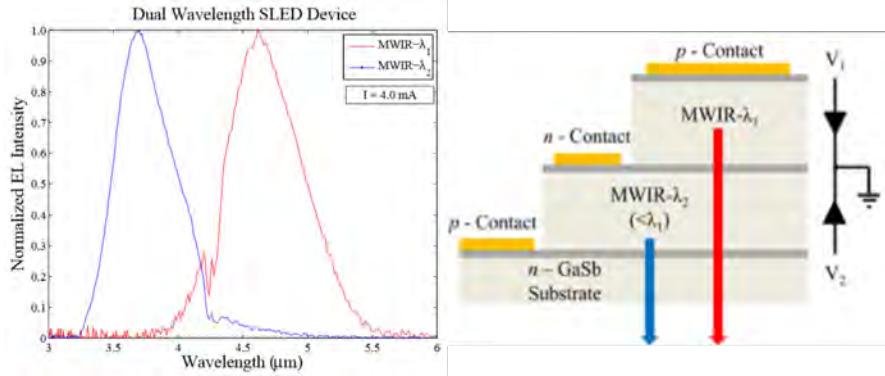
The SLEDS had many successes, including being tested at different laboratories in the country, running at 100Hz, and overall demonstrating that the technology is possible. However, being the first projector developed by our team, the SLEDS did not have the linearity and dynamic range desired to produce very realistic test scenarios. the reason for this is because the drive transistor was designed to be able to take big current loads in order to make the LEDs as bright as possible. The downside of this is that the transistors had very digital like curves almost like a clock pulse between the off state of the PMOS driver and the on state. This resulted in all of the output imagery being binary, either full on or full off, with little to no grayscale in between. Figure 3.3 is the perfect example of what we would see being projected on the SLEDS array. the top image on the small monitor is the actual video input being fed to the SLEDS projector, and the bottom screen shows the output being capture by a MWIR camera. On the output image only the white parts of the Donald Duck are visible while everything else is very dark or completely off[12, 11].

### 3.2 Two Color SLED Array

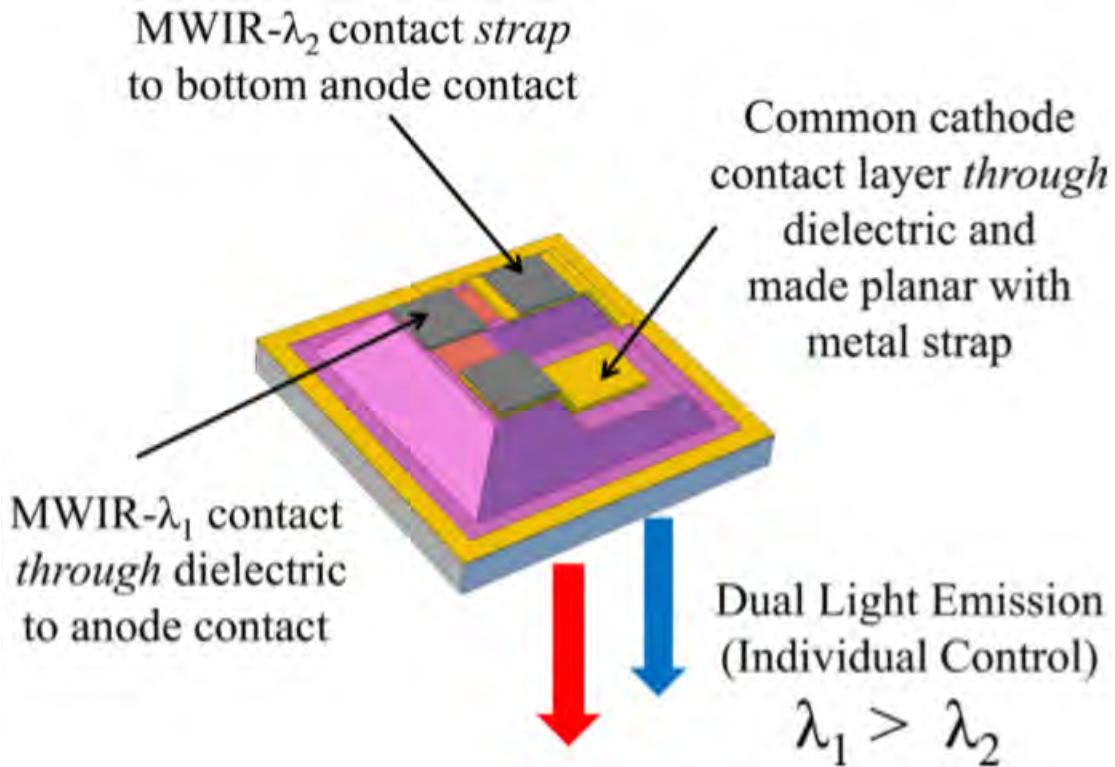


After making the SLEDS there were different other projects that surface, one of which was the Two Color SLED Array or TCSA. The focus of the TCSA project was to developed a system able to display in two different wavelengths in the MWIR region, and the other, was to increase the dynamic range that the SLEDS was missing.

The TCSA system introduced the first LED based IRSP that used dual emission

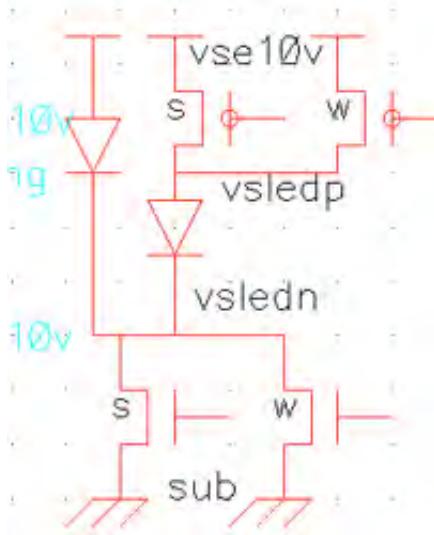


**Figure 3.4:** TCSA pixel wavelengths (left), and Stack structure for the TCSA pixel (right)



**Figure 3.5:** 3D representation of a single TCSA pixel

in two different wavelengths from a single LED stack structure. This dual layer structure for LEDs starts with a n-type GaSb substrate. The next layer consist of a second



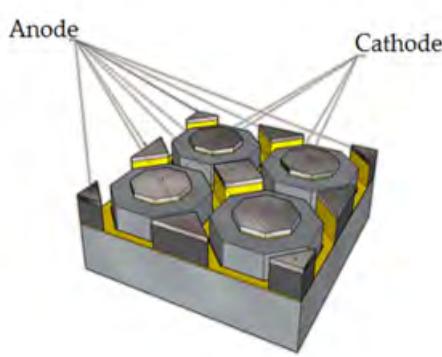
**Figure 3.6:** TCSA driver circuit with two gears per color

GaSb with a neutral doping as it acts as a buffer. Then a layer of AlAsSb is added to ensure the integrity of the lattice. After that layer the p-type GaSb is deposited as it serves as the Anode contact of the LED with wavelength  $\lambda_2$ . The actual emitter region for the  $\lambda_2$  LED is made of undoped 8.2/16 monolayer (ML) InAs/GaSb, and a super lattice (SL) active region that uses a reverse bias p-GaSb coupled to a n-AlInAsSb tunnel junction. A shared cathode contact between the  $\lambda_1$  and  $\lambda_2$  emitter regions is made of p-GaSb. The  $\lambda_1$  emission area is made of the same structure as the active regions of the other. However, the thickness is varied to 10.1/16 ML in order to get a different wavelength. Figures 3.4 shows the side view of the SLED stack for the two color pixel, and it also the intended wavelength for each of the emissions[13, 14, 10].

In the TCSA system we changed the pixel circuit on the RIIC in order to improve the dynamic range that the SLEDS was missing. In the SLEDS there was only one drive transistor and it was very strong. On TCSA a second smaller transistor was added to the mixture. On TCSA since there were two colors per pixel, each of the individual colors had a pair of drive transistors. We refer to the different sized transistors as gears, the smaller transistor being the weak gear and the bigger transistor being the strong

gear. Using these two sizes we had better control over the grayscale for background imagery, and the hot objects were drawn using the **strong** of the the two. Figure 3.6 has a simplified version of the pixel circuitry of the TCSA pixel. Note that because of the structure of the TCSA pixel stack, a pair of drivers are PMOS transistors, and the other NMOS.

### 3.3 Night Glow LED System



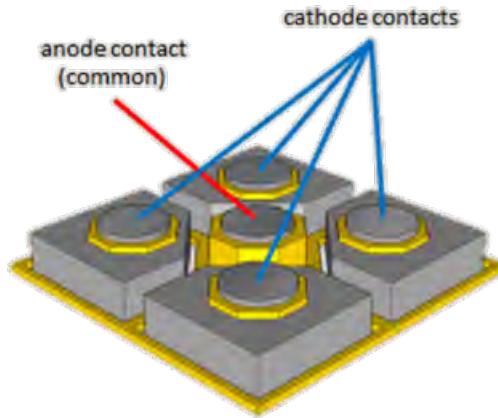
**Figure 3.7:** The NSLEDS Super Pixel consists of 4 pixels with sharing common anodes

The gap between the resolution Focal Plane Arrays (FPA) and the resolution of projector to test them has been getting bigger. A 512x512 resolution IRSP is not enough to test a 1Kx1K FPA or a 2Kx2K. Ideally it would make a better scenario if multiple IRSP pixels map to a single FPA, and not the other way around. The Night Glow LED System (NSLEDS) was part of the third generation of IRSPs which tried to meet the performance criteria that FPA require in order to be tested accurately. The NSLEDS stepped away from the two color scheme offered by TCSA, and instead it is a single **color** array in the  $3\text{-}5\mu\text{m}$  wavelength range. This new generation of emitter arrays also had the pixel pitch reduced to  $24\mu\text{m}$  making the density of pixel 4x as dense, and as a result the total resolution of the array increased to 1Kx1K rather than the previous 512x512 of TCSA and NSLEDS[15].

The NSLEDS RIIC pixel also changed from that of TCSA, the driver circuit consists of two NMOS transistors. Similar to TCSA one is bigger and can output bigger currents while the other is much smaller in size providing smaller currents for the gray scale of background objects. Different **that** TCSA however, there are no PMOS drive transistors as they are less efficient and take up more space.

On the flip side, the SLED pixels were combined into groups of four. A normal LED pixel requires a anode and a cathode contact to function. Since in the NSLEDS array the pixel area was reduced, in order to maintain a high emission area on the LED we wanted to reduce the space taken up by the metal contacts. For this reason each group of four pixels were made to share a common anode in the middle of them as shown in figure 3.7. Additionally there are pieces of anode contacts for every group of four pixels, these smaller anode contacts form complete contacts when tiled to others, we refer to this structure as a super pixel.

### 3.4 High Definition IR LED



**Figure 3.8:** In HDILED the super pixel only had one common anode in the middle

The NSLEDS has a total of five arrays that have been produced up to date, these have slight variations during the assembly process in order to test different features and obtain the best emitters possible. The High Definition IR LED (HDILED) system

is a continuation upon NSLEDS. Both the HDILED and the NSLEDS arrays can be considered to be generation three of IRSP. Just as NSLEDS, HDILED pixel pitch is  $24\mu\text{m}$  and it uses the same RIIC pixel to drive the SLED pixel. HDILED had a slight modification to the SLED super pixel. Different than NSLEDS in HDILED there is only the middle common anode contact per every 4 cathode contacts[16].

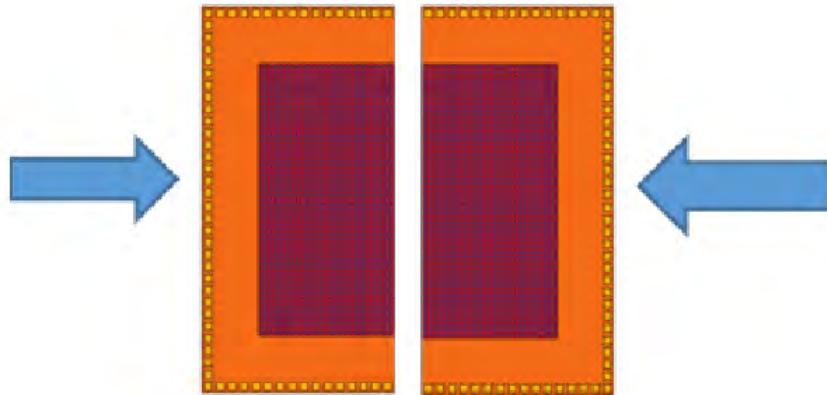
The HDILED system was the first IRSP to have reach a resolution of 2K x 2K pixels. This is a great leap forward in the task to close the gap between FPA and emitters. As of today there are two HDILED systems completed. One is at cvorg labs in the university of delaware and the other is in a lab facility at the university of florida hosted by the air force.

### 3.5 Road to future IR LED systems

We have demonstrated that LED based IRSPs are a feasible solution to the need of testing equipment in the Test and Evaluation (T&E) phase of IR systems. However, development continues and we have to think of ways to improve the current technology as IR systems become harder to test as they become more complex. Developing any sort of IRSP in a resolution of 2K x 2K or higher is very complicated and costly with the current methods. Even though our HDILED systems are operational, they are not at the level they need to be in order to be useful for T&E testing of IR systems. In order to create higher resolution IRSP in the future with high operability, and more cost effective, we have several projects that have explored such areas from different vectors. The focus of this thesis is one of these approaches to increase resolution of arrays by moving to a smaller pixel architecture. Other projects with the same ultimate goal are explained in the following subsections.

#### 3.5.1 AERIA

A way to increase the maximum resolution of our IR LED arrays is to combine multiple arrays into one bigger one by abutting. The Advance Infrared Emitter Array (AERIA) project consisted in growing rectangular RIICs and SLED arrays with a



**Figure 3.9:** Architectural overview of the AERIA arrays

pixels pitch of  $24\mu m$ , and a resolution of  $1K \times 2K$ . After processing, two rectangles are abutted together as close as possible to create a  $2K \times 2K$  single array as shown in figure 3.9. The big picture sounds simple but to get the etching and alightment correct for the two parts proved to be very difficult. As of the time this dissertation was written, the abutment has not been completed on two rectangular parts. More details about this project can be read on Josh Marks' dissertation [2].

## Chapter 4

### INTRODUCTION TO ADVANCE RIIC TECHNOLOGIES FOR INCREASING DENSITY OF ARRAYS

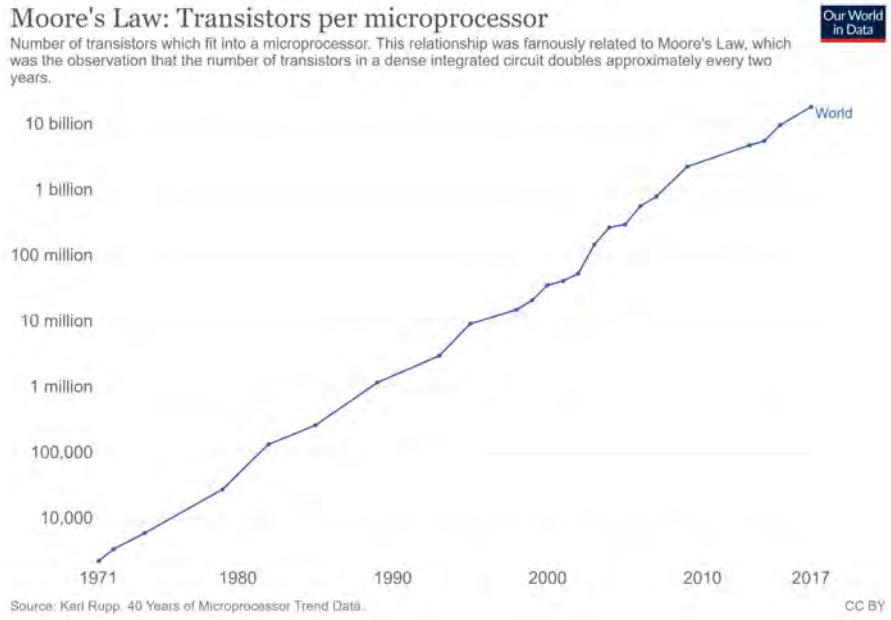
The Advance RIIC Technologies for Increasing Density of Arrays (ART-IDEA) was a program funded by the Guided Weapons Evaluation Facility (GWEF) in Eglin's Air Force Base (AFB). The project was a Small Business Innovation Research (SBIR) phase 1 program. Additionally the program had a partnership between the University of Delaware, Chip Design Systems (CDS) Limited Liability Company (LLC) and Firefly Photonics.

#### 4.1 Motivation for ART-IDEA

There is a big gap between the resolution of FPA used on IR systems and the IRSP systems used for T&E. There is a big need to close this gap and this is where the ART-IDEA program becomes relevant. The ART-IDEA program main goal was to explore a way to increase the resolution of projector arrays, and in the process, attempt to increase the wall-plug efficiency of the emitter systems as a whole.

Gordon E. Moore predicted that the number of circuits on a given surface area would double approximately every 2 years as shown in figure 4.1. With smaller transistors there is a possibility of decreasing the size of the RIIC pixel and thus increasing the number of pixels for a given area. The current pixel pitch used by our arrays is  $24\mu\text{m}$  and in a space of 1 inch squared we can fit 1Kx1K pixels. With the proposed architecture of the ART-IDEA RIIC we are aiming at a  $12\mu\text{m}$  pixel pitch with 2Kx2K pixels in the same space. For all of the previous generations of RIICs we used the AMIS500 CMOS technology where the smallest featured transistor width is  $.6\mu\text{m}$ . For

ART-IDEA we moved away to use a smaller transistor technology, ONC18, which has a  $.18\mu\text{m}$  featured size for the smallest width transistor.



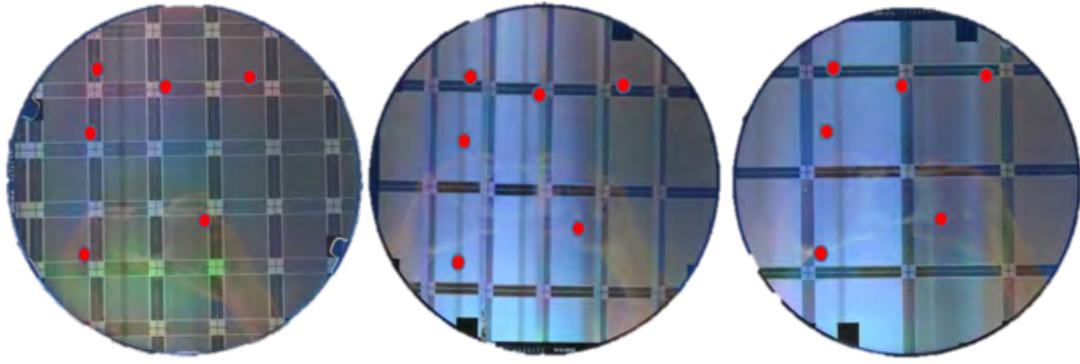
**Figure 4.1:** Moore's Law data collected over 40 years showing the expected behavior

## 4.2 Wafer Yields for RIICs

One of the biggest motives to pursue smaller RIICs is the increase in the number of working parts per wafer. In semiconductor fabrication, the yield of chips is a function of their surface area, human error, design flaws, processing error, contaminants, and individual yields for the different layers. Over the years the fabrication process for semiconductors has been refined to the point where for many modern wafer processes the yield can be as high as 98% or more[17, 18, 19]. With the current fabrication technology most of the issues that cause lower yields can be neglected and only the surface area of the chip stays as the dominant factor for lower yield[17, 18, 19]. This is illustrated on figure 4.2 which shows three different 8" wafers we have designed and fabricated at OnSemiconductor. The wafer on the far left corresponds to TCSA and

NLEDS RIIC die, the middle wafer is the AERIA RIICs, and the right wafer is the HDILED RIICs.

During the early stages of research and development (R&D) of our infrared systems, we had to fabricate and test the different versions of RIICs for the different programs. The RIICs have telemetry that can be configured to access most pixels on the RIIC and measure the current the drive transistors output for both gears. From the wafer testing phase we were able to discriminate those chips that didn't perform as expected from those that produce the correct behavior.

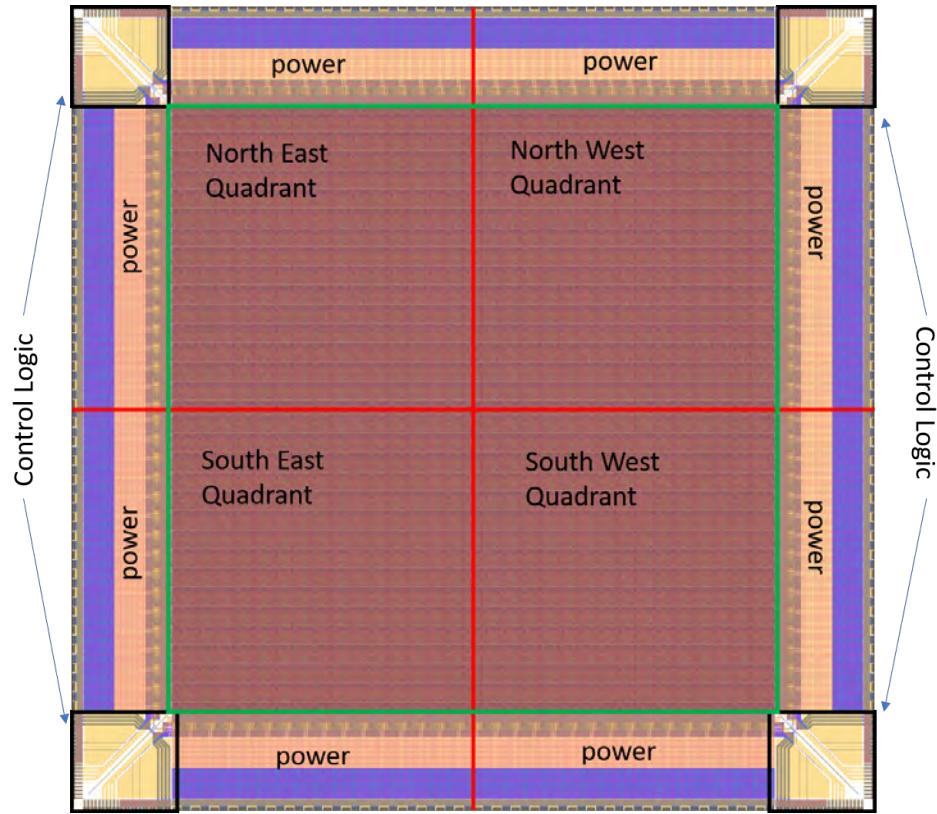


**Figure 4.2:** Bigger chip size per wafer greatly reduces the yield per wafer

#### 4.2.1 Wafer Testing Methodologies

The RIIC is designed to have all of the digital logic located on the corners of the chip. This logic includes many buffers, communication circuitry, bias circuits, shifters, address decoders, and many control circuitry. Each of the corners is identical to each other except for the fact that they are rotated 90 degrees in relation to their adjacent corners. The corners are not able to communicate with each other inside of the rest of the RIIC circuitry, in order to do this the carrier PCB board where the chip is mounted needs to enable this. As a result of the design, the RIIC is divided into four individually controlled quadrants where each of the corner logic controls a fourth of

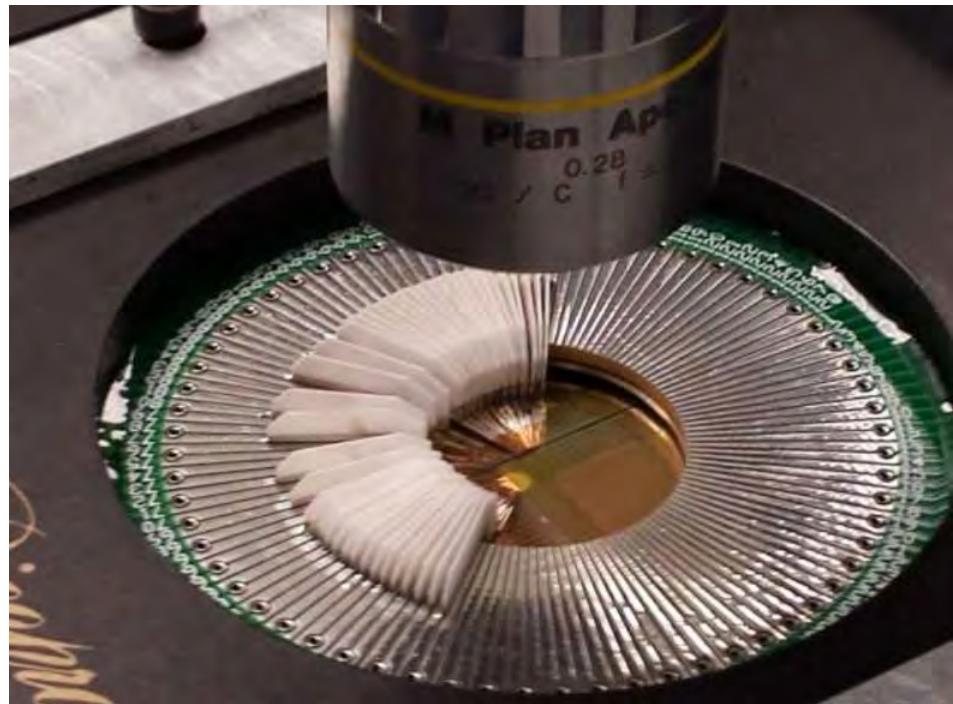
the pixels. To get a better picture, we can refer to figure 4.3 as it shows exactly the division on the RIIC.



**Figure 4.3:** Break down of the RIIC chip, each of the quadrants is controlled by the appropriate corners containing all the digital logic. The rest of the perimeter is used to bring in all the high power voltage rails and return paths

The RIIC architecture was done in such a way that the speed of writing data to a pixel can be controlled by the number of channels active. A channel is simply a path that delivers analog data to a pixel setting the brightness of such. A total of seven modes were implemented to the architecture of the RIIC, six of them are parallel, and one is serial. The parallel modes activate channels by powers of two, for instance, the mode one writes to 1 pixel per write cycle, mode two has two channels active and writes 2 pixels per write cycle, mode three does 4 channels, and so on until mode six which uses 32 channels per write cycle. In other words, mode six is 32X faster than mode

one, but, this also means that mode six uses 32 inputs where mode one only needs 1. Apart from the channel analog inputs, when using the RIIC in a parallel mode all the other signals that are required to write to a pixel, such as addressing lines, are also brought in using parallel inputs. Dealing with many signals makes it extremely hard to test RIICs on a wafer. For this reason, the serial mode on the RIIC was implemented. The serial mode uses the Serial Peripheral Interface (SPI) protocol and combines all the signals that would be required to run the RIIC in parallel mode one into a single stream of serial data. This greatly reduces the speed at which one can write to the RIIC, but during wafer testing the focus is to find out the yield of the chips thus speed is not important.



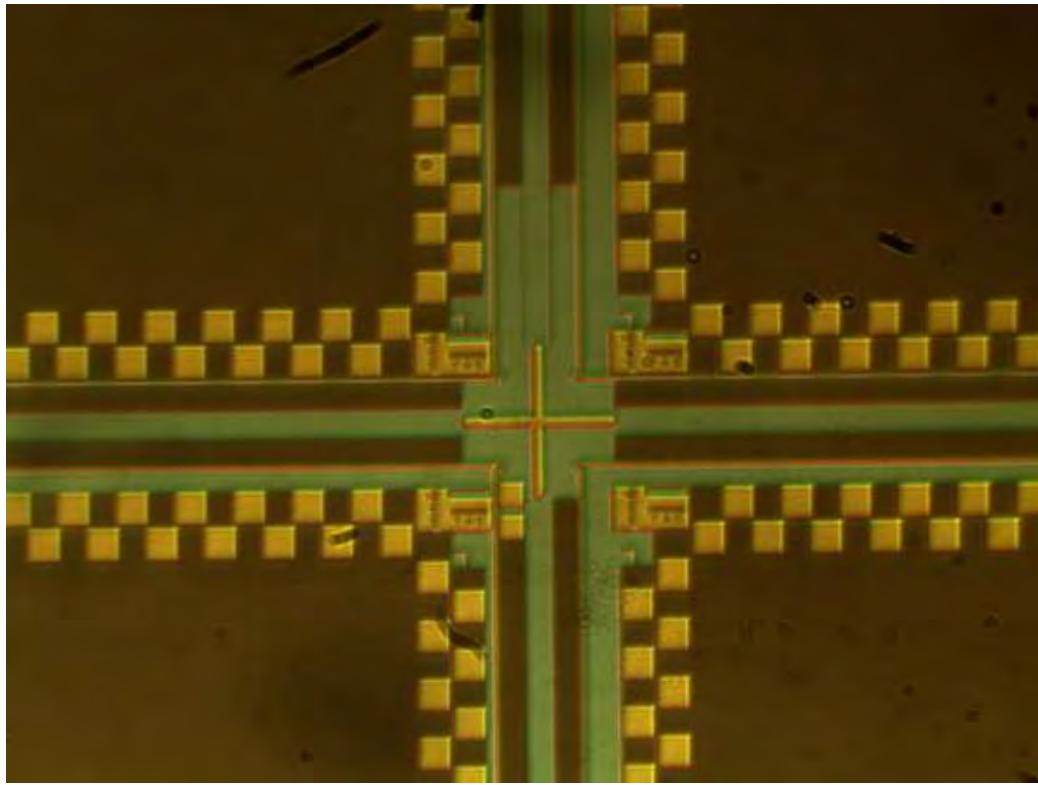
**Figure 4.4:** Custom probe card used to test RIICs on wafers

As shown in figure 4.4, we designed a custom probe card that allow us to touch down on the necessary RIIC pads required to make the chip run in SPI mode. Figure 4.5 shows an area of the wafer where four RIIC chips meet. The probe card only

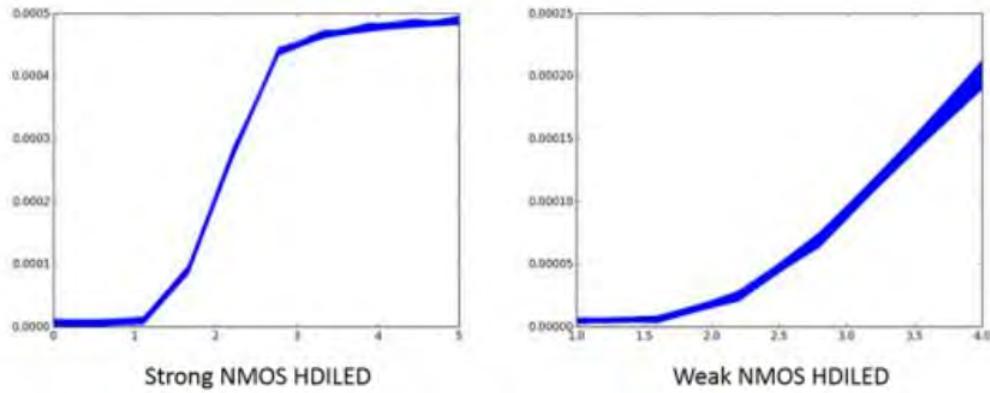
touched down on a single corner at the time, meaning that if we wanted to test a different corner of the same chip we rotated the wafer to match the orientation of the probe card. The test for all the RIICs on a wafer were as follows: 1) pick a corner of the chip, align the probe card and touch down. Then do a continuity test on certain points on the card to test for good contact. 2) Test all of the power rails for shorts against ground or other power rails. 3) Using the SPI features of the RIIC, program the chip to sweep the first 10 drive transistor in weak gear, and then in strong gear. The sweeps were set up to go from 0V to around 5V, depending on the chip, with 10 steps. The current output of the drive transistors was measured and collected with a Keithley 2400 meter and plotted as shown in figure 4.6. 4) If the RIIC showed signs of life, we picked a pseudo random pattern where 1 out of every 10 super pixels in the quadrant under test was swept for both their weak and strong gear. 5) Once finished with a RIIC we tested all others on the same corner as the probe card was lined up. 6) Rotate the wafer 90 degrees and do all previous steps. This was done until all corners of the RIICs were tested[20, 21, 22].

#### 4.2.2 Results of Wafer testing

All of the results obtained during wafer testing were logged and compiled into a database so that we can analyze them and pick the best performing RIICs. As this was a new design architecture there were no guidelines or standards to follow as to what is considered to be a "best performing RIIC". We only had simulation data to base our initial conclusions upon. After collecting data from the first wafer we realized a couple things, A RIIC's performance can vary from quadrant to quadrant, and the current output of the drive transistors can vary slightly in some RIICs. For our finalized agreement of qualification for a RIIC's performance we decided to compare curves against each other within their own corresponding quadrants. For a set of curves, the median was picked as the reference point. The reason why choosing the median is a better statistical choice for our data sets is because many data points had significant clusters of outliers that would skew the mean of the set. From the median curve a



**Figure 4.5:** RIIC corners under a microscope



**Figure 4.6:** Sample curves collected during wafer testing to check if the RIIC chip showed signs of lift<sup>↑</sup>

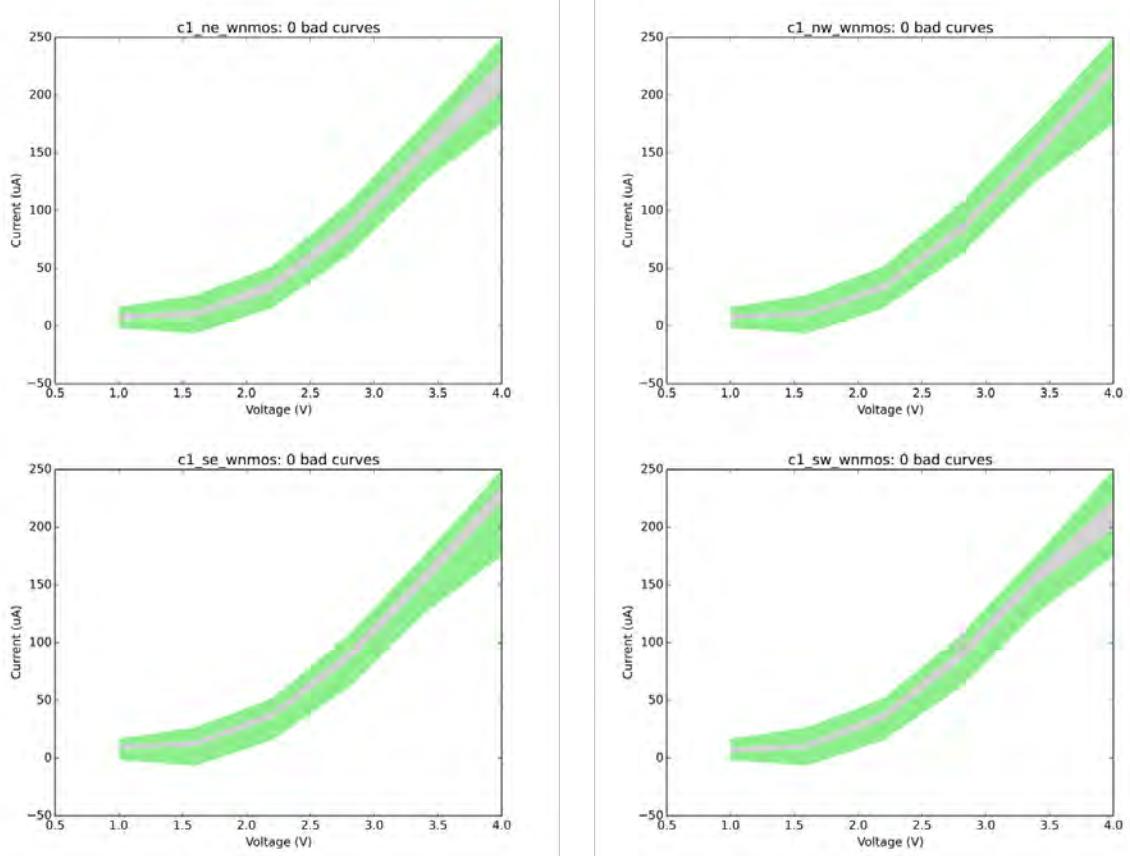
quantum range was chosen based on a number of standard deviations. This range was smaller for those points near 0V as there is almost no variation, but larger on the

higher end where the transistors' output varied more[22]. Figures 4.7 and 4.9 are an example of the visual output our analysis produced. The green area encompass all the area on which a curve can be considered "good" for the application of the RIIC, if a curve goes outside the green area it is labeled as "bad" and thus incapable of driving an LED pixel in a predictable manner. The gray area on the same figures are all of the curves that fall within the given range and thus considered "good". Last but not least the black colored curves are those that go outside the boundaries of the green area and produce undesired output. For this example, some of the best performing RIICs for NSLEDS and HDILED projects were picked[22].

In a NSLEDS or TCSA wafer it was common to find a few die that had 100% of the transistors tested output the expected curves. However, for our HDILED or AERIA wafers this was not the case. The HDILED set shown on figure 4.9 has a total of 183 detected "bad" curves, which represents about .6% of the total curves collected. This is not ideal but due to the low yields of the HDILED chips we took die like this one as an option for hybridization. Figures 4.8 and 4.10 display the exact location of all the pixels tested. Green colored pixels are all those labeled as "good", yellow are those that were labeled as "bad", everything are those pixels that did not get tested due to our psudo random pattern. The scale for the pixel map images are x and y coordinates in terms of super pixels. For instance, a NSLEDS RIIC has a resolution of 1024x1024 pixels, so each of its quadrants is 512x512, and since a super pixel is the grouping of 4 pixels, the scale on the image is 256x256 for each quadrant. The same applies to the HDILED image with the exception that the original resolution is 2048x2048 pixels.

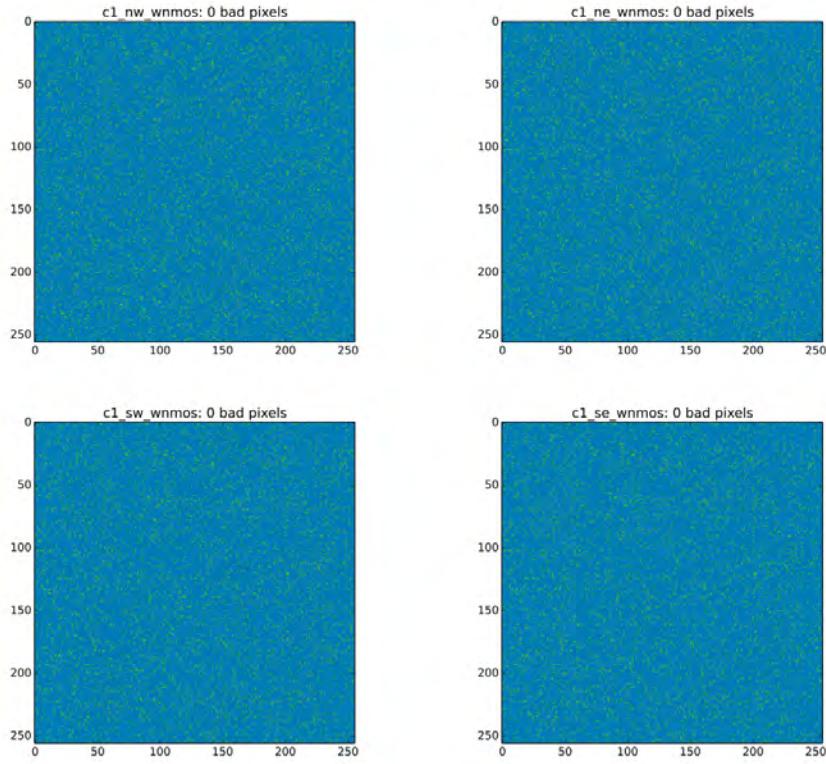
#### 4.2.3 Summary of Yield of RIICs

We know that IRSP have to reach higher resolutions to keep up with large format FPA. Higher resolution means bigger RIICs and SLED arrays. But after seeing the massive drop in wafer yield of the 2kx2k format of HDILED, we decided to explore other options to increase yield. Lower yields increase the cost of making hybrids as more wafers need to be fabricated, and more time and resources are allocated to testing



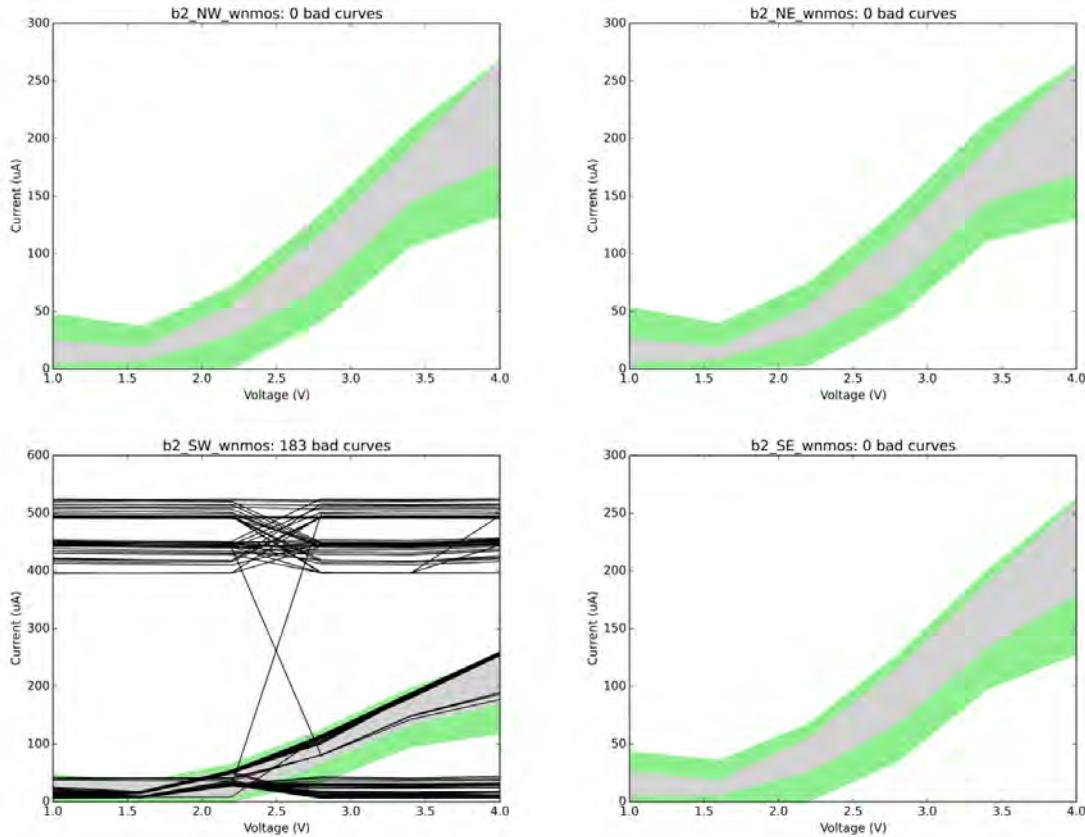
**Figure 4.7:** Example of NSLEDS yield of transistors, candidate for hybridization. Curves represent the current output of the transistors as a function of voltage applied at the gate.

them. For NSLEDS wafers we found at least 4 RIICs per wafer that could be used for hybrids, in AIREA wafers that number was 1 per wafer, and in HDILED it took 6 full wafer before we found a decent RIIC. The architecture for these three RIICs was the same, the only differentiating factor was their size. On an 8-inch wafer 19 NSLEDS RIIC can be grown, 8 AIREA RIICS, and only 4 HDILED RIICS. Figure 4.11 shows the cost per part to obtain a single RIIC. As of 2019 the largest resolution IRSP in the world is at the University of Delaware and it is the HDILED systems that is still being developed. Resistor array projectors have a 1Kx1K projector that is physically the same size as our HDILED hybrid. However, some FPAs would benefit from an even higher resolution IRSP, but the cost of such a part with the LED technology would

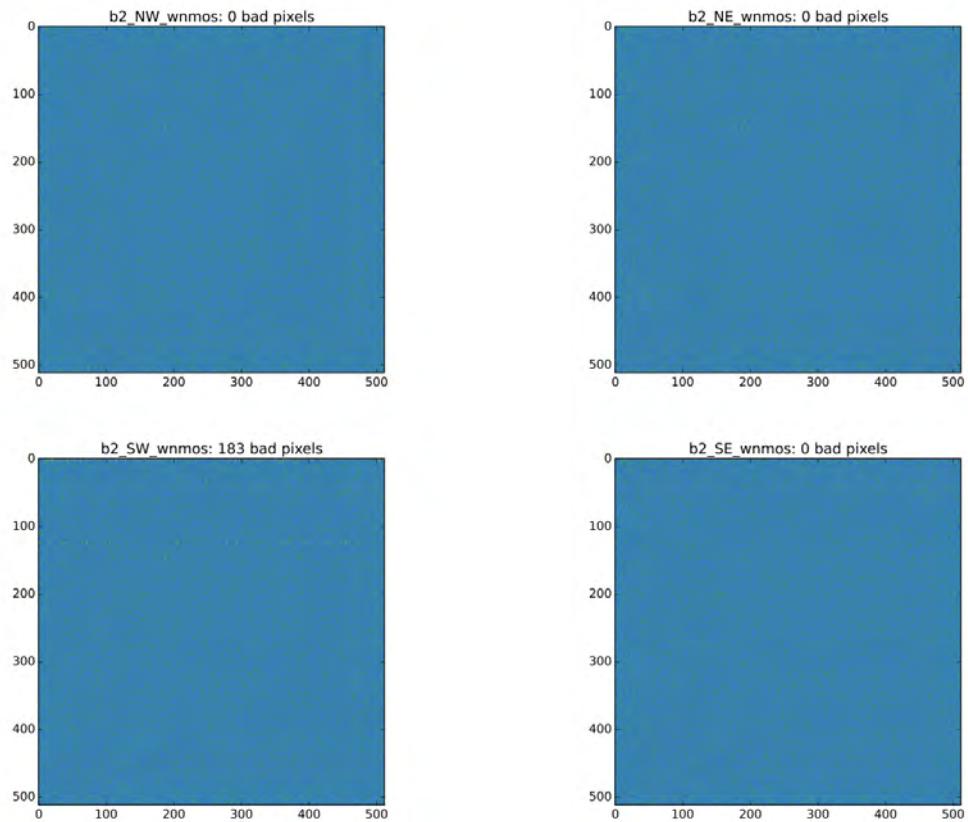


**Figure 4.8:** Pixel maps for all the quadrants of the NSLEDS RIIC shown on figure 4.7, the pixels are mapped one to one to their actual location on the RIIC

too high. If we continue with the same architecture the size of such RIIC would be 4X larger than the current HDILED, fitting only one part per wafer.

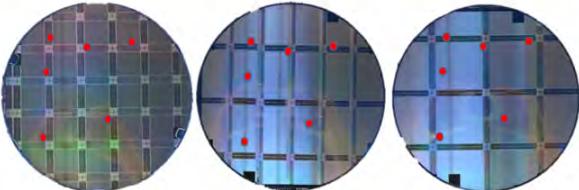


**Figure 4.9:** Example of HDILED yield of transistors, candidate for hybridization. Curves represent the current output of the transistors as a function of voltage applied at the gate. Because of the low yield of such a big chip, parts that had "bad" pixels were considered for hybridization as long as the number was below 1%



**Figure 4.10:** Pixel maps for all the quadrants of the HDILED RIIC shown on figure 4.9, the pixels are mapped one to one to their actual location on the RIIC

<b>Generation→</b>	<b>TCSA</b>	<b>NSLED</b>	<b>AIREA</b>	<b>HDILED</b>
<b>Physical size</b>	1"x1"	1"x1"	1"x2"	2"x2"
<b>Cost per die</b>	\$1K	\$1k	\$5k	\$30k
<b>Resolution in pixels</b>	512x512	1kx1k	1kx2k	2kx2k



TCSA/NSLEDS      AIREA      HDILED

**Figure 4.11:** cost per part for different RIICs, with the  $24\mu\text{m}$  pixel design it is very costly to make a 4+ million pixel projector

## Chapter 5

### DESIGN OF THE TEST CHIP

The goal of this effort is to create a prototype that showed there is a path to increase the resolution of IRSP by shrinking the pixel's area by four. There are various CMOS technology libraries that can be used to achieve the end result. However, different technologies may have certain advantages or disadvantages over others. The one parameter that remains true across any CMOS technology chosen is the fact that most of the logic is static. The only exception being the last stage of the pixel driver that uses an analog circuit. Static CMOS logic has very low power consumption, and in near ideal conditions this can be neglected and assumed to be very close to 0 W.

#### 5.1 Picking the right tools for the job

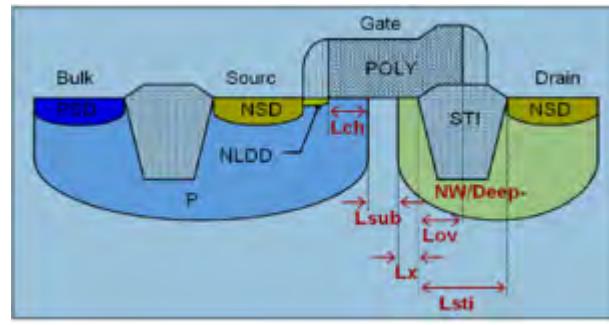
Attributes	AMIS500 5V	ONC18 1.8V	ONC18 3.3V	ONC18 5V
Minimum Feature Size	600nm	180nm	340nm	600nm
Single Device Area	6.40 $\mu\text{m}^2$	1.68 $\mu\text{m}^2$	1.86 $\mu\text{m}^2$	3.66 $\mu\text{m}^2$
Metal Layers	5	6	6	6
Thick Metal Option	yes	yes	yes	yes
High Voltage Transistor	12V	15V	15V	15V

**Figure 5.1:** Comparison between different CMOS technology libraries

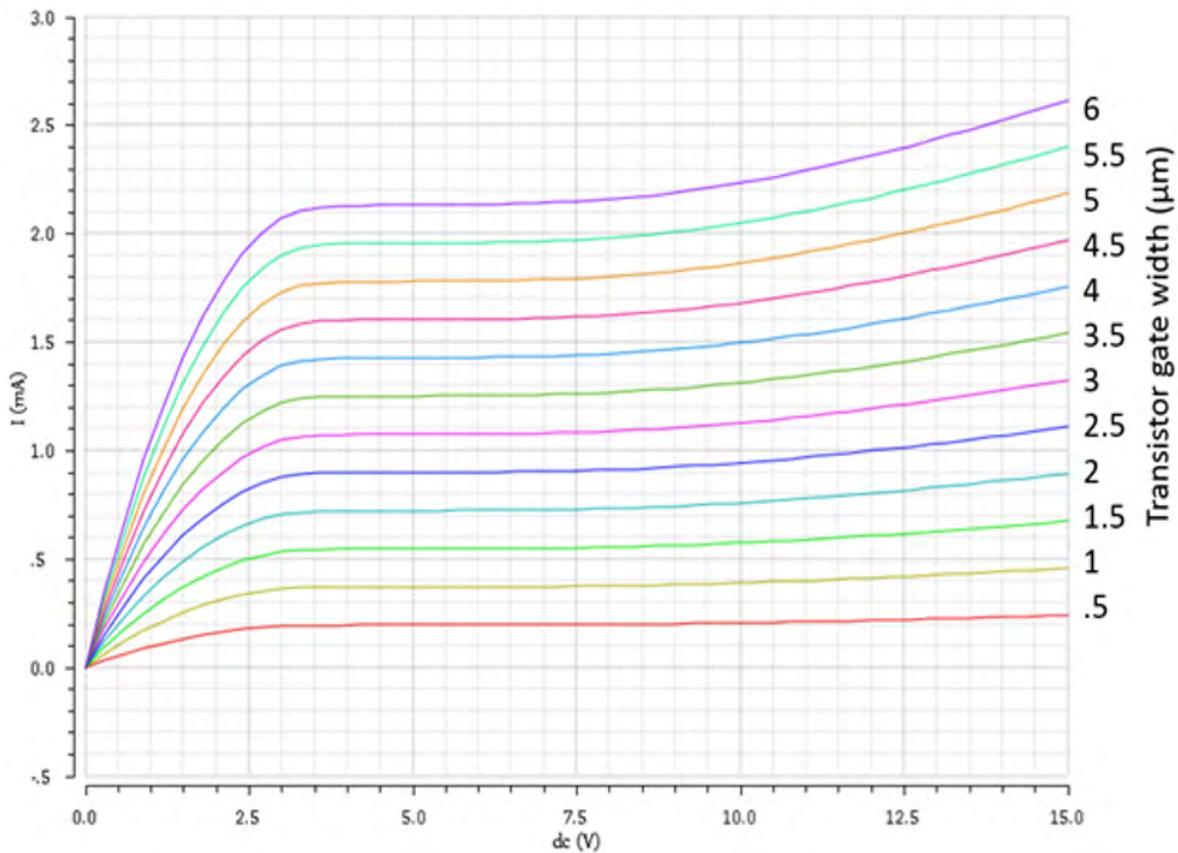
In order to be successful in increasing the number of pixels for LED based IRSPs, we decided to shrink the area of the RIIC and SLED pixel from  $24\mu\text{m}$  to  $12\mu\text{m}$  pitch. From the RIIC perspective this means that now there is a quarter of the area available to fit the circuitry. As previously mentioned, the circuitry architecture for all RIICs up to date has been done using the AMIS500 technology library from ON Semiconductor (OnSemi). The AMIS500 smallest base CMOS is a 5V with a minimum featured length

of 600nm and area of  $6.40\mu\text{m}^2$ . The ONC18 technology library, also from OnSemi, offers more options for smaller transistors. The smallest process is a 1.8V transistor with its smallest featured size being 180nm, followed by a 3.3V process with its smallest feature being 340nm. Table 5.1 shows a quick overview comparing the AMIS500 technology library to three of the candidate technology libraries offered by ONC18. The most important qualities I looked for when making the decision of which technology to used were the size of the components in terms of area and minimum feature size, and the high voltage transistors available. Originally, I thought the choice was obvious and it seemed that ONC18 1.8 V was the best option for the design. However, after initial experimental design work, ONC18 1.8V had minor inconveniences that had me considered the ONC18 3.3V option[23].

One limitation of the onc18 1.8V CMOS process is the fact that it does not contain any parts with a gate voltage of 1.8V and a Voltage drain to source ( $V_{DS}$ ) greater than 1.8V. The documentation for the onc18 library specifies that a 1.8V gate transistor with a  $V_{DS}$  of 5V is available. However, such a part does not exist and it turned out to be a typo in the documentation as confirmed by Onsemi. Thus, to continue to use the 1.8V process for the design, there would have to be level shifting circuitry introduced to the pixel to reach higher voltages and drive the larger transistors. Some disadvantages of using level shifters include increasing the total area needed for circuitry, the increase of power dissipation, and it could become error prone during operation. On the other hand, the 3.3V CMOS process has a transistor where the gate voltage is 3.3V and  $V_{DS}$  can go up to 15 Volts. The only disadvantage is that 3.3V transistors are slightly bigger by default than their 1.8 V counterparts, but the small difference is still manageable and it becomes nulled if more circuitry were to be introduced. Taking this into consideration I focused my efforts in moving forward with the design phase using the 3.3V process.



**Figure 5.2:** NLD MOS structure for the 3.3V process



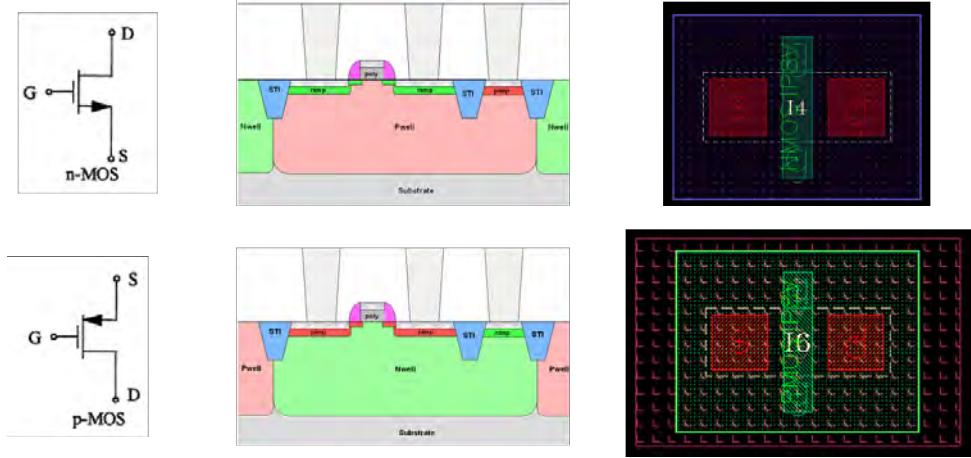
**Figure 5.3:** IV curves for NLD MOS transistors with different physical sizes

### 5.1.1 N-type laterally diffused high power transistor

As mentioned already the 3.3V process has a very attractive N-type laterally diffused MOS (NLDMOS). The NLDMOS found in the ONC18 technology library is shown on figure 5.2, and it has an asymmetric structure as it helps lower the on-resistance, the channel of an NLDMOS is a function of its source diffusion, drain diffusion and gate length. This type of transistors are widely used for radio frequency (RF) application as they can provide a higher gain for amplifier applications, and overall can handle higher voltages and currents without extra circuitry[24, 25]. For the purposes of the first prototype  $12\mu m$  RIIC pixel the NLDMOS offered great flexibility for the type of LED that can be used on a potential future hybrid. During the design phase it was hard to predict what a  $12\mu m$  pitch IR LED would behave like, or if it was going to work at all. Thus an adaptive RIIC that could handle different current and voltage levels became a necessary asset. As shown in figure 5.3, using these transistors available on the 3.3V process makes it possible to achieve that flexibility. Using a parametric DC sweep simulation, it is possible to obtain transistor IV curves where the gate is at 3.3V, source tied to GND and the drain swept from 0 to 15V, the full range of operation for these devices. The other variable is the actual size of the NLDMOS, the curves shown are for sizes starting at  $.5\mu m$ , the smallest available size for NLDMOS, up to  $6\mu m$ , anything bigger would take too much area of the RIIC pixel. The fact that the current holds very steady for a good portion of the curves, regardless of drain voltage, makes it ideal for designing a RIIC that can drive different SLED parts with different turn on voltages.

### 5.1.2 VLSI techniques relevant to the project

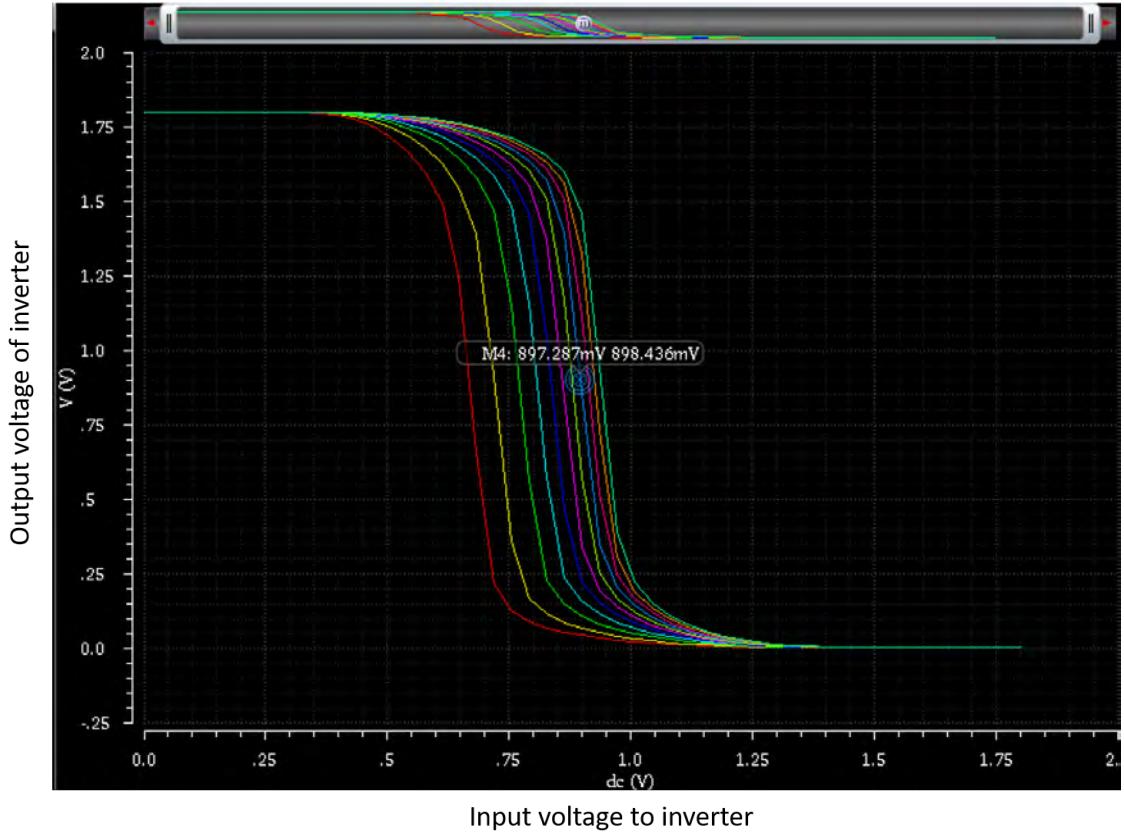
Very large scale integration (VLSI) is the process used by industry to create very complex integrated circuits (IC). This is the design at the semiconductor level in hardware. The basis for any IC is the transistor, the candidate technologies to make the first ART IDEA prototype RIIC use CMOS transistors as their base. In CMOS transistors there are two types of transistors, the NMOS and the PMOS. Between these



**Figure 5.4:** VLSI CMOS transistors, NMOS (top) are grown on a p-well, and PMOS (bottom) are grown on a n-well

two devices millions of combinations can be arranged in order to create simple circuits which can be combined to created very complex circuits in an IC. As seen in figure 5.4, CMOS transistors behave similar to a capacitor at the gate, there is a insulator between the polysilicon and the body of the transistor. In order for the transistor to turn on the voltage at the gate has to be  $V_{thres} \leq V_g$  for an NMOS or  $V_{thres} \geq V_g$  for a PMOS. For a NMOS transistor both the source and drain regions are negatively doped creating diodes where the body acts as the  $p$  and source or drained are the  $n$ . Similarly, these diodes are also formed on the PMOS but with reverse polarity as the source and drain are positively doped.

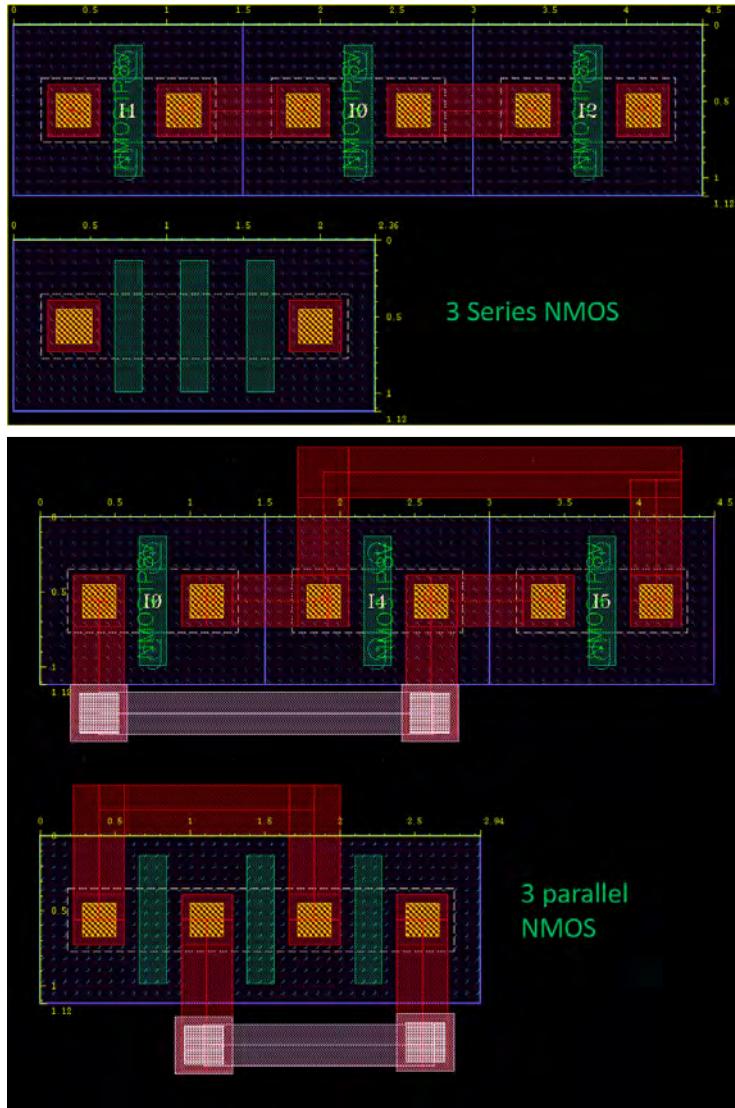
In Cadence, the software used to design the IC, the polysilicon mask for the gate of the NMOS is shown in green on figure 5.4, the metal contacts for the source and drain points are the solid red squares, the white dashed rectangle represents the active region where the transistor is formed. All of the structure is surrounded by a n-implant (nimp) mask that tells the software that the whole **area** will be negatively doped. The PMOS transistor is drawn very similar in Cadence, however, there are two differences. The first, a p-implant (pimp) mask is used to surround the entirety of the transistor area. The second, The n-well mask has to be drawn to indicate that the



**Figure 5.5:** This simulation shows the effect of having a mismatch in mobility of the pull-up and pull-down CMOS logic. Ideally the mobility has to equal on both the PMOS pull-up network or the NMOS pull-up network. However, in some scenarios it might be beneficial to have a faster rise time and a slow fall time, or vice versa. The simulation shown is a DC sweep of the input of an inverter where the size of the NMOS transistor is kept constant at 420nm while the PMOS size varies from 250nm to 2000nm with 11 steps. Since this is the ONC18 Technology the best match for no skew is when the PMOS is around 1400nm

transistor must be grown an n-well. The cadence software is configured to automatically assume that if there is not a n-well mask, then the underlying substrate is a p-well.

In VLSI a simple inverter is made from only two transistors, a NMOS and a PMOS, where the source of the NMOS is tied to ground (GND), the source of the PMOS is tied to voltage drain (VDD), the gates of both are tied together and serve as the input, the drains are also tied together and it becomes the output. The



**Figure 5.6:** Top: Sample shows how to utilized the techniques discussed to maximize area of Series CMOS. Bottom: Same techniques applied to a parallel network of 3 CMOS

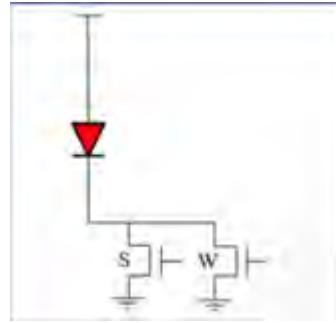
simple inverter is an important circuit because it allows us to easily understand certain characteristics about static logic. For example, the mobility of electrons is better than that of holes, in other words, NMOS transistors have better mobility than PMOS. For this reason, PMOS are usually larger in size than NMOS transistors to equalize the mobility variable. If the mobility of between the NMOS and PMOS logic in a static circuit differs, the fall and rise time will be skewed towards the network with

the highest mobility. In the ONC18 technology libraries the difference in mobility of NMOS is roughly 3 times bigger than the mobility of PMOS transistors. Figure 5.5 is a good visualization of how the fall time of the inverter shifts depending on the size of the PMOS pull-up network in relation to the NMOS pull-down network. This is true for all static logic circuits during fall or rise time. A good rule of thumb is to size the transistors depending on the worst case scenario and make their RC constants equal for such case.

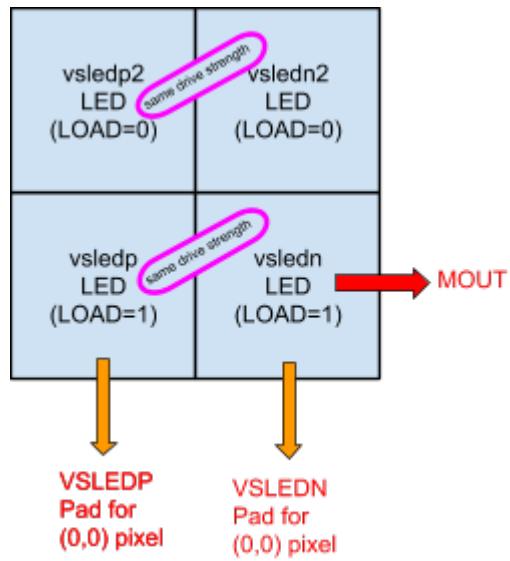
A very powerful technique that can be used in VLSI is combining several transistor by fusing common shared areas. Using this technique we can save valuable semiconductor layers area by condensing all logic into compact blocks. It works as follows: Whenever two or more transistors of the same type are next to each other, the wells can be joined together and shared. Whenever two or more transistor of the same type are connected in series, all of the inner contacts can be removed. Whenever two or more transistors of the same type are connected in parallel to each other, common metal contact points can be paired together into a single metal contact. Figure 5.6 is a basic example on how all these techniques can be used to greatly minimize the semiconductor area needed for a CMOS circuit. In the example three minimum size NMOS are connected in series and then in parallel. Ignoring the metal traces for the parallel connections, both of these configuration take up an area of  $4.5\mu m * 1.12\mu m = 5.04\mu m^2$ . When these two configurations are condensed the semiconductor area for the compacted series circuit is  $2.36\mu m * 1.12\mu m = 2.64\mu m^2$ , and for the parallel compacted circuit the area becomes  $2.94\mu m * 1.12\mu m = 3.29\mu m^2$ . This equates to 52% and 65% of the original area respectively. Taking these methods and applying them to millions of transistors helps decrease the total area for the chip significantly[26, 27].

## 5.2 Base Design is NSLEDS

The pixel design used for the NSLEDS RIIC has been tested and proven to work reliably, as a result this same design carried over to the HDILED RIIC. Both of these RIICs have a pixel pitch of  $24\mu m$ , have been hybridized to SLED wafers, and have been

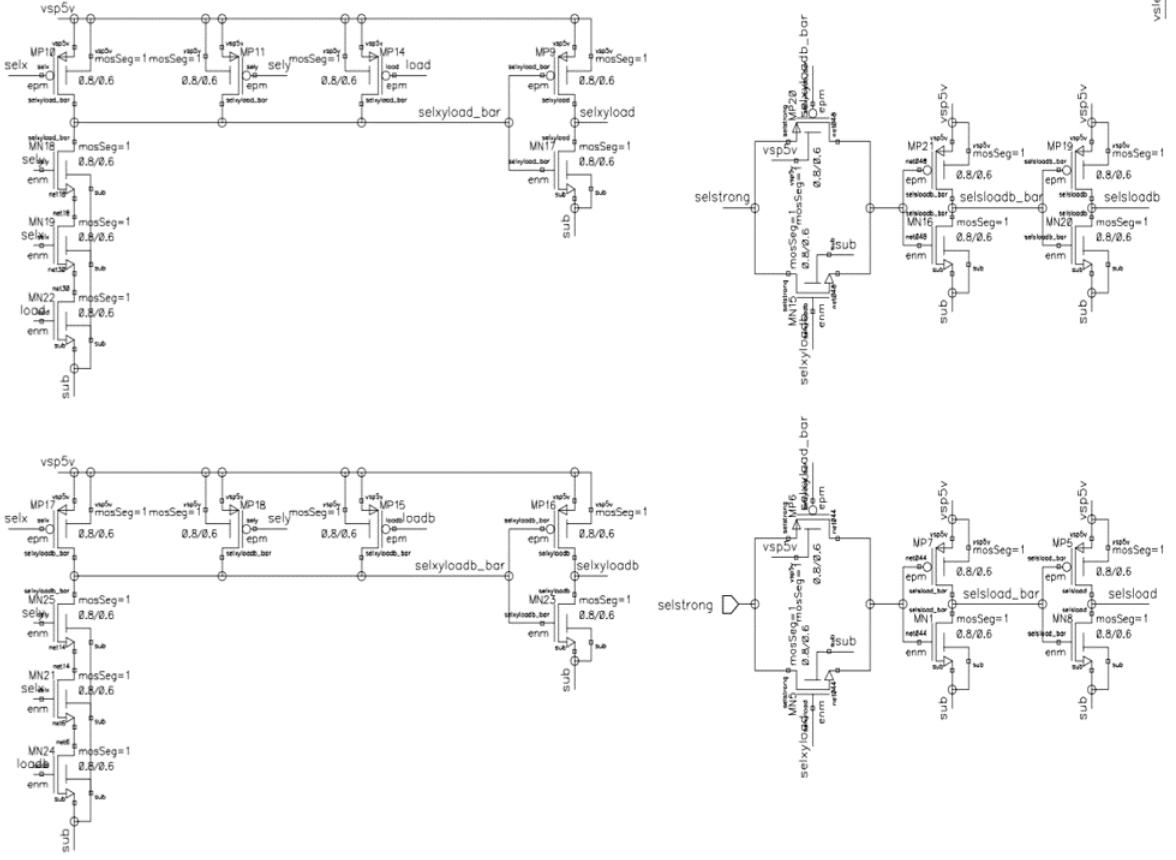


**Figure 5.7:** Simplified version of the NSLEDS pixel design



**Figure 5.8:** NSLEDS super-pixel top level design diagram

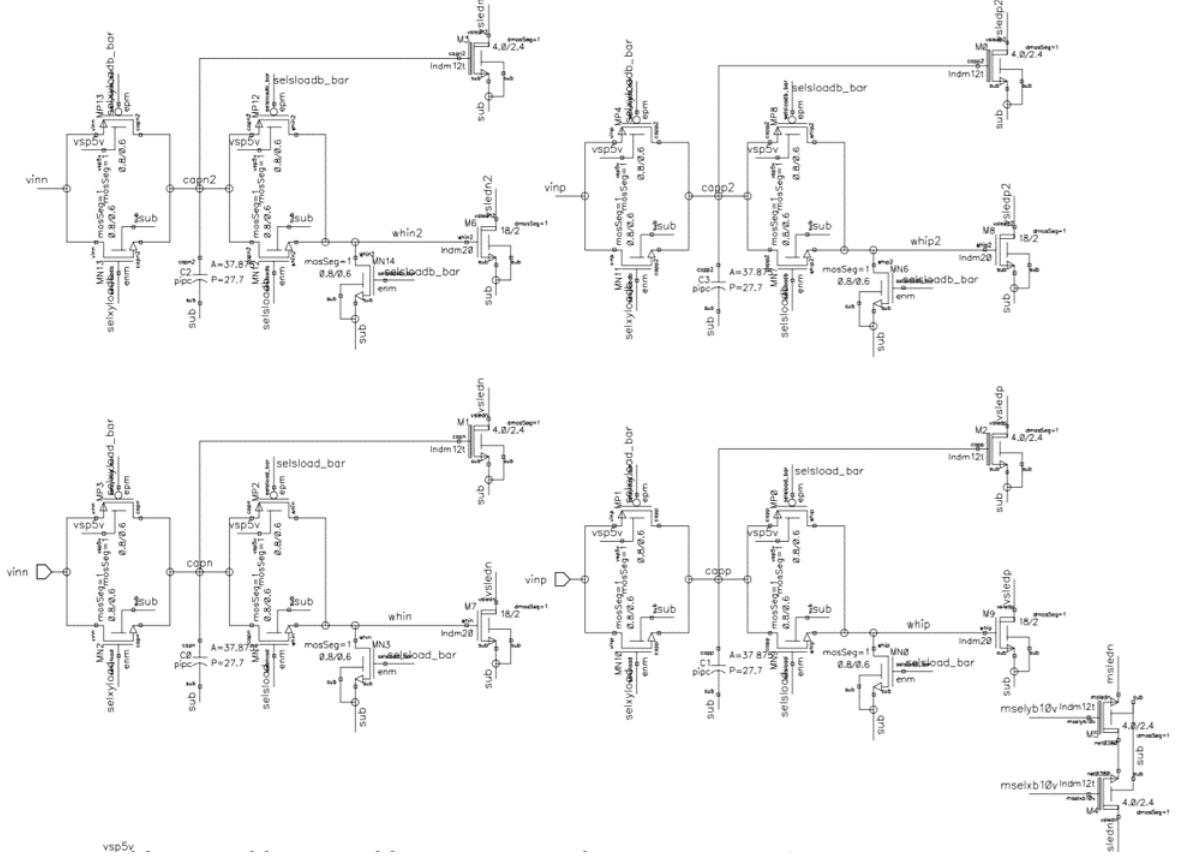
integrated into operational IRSPs at lab facilities in the University of Delaware and the Air Force base in Destin Florida. As a result, we decided the design of the ART-IDEA  $12\mu m$  pitch RIIC pixel would be based on the NSLEDS pixel. To better understand how the NSLEDS pixel works, let's take a look from a high level perspective and then start diving down into the details. The concept is very simple, at a high level a pixel on a hybrid consists of an emitter, in this case an IR LED, and a pair of transistors that provide a way to control the current flowing thru the LED. As mention before, we refer



**Figure 5.9:** Address decoder (left) and gear selector (right) circuits for the NSLEDS super-pixel design

to these transistors as gears, the reason being is because one transistor is much bigger in size compare to the other. As a result, the amount of current varies significantly as the smaller gear can only pull currents in the micro-amp range while the bigger gear can pull currents in the milli-amp range. Figure 5.7 shows the simplest way to think about a single pixel in any of our current generation IRSPs. Starting with TCSA, all the IRSPs we design have this dual gear in order to provide more dynamic range to imagery being displayed on the array. The small gear is utilized to draw atmosphere imagery while the strong gear is used to drawn objects that would appear really hot to the sensor such as a fire or explosion.

NSLEDS and HDILED RIICs use a 2x2 super-pixel architecture that can be



**Figure 5.10:** Driver circuits for all 4 pixels within a NSLEDS super-pixel and MOUT circuit (bottom right)

better understood by examining the diagram shown on figure 5.8. A 2x2 super-pixel works in a time multiplexing manner, within it, there are two pairs, the first pair is activated when the LOAD signal is asserted HIGH. This first pair of pixels uses the naming convention of vsledp and vsledn. The second pair of pixels, vsledp2 and vsledn2 are active when the LOAD signal is LOW. All of these pixels are identical and can reach the same drive strength if the user wishes to do so. Inside of the super pixel there is a small circuit that allows the user to get some telemetry data. This is the MOUT line that is used during wafer testing to check if the super-pixel is alive. However, due to spacing constraints within the super-pixel only vsledp and vsledn can be monitored during wafer testing. When either of the LOAD pairs are active two

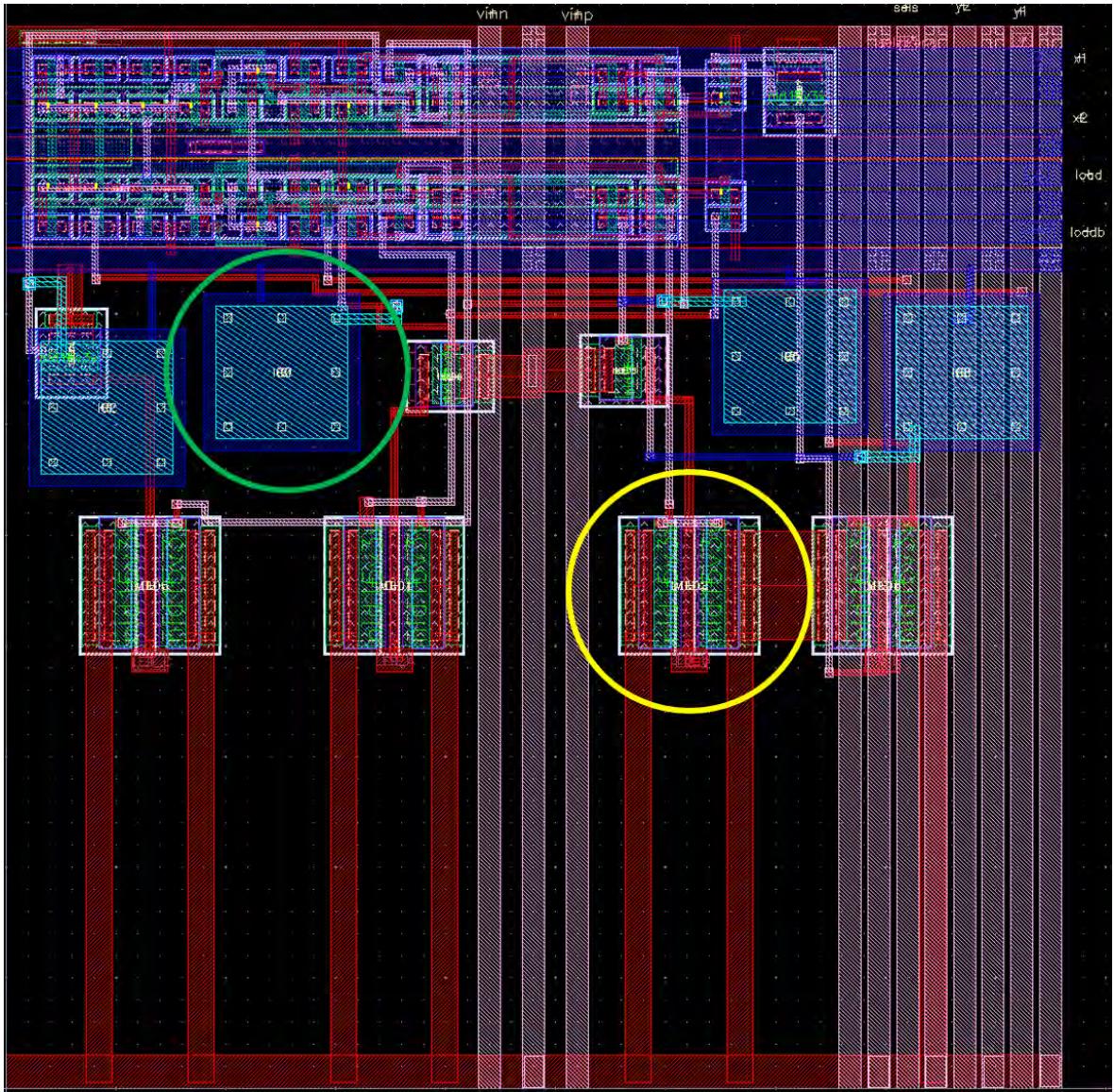
analog signals 'p' and 'n' charge the corresponding pixel to the value it needs to drive the LED. In this case 'p' and 'n' are not to be confused with positive or negative, they are simply labels given to those analog signals, hence vsledp and vsledn.

Diving down to the details of the actual schematic for the NSLEDS super-pixel, there are a few circuits that make up the logic that eventually controls the gears. The first set of circuits is shown in figure 5.9. There are two different circuits and two copies of each. The address decoders are the left circuits, these take in three inputs, selx and sely are the x and y addressing lines for the pixel, while the load inputs for these circuits are complementary of each other and derive from the same signal. This way, only one of pairs is active at the time depending whether load is HIGH or LOW. The whole circuit can be thought of as a 3-input AND/NAND gate. The last stage of the circuit is an inverter and the output signal is selxyload signifying that all three conditions are met. However, we also take the signal at the input of the inverter as an output, this signal is complementary of the other hence selxyload\_bar. With this naming convention a '\_b' or '\_bar' at the end of signal name means that it is a complementary signal of another input or output. To the right of the address decoder circuit is the next link of the chain, the gear selector circuit. This circuit takes in as an input a digital signal selstrong, which when asserted HIGH tells the strong gear to active in the later stages, otherwise the weak gear is selected. The selstrong signal passes thru a transmission gate which is control by the outputs of the address decoder. When the transmission gate is open and the sels signal makes it thru it passes thru two inverters in series. It may appear the inverters are completely redundant, but they serve two very important functions. First, since the selstrong signal is passing thru a transmission gate there isn't any filtration on the signal, which means that if the voltage level of the input signal is not adequate or if there is noise on the line, it would affect the logic down the pipe. By putting the signal thru both inverters the noise is completely cancel out and the voltage levels are always either HIGH or LOW, never in between. The second function of the two inverters is to provide the next stage of the pipeline with a pair of complementary signals, selsload and selsload\_bar.

The last stage of the super-pixel schematic corresponds to the driver circuits and monitor out circuit as shown in figure 5.10. Each of the driver circuits take in an analog signal vinn or vinp that controls the gate of drive transistors. There are two transmission gates that control the behavior of this circuit. The left most transmission gate only opens when the address decoder sets selxyload HIGH and selxyload\_bar LOW. The second transmission gate only opens when the gear selector circuit asserts the pixel is to be driven using the strong gear. By default the weak gear is always selected for drawing every time the pixel is addressed. In addition between the two transmission gates there is a small memory capacitor that helps store the value of the drive strength even after the first transmission gate closes. Both the weak and strong gear transistors are very large in comparison to all of the other components that make up the pixel circuit. For this reason, it is necessary to have a way to reset the charge trapped in the gate capacitor of the strong gear transistor after we no longer need to draw very hot objects. The small NMOS transistor acts a switch to ground that opens when the gear selector circuit disables the second transmission gate. Last but not least, the monitor out circuit is a pair of NMOS transistors that connect to a single pixel driver circuit and lets the user probe the output current of such transistors.

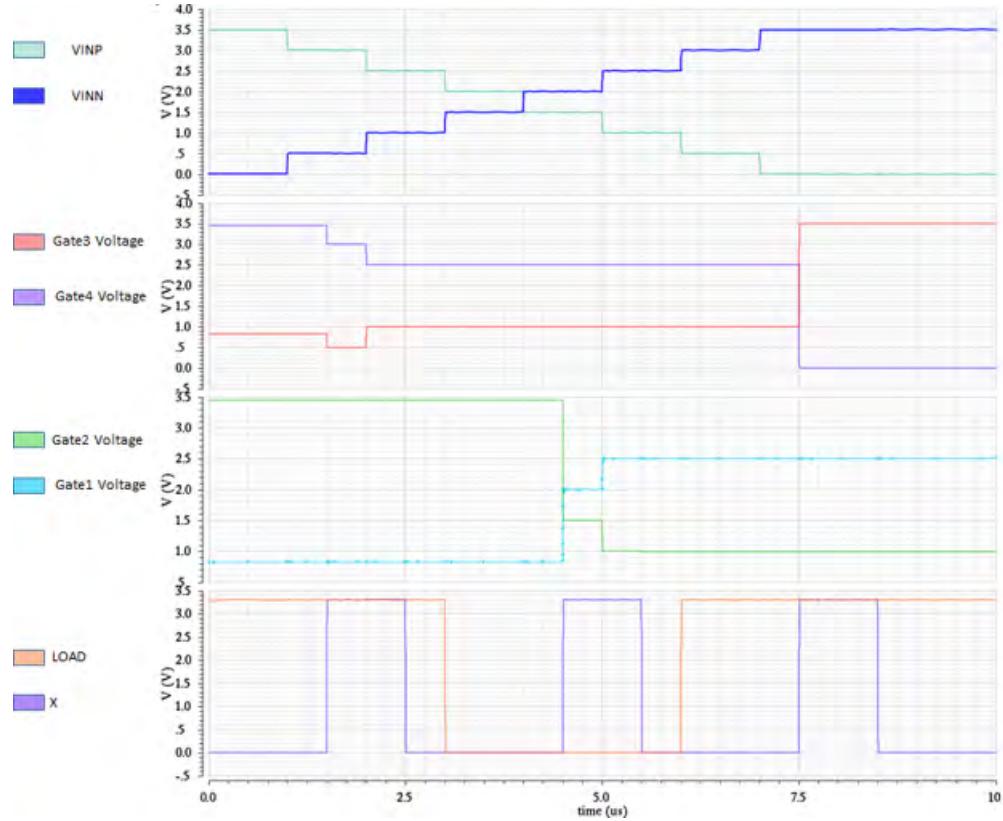
### 5.3 First iteration of the RIIC super pixel with the ONC18 libraries

Because this was the very first time that a new technology library was used to create a RIIC pixel, the first iteration of such was done without modifying the parts available in the library. Everything was default and generated automatically. Obviously, if the default sized devices are used, the layout will not be compacted or spaced efficient. As a result, the initial 2x2 super-pixel layout was designed without taking into consideration any space restraints in an area of  $48\mu\text{m} \times 48\mu\text{m}$ . Figure 5.11 shows the first completed layout of a 2x2 RIIC super-pixel. This first completed iteration with the 3.3V transistors was done using a total of four metal layers, one through three used for connecting all the components, layer four, being the thick layer, was saved for the metal contact that would be used on the hybridization process. Metal layer four is not



**Figure 5.11:** Final layout of a 2x2 super-pixel using the 3.3V technology library in an area of  $48\mu\text{m} \times 48\mu\text{m}$ . The memory capacitor (green circle) and the NLDNMOS (yellow circle) are the largest components in the layout

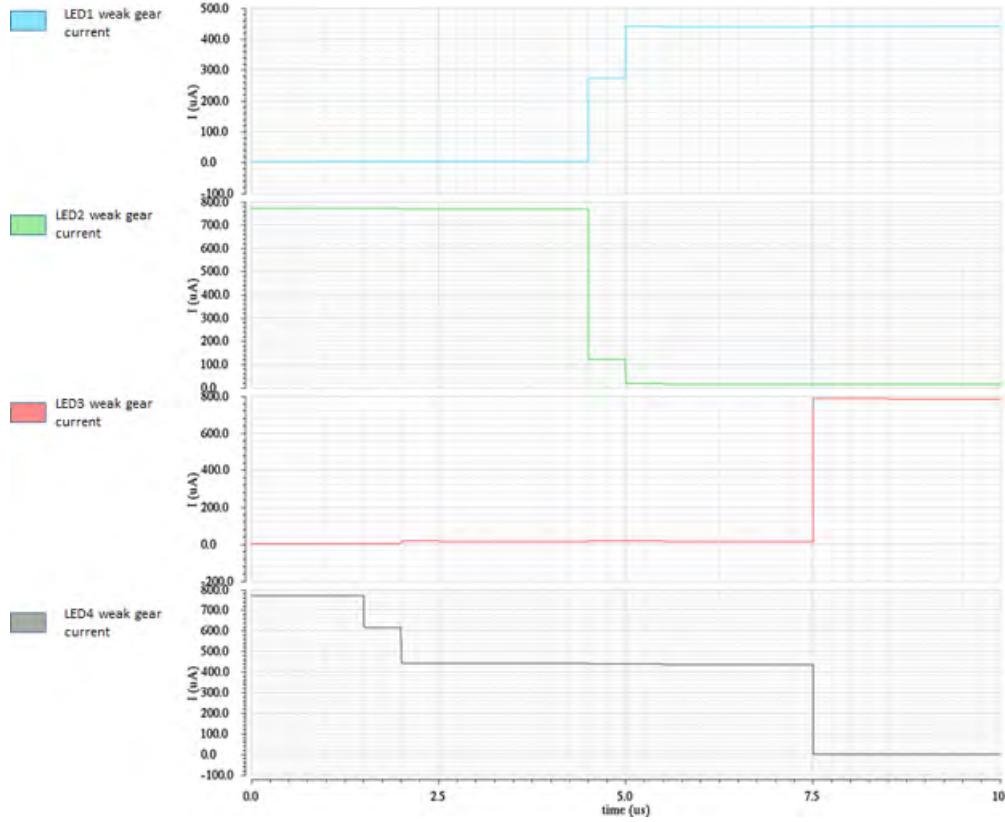
shown on the layout. The breakdown of the layout is as follows: The top area is where all of the digital circuitry is located. This was 100% based on the schematic shown on a previous section. The four analog drivers begin towards the left end of the top area, but the bigger components being the memory capacitor and the NLDNMOS parts are scattered below the digital circuitry. The metal-insulator-metaltop capacitors (CMIM)



**Figure 5.12:** post PEX simulation of inputs and gate states for a 2x2 super-pixel using the ONC18 3.3V flow process.

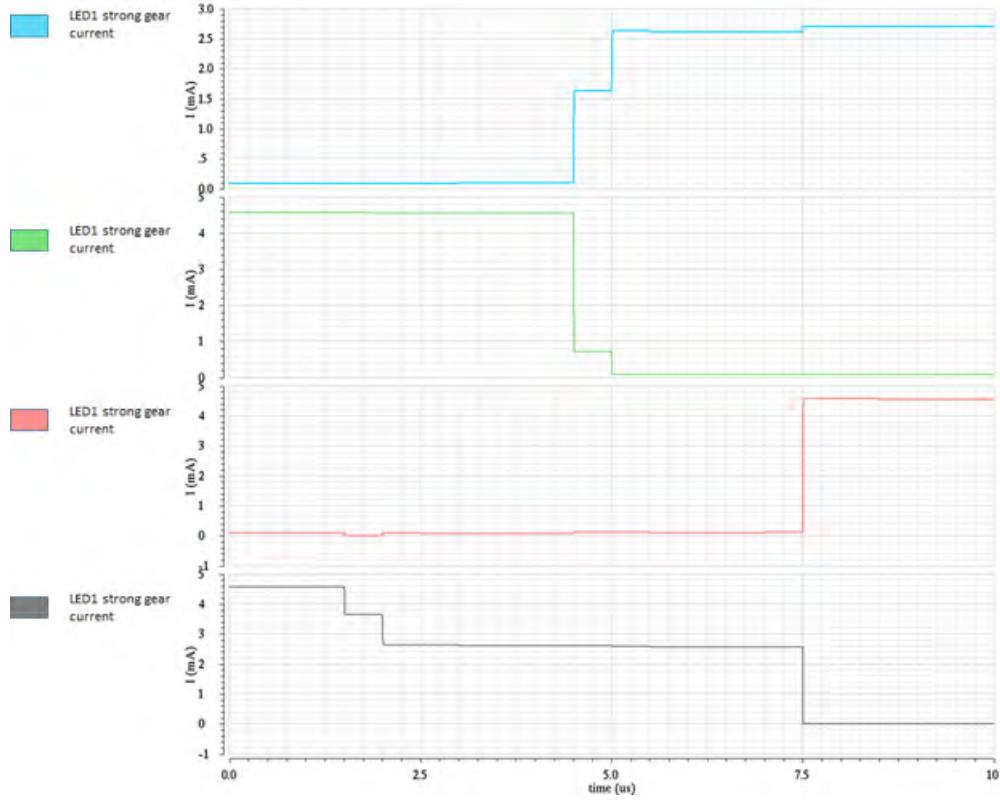
shown as the blue squares can't be smaller than  $2.2\mu m \times 2.2\mu m$ , which becomes a problem for a pixel in which the size restrain is  $12\mu m^2$ . In addition CMIMs take area away from the top metal layer, in this case metal four, which could result in shorts during hybridization. A big takeaway from this first iteration was that there was need for a different way to add capacitance to the circuit.

After completing the layout it needs to be checked for correctness and in the **virtuoso cadence** software there are three essential tools to get the job done. The first tool is the design rule check (DRC). There are thousands of rules that a VLSI designer must follow and they all depend on the process being used for the layout. DRC checks all of the rules that apply to the flow process being used. For example, minimum distance between metal layer, floating gates, missing well diodes, un-doped



**Figure 5.13:** post PEX simulation of the weak gears based on the inputs provided for fig 5.12 for a 2x2 super-pixel using the ONC18 3.3V flow process.

polysilicon traces, etc.. The next tool is the layout versus schematic (LVS) check. This tool compares all the instances as well as nets in the schematic files and compares that they exist and are connected correctly on the layout belonging to such schematic. The third tool is the parasitic extraction (PEX) check. This tool is very powerful as it lets the user analyze in detail all of the undesired resistances, inductances and capacitances that become part of the circuit due to the placement and routing of the layout. Every single metal path on the layout has some resistance  $R$  that changes based on the length and width of the metal trace. Same goes for capacitance that can be found almost everywhere from two metal traces running next to each other to capacitance formed in the substrate of the semiconductors. All of these parasitics are aggregated into a new schematic that contains all of the original ideal components



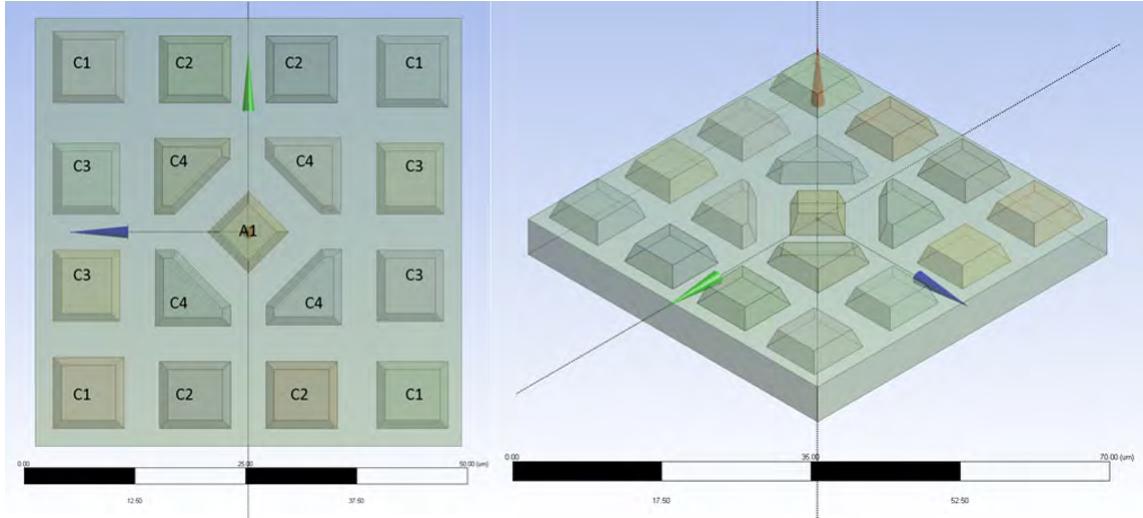
**Figure 5.14:** post PEX simulation of the strong gears based on the inputs provided for fig 5.12 for a 2x2 super-pixel using the ONC18 3.3V flow process.

plus all of the parasitics incorporated into them. The output schematic can then be simulated to ensure the parasitic components do not affect the integrity of the design.

The simulation results of the post-PEX extraction are shown in figures ?? and 5.14. Figure 5.12 shows how the input signals VINN and VINP where set up to rise and fall over the same amount of steps in a time of  $10\mu s$ . These input signals control the gate of the gears. For the simulation the Y address bit was always held high, thus it is not shown on the figures, the X address bit and the LOAD signal where both toggled at different speeds. In simple terms, only when both the X signal is high either gates 1 and 2 will be active if LOAD is LOW, or gates 3 and 4 if LOAD is HIGH. During any other time the gates of the drive transistors will just hold the value that gets stored in the memory capacitor of the circuit. Using the same set of input, the simulation was repeated for two scenarios, the first being when the gear selector circuit choses the

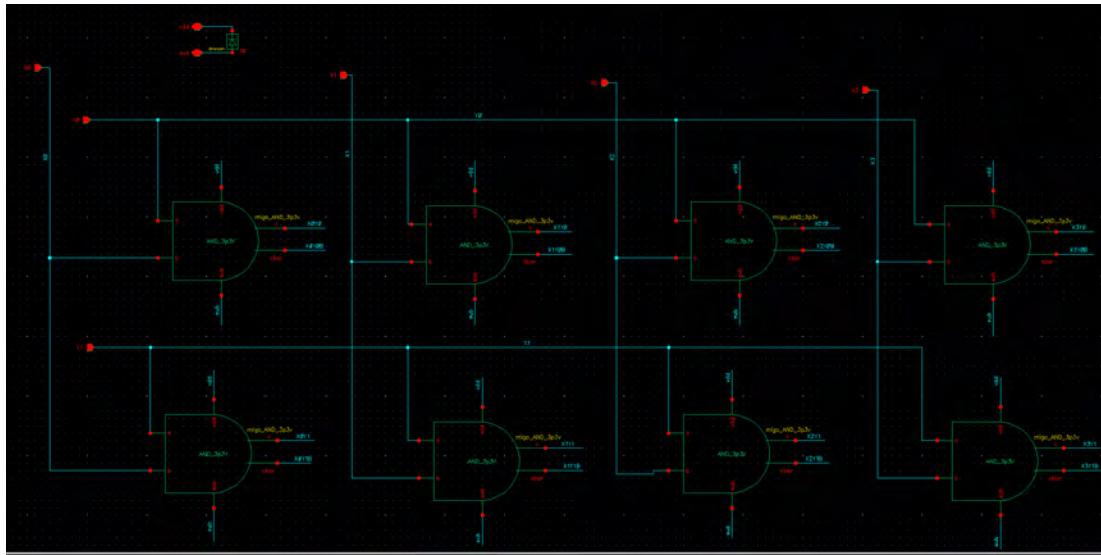
weak gear and the second for the strong gear output. Figure 5.13 and 5.14 show the the output currents of the two drive gears for the four pixels within the super-pixel. These curves also follow the same input signals from 5.12. All the outputs worked as expected as they only change value when either of the address selector circuits are active.

#### 5.4 Adaptations for the design of the ART-IDEA super-pixel

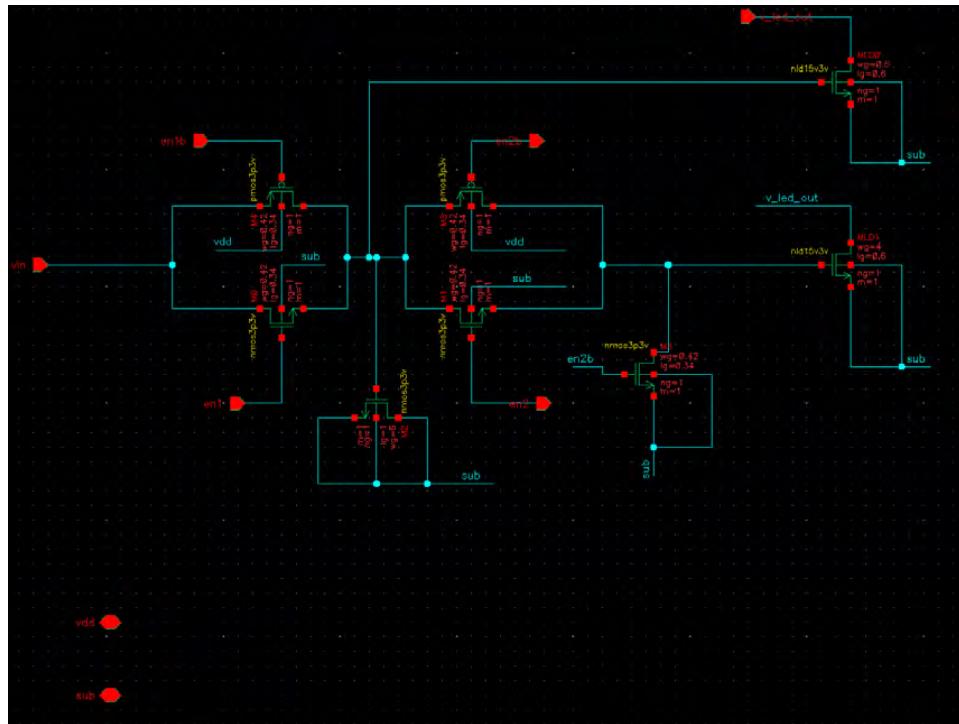


**Figure 5.15:** 4x4 super-pixel concept to be used on the RIIC and SLED designs of ART-IDEA

The ART-IDEA project uses the concept of a super pixel, but it takes it a step further than NSLEDS or HDILED models. As mentioned in earlier sections, a super pixel design refers to a group of individually addressable pixels which share common pixel-level circuitry on the RIIC, and common contacts on the SLED super-pixel. This is a useful technique to maximize utilization of the available space on both components of the hybrid array. For instance, every LED requires an anode and a cathode connection for proper operation. In the NSLEDS and HDILED design the SLED super-pixel grouped together four LEDs that shared the same common anode contact. For the ART-IDEA super pixel, the LEDs will be grouped in a small grid of 4x4 sharing with a single common anode in an area of  $48\mu\text{m}^2$ . The main reason as to



**Figure 5.16:** address decoder for a 4x4 super-pixel



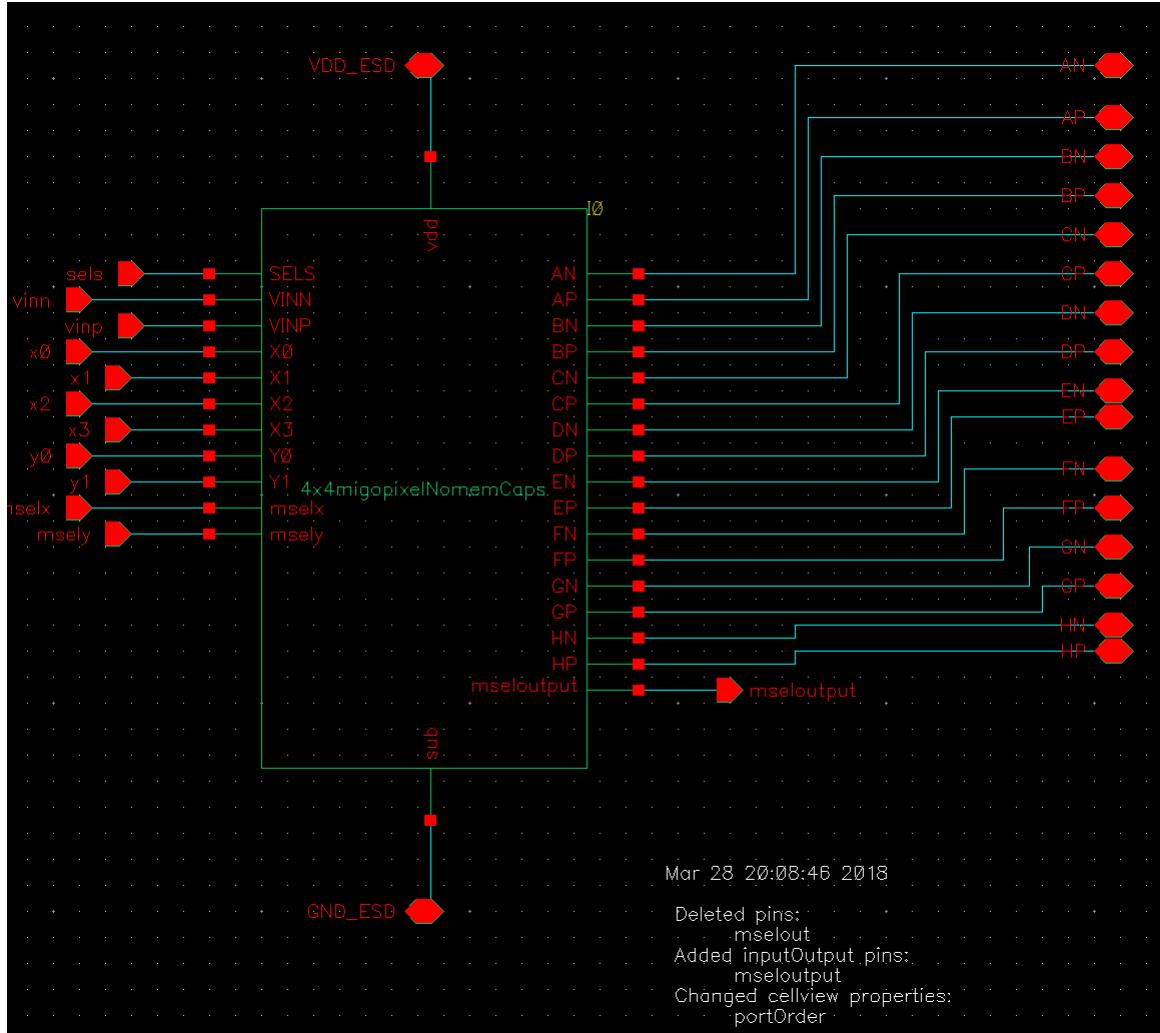
**Figure 5.17:** address decoder for a 4x4 super-pixel

why it was decided that the 2x2 super-pixel would not suffice for a  $12\mu m$  pitch pixel design was that there was not enough space to layout all the components. This was very apparent after the first iteration of the layout of the 2x2 RIIC super-pixel. In order to make everything fit in the RIIC more of the logic can be combined if more pixels are grouped together within a common area. The final conclusion was to aim to make a prototype where the circuitry for sixteen pixels had to share a tile of  $48\mu m \times 48\mu m$ . The concept also carried out to the SLEDS as shown in figure 5.15, where all the contacts denoted with 'C' are the cathode contacts for each of the individual pixels, in the center the contact denoted with the 'A' is the common anode shared by all 16 pixels[23].

There were other changes that were made to the architecture of the schematic of the RIIC. One of which is the fact that the LOAD signal was completely eliminated from the design, and instead another address line was added. Now, in the ART-IDEA super pixel each individual pixel is addressed directly without the need to time multiplex between pairs. The new design for the address decoders is much more straight forward as shown in figure 5.16, it consists of an array of AND gates with a complementary output, where the vertical nets are the address bits for the X direction and the horizontal nets the Y direction. Because there are still two analog input V<sub>INN</sub> and V<sub>INP</sub>, each AND gate enables a pair of pixels. Another change to the schematic was done on the driver circuits for all sixteen pixels. On the driver circuit the memory capacitor was replaced by a NMOS device with its source, drain and bulk shorted to ground, and the gate connected between the two transmission gates as shown in figure 5.17. This is possible because of the property of CMOS devices where the gate forms a capacitor with the substrate. Additionally, the transistor is much smaller than the CMIMs and the top metal is not used, making it ideal for the pixel circuits.

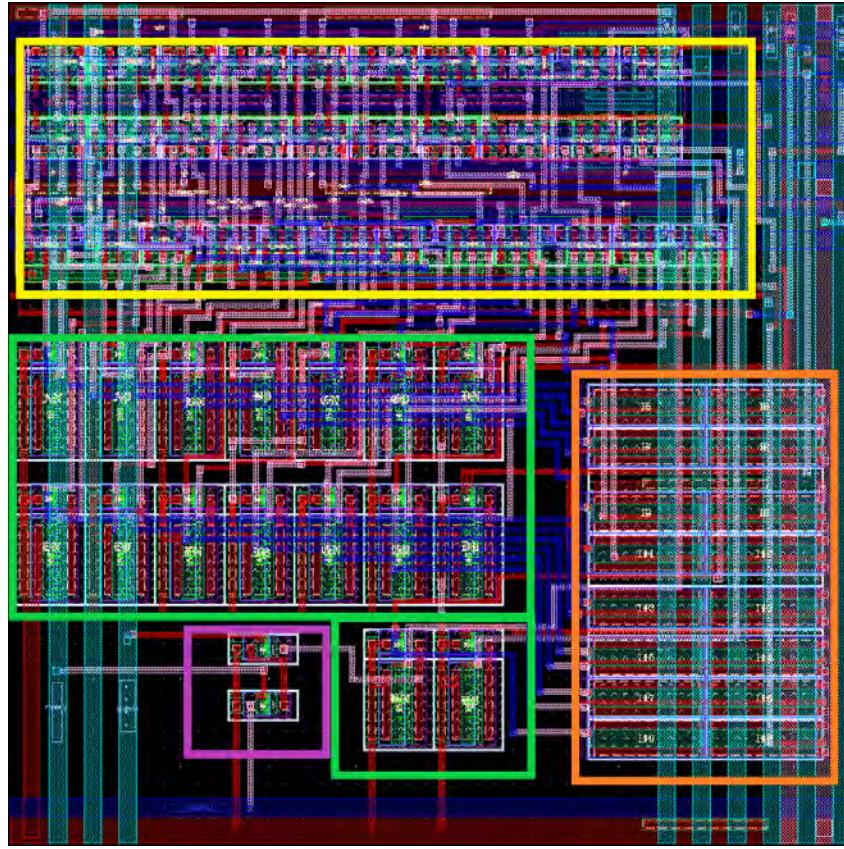
## 5.5 Final layout 4x4 ART-IDEA super-pixel

The final design for the ART-IDEA RIIC pixel was done based on the 4x4 super-pixel discussed in section 5.4. The top cell for the design is as shown in figure 5.18, there are a total of eleven inputs, and seventeen outputs on the super-pixel. The inputs are as follows.



**Figure 5.18:** top level cell for the 4x4 super-pixel of ART-IDEA

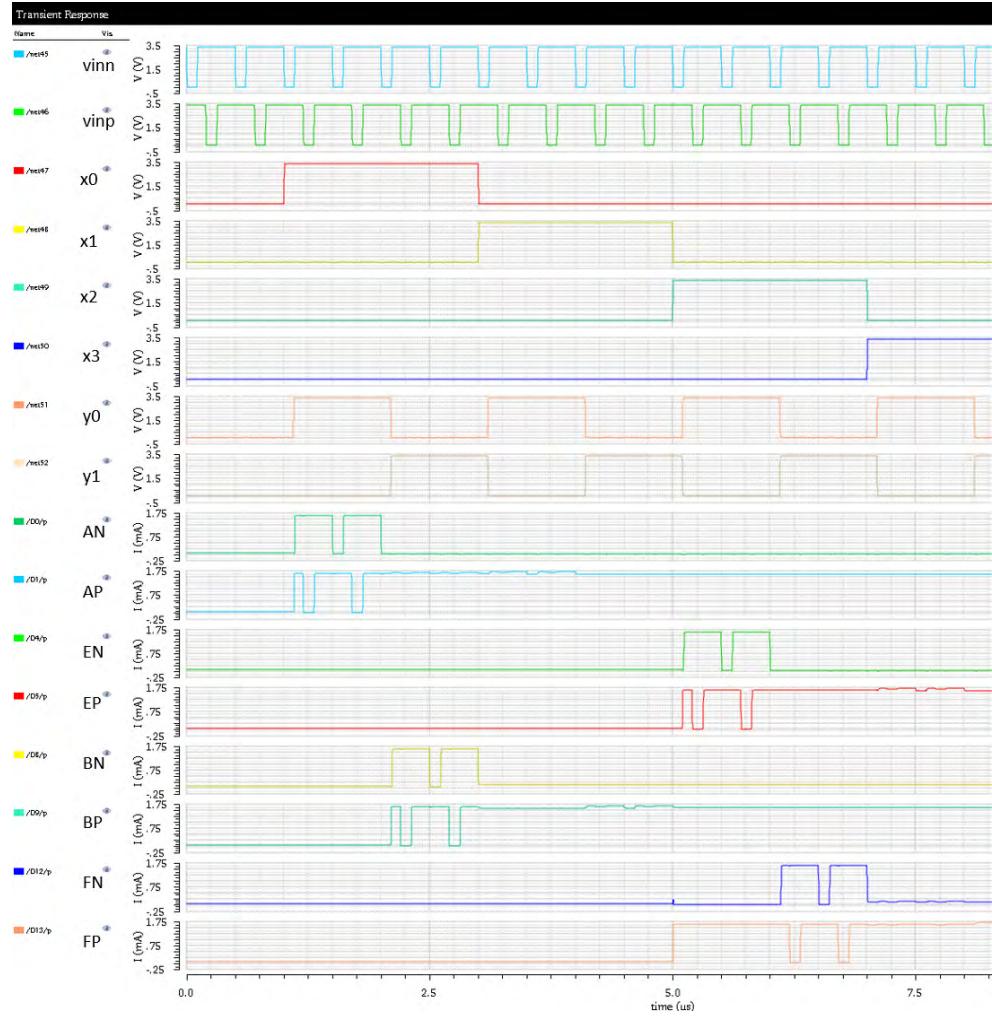
- **sels:** is a signal that selects the drive gear for all sixteen pixels.
- **vinn and vinp:** these two are analog inputs that control the gates of the drive transistors. Each super-pixel will write two pixels at a time, thus the need for two analog inputs.
- **x0,x1,x2,x3:** digital input signals for addressing the pixel along the x direction, from left to right.
- **y0, y1:** digital input signals for addressing the pixel along the y direction, from top to bottom.



**Figure 5.19:** Final Layout for the ART-IDEA 4x4 super-pixel design

- **mselx, msely:** these are control signals that open a path for telemetry in the pixel. In this version of the super pixel only one of the sixteen pixel can be monitored. This is something that would be used during wafer testing in future tiled designs.

The outputs are mostly LED current sources. They are denoted with two letters, the first is the pair letter and position within the layout, the second is whether it is controlled by vinn (if second letter is N) or vinp (if second letter is P). A and B are the first row, C and D the second row, E and F the third, and G and H the last row. The last output is the **telemetry output** for pixel HN that can be used for ensuring proper functionality during wafer testing. The reason why not all pixels get telemetry is because the number of metal traces needed would grow exponentially and space would become a problem.



**Figure 5.20:** Post PEX simulation for the 4x4 ART-IDEA super-pixel

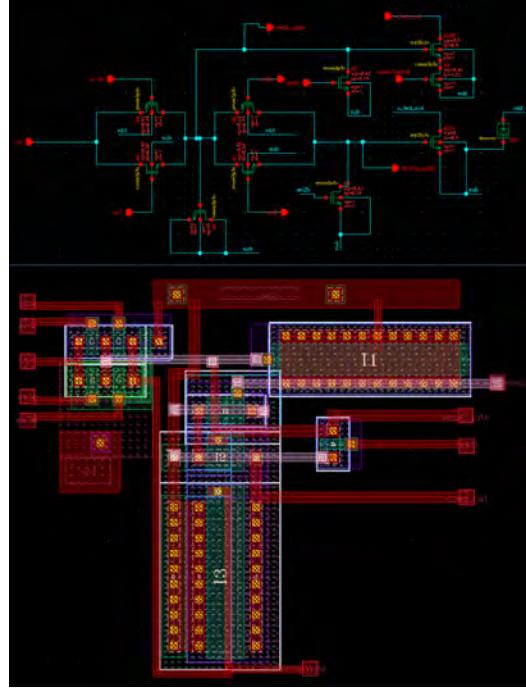
The final layout for the ART-IDEA 4x4 super-pixel was done in a total area of  $48\mu m \times 48\mu m$  with a total of five metal layers as shown in figure 5.19. In the layout, the top area in the yellow square is where most of the circuits lay as it contains all the logic CMOS circuits and all of the VLSI space saving techniques were applied. On the bottom portion surrounded by the orange square the memory capacitors are connected, and as mentioned before, these are NMOS devices configured as capacitors. The drive capacitors are grouped together towards the middle and bottom, these are surrounded by the green squares. Finally the pink square is where the MOUT telemetry circuit is

placed.

Once the final layout for the ART-IDEA super-pixel had passed the DRC and LVS check, the PEX was performed and the non-ideal schematic was generated with all the parasitic components. The newly created schematic was simulated by introducing a series of input combinations that would test all the different states of the pixel logic would work as designed. The simulation were done for every scenario possible that could happen on a RIIC. An example of the simulation data can be observed on figure 5.20. Starting from the top, are the two analog signals that control the pixel strength, vinn in cyan and vinp in green. For these the input values are identical but shifted slightly so that the rising and falling edges differ from one another, and both swing from 0 V to 3.5 V. The next group of signals shown on the sample simulation are the addressing lines. x0 in red, x1 in yellow, x2 in cyan, x3 in dark blue, y0 in orange and y1 in tan. By looking at the addressing lines one can figure out which pair pixels should be active within the 16 available pixels. The current output of the strong gear transistors are the rest of the curves. These output mimic the analog inputs whenever they are activated by the address lines. The first pair belongs to the LED pair of AN and AP in the green and blue colors respectively. When y0 and x0 are both high AN and AP are active and follow the corresponding input pattern. When y0 goes LOW around  $2.1\mu s$  whatever value was last seen on the pixel gets stored on the memory capacitors and holds it. The next pair to be activated is BN and BP in yellow and cyan respectively around the  $2.1\mu s$  mark. Pair EN and EP are activated around the  $5.1\mu s$  mark and finally FN and FP activate on the immediate address cycle.

### 5.5.1 experimental circuits

When designing the ART-IDEA pixel we had the opportunity to also experiment with small changes that would improve and solve known issues that we had observed in the past on the NSLEDS pixel. One such experimental circuit consisted on lowering the strength of the weak gear in order to increase the bit accuracy of background and colder objects. The minimum size for the NLDMOS used as the weak gear on the



**Figure 5.21:** Final schematic and Layout for the improved driver circuit. This design was based on the simulations performed on Appendix A

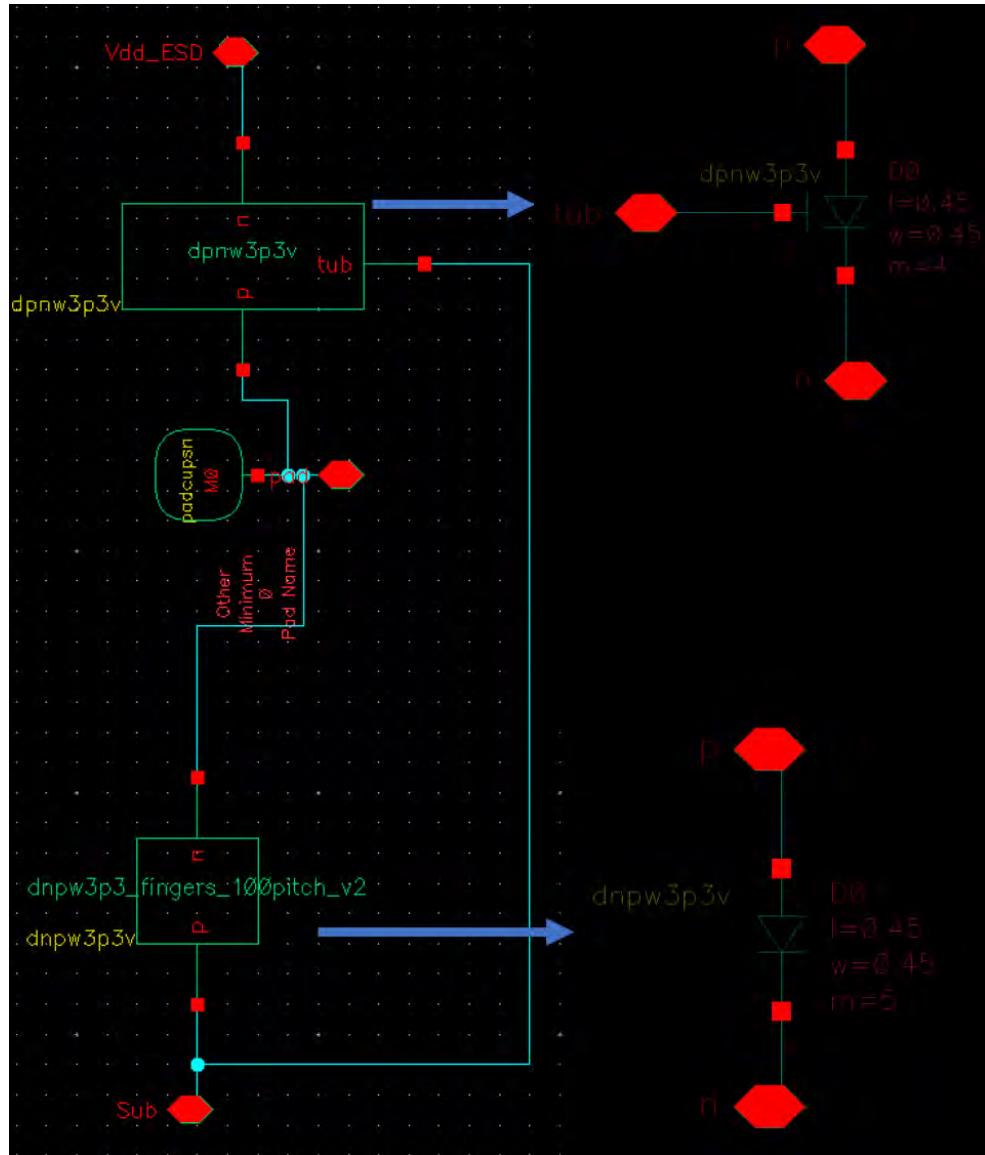
ART-IDEA pixel has a turn on voltage of around 800mV and the max current output is  $240\mu A$  when the drain is at 15 V and the source grounded as shown in figure A.2. One idea to decrease and have finer control over the lower end of output currents is to use a resistor to limit the current flow of the weak gear. The problem is that resistor are gigantic and have a fixed resistance, however, a NMOS transistor can be used as a current limiting resistor simply by cascading it to the weak gear. The circuit schematic shown in figure A.1 was used to simulate the effects of having a NMOS or a PMOS transistor acting as a resistor. The width and the length of the NMOS and PMOS along with the voltage at the gate were simulated to observe the effect they would have on the weak gear NLDMOS. For the PMOS transistor the results were not very good as the turn on voltage of the path increased giving less voltage range to work with. On the other hand, the NMOS cascaded path worked as expected giving very interesting results on the simulations. All of the results for the simulations can be

found on Appendix A.

Another minor change that will improve the overall functionality of the pixel circuit is the ability to reset the each pixel individually. The way resetting the array is being handled by the current generation of RIICs is by applying a global reset. What this means is that after every frame written there is a period on which the entire array goes thru a reset period on which all of the pixel are turned off. However, for many scenarios that need to drawn to the array not all of the image is changing at the same rate. in many cases the backgroud could be static for very long times with a single dynamic object moving around. If we only reset those parts of the array that need to be updated, the entire systems will be able to display at much faster framerates[28]. This idea is being implemented by member of our team at a software level, but adding a the reset at the pixel level will add this feature at a hardware level. Another advantage of the line reset for each pixel is that it helps keep leaky transistors in check. Transistor are not perfect and there is always a small leakage current associated with each device. Most of the time it is so small that it will never affect the behaviour of pixels. However, we have come across instances where these leaks are enough to cause individual pixel to start blooming or emitting light when the array is sitting in idle state. The reset line on the memory capacitor will solve this issue as show on the simulation A.7. The improved circuit schematic and layout are shown in figure 5.21. It contains the reset line and the cascaded weak gear appropiatly sized to a width of  $.42\mu m$  and a length of  $1.22\mu m$  based on the best values observed on the simulations.

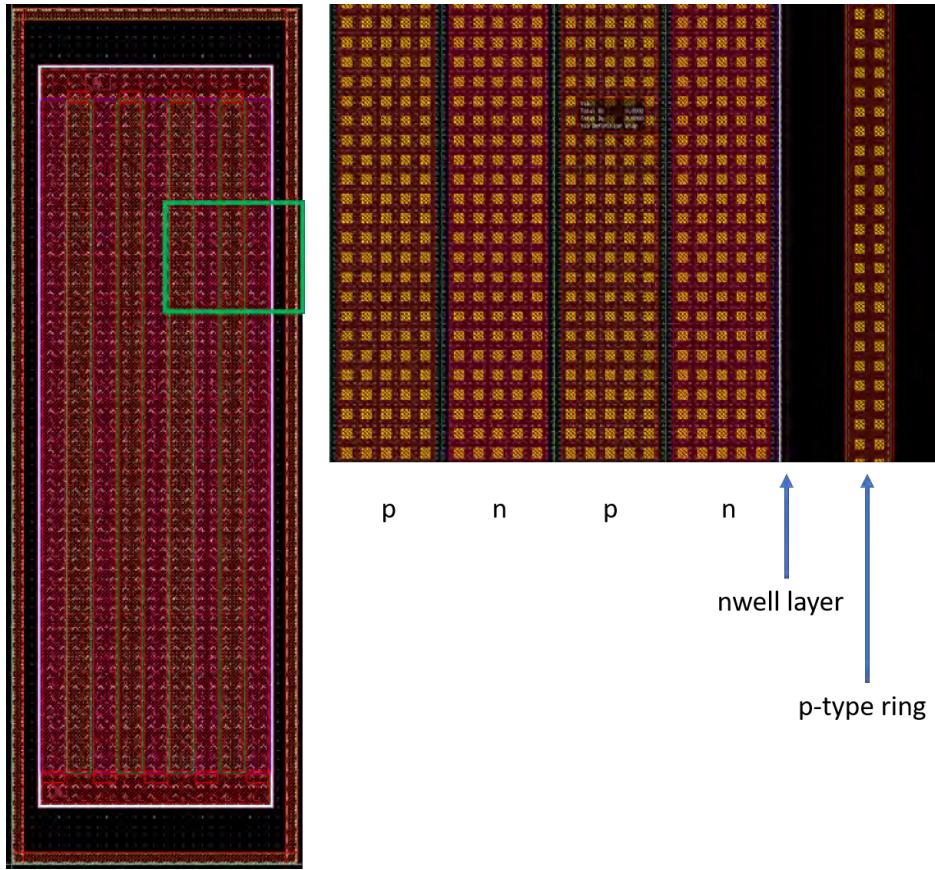
## 5.6 Contact pads and ESD protection

Electrostatic discharge (ESD) is a natural phenomena that can happen at any time whenever friction is applied between two different bodies and static electric charges build up on the surface. As integrated circuits become smaller they become more susceptible to getting permanently damaged by an ESD event. For instance, high current ESD events create voltages based on the impedance of the material they are flowing through in part creating electric fields and damaging thin films on the IC.



**Figure 5.22:** schematic for the input pads with ESD protecting diodes

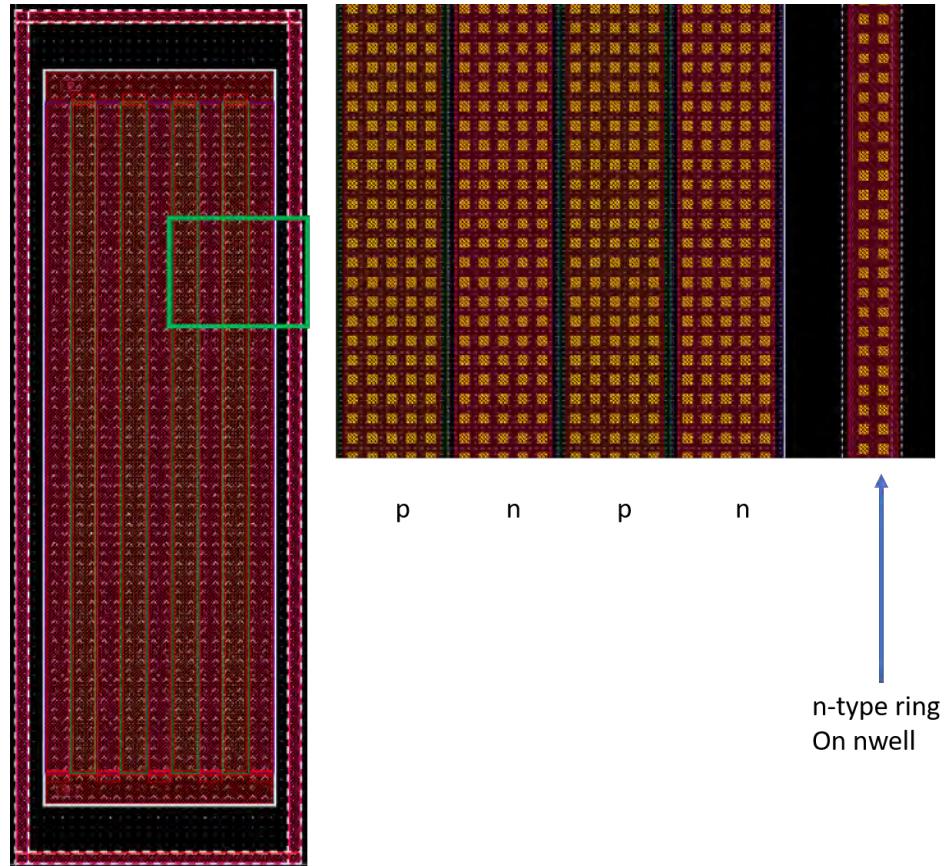
Material such as polysilicon can become less resistive during an ESD event, causing more current and voltage to pass through creating failure. On bipolar transistors, the emitter-base junction may become leaky or shorted after an ESD event. On MOSFET transistors the gate plate can melt due to the thermal energy that may be produced, additionally, the diode junctions on the drain can also be damaged [29].



**Figure 5.23:** ESD diode to be connected to VDD\_ESD, the diode is interlace with p and ntype fingers and grown on a nwell. The entire diode is also surrounded by a p+ substrate contact for isolation

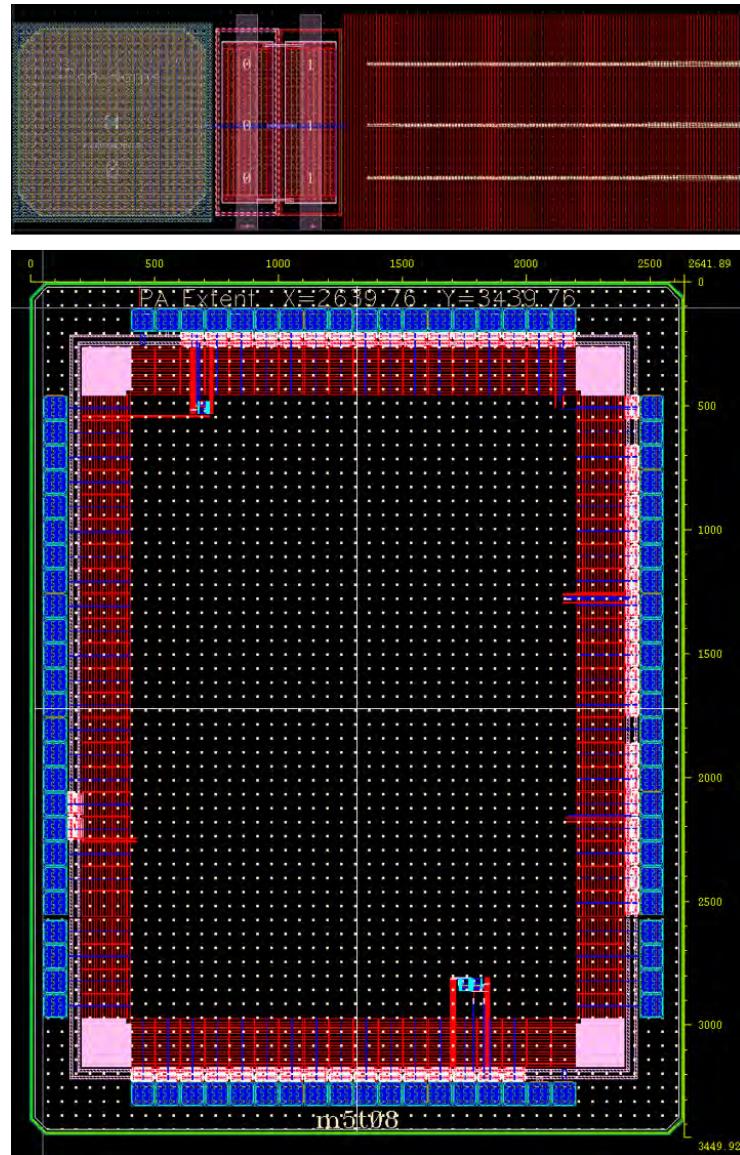
For this reason, it has become a necessity that all IC devices have some sort of ESD protection in order to reduce the risk of destruction associated. A common practice for ESD protection is to have diodes with a low reverse bias voltage **in the input pins of an IC** as shown in figure 5.22. During normal operating conditions the diodes are off and there is no current flow across them. However, if the voltage at the pin exceeds their rated breakdown voltage the diode effectively act as a wire that shorts the path to a ground plane or a power plane, thus taking the stress away from the internal circuitry.

The actual Layout for the diodes shown in figure 5.22 had to be custom made to meet the ESD guidelines recommended for an IC. The custom diodes were made using



**Figure 5.24:** ESD diode to be connected to GND\_ESD, the diode is interlace with p and ntype fingers and grown directly on the p-sub. The entire diode is also surrounded by a n+ nwell contact for isolation

the MOS S/D junctions on the OnSemi 3.3V technology library, these junctions are effectively a diode with a breakdown voltage between 8 to 10 volts. Additionally, two types of diodes are being used, the first is a nwell diode with a p+ wall around the entire diode area. The second diode is a p-sub diode with n+ guard wall grown on a nwell. Furthermore, an ESD diode has to have very low capacitance and low series resistance to keep the impedance to a minimum. For this reason, the ESD diodes were made deliberately large and with a fingered pattern. The finger pattern helps in keeping the perimeter very large and thus the capacitance low.



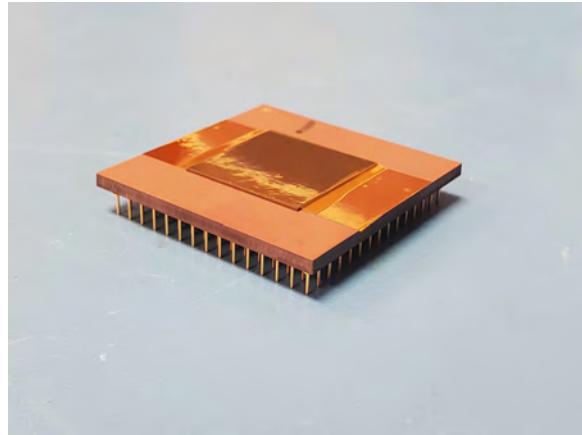
**Figure 5.25:** Top: zoomed in layout of a single IO pad with ESD diodes and signal paths. Bottom: Final chip layout, a total of six circuit layouts are brought out to the pads for wirebonding

## 5.7 Final Test Chip Layout to be Fabricated

Using the 3.3V process from onc18, various test circuits were created in order to have the ability to test every single component that makes up the 4x4 RIIC superpixel. Every circuit that was put into the final design was simulated post-PEX to verify proper theoretical function prior to fabrication. The following circuits make part of

the final test chip layout, the schematics and layouts for these circuits can be found on appendix B and the final top level layout is shown on figure 5.26.

- **Stand alone gears:** Different size NDL transistors will be brought out to pins on the test chip. This will allow us to characterize the devices by themselves and their ability to drive LEDs.
- **Single pixel driver circuit:** The pixel driver circuit used in NSLEDS and HDILED RIICs was shrunk using the 0.18 CMOS process to operate smaller pixels. The stand-alone circuit will serve as a unit test piece to verify functionality and serve as the control unit for comparing other driver circuits with enhancements.
- **Single pixel driver with reset line and limited weak gear:** On previous hybrids, we have observed that random pixels may emit light when the IRSP is in an idle state. We attribute this behavior to leaky gates on the digital logic. The proposed reset mechanism is directly embedded on the drive circuitry. This means that we can reset the array even before it becomes programmed. Furthermore, resetting will be fully firmware controllable, meaning that we may or may not reset after a scene is drawn. It will all depend on the tests being done and/or the detector specs. The NLD transistor minimum size is  $0.5\mu m$  and it can output currents of up to  $200\mu A$ . However, we might need to decrease this current depending on how bright the LEDs turn out to be once fabricated. We added a series transistor to the weak gear to act as a resistor. The idea is to operate the added transistor in the linear region so that to the weak gear it will appear as a resistance, thus, the current will be reduced.
- **Address decoder and gear selector:** A stand-alone version of the address decoder for the RIIC super pixel will be added to the test chip for verification of proper functionality. A stand-alone gear selection circuit will be added to the test chip for verification of functionality. This circuit dictates which gear needs to be active to drive the LED based on external control signals.
- **ART-IDEA super-pixel:** A version of a 4x4 RIIC super pixel on a  $48\mu m^2$  area will be the main focus of the test chip. After PEX simulations indicate that the design should work as intended. This design features 16 sets of SLED pixel drivers, an address decoding circuit, and gear selection circuits for all drivers. All 16 sub pixels in the super pixel are independently addressable.
- **Tiled ART-IDEA super-pixel:** This circuit layout will help us test the ability of the RIIC super pixel to be tiled to form a bigger RIIC. The cell was designed to be tileable in any direction.



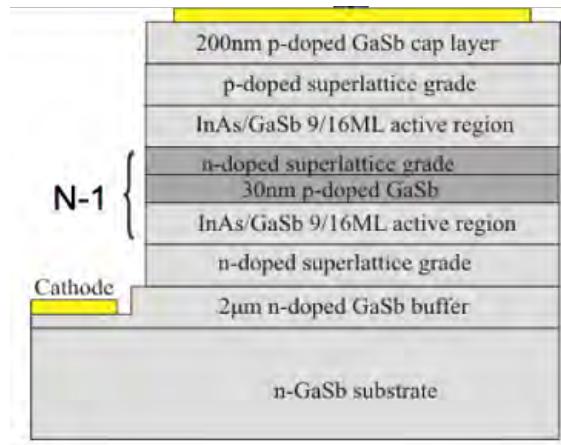
**Figure 5.26:** RIIC chip prototype packaged in a 144 PGA package

## 5.8 Packaging

The final chip layout shown on figure 5.26 was submitted to OnSemi foundaries for fabrication. The area purchase for fabrication of the ART-IDEA RIIC part had a total area of 5mm x 5mm on a shared wafer run. A total of 20 die were fabricated within this area. After dicing, the five of the chips were sent to Majelac Technologies LLC to be wired bonded to a 144 pin grid array (PGA) package. The wire bonding layout used, along with the final pinout of the devices can be found on appendix C.

## Chapter 6

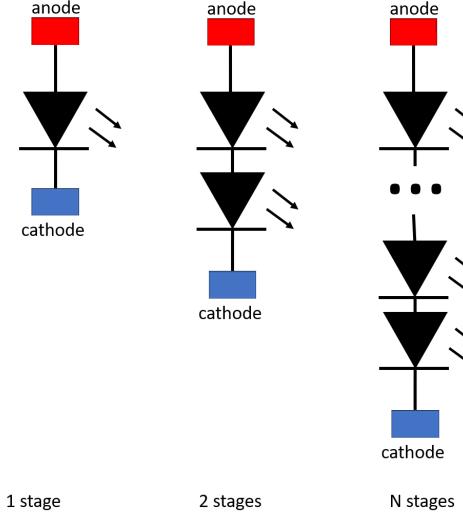
### DESIGN OF THE LED DEVICES FOR ART-IDEA



**Figure 6.1:** SLED stack diagram showing all the layers used to make a single device. Some of these layers may repeat N times depending on the number of stages the specific device has

This chapter will discuss the methodologies that were implemented during the design and fabrication of the first batch of SLEDs pixels for the ART-IDEA project. This was the very first time that such device was attempted and we learned many valuable lesson from this first iteration. The work discussed in this section was mostly performed by Firefly Photonics, our partner in this effort.

The SLED devices used for making our projectors emit in the midwave region of the IR spectrum between  $3\mu m$  to  $5\mu m$ . The exact wavelength may vary slightly depending on the generation of projector or goal of the programs that funded such projects. The SLED devices are grown on GaSb using molecular beam epitaxy (MBE), and the super lattice (SL) active regions are InAs/GaSb layers. The stack compositon

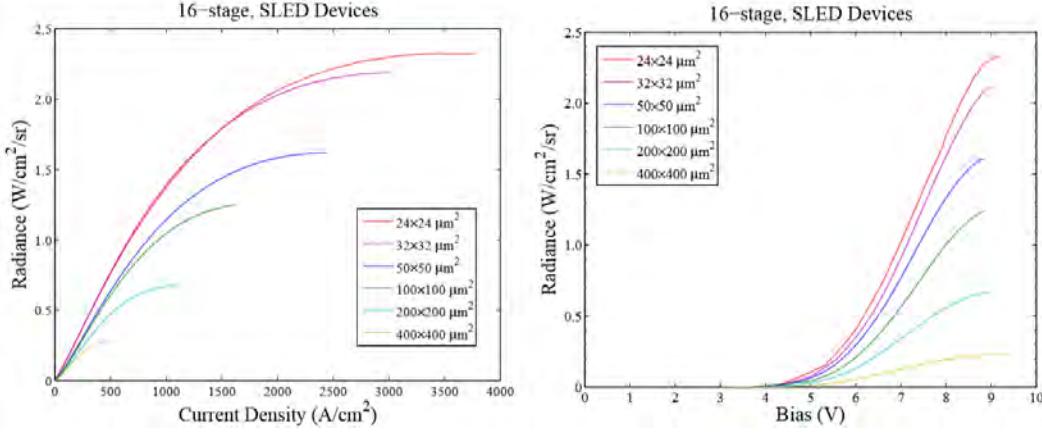


**Figure 6.2:** A SLED stage is composed of an active region and a tunnel junction as shown on figure 6.1. However, it is easier to think of them as single LEDs where the number of LEDs is the number of stages of the structure

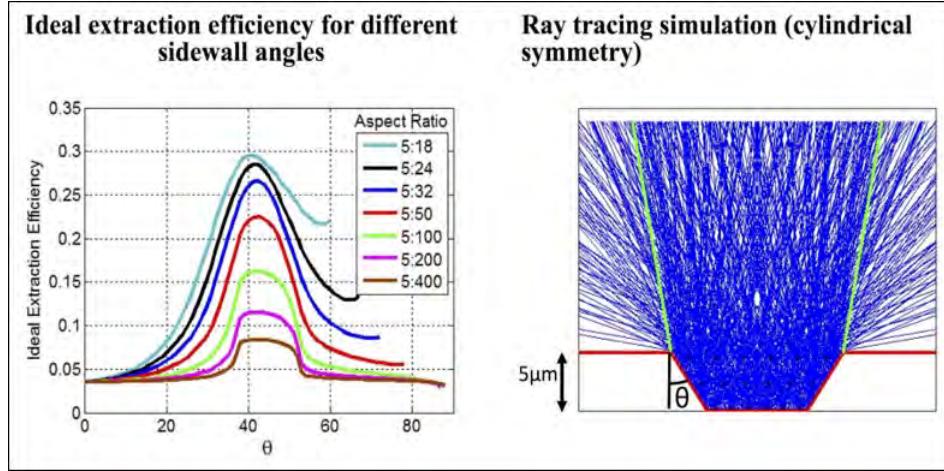
for the SLED devices is shown in figure 6.1. A SLED device by default will have at least one active SL region that **emmits** light, we call this a stage. More stages can be **sandwiched** in the middle of the stack, each separated by a tunnel **jucntion** of type n and p doped GaSb. If a SLED device is **refer to** as having N stages, it means that N-1 stages were added in the middle of the sandwich[10, 30]. This is easier to understand by looking at figure 6.2, since each active InAs/GaSb SL region emmits light under the proper bias conditions, each stage can be represented as an LED on a series chain of N LEDs.

## 6.1 Motivation for decreasing the LED size

As mentioned before in the previous chapter, with this work we were trying to close the gap between the current resolution of sensing technologies and the emitter technology. However, this is not the only motivation for going smaller. We observed a phenomena with SLEDs created on previous programs that demonstrated that the light extraction became more efficient with smaller size LED pixels. Denis Norton, a former PhD student at the University of Iowa, wrote about these observations on his



**Figure 6.3:** Current density (left) and bias voltage versus randiance for different size 16-stage SLED devices



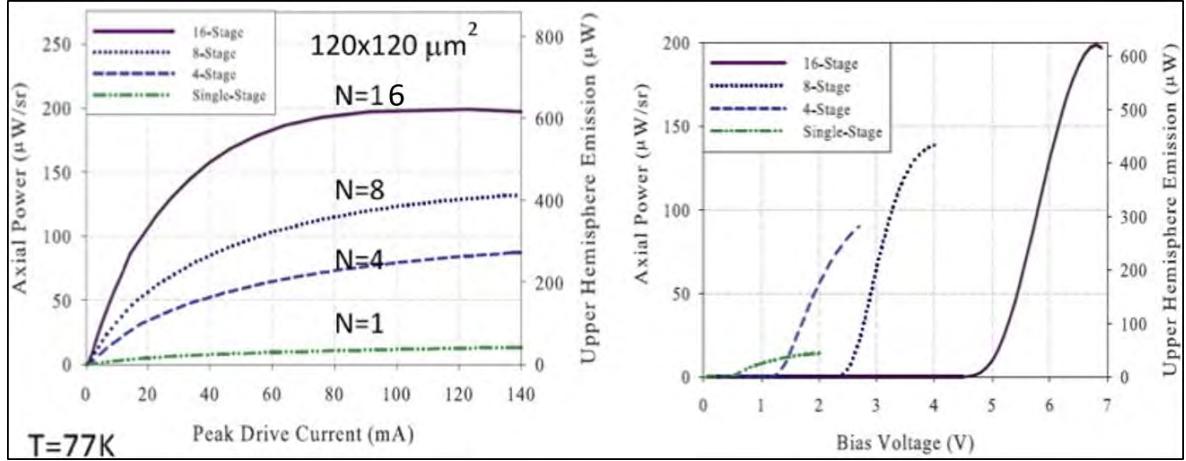
**Figure 6.4:** Simulations that show the ideal wall angle for the best extraction, this angle would be around  $45^\circ$ . The other is a ray tracing simulation that predicts the path of light with angled sidewalls on the SLED device



dissertation[10]. An experiment was conducted on which SLED devices of different areas were grown and the Radiance vs. voltage and current density was captured. The constant between the different SLED devices was that the number of stages was 16. On figure 6.3 it can be seen from the data collected that as the area of the SLED device decreases the radiance increases. This is believed to be caused by the angle of the sidewall becoming more efficient as the ratio of mesa height to SLED width increases

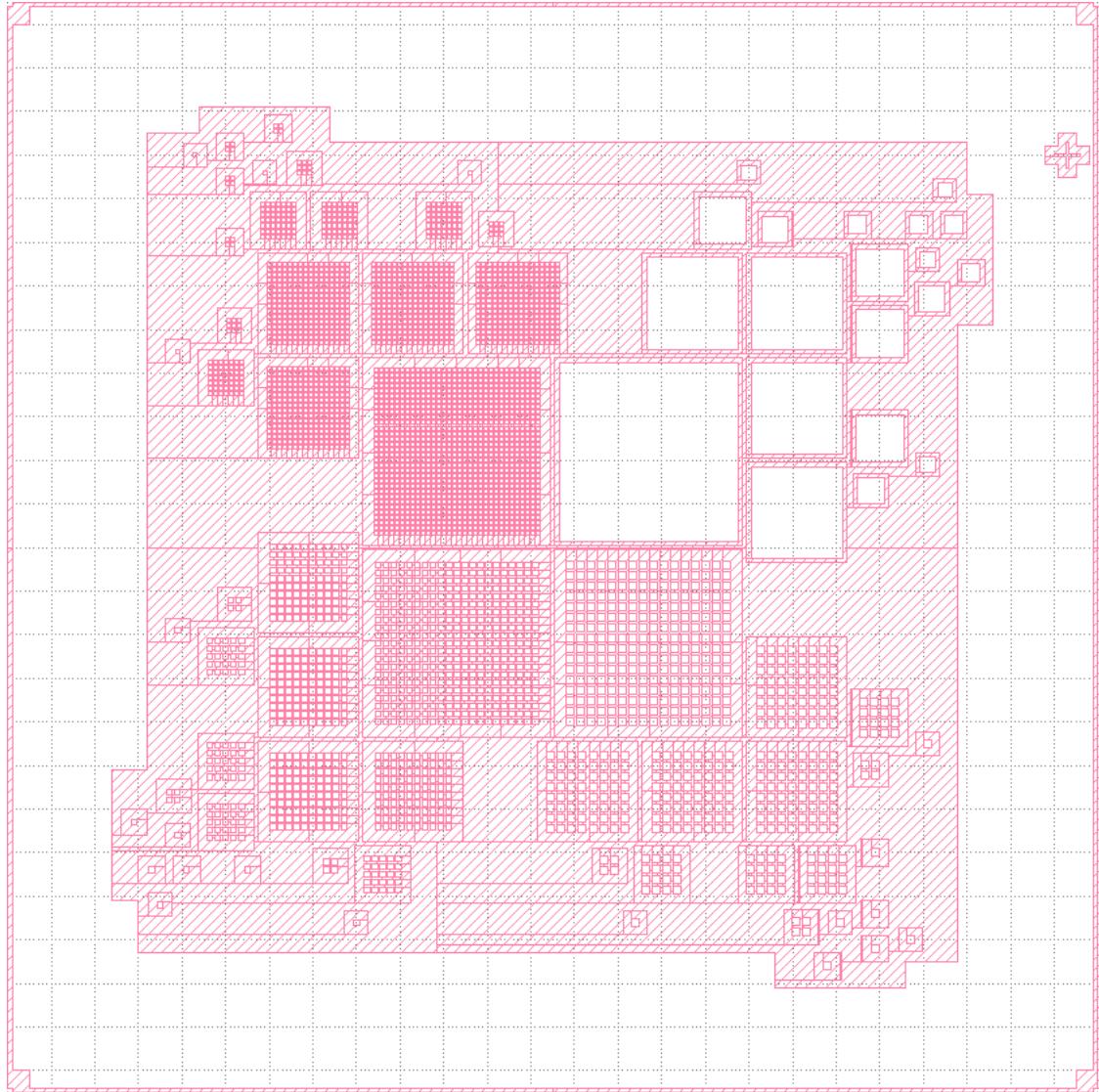
[10, 23, 30]. This theory is backed by the two simulations shown on figure 6.4 where the best light extraction of the substrate happens if the angle of the sidewall is  $45^\circ$ , and it increases as the ratio between the height and the size of the mesa increases.

## 6.2 Fabrication of the SLED devices



**Figure 6.5:** Two plots that show the effect of having different number of stages on SLED devices. With higher number of stages the maximum light out from a SLED increases, however, this increases the turn on voltage of the SLED device

During the very early states of design of the SLED devices that would be paired with the ART-IDEA RIIC we had to decide the specs of such. Most of the previous SLED arrays created for other projectors use a stack of 16 stages. However, with an increasing number of stages the turn on voltage for the SLED arrays increases by a similar factor Figure 6.5 is a good example on how the number of stages affects the properties of the SLED device. In this case four devices were grown with different number of stages but the area was kept constant at  $120\mu\text{m} \times 120\mu\text{m}$  for all of them. The SLED with 16 stages output the most light but it also had the highest turn on voltage around 5V. For this project we wanted to explore a path towards a projector that could be operated at a lower voltage as this would decrease the total power consumption of the system. Additionally, this was the very first time we considered making device



**Figure 6.6:** Mask used for fabricating the SLED devices. The mask is geometrically symmetrical between the four quadrants, each contains different sized mesas and partition mesas that help us compare the differences between them

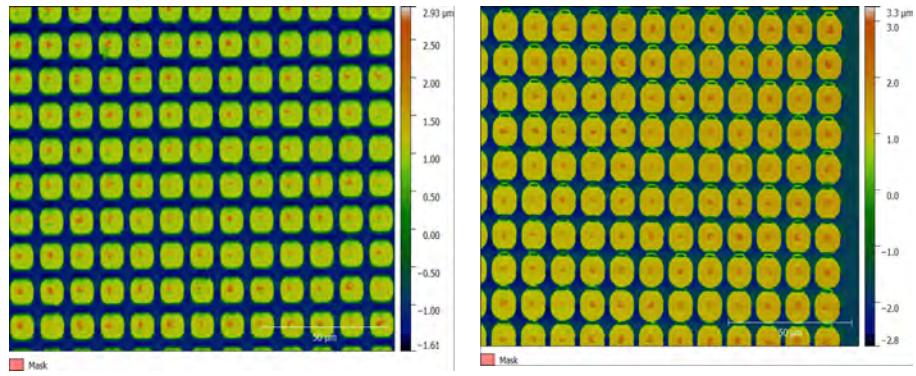
smaller than those found in a  $24\mu m$  pitch array. In simpler terms, a device with a higher number of **satges** also becomes taller, a taller device with a small area translates to smaller mesas and less space for the metal contacts as the sidewalls have an angle. These were the main reason why we decided not to try the 16 stage devices in the first run, instead we opted for the 8 stages device as they are a good middle ground between

the light output we want to achieve, the turn on voltage is reasonable and it would not be as tall as the 16 stage device.

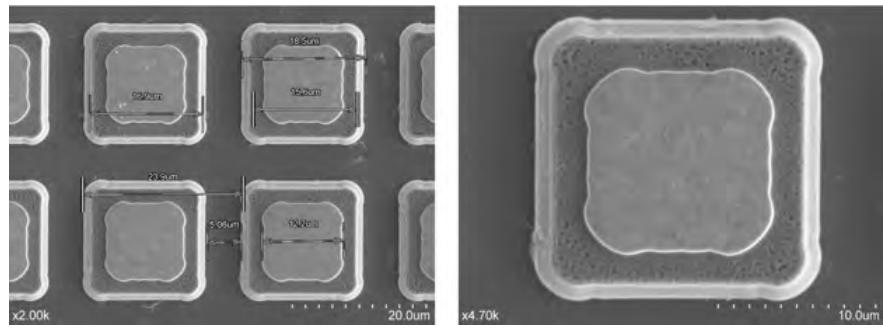
In the end, two different types of 8-stage devices were grown on 3" wafers, the main difference between the two is the stage thickness, and by secondary effect the etch depth. The first wafer is IAG739 which has a stage thickness of 193nm and an etch depth of  $2\mu m$ , the second wafer, IAG740, has a stage thickness of 326nm and an etch depth of  $3\mu m$ . Also is worth mentioning that as reference, the usual 16-stage device has a stage thickness of 133nm and a etch depth of  $4\mu m$ . The photolithography mask designed for dividing the SLED devices is shown on figure 6.6. The mask was designed for testing different size small format pixels. There are four quadrants that are symmetrically identical but partition differently. The first quadrant features LEDs starting at  $24\mu m \times 24\mu m$  for the smallest and  $406\mu m \times 406\mu m$  for the largest without any partitions. The second quadrant is also broken down into different sized areas with the same dimensions as quadrant 1, however, the areas were further partitioned/etched to create  $12\mu m$  pitch pixels. For instance, an area of  $24\mu m \times 24\mu m$  on quadrant 2 is further partitioned to create a mini array of four  $12\mu m$  pitch pixels with a lane width of  $3\mu m$  and effective pixel width of  $7\mu m$ . The third and fourth quadrants are similar to quadrant 1 with the exception that the partitions are  $18\mu m$  pitch and  $24\mu m$  pitch pixels respectively. The finalized list of SLED pixels fabricated during this work is found of appendix D. Having mini arrays as well as single pixels allow us to compare the light extraction between different mini arrays and full size pixel, comparing if the wall angles in fact do help with extraction. Additionally, for the very small pixel, it might become difficult to precisely measure the light output with the current equipment. Having a small grid light up help with light collection as the aggregate output increases.

### 6.2.1 Challenges Encountered During SLED Fabrication

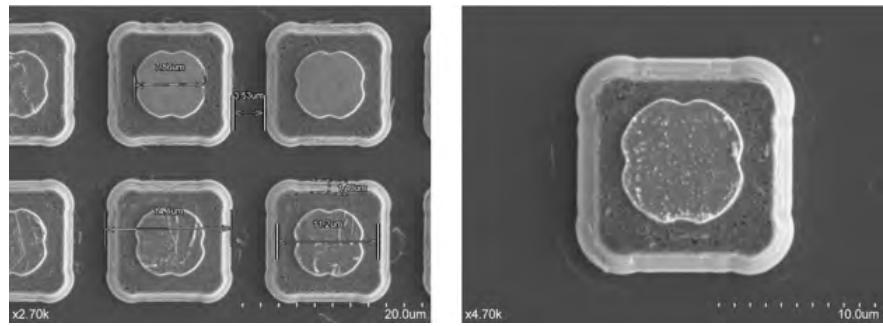
Creating an IR SLED pixel smaller than a  $24\mu m$  pitch had never been attempted; hence we encounter a few challenges during the fabrication process. Although



**Figure 6.7:**  $12\mu m$  mini arrays for IAG739 (left) and IAG740(right)

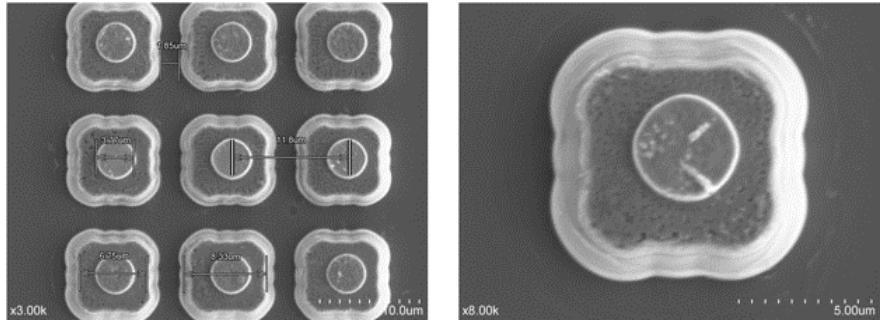


**Figure 6.8:** SEM for a  $24\mu m$  pitch SLED device



**Figure 6.9:** SEM for a  $18\mu m$  pitch SLED device

undesirable, none of them were show stoppers, but they did provide valuable lessons to be learned for potential future runs. One such issue can be observed on figure 6.7,

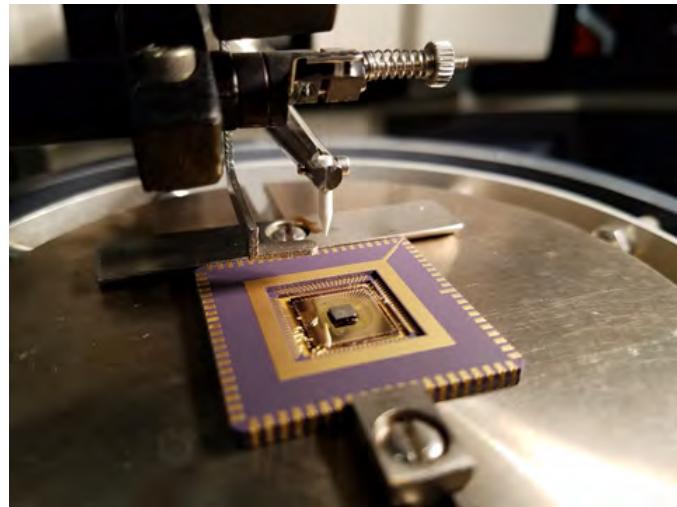


**Figure 6.10:** SEM for a  $12\mu m$  pitch SLED devie

The figure shows an image of two sets of  $12\mu m$  pitch mini arrays, the one on the left corresponds to a IAG739 device with its thickness per stage being  $193nm$ , and the image on the right is a IAG740 device with stage thickness of  $326nm$ . The problem was that on the thicker 739 wafer there was some bridging between the  $12\mu m$  pitch devices. This was likely due to poor clearance of etched material between these small devices as the  $18\mu m$  and  $24\mu m$  pitch features did not have this problem on the same wafer. Additionally, the masks used to make the SLED devices had optical proximity correction (OPC) issues, the pixels and contacts were designed to be square, but as the features became smaller the contacts became more rounded. Scanning electron microscopy (SEM) images were taken for small format pixels, figures 6.8, 6.9, and 6.10 show the resulting devices created for the project. The circular contacts are more prominent on the  $18\mu m$  and  $12\mu m$  pitch SLED pixels. A new mask with better OPC will be used in the future to prevent issues like this one from happening again.

### 6.3 packaging

The pakaging of the SLED devices was entirely handled by Firefly photonics using the facilities in the University of Iowa (UIowa). The devices were bonded to fan-out headers and then wire bonded to a 84-pin LLC package as shown in figure 6.11. The wire bonding was very difficult to do on the smaller  $18\mu m$  and  $12\mu m$  pitch devices, as a result the yield of working pixels was fairly for these devices for both the



**Figure 6.11:** SLED part being wired bonded to an 84-pin LCC package

single and the grouped mesas. However, it is important to note that by default the yield of the SLED devices, even the large mesa parts, is about 60% in most cases. For more details on the packaing refer to appendix [D](#).

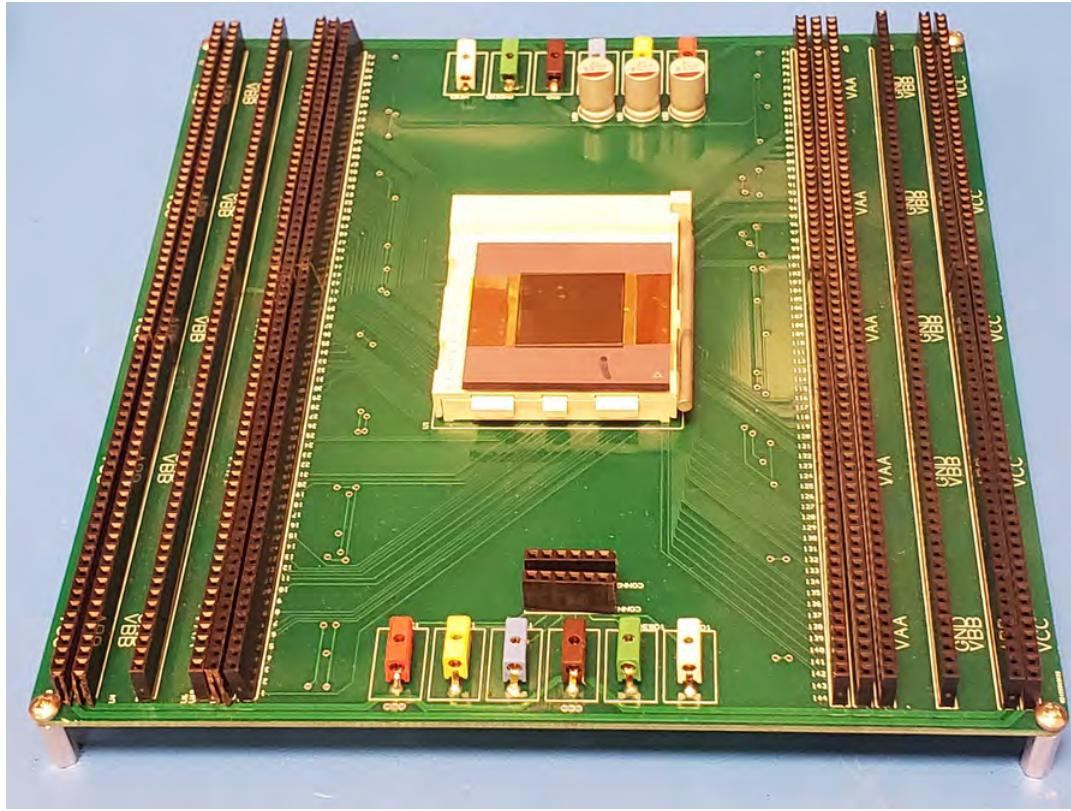
## Chapter 7

### RESULTS OF TESTING THE RIIC AND SLED PIXELS

To create a road map towards future generations IRSPIs based on LED technology, both components that make up a hybrid need to be **restrcutured** and **rethink** the way hybrids have been made up to date. This section goes over the test results of the physical parts for both the RIIC pixels and the SLED pixels. It is important to hightlight that there was no hybridization between the two parts, however, proof of concept testing was done using the RIIC to drive the SLED pixels fabricated. The results are also discussed in this section.

#### 7.1 RIIC pixels test results

The RIIC circuits were packaged on a 144 PGA ceramic package, thus in order to test it a **pcb was with** a PGA socket was designed to bring out all the signals of the chip. Figure 7.1 shows how the chip mounts in the center of the PCB and all 144 pins are brought out to numbered-female jumper connectors. There are also three power rails, VAA, VBB and VCC that the user can utilize as power buses. Power and ground are brought in via a Tektronix PS2521G programmable power supply using mini banana connectors. The main measuring piece of equipment is a Keithley 24XX meter/supply. The final piece of test set up is a Digilent explorer board to supply the digital signals for the chip. All of these components were controlled from a control PC used during all of the testing. Figure 7.2 display the setup used during the testing. The data collection was handled by the control PC and stored as a .json file, both the tektronix and the keithley were controllable through a python script used to set the voltage and current levels of the power supply, and read values read by the keithley meter. The explorer board was configured with the Waves software provided on Diginents website.



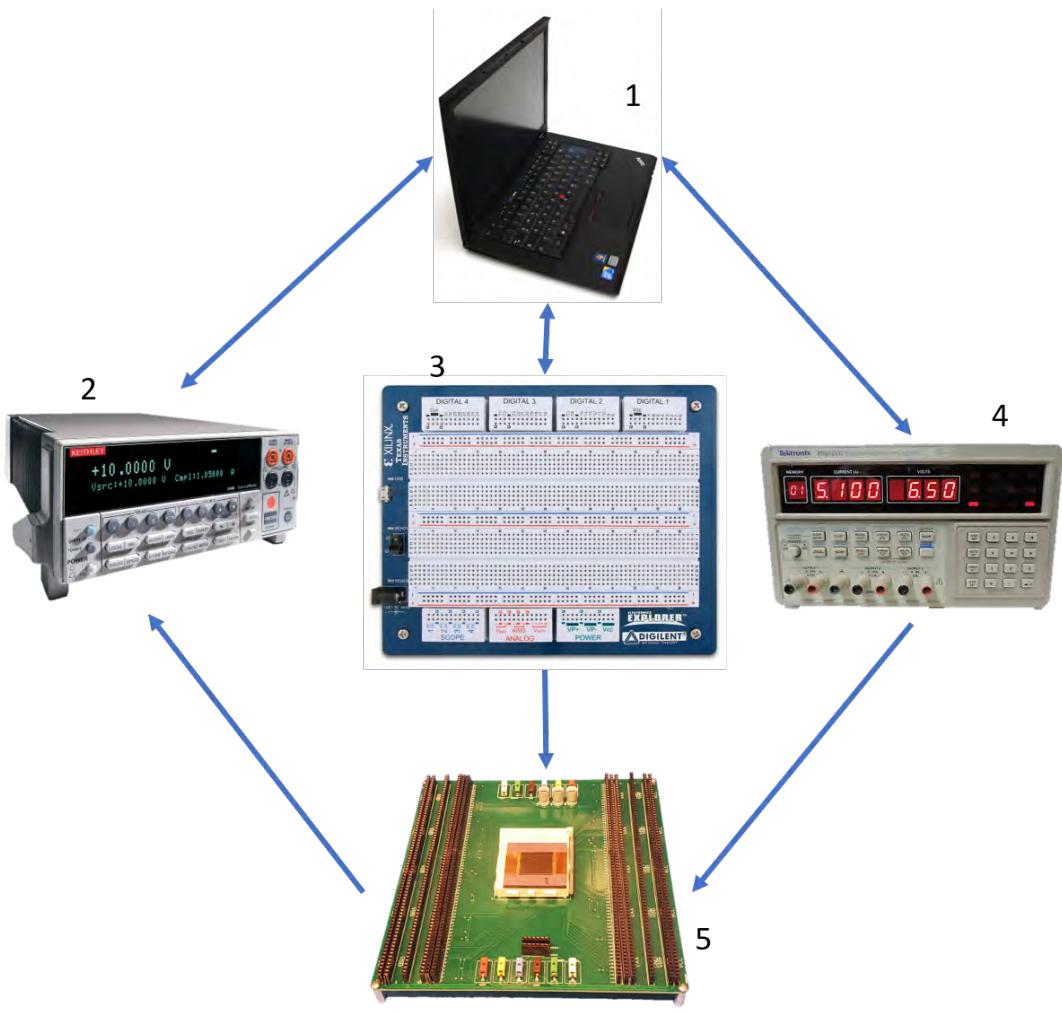
**Figure 7.1:** PCB used for housing the 144 PGA chips. It brings out all 144 pins to two rows of female jumper connectors. ESD diodes can be installed on the underside of the PCB if the user desires.



### 7.1.1 First test on the 4x4 super-pixel

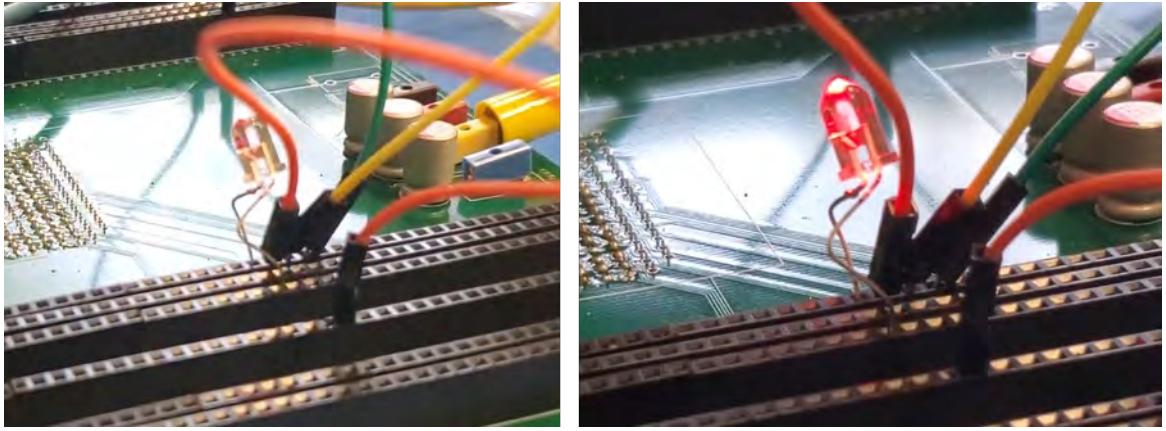
The most important circuit layout to be tested was the ART-IDEA RIIC super-pixel design as it is the basis for a future  $12\mu m$  pitch design. As mentioned in section 5.5, the circuit has 16 LED driver outputs, two analog inputs, six address lines and three telemetry signals. The very first test done on this circuit was a proof of life test with the following settings:

- **sels:** logic LOW at 0V using digital pin on Explorer board.
- **x0,x1,x2,x3:** HIGH,LOW,LOW,LOW where HIGH = 3.3V, these use digital pins on Explorer board.
- **y0,y1:** HIGH,LOW, also using the explorer board.
- **mselx,msely:** tied to ground.



**Figure 7.2:** Set up use to test the RIIC chip. (1) control PC, (2) Keithley meter, (3) digilent Explorer board, (4) Tektronix power supply, (5) RIIC chip mounted on break out pcb

- **vinn:** channel 2 on Tektronix supply, set to 0V.
- **vinp:** channel 3 on Tektronix supply, set to 0V.
- **VDD:** channel 1 on Tektronix supply, set to 3.3V.
- **LED line AN:** macro LED tied to 5V on Keithley meter. The macro LED chosen for the first test was just a standard off the self red LED.
- **All other outputs:** tied to ground.

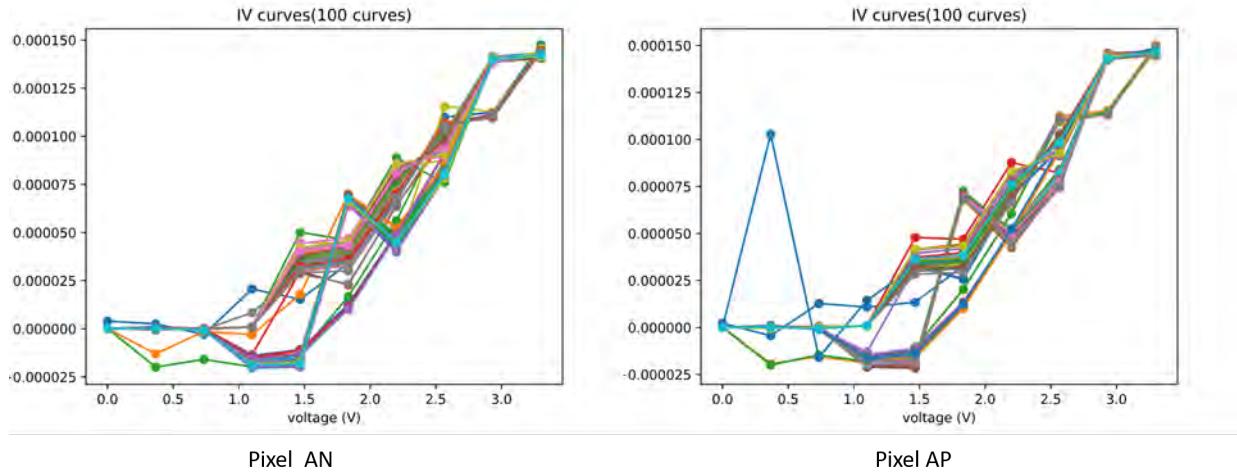


**Figure 7.3:** Lighting up an LED using a single RIIC pixel was the first test done on the 4x4 super-pixel. Left - the weak gear is driving the pixel. Right - the strong gear is driving the pixel

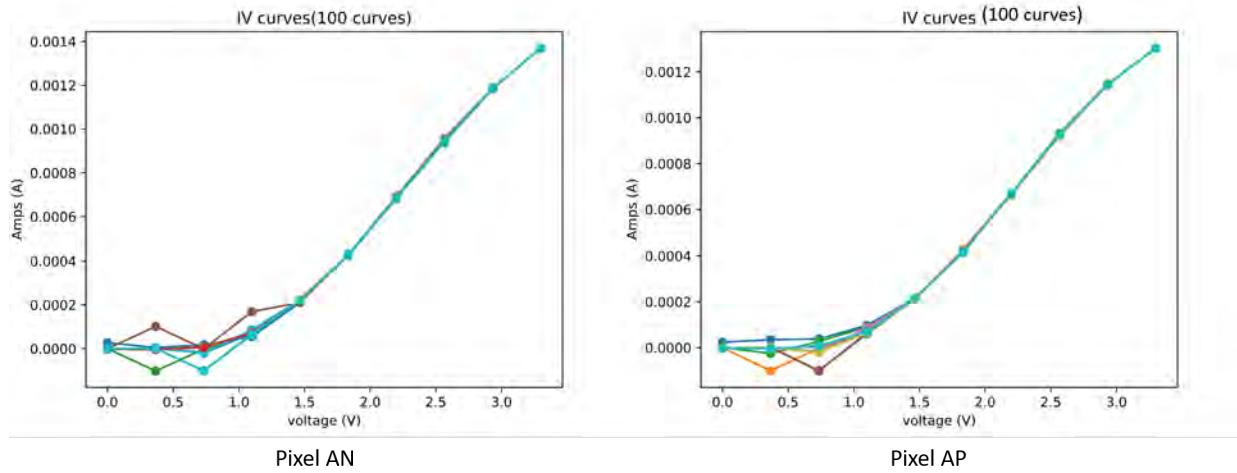
With the settings above pixels AN and AP are activated for writing, however, since AP is tied to ground there will be no current flow on it even if the analog signal  $v_{inp}$  goes above the threshold voltage needed to turn on the drive transistor. Additionally, the LED power voltage on line AN was intentionally kept at 5V just as a safety measure for the first test. For the test, all the values were kept constant as the settings above with the exception of the analog input  $v_{inn}$ . Manually, this value was slowly raised until 3.3V were reached, as that is the maximum allowed value for this input. After successfully demonstrating light on the LED, the test was repeated with the same setting and procedures with the exception of the  $sels$  signal being HIGH as it can be seen on figure 7.3.

### 7.1.2 characterization of the RIIC pixels

Using a python script that controlled the Keithley meter through RS232 serial protocol and the Tektronix supply via GPIB interface, the subsequent tests consisted on collecting IV data of the driver circuitry under different scenarios. The first of these series of tests was done on pixel AN using the weak gear, sweeping the analog  $v_{inn}$  signal from 0V to 3.3 V with a total of 10 steps in between. The LED power supply was provided by the keithley and kept constant at 5V during the duration of the sweep.

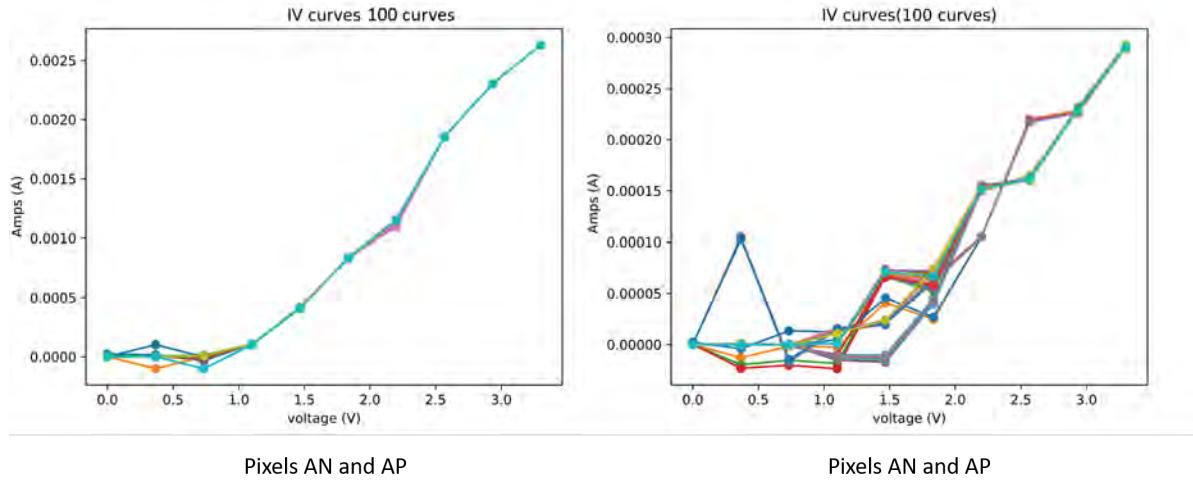


**Figure 7.4:** 100 sweeps of pixel AN and AP using vinn and vinp analog input signals respectively, the weak gear was more noisy than expected

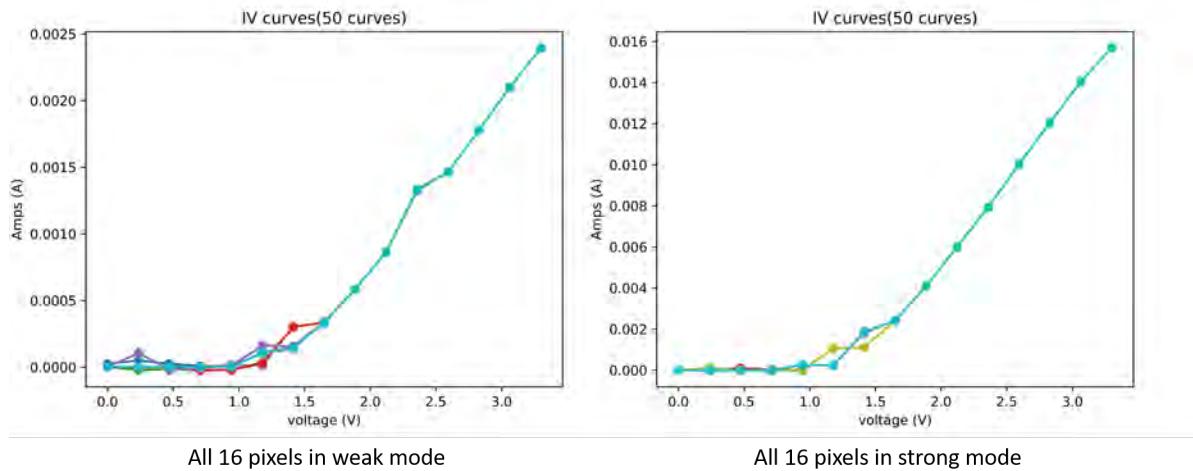


**Figure 7.5:** 100 sweeps of pixel AN and AP using vinn and vinp analog input signals respectively. The strong gear worked as expected and matched simulation results

Since there are two analog inputs per pixel pair, AP was tested with same methods, but with vinn held at 0V while vinp was swept from 0V to 3.3 V. The resulting IV curves for the weak gears of pixel AN and AP are shown in figure 7.4. The following plots on figure 7.5 display the results of sweeping the strong gear for the same pixel

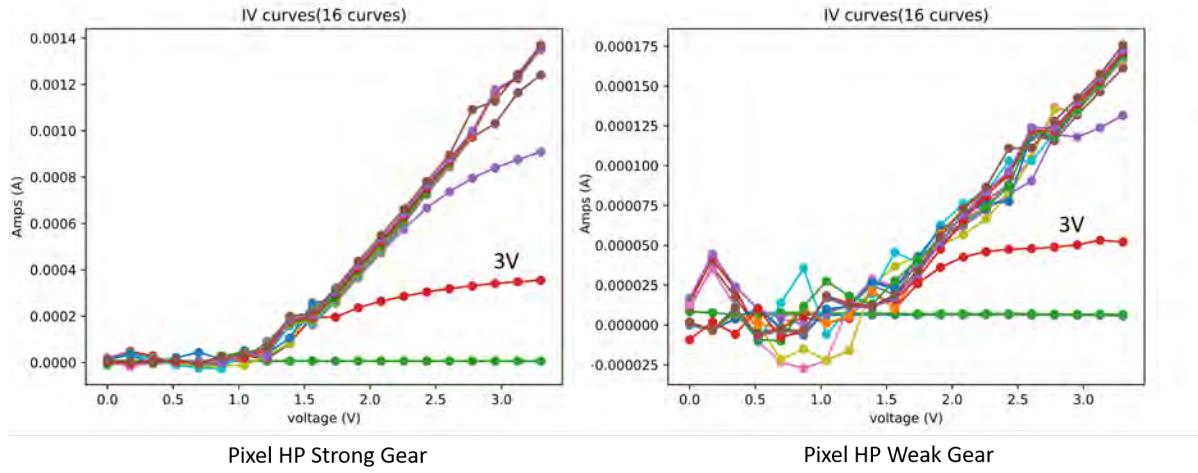


**Figure 7.6:** 100 sweeps of pixel AN and AP at the same time. Since both vinn and vinp ran simultaneously the current double as expected

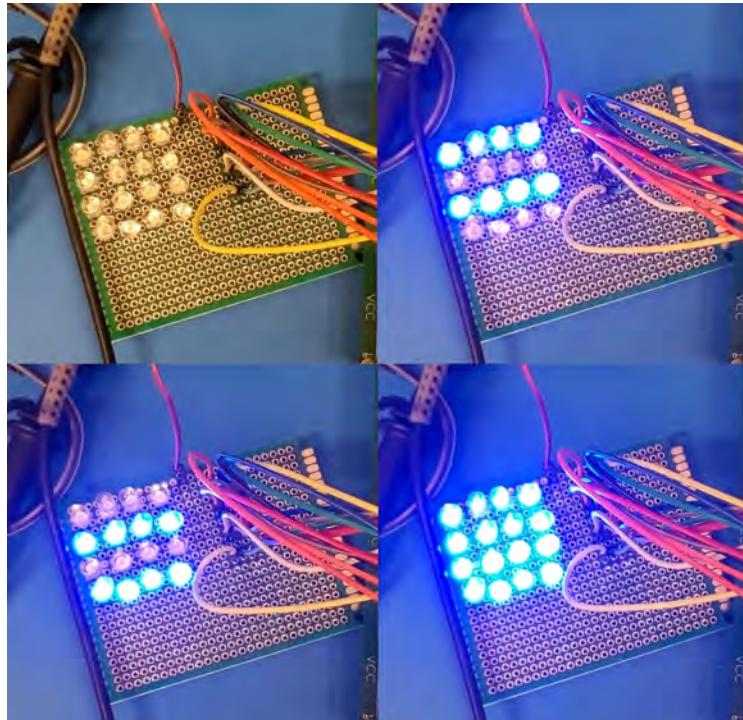


**Figure 7.7:** 50 sweeps of all 16 pixels at the same time. The weak gear is not as noisy

pair, the setting were kept the same between runs and the load was a macro LED. During both tests, the same pixel pair was swept 100 times as this gives a better idea of consistency and repeatability of the pixels. Weak gear will need to be investigated more in detail if we proceed with this design for a future RIIC. On the other hand, the strong gear was very consistent between runs, only a few times a bit of noise was



**Figure 7.8:** parametric sweep displaying the behavior of both gears with varying Voltage on the LED supply and sweeping  $v_{inj}$



**Figure 7.9:** A 4x4 mini grid of macro LEDs being dirven by the 4x4 RIIC super pixel

observed before the turn-on voltage, likely due to a very improvised test set up.

The next set of tests run on the RIIC super-pixel were aimed to verify that

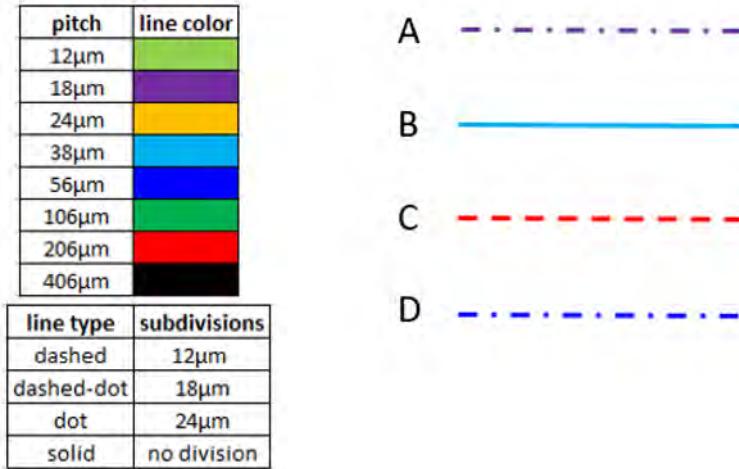
multiple pixels can operate at the same time and the effect it has on current draw. For these test, multiple address lines within the pixel were selected, in the first example shown in figure 7.6 only address lines  $x_0$ ,  $y_0$  were enabled to activate pixels AN and AP. For the example shown in figure 7.7, all of the address lines were enabled, thus putting all the pixels in write mode. The current consumption increased more or less linearly with the number of pixels turned on. Interestingly, the noise observed on the weak gear for single pixel sweeps was not apparent with all the pixels on.

During the design stage explain in an earlier section, simulations of the NLD-MOS demonstrated the gears could be operated at voltages up to 15V with a very stable current output. Figure 7.8 shows the IV curves for a parametric sweep where  $v_{inp}$  varied from 0 to 3.3 V and the LED power line increased by 1V after every sweep until the max allowed voltage of 15V. For this test the first voltage point able to turn on the LED was 3V. After setting the LED power line to 5V and above, there is very little change on the current output of the gears. As expected, with this design we have the comodity to adjust the LED voltage supply depending on the type of IR LEDs used and their turn on voltage.

The rest of the test performed on the RIIC dealt with prooving more functionalities. For instance, creating input patters that activate certain pixel, sweeping every pixel individually to ensure they work, or testing the other circuits such as the tiled super pixel or the improve driver circuit. An example of such test is figure 7.9, on this example all of the pixels were activated with their respective address lines, strong gear enabled on all pixels,  $v_{inn}$  and  $v_{inp}$  changing values as a 2 bit counter once per second. When  $v_{inn}$  is HIGH the top and third rows light up, and when  $v_{inp}$  is HIGH the second and bottom rows light up.

## 7.2 SLED pixels test results

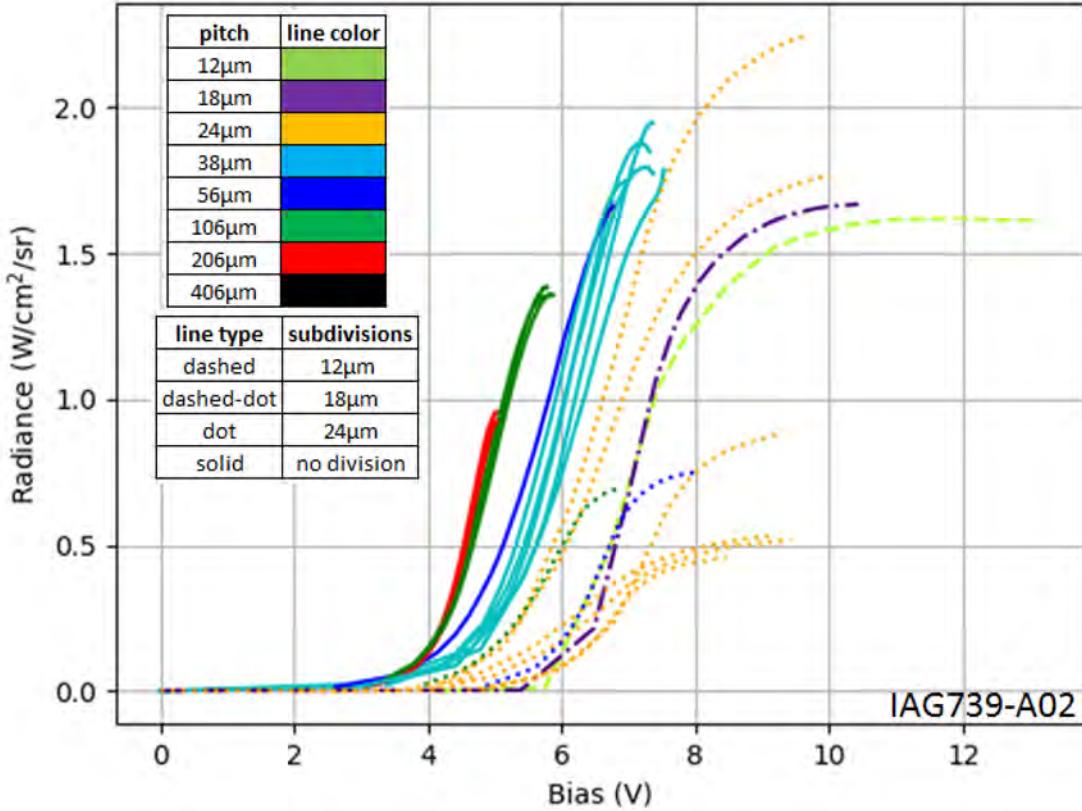
The SLED testing was performed at UIwoa facilities by the team that grew the LEDs for the project. The testing was done in a JK Henriksen CTS-1360 dewar at 77K. The devices under test emmit in the MWIR spectrum, thus an InSb detector



**Figure 7.10:** Legend for reading SLED plots. Solid lines = single mesas. Broken/dotted lines: Dashed =  $12\mu\text{m}$  pitch subdivisions, Dash-Dot =  $18\mu\text{m}$  pitch subdivisions, Dot =  $24\mu\text{m}$  pitch subdivisions

was used for all the data collection. It is worth mentioning that the test chips had a very low yield for  $24\mu\text{m}$ ,  $18\mu\text{m}$  and  $12\mu\text{m}$  pixels. The low yield is due to the test chip bonding process and layout, not the small mesas. The following plots in this section show the radiance of several test chips tested. The radiance for mesas larger than those found on the  $24\mu\text{m}$  pitch devices behaved and emitted light as expected for a device with 8-stages. However, the small format pixels displayed **very scatter** and low radiance results across the data collected.

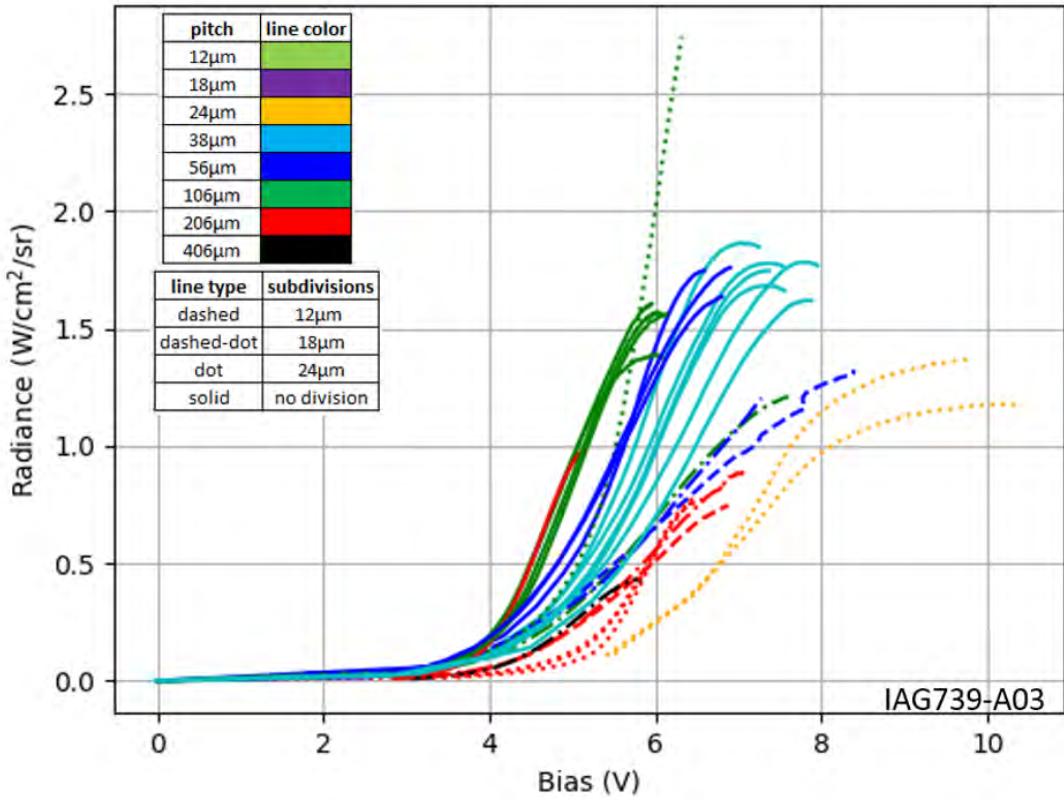
Before analyzing the data collected it is important to understand how to read the plots. Figure 7.10 is the legend for reading the plots in this section. In section 6.2 it was discussed how the SLED devices come in different sizes, and for some of the quadrants on the wafer, these areas were subdivided to create mini arrays of small format pixels. Four examples are given in the legend, sample A is purple meaning is a device grown on a  $18\mu\text{m} \times 18\mu\text{m}$  area, then it is also a Dash-Dot line meaning it was subdivided to make a  $18\mu\text{m}$  pitch SLED device. In this particular case, only one device fits in that area. Sample B is very straight forward, it is a  $38\mu\text{m} \times 38\mu\text{m}$  mesa from quadrant 1 with no **partitions**. Sample line C is a  $206\mu\text{m} \times 206\mu\text{m}$  area subdivided



**Figure 7.11:** SLED test chip IAG739-A02 radiance vs. voltage 

into  $12\mu m$  pitch pixels. Finally D, a  $58\mu m \times 58\mu m$  area with  $18\mu m$  pitch partitions.

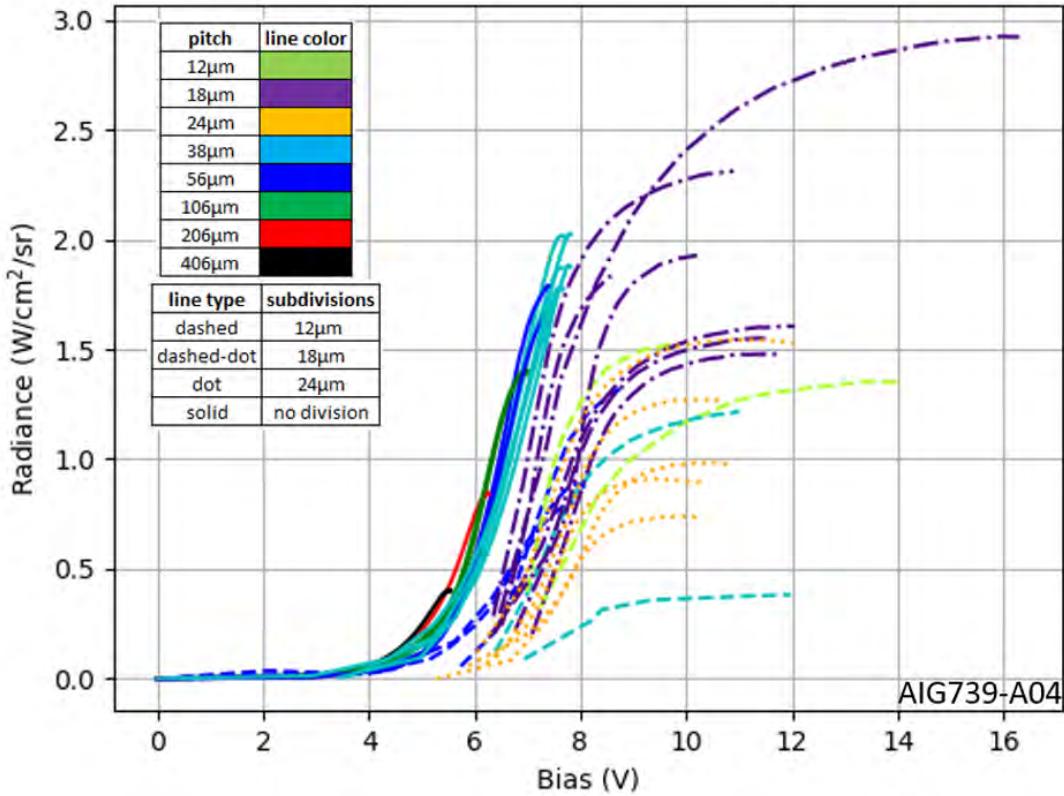
The following radiance versus voltage plots belong to 3 different SLED test chips. The 8-stage devices were chosen to reduce the turn on voltage of the pixels, however from the data collected the turn on voltage is higher than desired ranging from 4 Volts for large mesa devices and up to 6 volts for small mesa devices. The trend of increasing light extraction can be observed on all of the test chips but it varies where the radiance start to decrease with pixel size. This first iteration of SLED devices was not a very good one for small format pixels with a pitch less than than or equal to  $24\mu m$ . In the case of test chip IAG739-A02 the pixel with the highest radiance had a pixel pitch of



**Figure 7.12:** SLED test chip IAG739-A04 radiance vs. voltage

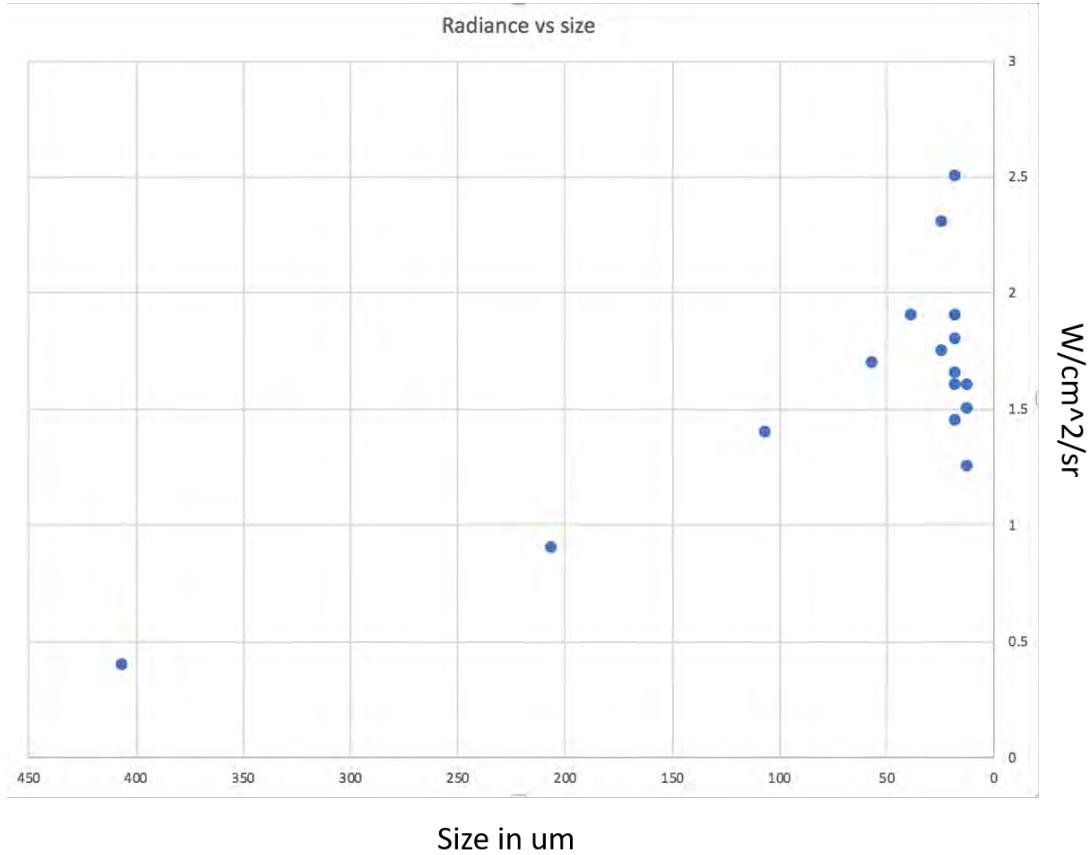
$24\mu m$ , however in that same test chip other  $24\mu m$  pitch devices performed very poorly. The 12 and 18 micron pitch devices on IAG739-A02 did not perform better than their larger counterparts, and both had similar radiance 

Test chip IAG739-A03 on figure 7.12 had some interesting results revealed by the lines brought out to the test pins. An area of  $106\mu m^2$  subdivided into a mini grid of  $24\mu m$  pitch pixels radiated more light than the devices with no partition and same area. Four quadrants with the same area but different subdivisions were tested on IAG739-A03. These are the red curves on figure 7.12, the non-divided mesa with an area of  $206\mu m^2$  had the lowest turn on voltage but the radiance was comparable to that of the mini grids for all small format pixels on other quadrants. However, this particular test chip had very low radiance for all around. The results for the third



**Figure 7.13:** SLED test chip IAG739-A04 radiance vs. voltage

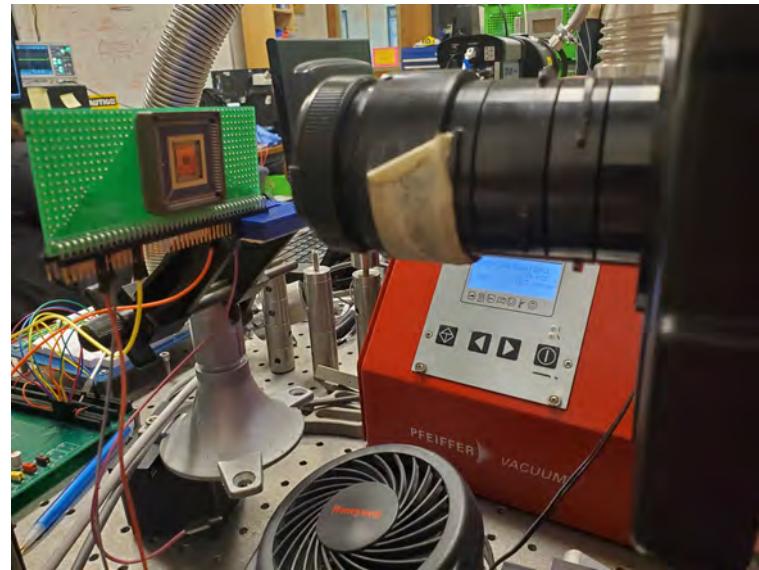
chip tested can be observed on figure 7.13. In this particular test chip the brightest pixel was a  $18\mu m$  pitch device, but other small format pixels performed poorly. The best way to understand the test results is by aggregating all data collected at UIowa and comparing it in a single plot shown in figure 7.14. The plot compares the max radiance observed for different SLED devices of different sizes, the trend for higher light extraction is observed as the physical size of the pixel decreases. However, for the small format pixels the resulting light extraction is very scattered. The highest radiance observed was an  $18\mu m$  pitch device, but it was a single occurrence as other same-size pixels showed lower radiance. As for the  $12\mu m$  pitch pixels, the results did not show the higher radiance expected.



**Figure 7.14:** Comprehensive view of SLED devices tested by pixel-pitch, values represent the max radiance observed on data collected at UIowa 

### 7.3 combined test results

The final goal for any mature IRSP system based on LED technology is to create a working hybrid with teh RIIC and SLED parts. This process is very expensive and it is usually exclusive to mature parts and not experimental devices. Nontheless, it is worthwhile to combine the RIIC and LEDs created for this project and figure out how well they work together. The test set up for these experiments is the same as the one discussed in section 7.1 and figure 7.2, but with the addition of a PLCC84 socket to hold the SLED test chips and a SC6800 FLIR camera as seen on figure 7.15. One of the most important tests was to show that the RIIC had the ability to light up and control the brightest of the LEDs. For this test the LED power supply was kept at



**Figure 7.15:** In order to test the SLED test chips in conjunction with the RIIC test chip, a PLCC86 socket was added to the test set up to hold the SLED test chips, and a FLIR SC6800 camera to capture the light



**Figure 7.16:** Using the RIIC pixel to drive a SLED pixel at different light intensities

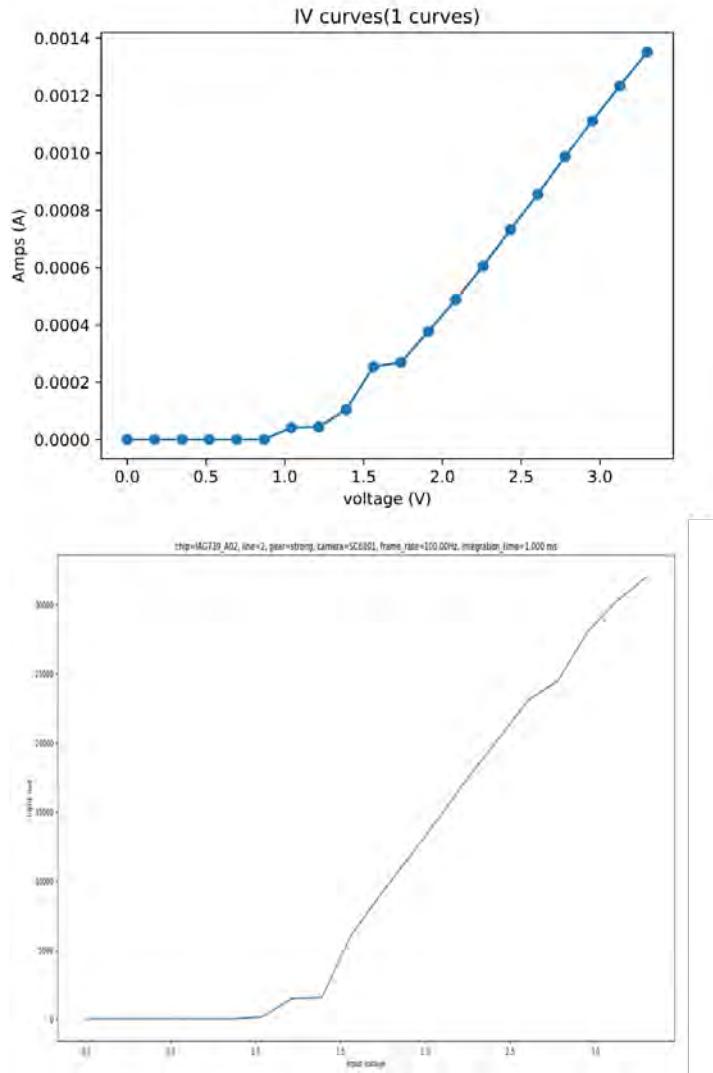
15V using the keithley meter, then the RIIC was configured to step through the full analog input range of 0V to 3.3V. A working LED on the SLED test chip was tied



**Figure 7.17:** Post-process camera image captured for a  $38\mu m^2$  mesa SLED device on test chip IAG739-A02 line 2 using strong gear

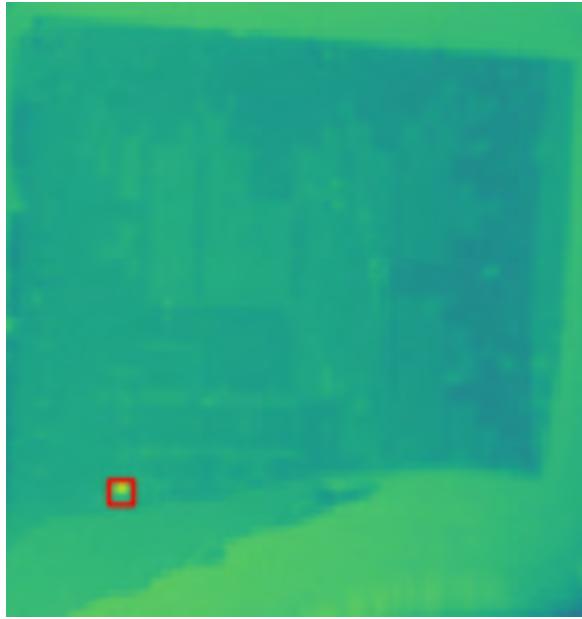
pixel AN on the RIIC using jumper wires. The test was successful and images of the light captured by the camera are shown on figure 7.16, going from left right and top to bottom, the image captures different stages of light emission as the control analog signal ramps up.

Three SLED test chips underwent testing at Udel's facilities, each had a slight variation to the process. Plots for SLED chip IAG739-A02 are discussed in this section as it has the specs that were originally set for the goals of the SLEDS, 8-stage devices for lower turn-on voltage. The other two test chips are more experimental and results can be found on appendix E. The following plots correlate the demonstrate the relationship between the light captured by the IR camera in units of camera-counts, and the current consumption of the pixel. The method for gathering data consists of stepping the driving gear from minimum to maximum value using a vin analog control signal and keeping the LED power at 15V. A total of 20 steps are taken between 0V and 3.3V and



**Figure 7.18:** Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested -  $38\mu m^2$  mesa SLED device on test chip IAG739-A02 line 18 using strong gear

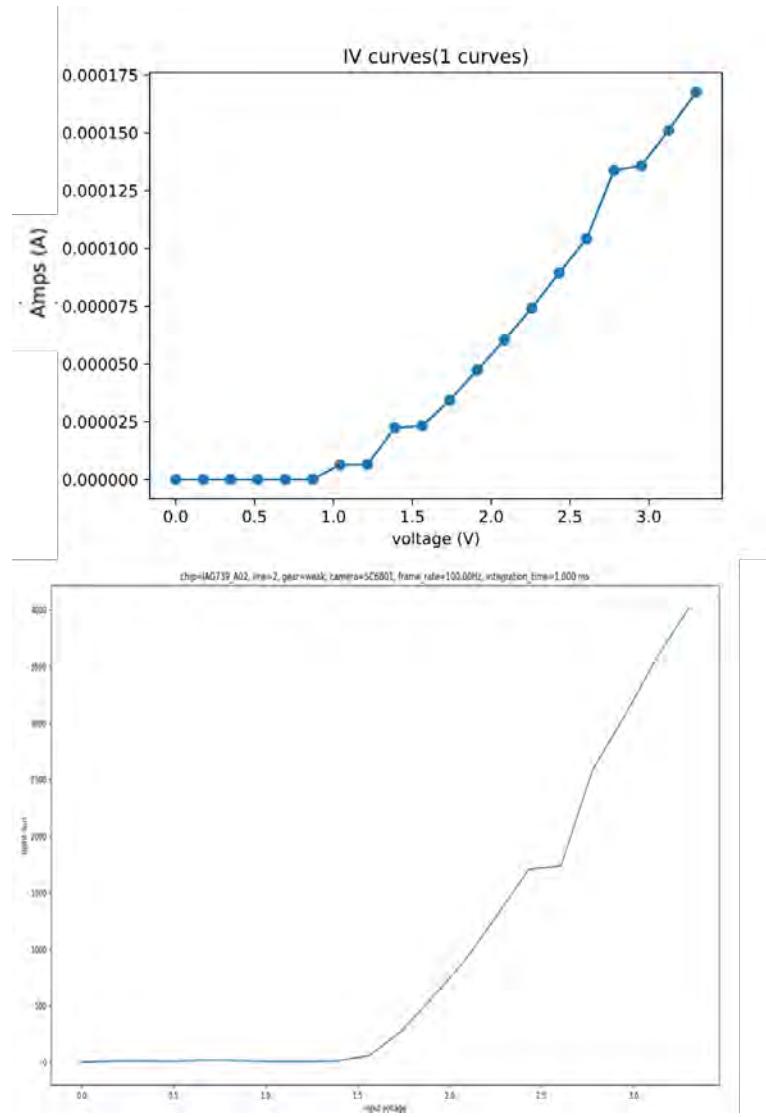
for each of those voltage steps 10 camera frames are captured. The camera was set to process frames at 100Hz with an integration time of 1ms. Frames capture by the camera are processed by performing background subtraction, where the background frames are collected before any light is emitted from the pixel. Ideally the resulting Delta should be enough to figure out the total light captured by the camera, however, due to ambient



**Figure 7.19:** Post-process camera image captured for a  $38\mu\text{m}^2$  mesa SLED device on test chip IAG739-A02 line 2 using weak gear

noise a region of interest is used around the pixel of interest to eliminate the noise[?]. All of the testing done on the chips were performed at ambient temperature about 300K. Figures 7.21 through 7.20 show the results for a  $38\mu\text{m}^2$  unpartitioned mesa for both the weak and strong gears. And figures 7.21 and 7.22 are the test results for a  $12\mu\text{m}$  pitch SLED device.

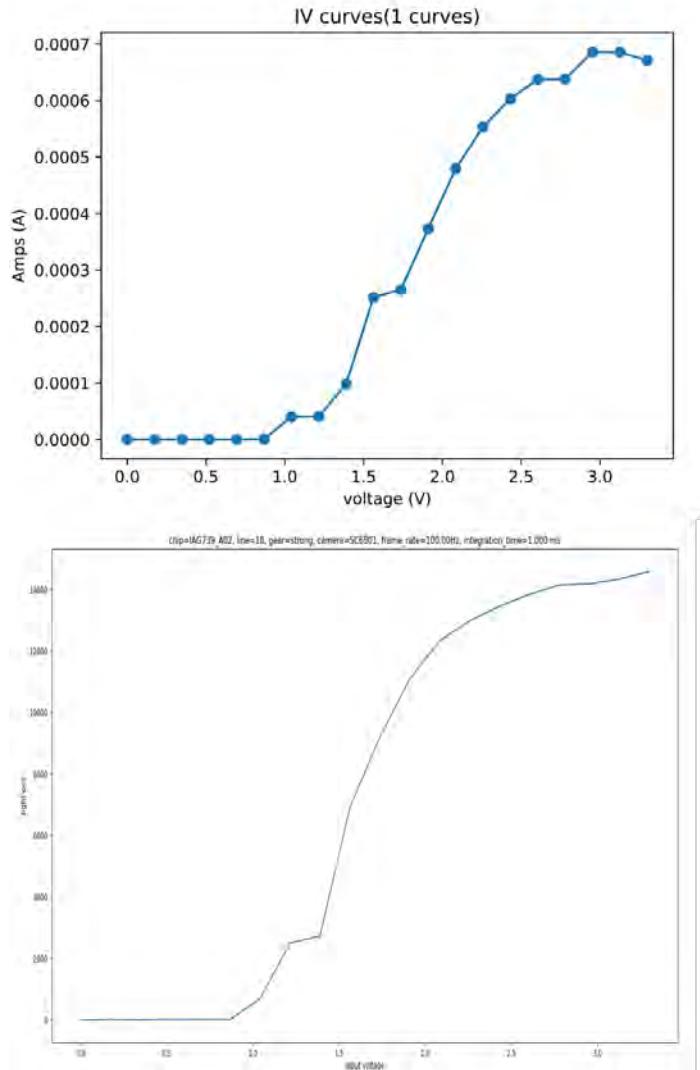
As discussed in section 5.1.1, the gears on the RIIC super-pixel are compatible with LEDs with different turn-on voltages as the NLDNMOS current stays ralatively constant from 4V onward. The current measure on the  $38\mu\text{m}^2$  SLED device was identical to the current that was measured on the macro LED for both the weak and the strong gear. It is important to note that the turn on voltage for a macro LED is usually less than a volt while the turn on voltage for the particular SLED device shown on the figures is 6 volts. The pixel data collected shown on figure 7.22 was slightly different than other data collected on the same test chip for other SLED devices as a saturation point was reached on the device. This is believed to be a device-specific behavior likely due to the low yield of the chips.



**Figure 7.20:** Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested -  $38\mu\text{m}^2$  mesa SLED device on test chip IAG739-A02 line 18 using weak gear



**Figure 7.21:** Post-process camera image captured for a  $12\mu m$  pitch SLED device on test chip IAG739-A02 line 2 using strong gear



**Figure 7.22:** Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested -  $12\mu\text{m}$  pitch SLED device on test chip IAG739-A02 line 18 using strong gear

## Chapter 8

### CONSLUSION

Infrared scene projectors are valuable tools used in hardware in the loop test scenarios. Over the years the sensor technology has advanced drastically and reached very high resolutions. MWIR cameras and sensors are no exception to the advancement in technology. Demands for higher resolution IRSPs are at an all-time high as they provide a cost-effective solution to field testing. In 2008, CVORG, a research group led by Dr. Fouad Kiamilev at the University of Delaware, became involved in the research of creating better IRSPs using LED technology. The **emmitter** array developed consists of two main components, the RIIC and the SLEDs, which are bonded together via flip chip bonding using indium bumps.

The very first successful LED based IRSP was produced in 2014 with a resolution of 512 x 512 pixels. Although it had some limitation in the dynamic range, it proved the technology was viable and open the path for further research. In the following years, a variety of IRSPs were developed, including TCSA a two-color system with a resolution of 512 x 512, NSLEDS a single color 1024 x 1024 pixel resolution systems, and HDILED a high definition 2048 x 2048 pixel resolution system. The most successful systems developed up to date have been the NSLEDS projector and much of it is due to the higher yields per wafer. However, a 1024 x 1024 projector does not have the resolution desired by systems that undergo the testing. HDILED on the other hand, has the resolution desired but due to the pixel pitch being the same as NSLEDS,  $24\mu m$ , the physical size of the hybrid has a huge impact on the yield of working parts making it very costly to produced.

The work described in this dissertation explored a new approach to increasing the density and resolution of pixels for future IRSPs. This was the very first time the

fabrication process was changed on the RIIC side as the technology database for the VLSI design was updated. Additionally, the architecture of the RIIC super-pixel was modified to make better utilization of space. The results of the new RIIC architecture were very positive as the 4x4 super-pixel design worked reliably. The use of NLDMOS as drive gears made it very versatile to try different types of LEDs with different turn-on voltages or number of stages.

On the SLED side, a series of LED pixels of different sizes were created, including the very first time that LED with a pitch of  $18\mu m$  and  $12\mu m$  was attempted in MWIR. The results for the SLED devices were positive in demonstrating light emission from the  $18\mu m$  and  $12\mu m$  pitch pixels. This was the very first time this has ever been attempted, no one in the world has ever succeeded in trying this. However, there were inconclusive results as to whether decreasing the size of the pixel past  $24\mu m$  pitch actually helps with the light extraction. During fabrication, there were proximity issues with the lithography of small format pixels, and an aluminum cell problem that might have skewed the characteristics of the SLED devices.

Since the completion of the program that funded this work, there have been major improvements to the SLED technology. Current improvements claim to have improved the efficiency of the LED by 7x. An array has not been fabricated with such claimed improvements but it is inevitable that it will happen in the near future. It is certain that the need for higher resolution arrays will stay until resolutions of 4096x4096 or higher are reached. The RIIC super pixel designed and proven to work in this project will be one of the bridges that will enable the cross to such resolutions.

## REFERENCES

- [1] B. E. Cole and C. J. Han, “Low power infrared scene projector array and method of manufacture,” Feb. 4 1997. US Patent 5,600,148.
- [2] J. Marks, *Abuted IRLED infrared scene projection design and their characterization*. PhD thesis, University of Delaware, 2019. sequester.
- [3] S. B. Infrared, “Mirage dynamic ir scene projectors.” <https://sbir.com/dynamic-ir-scene-projectors/>, 2019. Accessed on 2019-10-10.
- [4] C. Wood, “Materials for thermoelectric energy conversion,” *Reports on progress in physics*, vol. 51, no. 4, p. 459, 1988.
- [5] KentOptronics, “Infrared scene projector.” <http://www.kentoptronics.com/infrared.html>, 2014. Accessed on 2019-10-4.
- [6] T. K. Ewing and W. R. Folks, “Liquid crystal on silicon infrared scene projectors,” in *Technologies for Synthetic Environments: Hardware-in-the-Loop Testing X*, vol. 5785, pp. 36–45, International Society for Optics and Photonics, 2005.
- [7] S. Iijima, “Helical microtubules of graphitic carbon,” *nature*, vol. 354, no. 6348, p. 56, 1991.
- [8] J. Chen, V. Perebeinos, M. Freitag, J. Tsang, Q. Fu, J. Liu, and P. Avouris, “Bright infrared emission from electrically induced excitons in carbon nanotubes,” *Science*, vol. 310, no. 5751, pp. 1171–1174, 2005.
- [9] S. Iijima and T. Ichihashi, “Single-shell carbon nanotubes of 1-nm diameter,” *nature*, vol. 363, no. 6430, p. 603, 1993.
- [10] D. T. Norton Jr, “Type-ii inas/gasb superlattice leds: applications for infrared scene projector systems,” 2013.
- [11] G. A. Ejzak, J. Dickason, J. A. Marks, K. Nabha, R. T. McGee, N. A. Waite, J. T. Benedict, M. A. Hernandez, S. R. Provence, D. T. Norton, *et al.*, “512x512, 100 hz mid-wave infrared led microdisplay system,” *Journal of Display Technology*, vol. 12, no. 10, pp. 1139–1144, 2016.
- [12] K. Nabha, “100 hz 512x512 sleds system design,” Master’s thesis, University of Delaware, 2014.

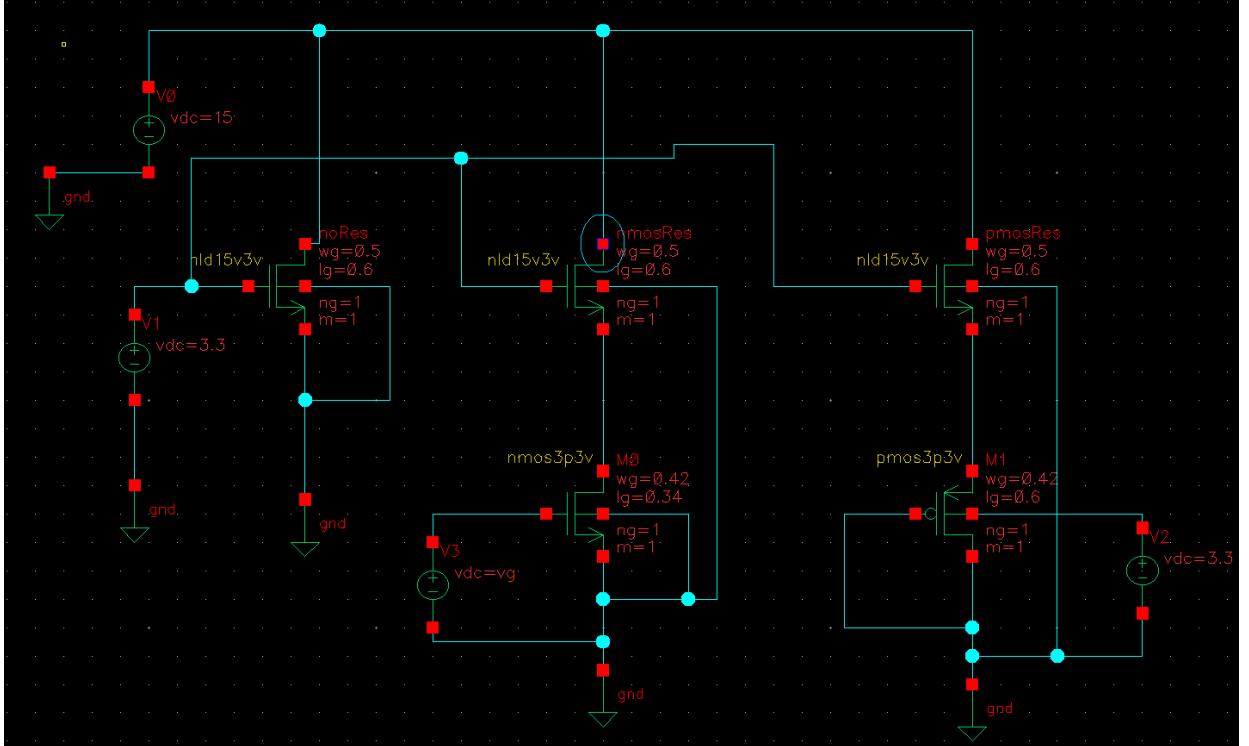
- [13] D. T. Norton, J. T. Olesberg, R. T. McGee, N. A. Waite, J. Dickason, K. Goossen, J. Lawler, G. Sullivan, A. Ikhlassi, F. Kiamilev, *et al.*, “512x512 individually addressable mwir led arrays based on type-ii inas/gasb superlattices,” *IEEE Journal of Quantum Electronics*, vol. 49, no. 9, pp. 753–759, 2013.
- [14] R. F. Farrow, *Molecular beam epitaxy: applications to key materials*. Elsevier, 1995.
- [15] J. Benedict, R. McGee, J. Marks, K. Nabha, N. Waite, G. Ejzak, J. Dickason, H. Ahmed, M. Hernandez, P. Barakhshan, T. Browning, J. Volz, R. Ricker, F. Kiamilev, J. Prineas, and T. Boggess, “1kx1k resolution infrared scene projector at 24 $\mu$ m pixel pitch,” *GOMAC Tech Reno NV*, 2017.
- [16] J. Benedict, R. McGee, H. Ahmed, M. Hernandez, P. Barakhshan, R. Houser, J. Marks, K. Nabha, G. Ejzak, N. Waite, J. Dickason, T. Browning, R. Ricker, A. Muhowski, R. Heise, F. Kiamilev, and J. Prineas, “4-megapixel infrared scene projector based on superlattice light emitting diodes,” *GOMAC Tech Miami FL*, 2018.
- [17] C. H. Stapper and R. J. Rosner, “Integrated circuit yield management and yield analysis: Development and implementation,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 8, no. 2, pp. 95–102, 1995.
- [18] “International roadmap of devices and systems 2017 edition: Yield enhancement.,” tech. rep., IRDS, IEEE, 2018.
- [19] I. C. E. Corporation, “Yield and yield management.” <http://smithsonianchips.si.edu/ice/cd/CEICM/SECTION3.pdf>.
- [20] M. Hernandez, J. Dickason, P. Barakhshan, N. Waite, R. McGee, and F. Kiamilev, “Scalable testing platform for cmos read-in integrated circuits,” *GOMAC Tech Orlando FL*, 2016.
- [21] M. Hernandez, J. Dickason, P. Barakhshan, J. Marks, G. Ejzak, A. Deputy, A. Waite, R. McGee, and F. Kiamilev, “Results of testing read-in integrated circuit (riic) wafers and hybrids,” *GOMAC Tech Reno NV*, 2017.
- [22] M. Hernandez, “Data collection and analysis of read-in integrated circuits designed to drive arrays of infrared light emitting diodes using a scalable and modular testing platform for infrared scene projectors,” Master’s thesis, University of Delaware, 2016.
- [23] M. Hernandez, J. Marks, E. Koerperick, P. Barakhshan, G. A. Ejzak, K. Nabha, J. Prineas, and F. Kiamilev, “Improving density and efficiency of infrared projectors,” *IEEE Photonics Journal*, 2019.

- [24] B. Van Zeghbroeck, “Principles of semiconductor devices,” *Colarado University*, vol. 34, 2004.
- [25] J. P.-B. Hanson and J. Pritiskutch, “Understanding ldmos device fundamentals,” 2000.
- [26] R. A. Hastings and R. A. Hastings, *The art of analog layout*, vol. 2. Pearson Prentice Hall New Jersey, 2006.
- [27] N. H. Weste and D. Harris, *CMOS VLSI design: a circuits and systems perspective*. Pearson Education India, 2015.
- [28] C. Jackson, T. Browning, A. Landwehr, D. May, H. Ahmed, A. Waite, and F. Kiamilev, “Demonstration of packetized display protocol (pdp) to overcome speed and resolution limitations of conventional display protocols,” in *2019 IEEE Research and Applications of Photonics in Defense Conference (RAPID)*, pp. 1–1, IEEE, 2019.
- [29] J. E. Vinson and J. J. Liou, “Electrostatic discharge in semiconductor devices: an overview,” *Proceedings of the IEEE*, vol. 86, no. 2, pp. 399–420, 1998.
- [30] E. J. Koerperick, D. T. Norton, J. T. Olesberg, B. V. Olson, J. P. Prineas, and T. F. Boggess, “Cascaded superlattice inas/gasb light-emitting diodes for operation in the long-wave infrared,” *IEEE Journal of Quantum Electronics*, vol. 47, no. 1, pp. 50–54, 2010.

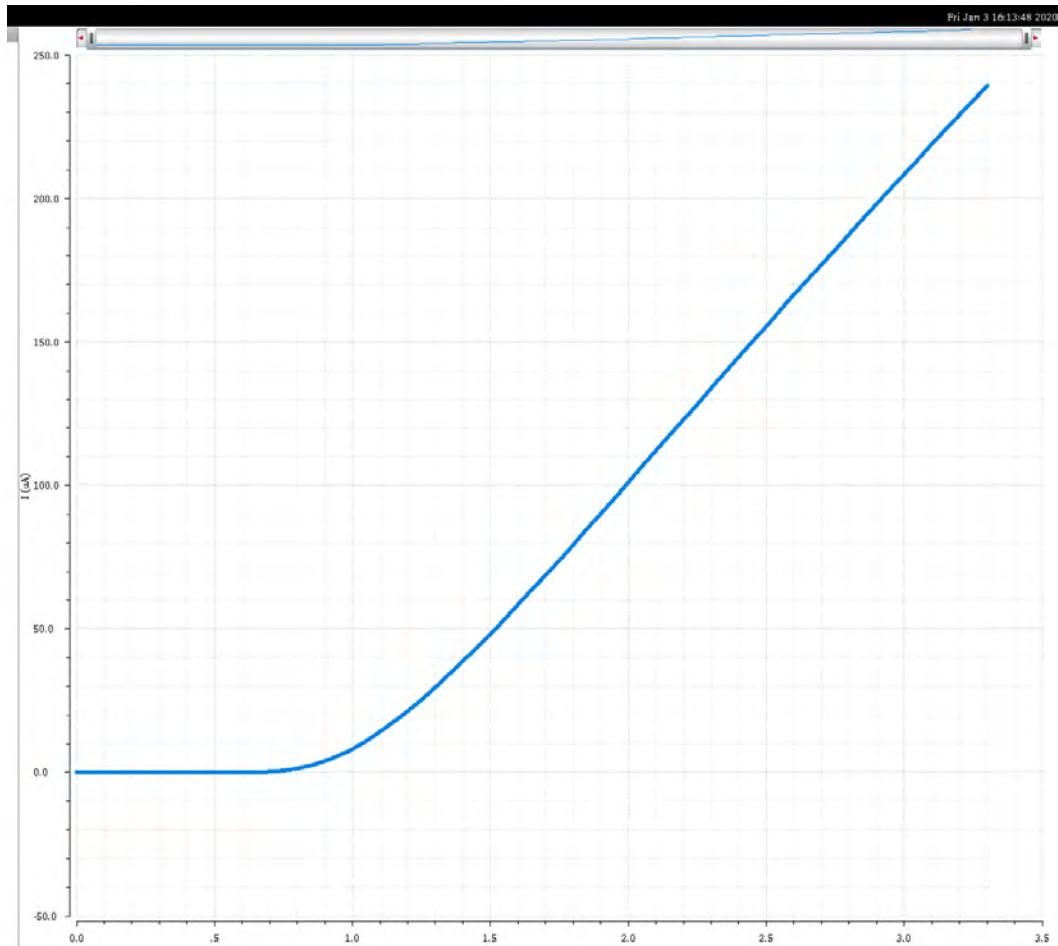
## Appendix A

### EXPERIMENTAL CIRCUITS SIMULATIONS AND FIGURES

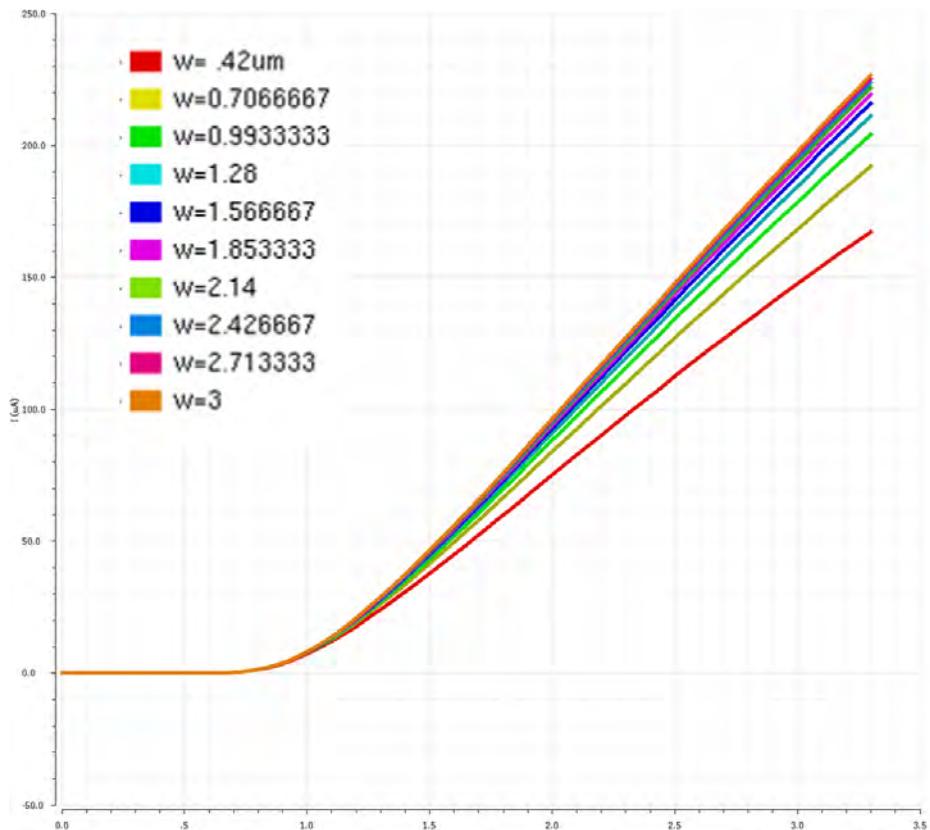
This is supporting material for section 5.5.1. It contains the results of the simulations performed and the circuits used to simulate them. The results were used to determine the correct components to be used to improve the driver circuit on the ART-IDEA pixel. The final driver circuit that resulted from these experiments was laid out on Cadence and incorporated to the final chip layout to be fabricated by OnSemi. The new prototype driver circuits has a reset line added to the node at the memory capacitor in order to fully discharge it, and a properly sized NMOS transistor cascaded to the weak gear to allow for finer control of the lower end of light emission.



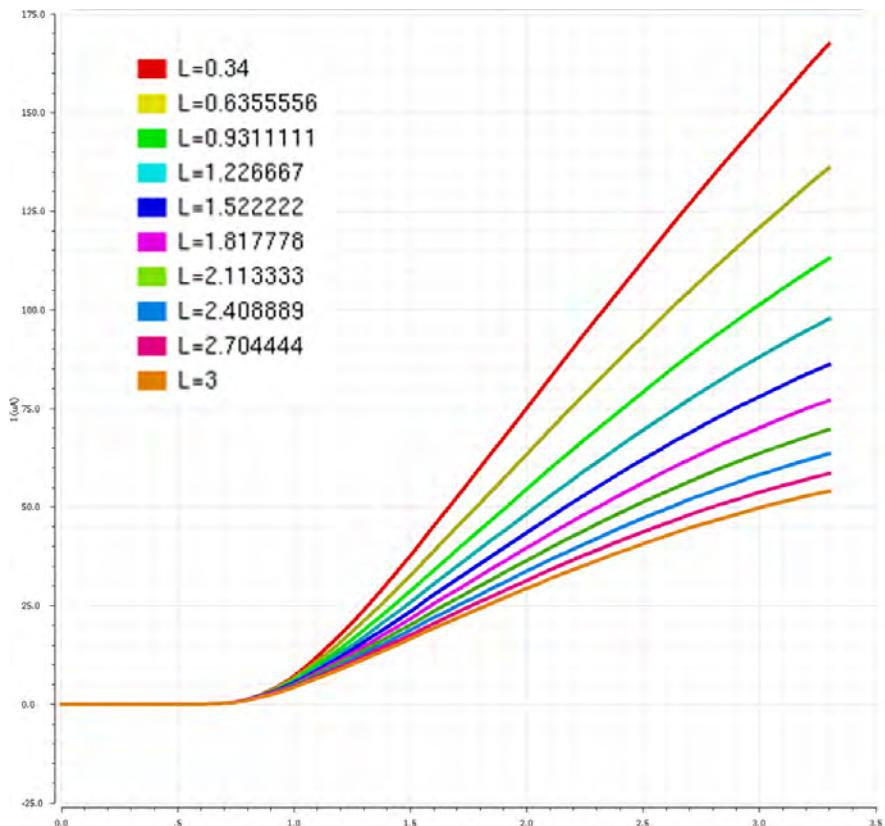
**Figure A.1:** cascoding transistors simulation schematic. The three paths are a stand alone NLD MOS transistor, middle path uses a NMOS transistor as resistor, right path uses a PMOS



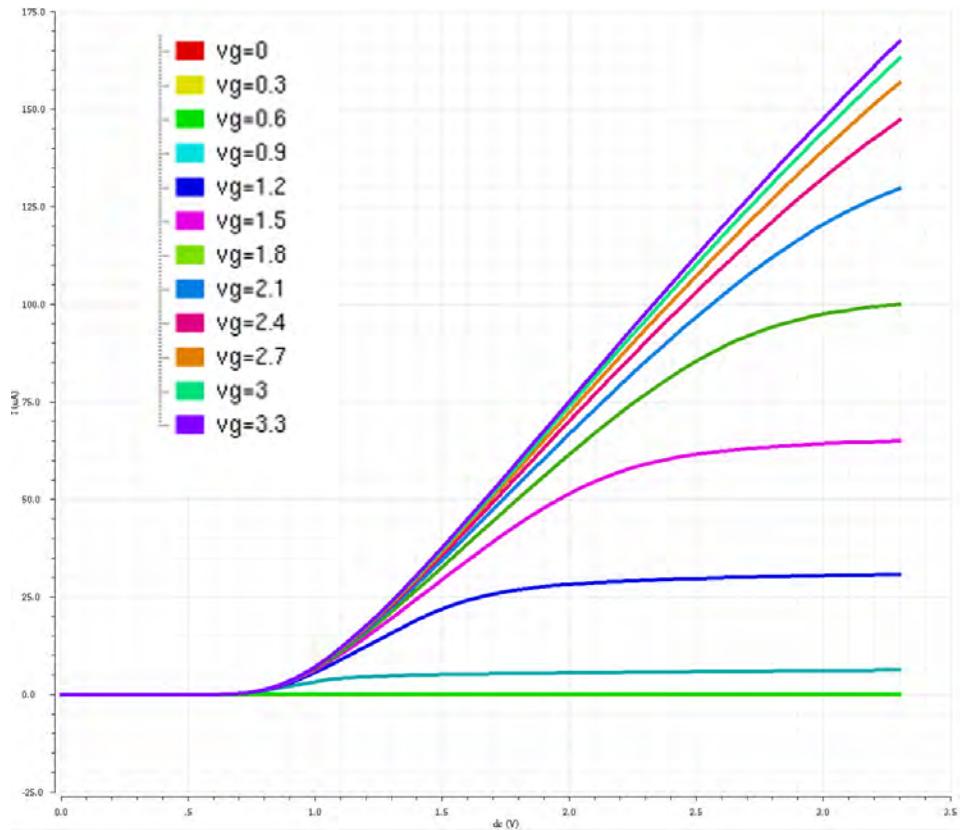
**Figure A.2:** For reference, this is the Current vs Voltage curve for the weak gear NLD MOS of the ART-IDEA pixel



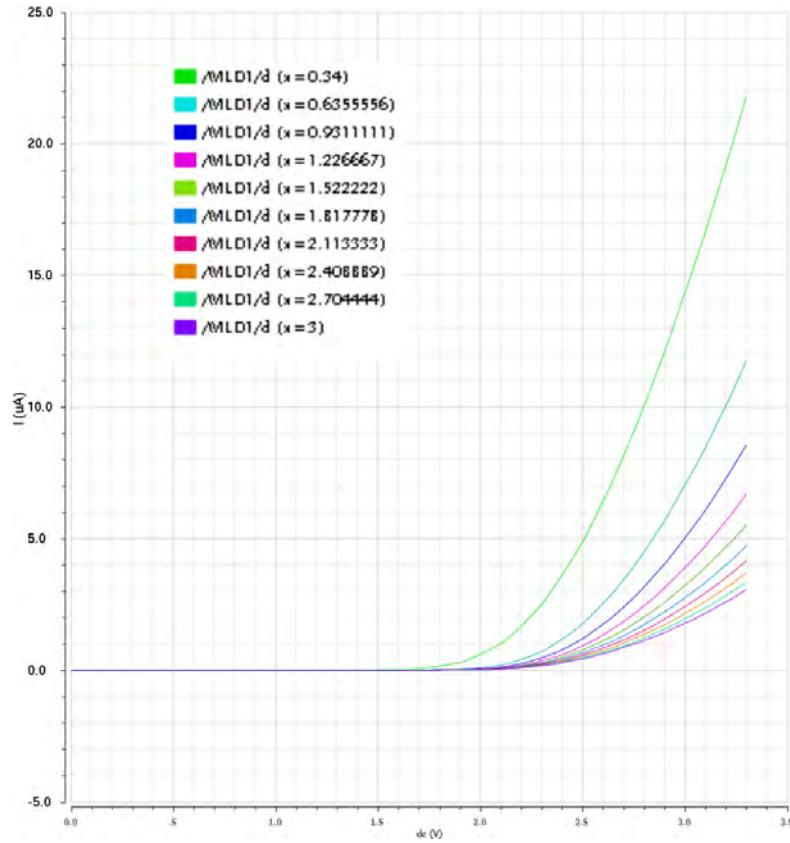
**Figure A.3:** Varying the width of the NMOS transistor on the cascode circuit did not have a big effect as expected. This is because the larger the width of the device, the wider the channel will be. In other words, there is a bigger highway for electrons to flow.



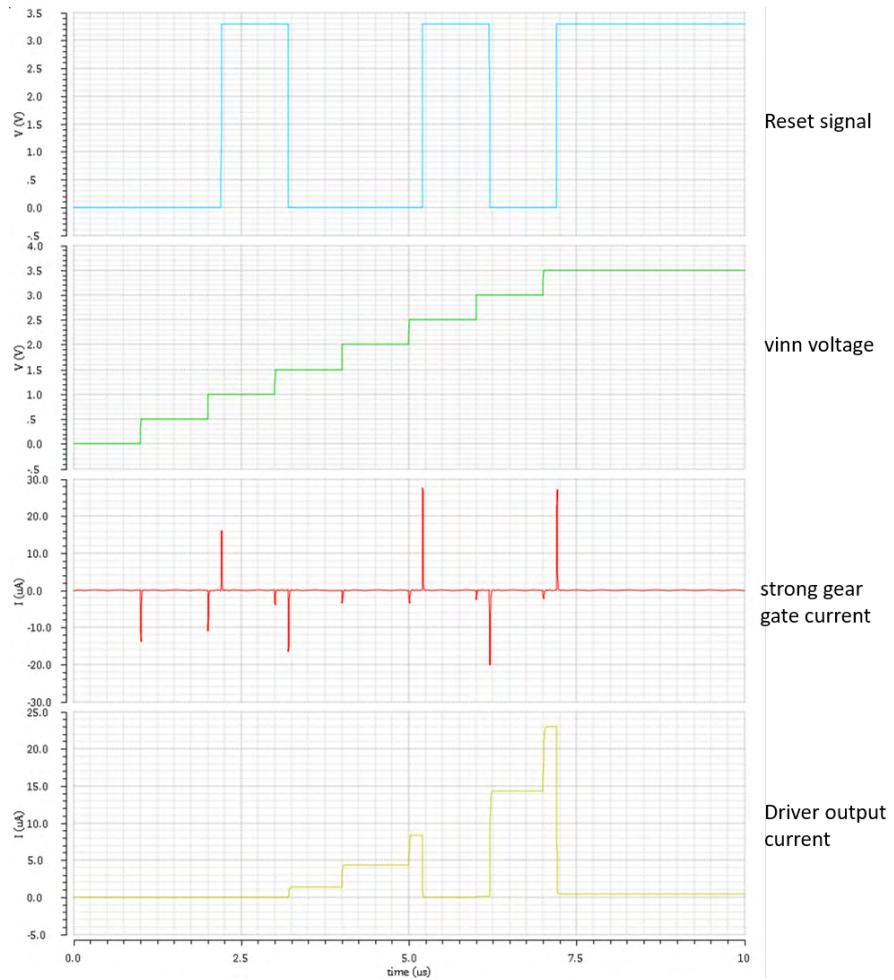
**Figure A.4:** Varying the Length of the transistor creates a longer channel on the transistors. As a result the electrons have to travel a longer distance to reach the other side. This increases the impedance of the device decreasing the amount of current that can flow.



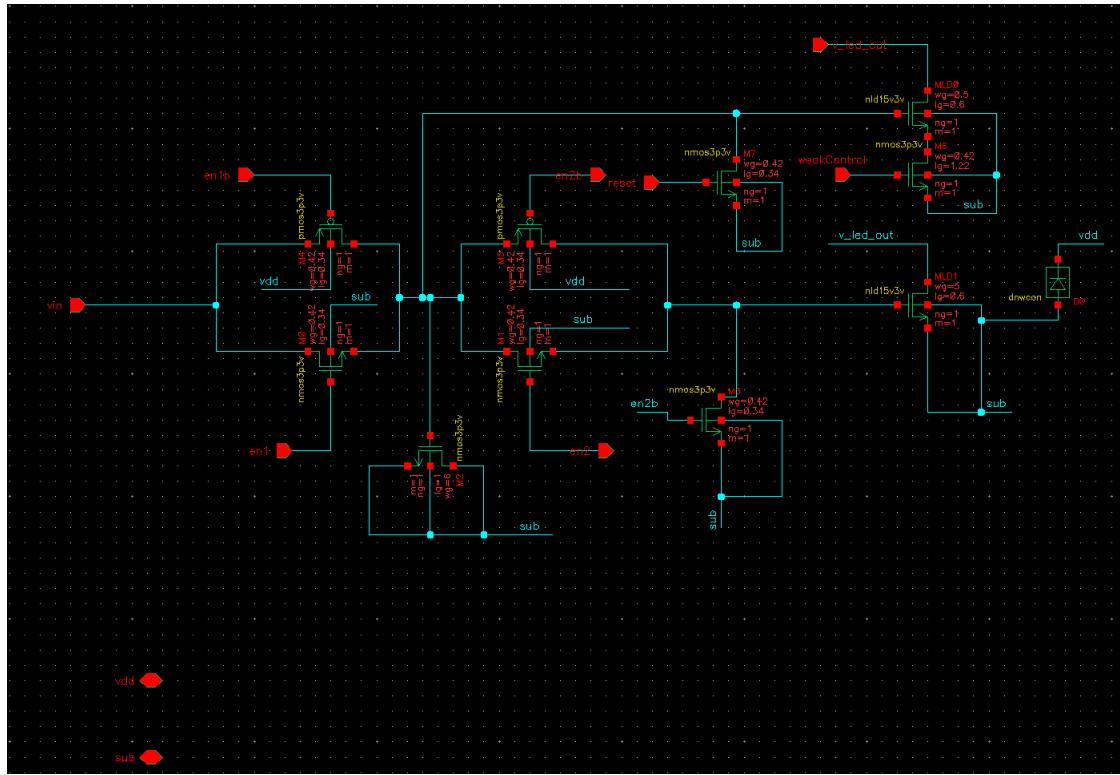
**Figure A.5:** Varying the voltage at the gate ( $V_g$ ) of the MOS transistors puts it in different modes of operation. In the linear region the MOS acts as a resistor and the value of equivalent resistance changes depending on the value of  $V_g$



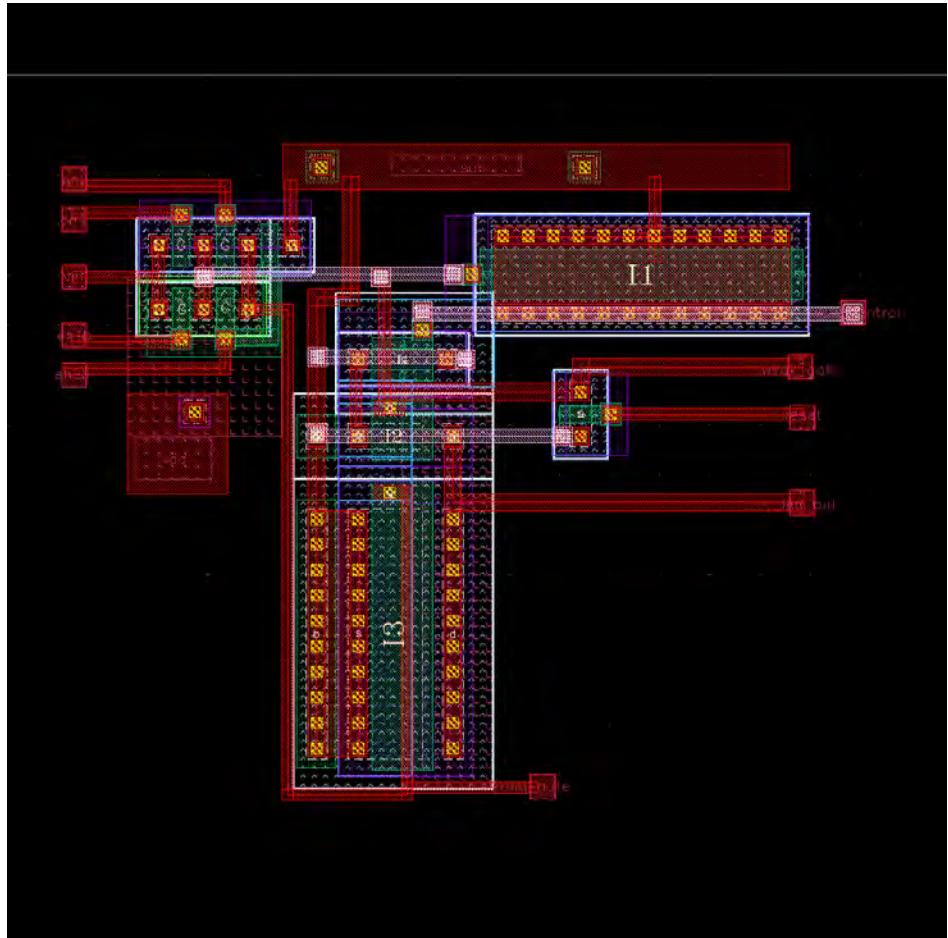
**Figure A.6:** Varying the length of the PMOS transistor yields very high apparent resistance but the threshold voltage for the path increases significantly. For this reason further investigations into using a PMOS device as a resistor were dropped



**Figure A.7:** Simulation that shows the effect of the reset line on the drive circuit



**Figure A.8:** Improved driver circuit with a reset line and a cascaded weak gear

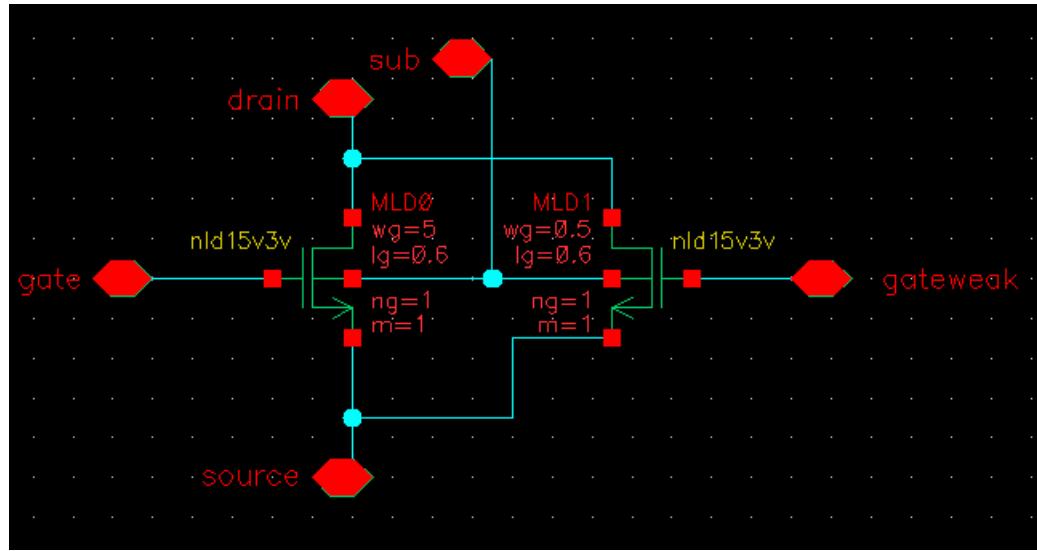


**Figure A.9:** Improved driver circuit layout for the ART-IDEA pixel

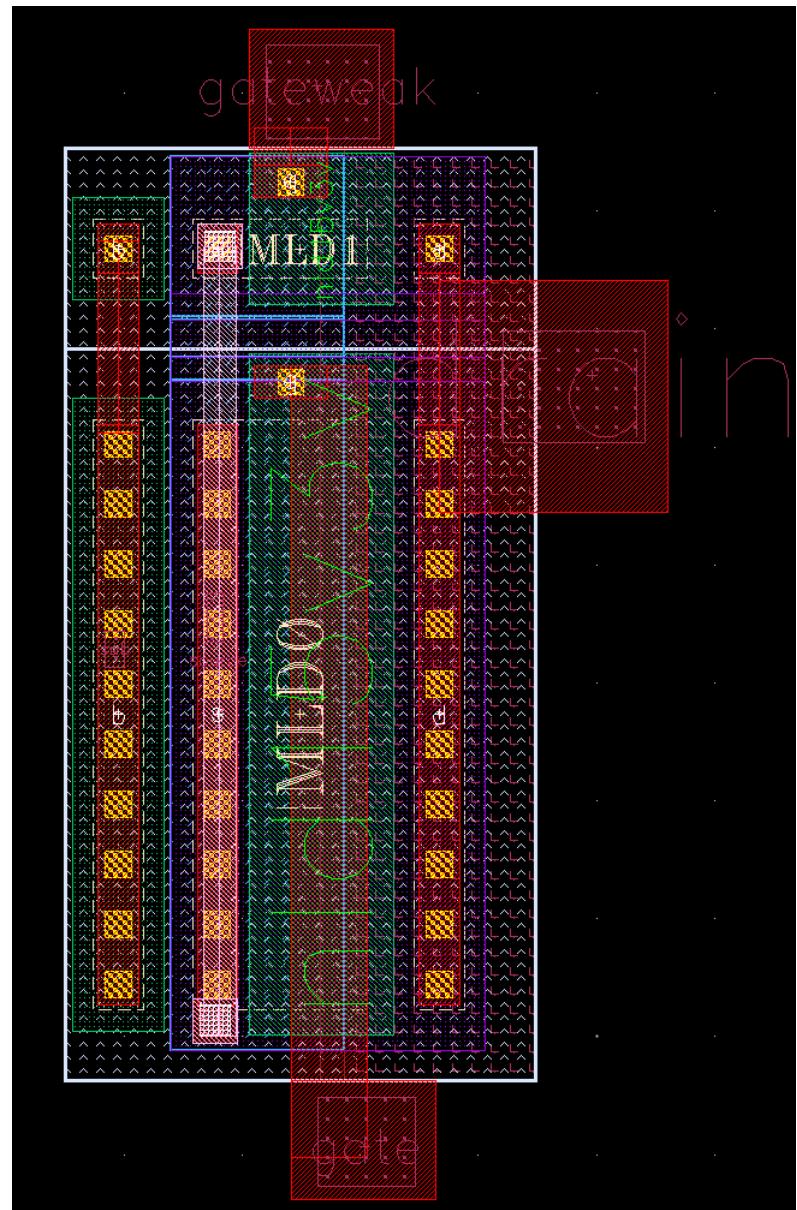
## Appendix B

### FINAL TEST CHIP LAYOUT CIRCUITS

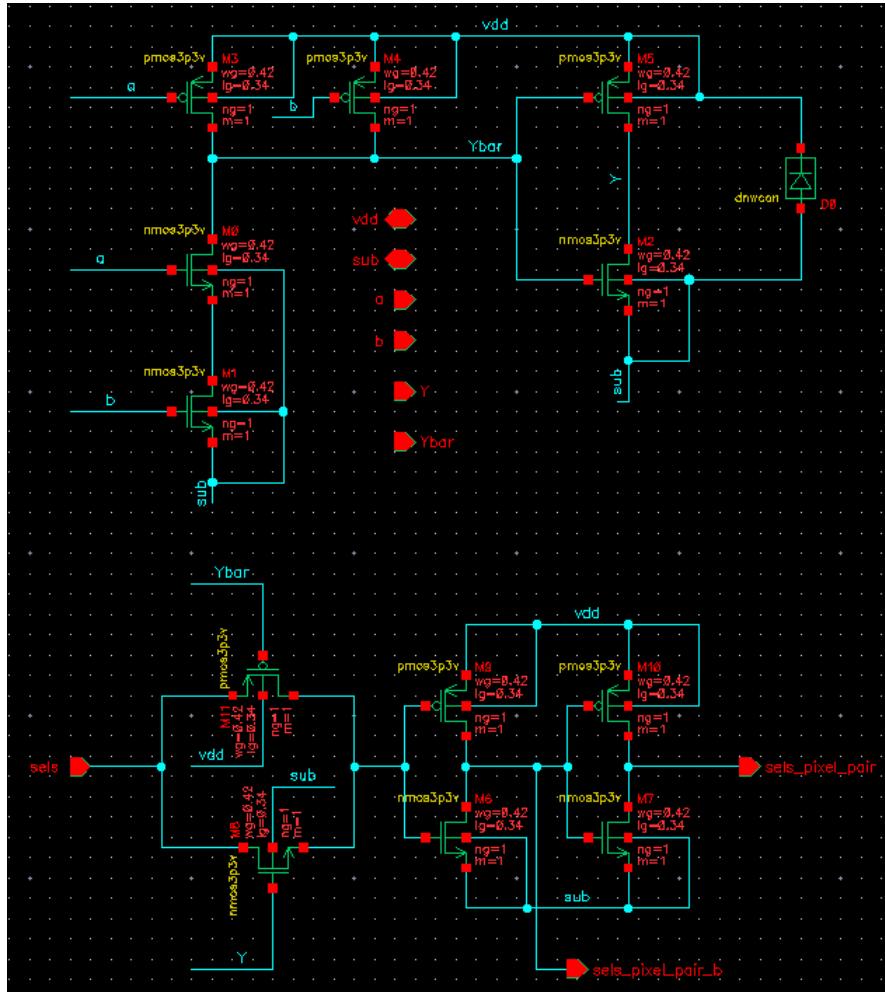
The information here is supporting material for section 5.7. These are all of the different circuits that were fabricated on the first ART-IDEA prototype chip.



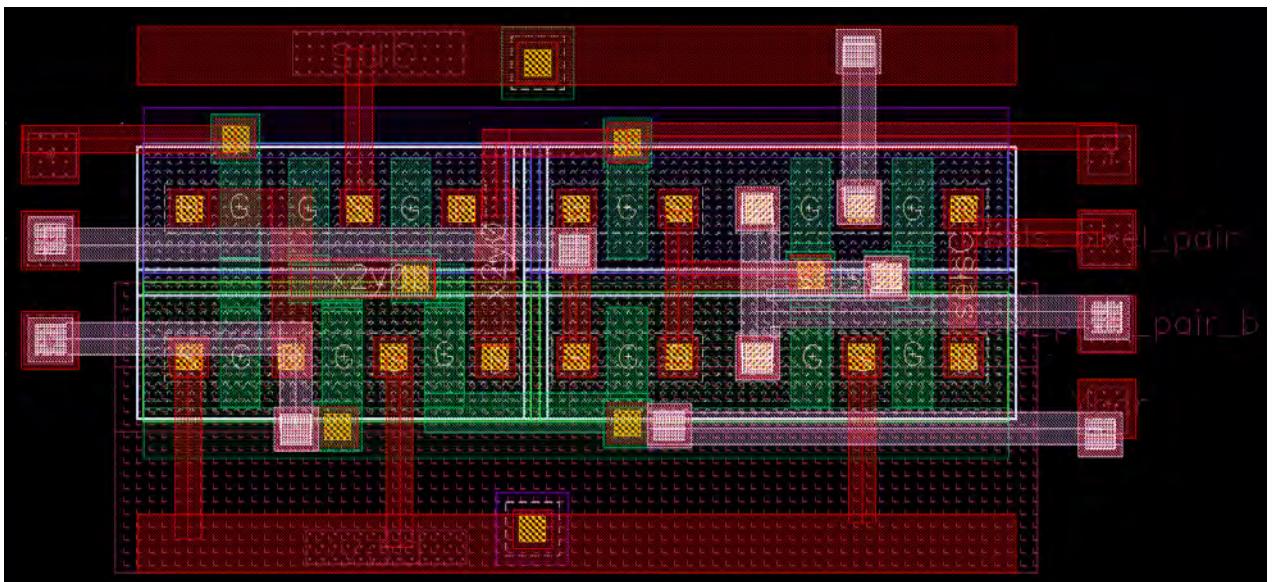
**Figure B.1:** NLD MOS Drive transistors circuit with the same size as they would have in the 4x4 super-pixel



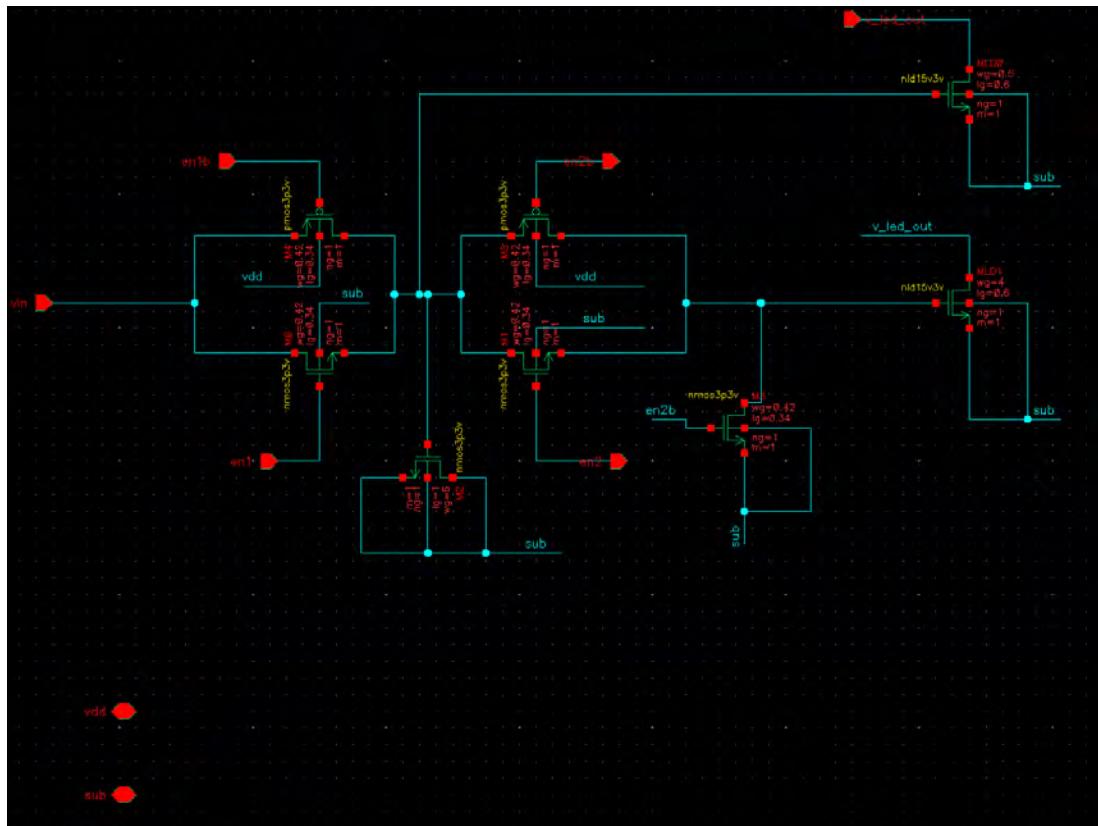
**Figure B.2:** NLD MOS Drive transistors Layout. Top portion is the weak gear and bottom portion is the strong gear



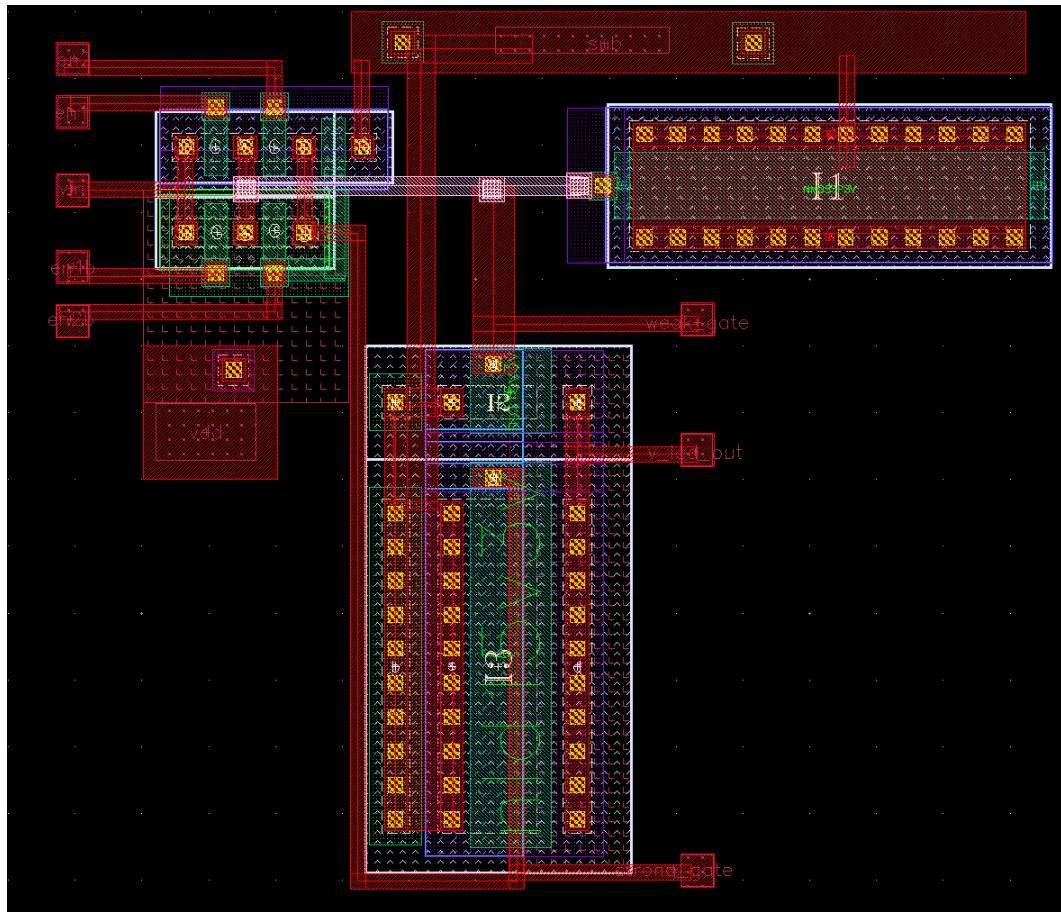
**Figure B.3:** Address Decoder circuit and gear selector are combined into one block on the test chip



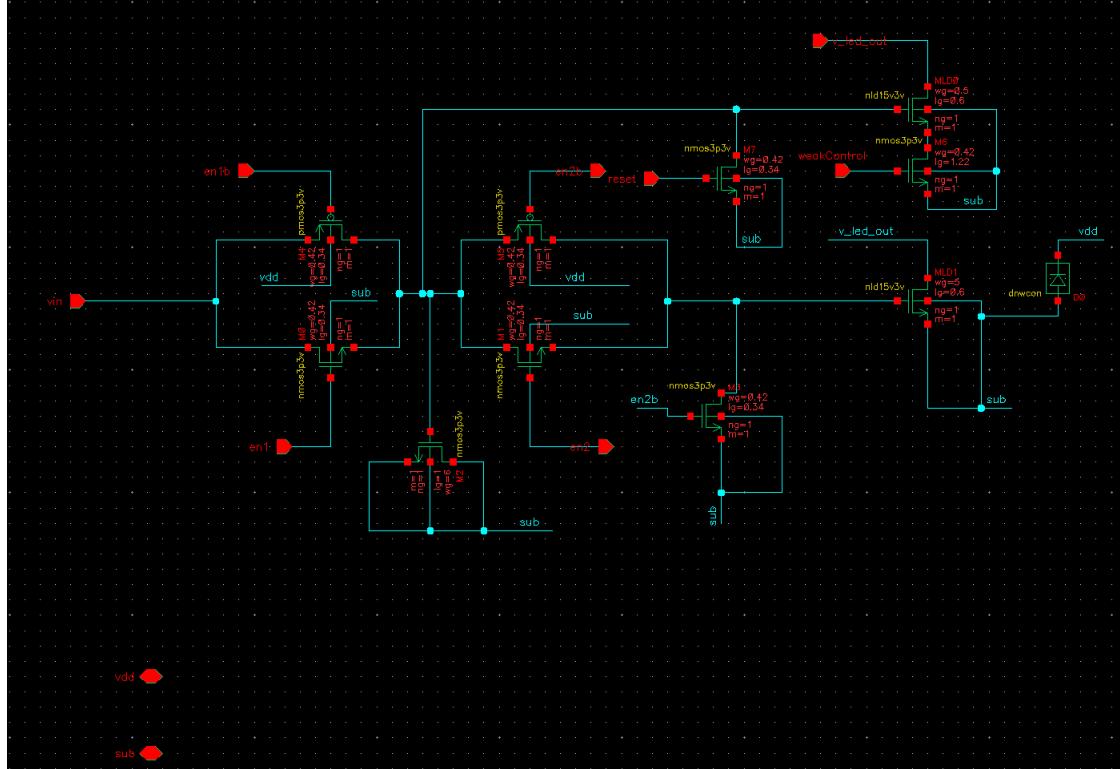
**Figure B.4:** Layout block for the address decoder and gear selector circuit



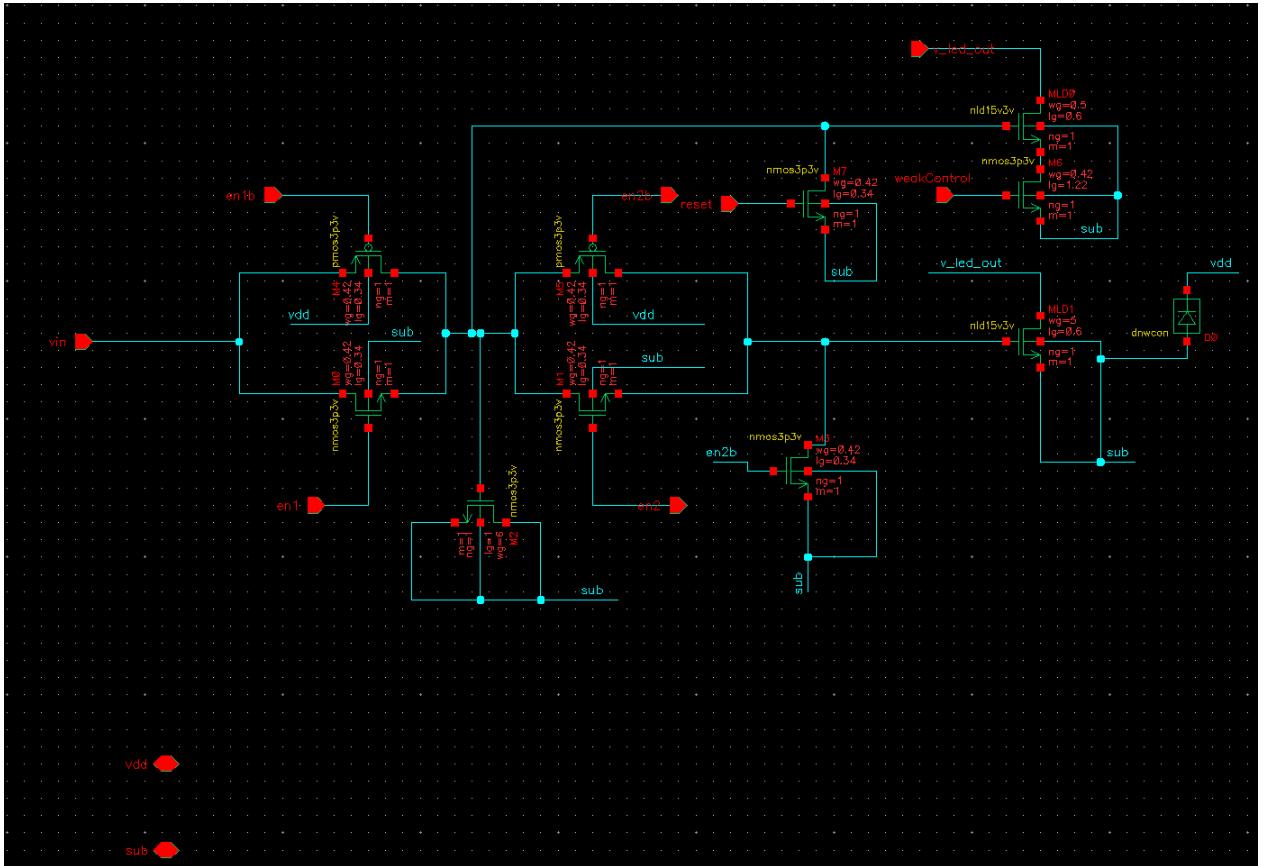
**Figure B.5:** Circuit schematic for the LED driver. This version has been used on previous RIICs



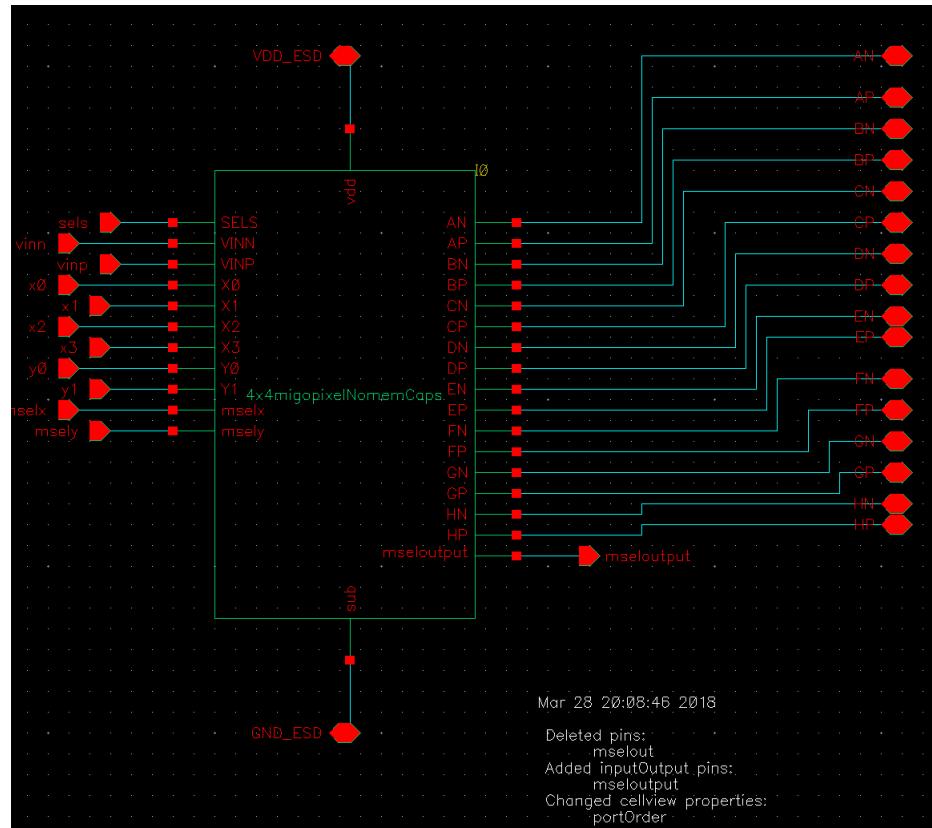
**Figure B.6:** Layout for the driver circuit shown on figure B.5



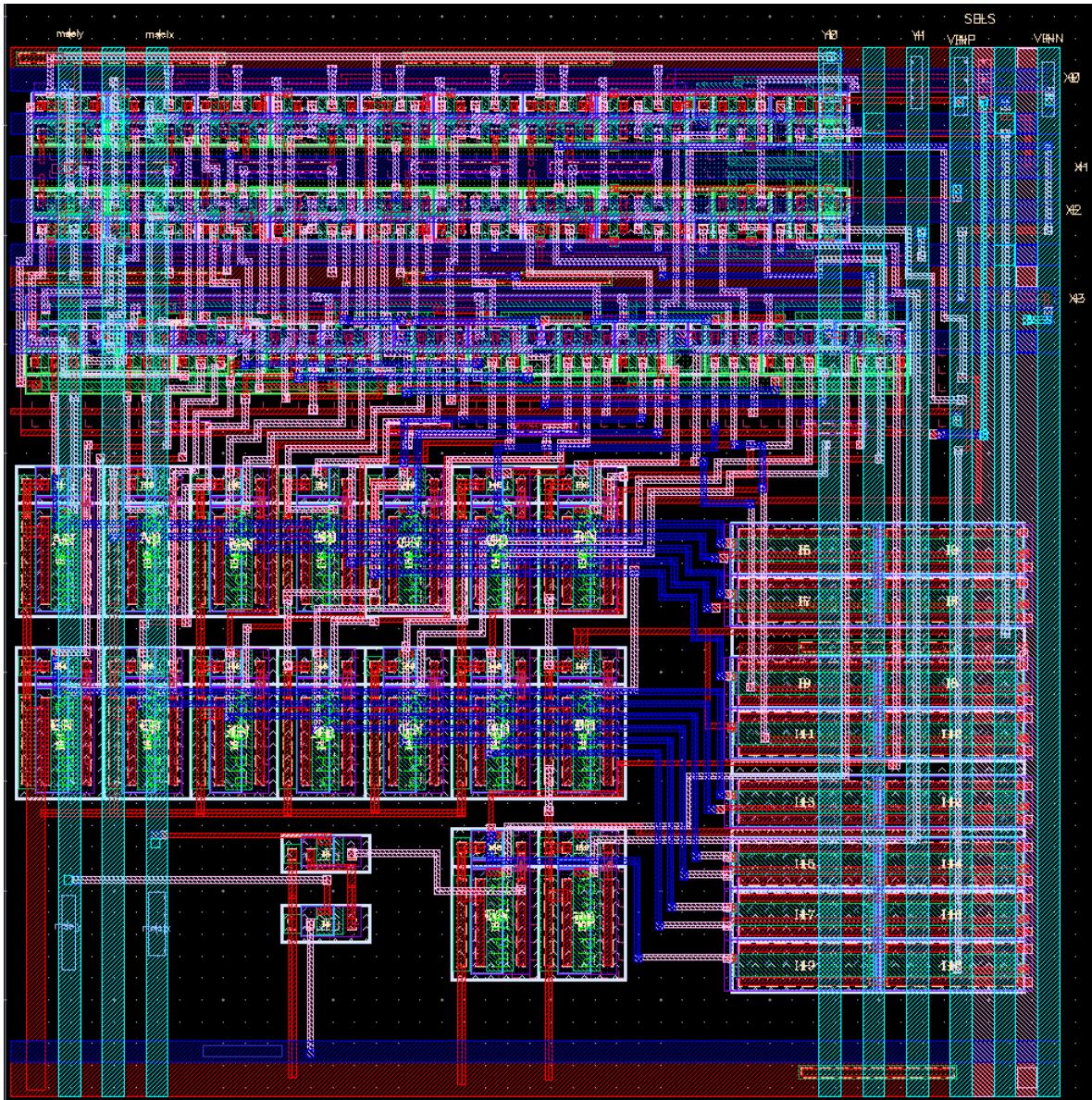
**Figure B.7:** Circuit Schematic for the enhanced driver circuit. This circuit was derived after many simulations. It contains a pixel level reset line, and a properly sized cascoded weak gear. If it proves to be effective after testing it will be implemented to the main design and replace the current drive circuit



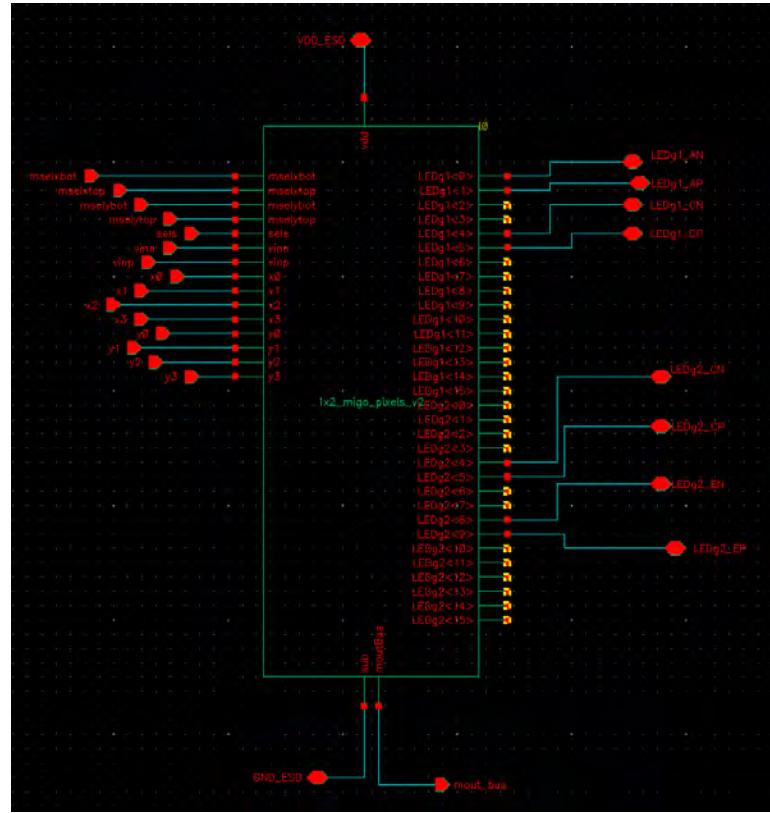
**Figure B.8:** This is the layout that corresponds to the driver schematic with a reset line and cascoded weak gear shown in figure ??



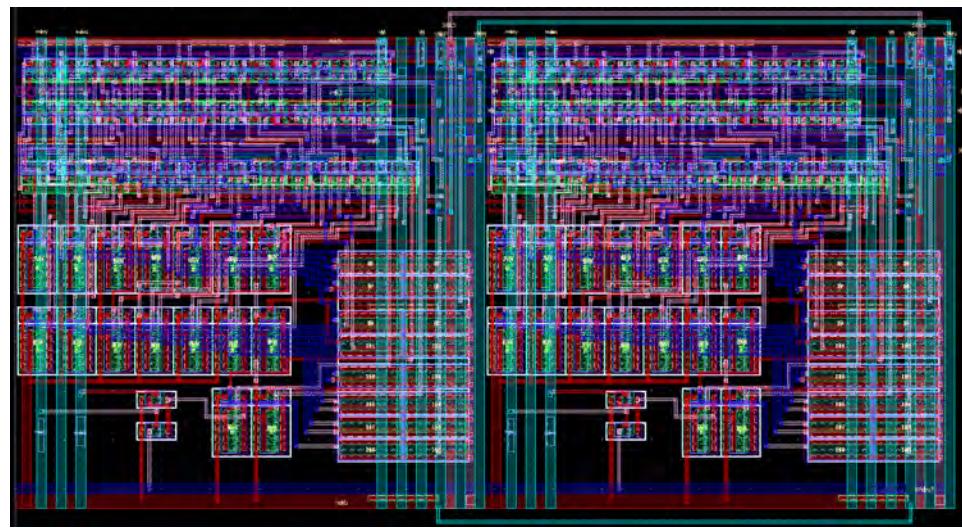
**Figure B.9:** This is the top cell schematic for the 4x4 RIIC super-pixel. Inputs are on the left side, and all 16 LED outputs plus the telemetry pin are on the right side



**Figure B.10:** Layout for the 4x4 RIIC super-pixel that was submitted for fabrication after passing DRC, LVS and post PEX simulation tests



**Figure B.11:** Top cell for a 2x1 ART-IDEA super-pixels, a total of 32 pixel can be driven with this design

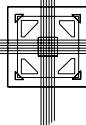
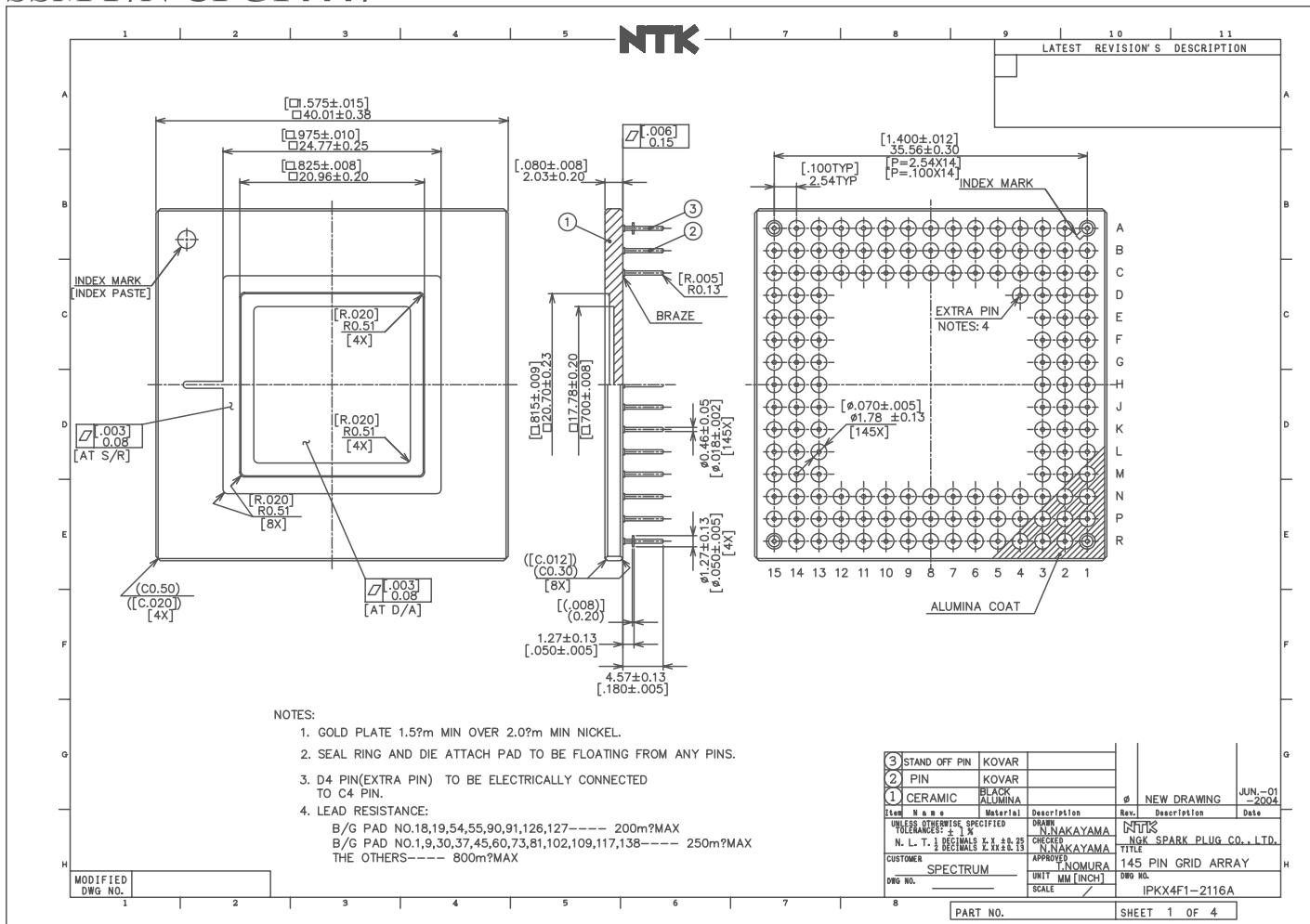


**Figure B.12:** Layout of two tiled ART-IDEA super-pixels. This was done to prove that the design is easily scalable

**Appendix C**

**RIIC SUPER PIXEL PACKAGING**

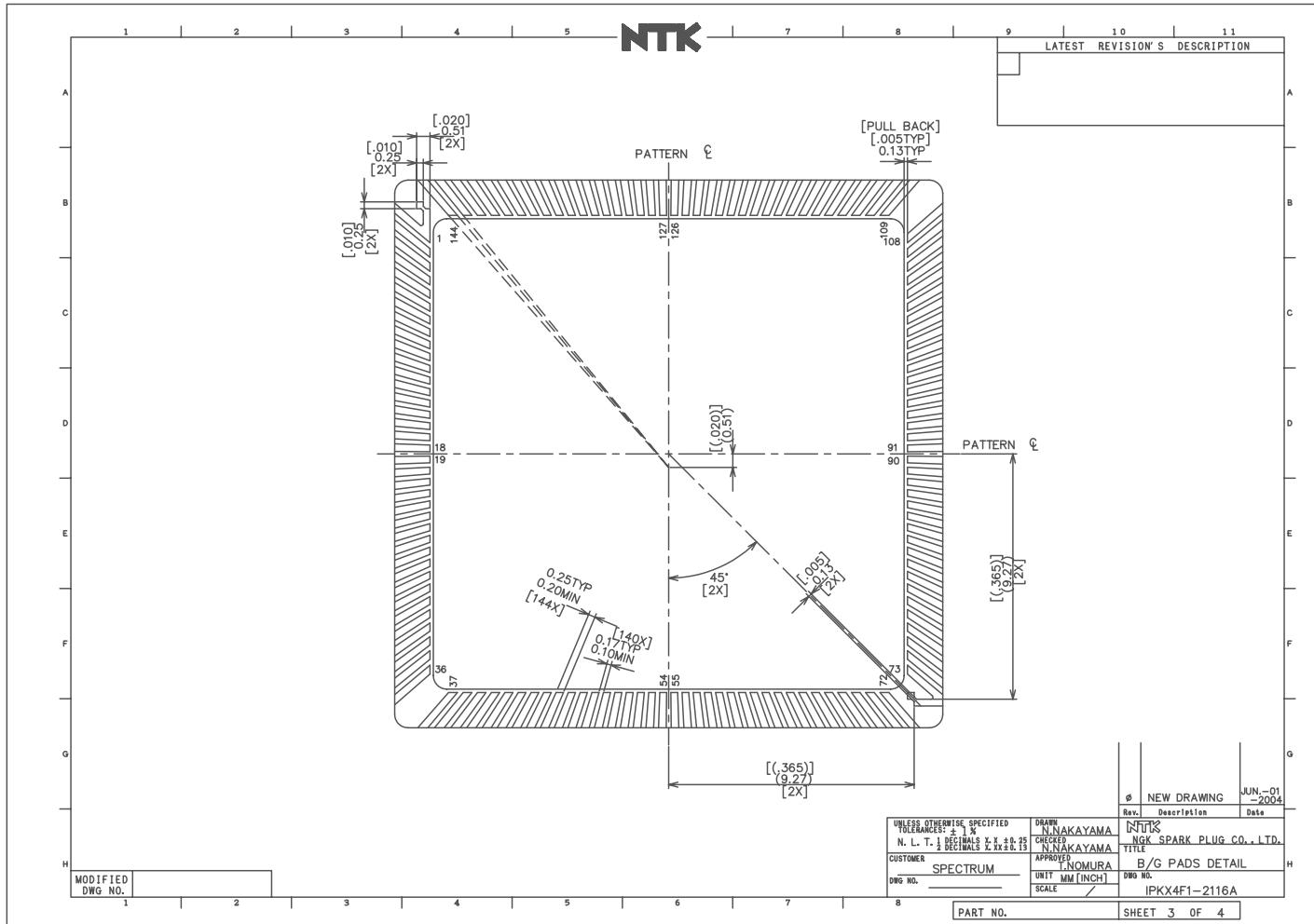
# SSM P/N CPG14447



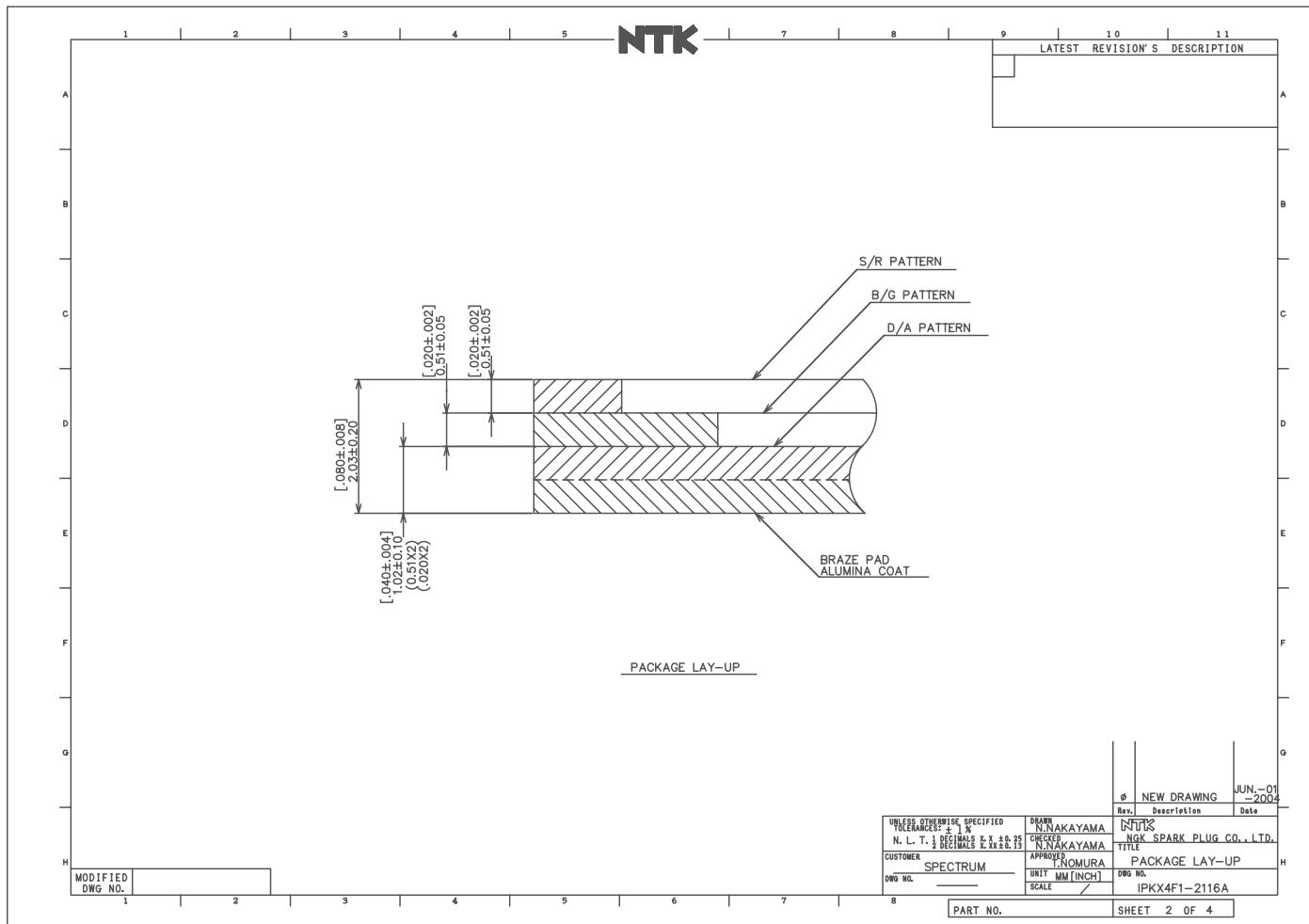
**SPECTRUM**  
SEMICONDUCTOR MATERIALS, INC.

www.spectrum-semi.com Phone: 408-435-5555 Fax: 408-435-8226

# SSM P/N CPG14447



# SSM P/N CPG14447



www.spectrum-semi.com Phone: 408-435-5555 Fax: 408-435-8226

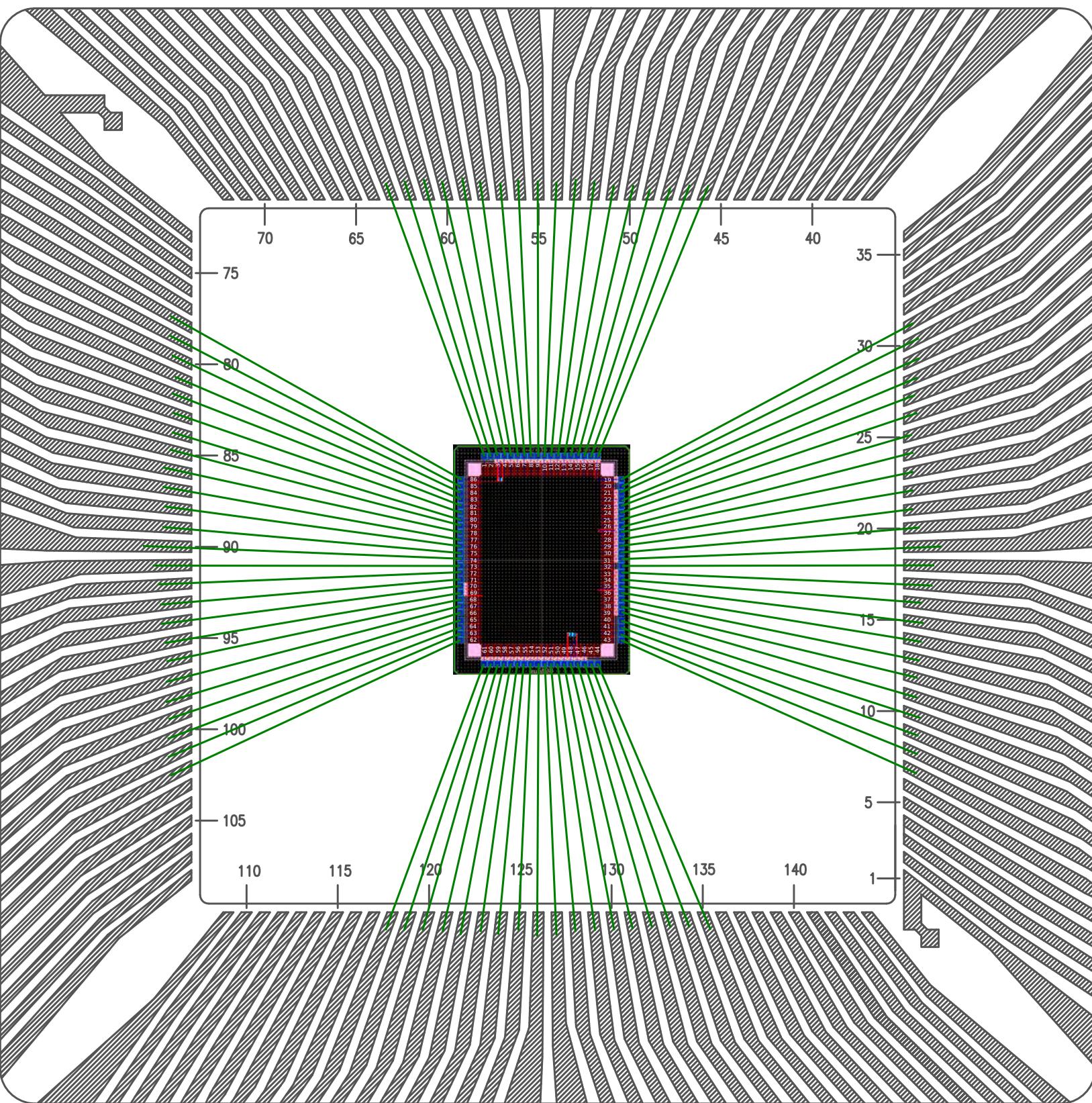
# SSM P/N CPG14447

1	2	3	4	5	NTK	7	8	9	10	11					
					LATEST	REVISION'S	DESCRIPTION								
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H
CONNECTION TABLE															
W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	S/R	N/C		
1	D3	27	M1	53	R8	79	L14	105	D13	131	B6	EXTRA PIN(D4)	C4		
2	C2	28	N1	54	N8	80	M15	106	C13	132	C6				
3	B1	29	M2	55	N9	81	K13	107	B14	133	A5				
4	D2	30	L3	56	R9	82	K14	108	A15	134	B5				
5	E3	31	N2	57	R10	83	L15	109	C12	135	A4				
6	C1	32	P1	58	P9	84	J14	110	B13	136	A3				
7	E2	33	M3	59	P10	85	J13	111	A14	137	B4				
8	D1	34	N3	60	N10	86	K15	112	B12	138	C5				
9	F3	35	P2	61	R11	87	J15	113	C11	139	B3				
10	F2	36	R1	62	P11	88	H14	114	A13	140	A2				
11	E1	37	N4	63	R12	89	H15	115	B11	141	C4				
12	G2	38	P3	64	R13	90	H13	116	A12	142	C3				
13	G3	39	R2	65	P12	91	G13	117	C10	143	B2				
14	F1	40	P4	66	N11	92	G15	118	B10	144	A1				
15	G1	41	N5	67	P13	93	F15	119	A11						
16	H2	42	R3	68	R14	94	G14	120	B9						
17	H1	43	P5	69	N12	95	F14	121	C9						
18	H3	44	R4	70	N13	96	F13	122	A10						
19	J3	45	N6	71	P14	97	E15	123	A9						
20	J1	46	P6	72	R15	98	E14	124	B8						
21	K1	47	R5	73	M13	99	D15	125	A8						
22	J2	48	P7	74	N14	100	C15	126	C8						
23	K2	49	N7	75	P15	101	D14	127	C7						
24	K3	50	R6	76	M14	102	E13	128	A7						
25	L1	51	R7	77	L13	103	C14	129	A6						
26	L2	52	P8	78	N15	104	B15	130	B7						
MODIFIED DWG NO. <input type="text"/> PART NO. <input type="text"/> SHEET 4 OF 4															
1 2 3 4 5 6 7 8															

UNLESS OTHERWISE SPECIFIED  
TOLERANCES:  $\pm 0.05$   
N. L. T. 1 DEGREE X, Y, Z & 0.25 DEGREES X, Y, Z & 0.15  
DRAWN BY N.NAKAYAMA APPROVED N.NOMURA  
N.GK SPARK PLUG CO., LTD. TITLE CONNECTION TABLE  
CUSTOMER SPECTRUM DWG NO. IPKX4F1-2116A  
DWG NO. UNIT MM (INCH)  
SCALE /



www.spectrum-semi.com Phone: 408-435-5555 Fax: 408-435-8226



chipCircuit	Signal Name	type	pin Count	pad number	PGA pin
4x4 super-pixel	GND_ESD	power gnd	1	T0	63
4x4 super-pixel	VDD_ESD	power vdd(3.3V)	2	T1	62
4x4 super-pixel	sels	signal input	3	T2	61
4x4 super-pixel	vinn	signal input	4	T3	60
4x4 super-pixel	vinp	signal input	5	T4	59
4x4 super-pixel	x0	signal input	6	T5	58
4x4 super-pixel	x1	signal input	7	T6	57
4x4 super-pixel	x2	signal input	8	T7	56
4x4 super-pixel	x3	signal input	9	T8	55
4x4 super-pixel	y0	signal input	10	T9	54
4x4 super-pixel	y1	signal input	11	T10	53
4x4 super-pixel	mselx	signal input	12	T11	52
4x4 super-pixel	msely	signal input	13	T12	51
4x4 super-pixel	mseloutput	signal output	14	T13	50
Driver Circuit	en1b	signal input	15	T14	49
Driver Circuit	en1	signal input	16	T15	48
Driver Circuit	en2b	signal input	17	T16	47
Driver Circuit	en2	signal input	18	T17	46
Driver Circuit	vin	signal input	19	R0	31
Driver Circuit	led_out	signal output (LED)	20	R1	30
Driver Circuit	weak_gate	signal input	21	R2	29
Driver Circuit	strong_gate	signal input	22	R3	28
Driver Circuit with Weak control	en1b	signal input	23	R4	27
Driver Circuit with Weak control	en1	signal input	24	R5	26
Driver Circuit with Weak control	en2b	signal input	25	R6	25
Driver Circuit with Weak control	en2	signal input	26	R7	24
Driver Circuit with Weak control	reset	signal input	27	R8	23
Driver Circuit with Weak control	vin	signal input	28	R9	22
Driver Circuit with Weak control	weakControl	signal input	29	R10	21
Driver Circuit with Weak control	strong_gate	signal input	30	R11	20
Driver Circuit with Weak control	weak_gate	signal input	31	R12	19
Driver Circuit with Weak control	led_out	signal output(LED)	32	R13	18
adress decoder	a	signal input	33	R14	17
adress decoder	b	signal input	34	R15	16
adress decoder	sels	signal input	35	R16	15
adress decoder	Y	signal input	36	R17	14
adress decoder	Ybar	signal input	37	R18	13
adress decoder	sels_px_pair	signal input	38	R19	12
adress decoder	sels_px_pairb	signal input	39	R20	11
tiled super-pixel	LEDg_CP	power	40	R21	10
tiled super-pixel	LEDg1_CN	power	41	R22	9
tiled super-pixel	LEDg1_AP	power	42	R23	8
tiled super-pixel	LEDg1_AN	power	43	R24	7

tiled super-pixel	GND_ESD	power	44	B0	135
tiled super-pixel	VDD_ESD	power(only bottom)	45	B1	134
tiled super-pixel	sels	signal input	46	B2	133
tiled super-pixel	vinn	signal input	47	B3	132
tiled super-pixel	vinp	signal input	48	B4	131
tiled super-pixel	x0	signal input	49	B5	130
tiled super-pixel	x1	signal input	50	B6	129
tiled super-pixel	x2	signal input	51	B7	128
tiled super-pixel	x3	signal input	52	B8	127
tiled super-pixel	y0	signal input	53	B9	126
tiled super-pixel	y1	signal input	54	B10	125
tiled super-pixel	y2	signal input	55	B11	124
tiled super-pixel	y3	signal input	56	B12	123
tiled super-pixel	mselxtop	signal input	57	B13	122
tiled super-pixel	mselytop	signal input	58	B14	121
tiled super-pixel	mselxbot	signal input	59	B15	120
tiled super-pixel	mselybot	signal input	60	B16	119
tiled super-pixel	mout_bus	output	61	B17	118
tiled super-pixel	LEDg2_EN	signal input	62	L0	102
tiled super-pixel	LEDg2_EP	signal input	63	L1	101
tiled super-pixel	LEDg2_CN	signal input	64	L2	100
tiled super-pixel	LEDg2_CP	signal input	65	L3	99
null	null	null	66	L4	98
drive transistors	drain	power/output	67	L5	97
drive transistors	source	power	68	L6	96
drive transistors	strong_gate	signal_input	69	L7	95
drive transistors	weak_gate	signal input	70	L8	94
4x4 super-pixel	HP	power/output	71	L9	93
4x4 super-pixel	HN	power/output	72	L10	92
4x4 super-pixel	GP	power/output	73	L11	91
4x4 super-pixel	GN	power/output	74	L12	90
4x4 super-pixel	FP	power/output	75	L13	89
4x4 super-pixel	FN	power/output	76	L14	88
4x4 super-pixel	EP	power/output	77	L15	87
4x4 super-pixel	EN	power/output	78	L16	86
4x4 super-pixel	DP	power/output	79	L17	85
4x4 super-pixel	DN	power/output	80	L18	84
4x4 super-pixel	CP	power/output	81	L19	83
4x4 super-pixel	CN	power/output	82	L20	82
4x4 super-pixel	BP	power/output	83	L21	81
4x4 super-pixel	BN	power/output	84	L22	80
4x4 super-pixel	AP	power/output	85	L23	79
4x4 super-pixel	AN	power/output	86	L24	78

## Appendix D

### PARTITIONED SVSM - 84-PIN LCC SOCKET

The following lists correspond to all of the SLED devices that were brought out to the pins of an 84-pin LCC package. The lists are divided by quadrant number on the SLED wafer.

DIODevice SLEDSwitchV2-Q1 — SLEDSwitchV2-Q2 —SLEDSwitchV2-Q3 —  
SLEDSwitchV2-Q4

# Quadrant 1:

# Pitch = inf um, lane width = 0.0 um, effective pixel width = inf um

Line 74, 206x206um	206 x 206	81	81	81	40, 81
Line 75, 056x056um	056 x 056	81	81	81	44, 81
Line 76, 030x030um	030 x 030	81	81	81	48, 81
Line 77, 106x106um	106 x 106	81	81	81	52, 81
Line 78, 206x206um	206 x 206	81	81	81	56, 81
Line 79, 106x106um	106 x 106	81	81	81	60, 81
Line 80, 056x056um	056 x 056	81	81	81	64, 81
Line 81, 038x038um	038 x 038	81	81	81	68, 81
Line 82, 030x030um	030 x 030	81	81	81	72, 81
Line 83, 038x038um	038 x 038	81	81	81	76, 81
Cathode 84	x	81	81	81	80
Line 01, 030x030um	030 x 030	00, 81	81	81	81
Line 02, 038x038um	038 x 038	04, 81	81	81	81
Line 03, 106x106um	106 x 106	08, 81	81	81	81
Line 04, 038x038um	038 x 038	12, 81	81	81	81
Line 05, 206x206um	206 x 206	16, 81	81	81	81
Line 06, 056x056um	056 x 056	20, 81	81	81	81
Line 07, 030x030um	030 x 030	24, 81	81	81	81
Line 08, 106x106um	106 x 106	28, 81	81	81	81
Line 09, 206x206um	206 x 206	32, 81	81	81	81
Line 10, 406x406um	406 x 406	36, 81	81	81	81

=====

# Quadrant 2:

# Pitch = 12.0 um, lane width = 3.0 um, effective pixel width = 7.0 um

Line 11, 112x112um	112 x 112	40, 81	81	81	81
Line 12, 021x021um	021 x 021	44, 81	81	81	81
Line 13, 007x007um	007 x 007	48, 81	81	81	81
Line 14, 049x049um	049 x 049	52, 81	81	81	81
Line 15, 112x112um	112 x 112	56, 81	81	81	81
Line 16, 049x049um	049 x 049	60, 81	81	81	81
Line 17, 021x021um	021 x 021	64, 81	81	81	81
Line 18, 014x014um	014 x 014	68, 81	81	81	81
Line 19, 007x007um	007 x 007	72, 81	81	81	81
Line 20, 014x014um	014 x 014	76, 81	81	81	81
Cathode 21	x	80	81	81	81
Line 22, 007x007um	007 x 007	81	00, 81	81	81
Line 23, 014x014um	014 x 014	81	04, 81	81	81
Line 24, 049x049um	049 x 049	81	08, 81	81	81
Line 25, 014x014um	014 x 014	81	12, 81	81	81
Line 26, 112x112um	112 x 112	81	16, 81	81	81
Line 27, 021x021um	021 x 021	81	20, 81	81	81
Line 28, 007x007um	007 x 007	81	24, 81	81	81
Line 29, 049x049um	049 x 049	81	28, 81	81	81
Line 30, 112x112um	112 x 112	81	32, 81	81	81
Line 31, 224x224um	224 x 224	81	36, 81	81	81

---

# Quadrant 3:

# Pitch = 18.0 um, lane width = 4.5 um, effective pixel width = 11.5 um

Line 32, 115x115um	115 x 115	81	40, 81	81	81
Line 33, 023x023um	023 x 023	81	44, 81	81	81
Line 34, 011x011um	011 x 011	81	48, 81	81	81
Line 35, 057x057um	057 x 057	81	52, 81	81	81
Line 36, 115x115um	115 x 115	81	56, 81	81	81
Line 37, 057x057um	057 x 057	81	60, 81	81	81
Line 38, 023x023um	023 x 023	81	64, 81	81	81
Line 39, 011x011um	011 x 011	81	68, 81	81	81
Line 40, 011x011um	011 x 011	81	72, 81	81	81
Line 41, 011x011um	011 x 011	81	76, 81	81	81
Cathode 42	x	81	80	81	81
Line 43, 011x011um	011 x 011	81	81	00, 81	81
Line 44, 011x011um	011 x 011	81	81	04, 81	81
Line 45, 057x057um	057 x 057	81	81	08, 81	81
Line 46, 011x011um	011 x 011	81	81	12, 81	81
Line 47, 115x115um	115 x 115	81	81	16, 81	81
Line 48, 023x023um	023 x 023	81	81	20, 81	81
Line 49, 011x011um	011 x 011	81	81	24, 81	81
Line 50, 057x057um	057 x 057	81	81	28, 81	81
Line 51, 115x115um	115 x 115	81	81	32, 81	81
Line 52, 241x241um	241 x 241	81	81	36, 81	81

=====

# Quadrant 4:

# Pitch = 24.0 um, lane width = 6.0 um, effective pixel width = 16.0 um

Line 53, 128x128um	128 x 128	81	81	40, 81	81
Line 54, 032x032um	032 x 032	81	81	44, 81	81
Line 55, 016x016um	016 x 016	81	81	48, 81	81
Line 56, 064x064um	064 x 064	81	81	52, 81	81
Line 57, 128x128um	128 x 128	81	81	56, 81	81
Line 58, 064x064um	064 x 064	81	81	60, 81	81
Line 59, 032x032um	032 x 032	81	81	64, 81	81
Line 60, 016x016um	016 x 016	81	81	68, 81	81
Line 61, 016x016um	016 x 016	81	81	72, 81	81
Line 62, 016x016um	016 x 016	81	81	76, 81	81
Cathode 63	x	81	81	80	81
Line 64, 016x016um	016 x 016	81	81	81	00, 81
Line 65, 016x016um	016 x 016	81	81	81	04, 81
Line 66, 064x064um	064 x 064	81	81	81	08, 81
Line 67, 016x016um	016 x 016	81	81	81	12, 81
Line 68, 128x128um	128 x 128	81	81	81	16, 81
Line 69, 032x032um	032 x 032	81	81	81	20, 81
Line 70, 016x016um	016 x 016	81	81	81	24, 81
Line 71, 064x064um	064 x 064	81	81	81	28, 81
Line 72, 128x128um	128 x 128	81	81	81	32, 81
Line 73, 256x256um	256 x 256	81	81	81	36, 81

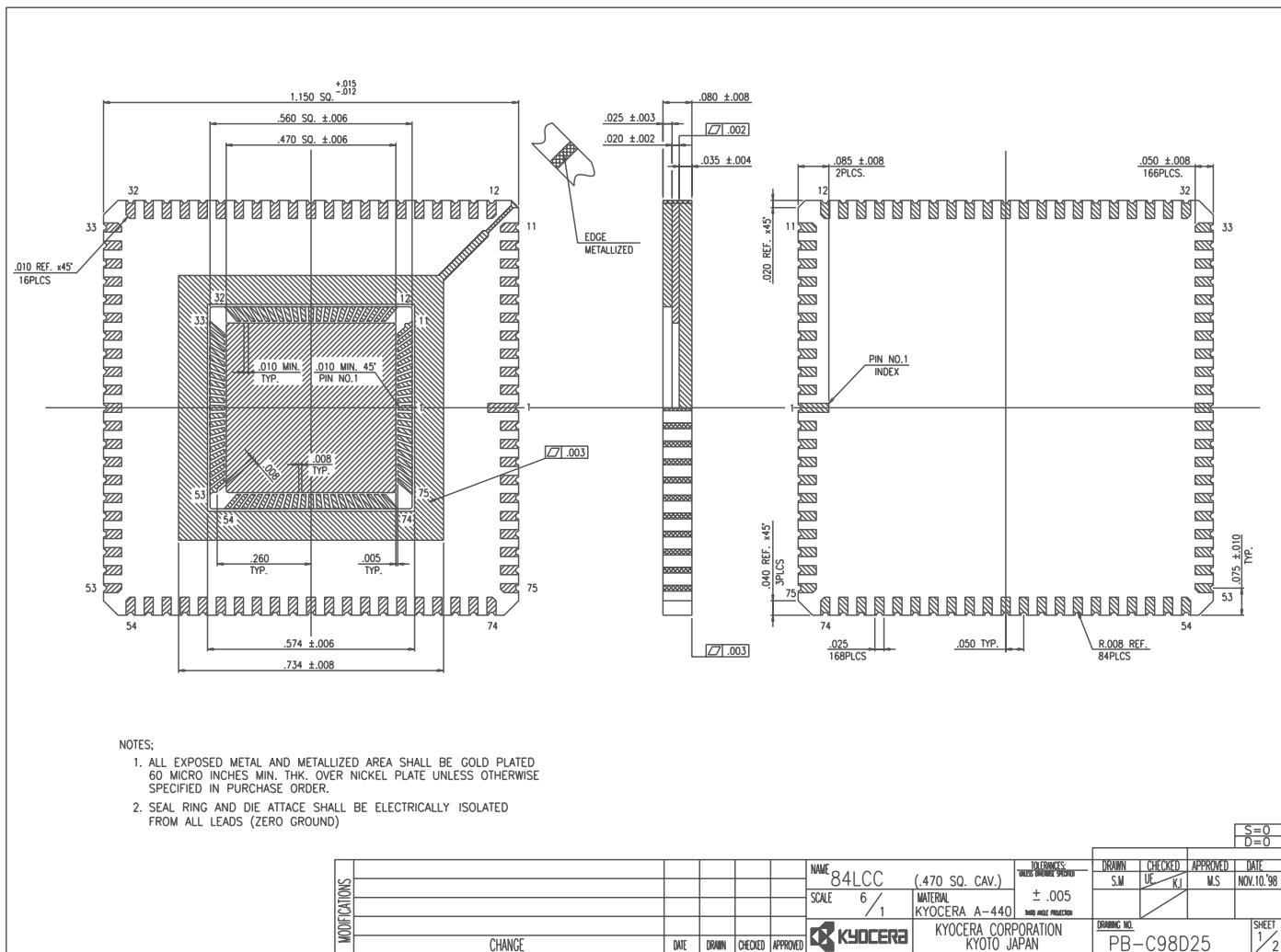
# Continuity and cathode checks

Open — — — — —

Open with cathodes — — 81 — 81 — 81 — 81

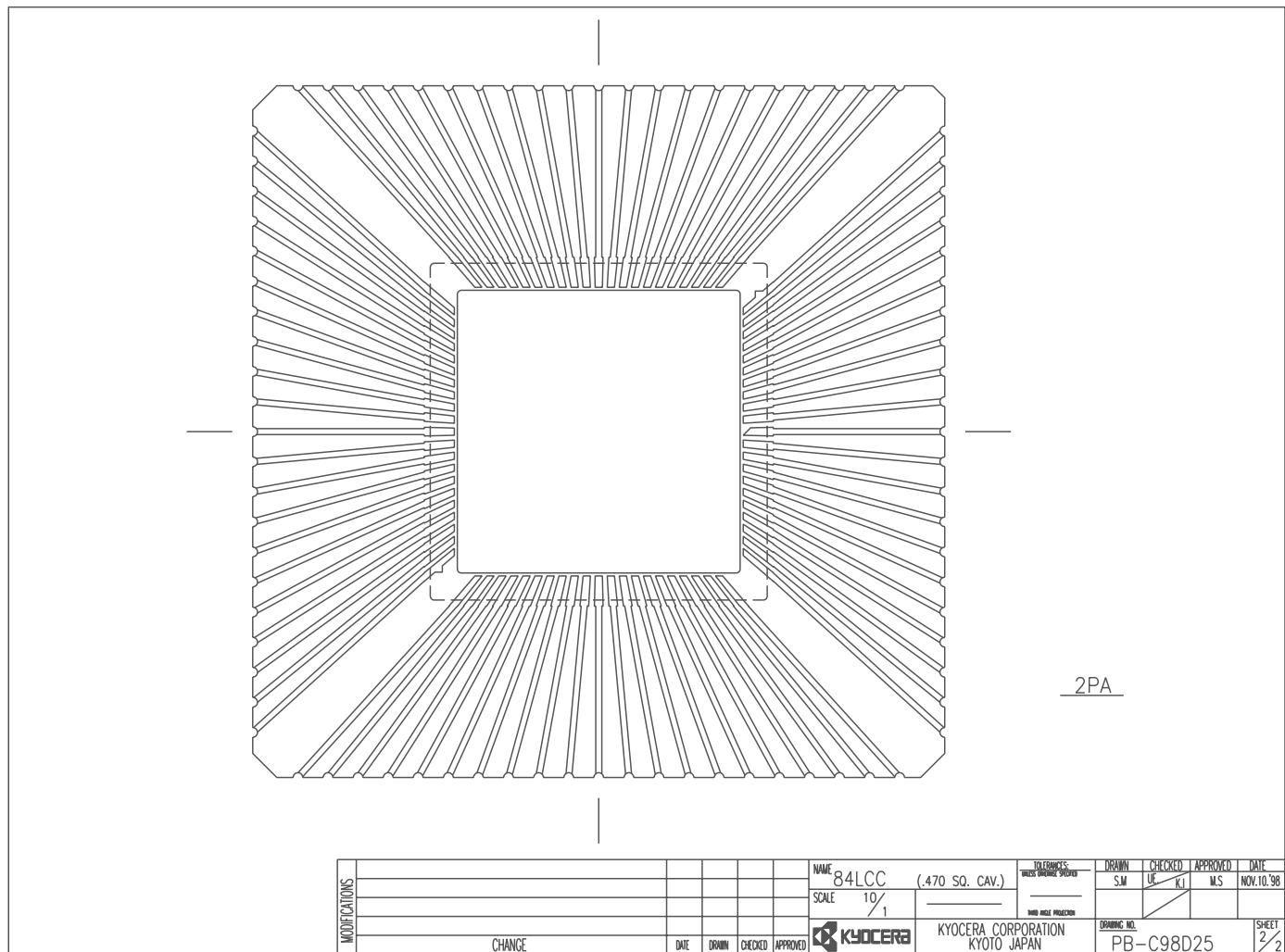
Cathode 42 short — — — 80, 81 — —

## SSM P/N LCC08422

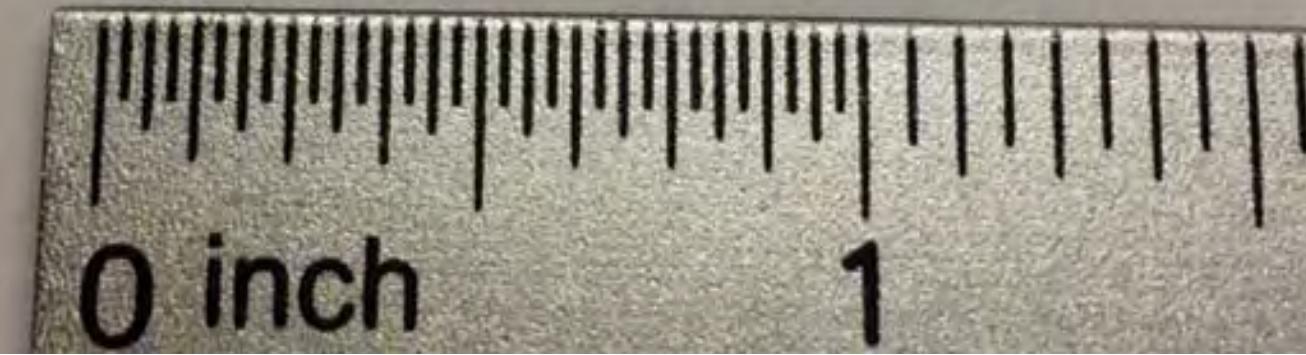
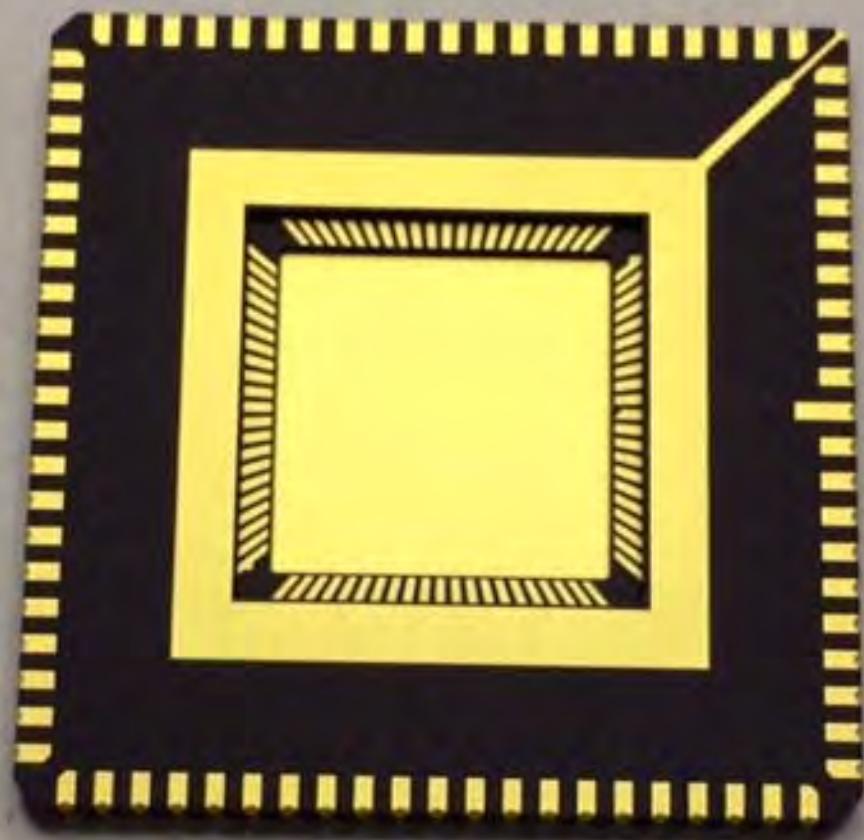


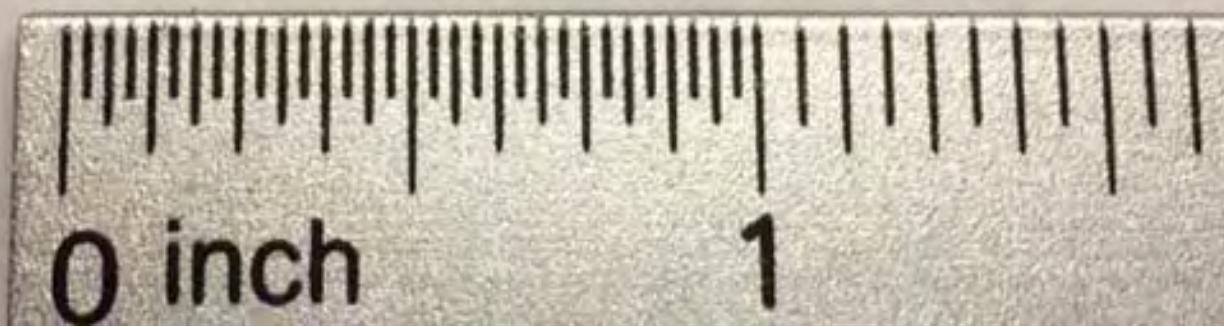
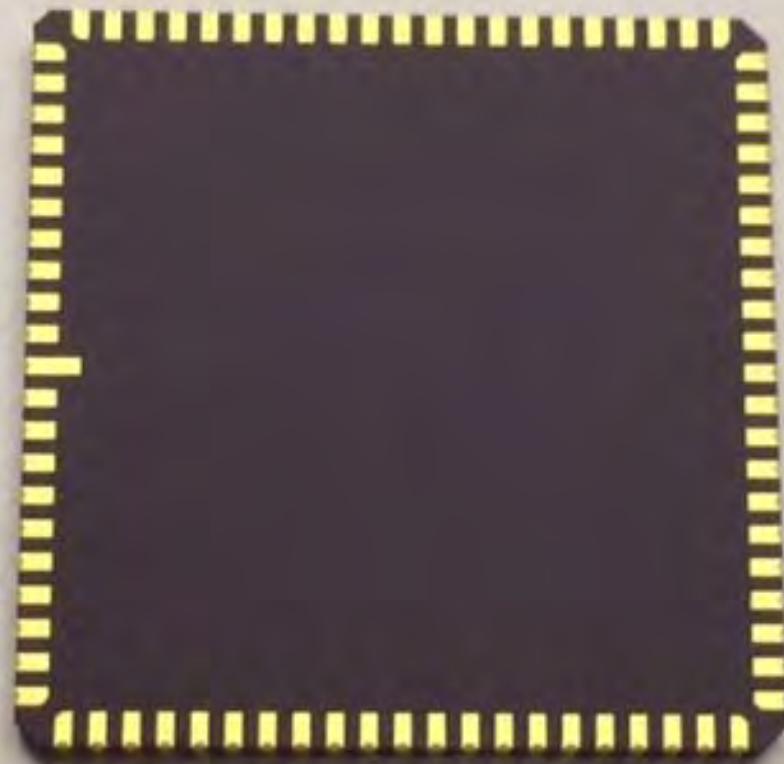
www.spectrum-semi.com Phone: 408-435-5555 Fax: 408-435-8226

SSM P/N LCC08422



www.spectrum-semi.com Phone: 408-435-5555 Fax: 408-435-8226





## Appendix E

### AUXILARY TEST RESULTS

The following appendix contains data collected from testing the RIIC test chip and the SLED test chips relevant to the work presented. The first section has data regarding the RIIC test chip, the second section has data on the SLED test chips, and the third section has data collected while both components worked together.

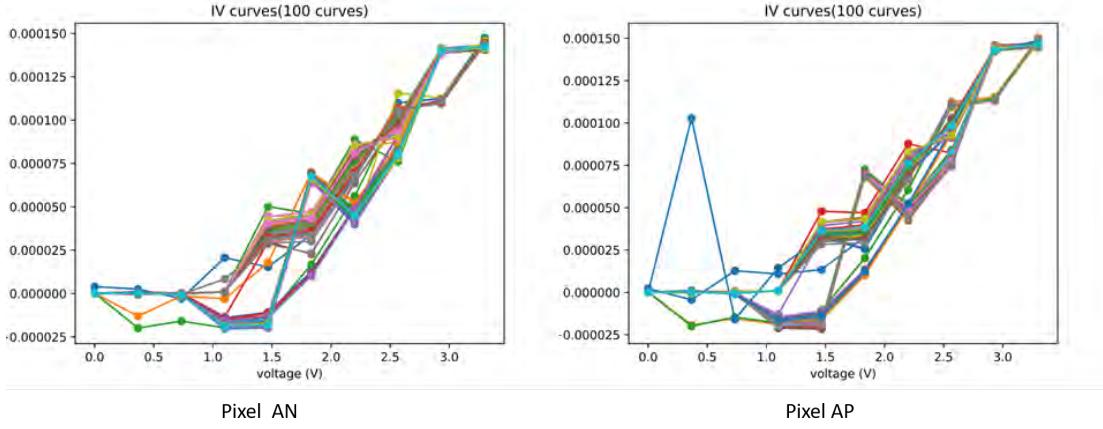
#### E.1 RIIC Test Chip Auxilary Results

The ART-IDEA RIIC super-pixel has two analog inputs that control the current output of the drive transistors. These lines are **vinn** and **vinp**. Additionally, each pixel has two gears, strong and weak, and are selectable via a digital input-signal **sels**. The inner pixels within the super-pixel are addressed in pairs by the **x** and **y** addresses. For example, pixel AN and AP are addressed at the same time but get their analog input value from either **vinn** or **vinp** respectively.

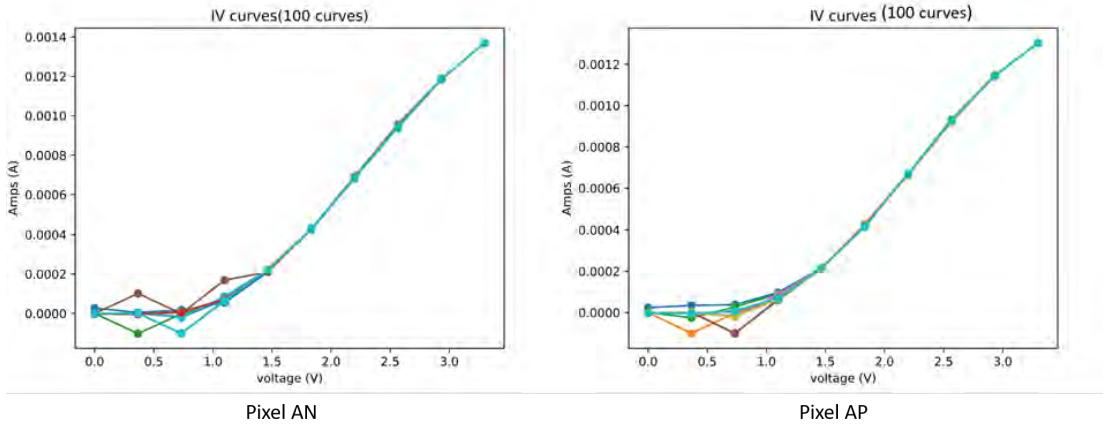
In the RIIC super-pixel there are a total of 16 pixels. There is a total of 8 pairs denoted with a letter from A-H, and for those groups either N or P depending on the analog line used to drive them. The following plots [E.8](#) through [E.12](#) are sets of 10 curves each for each of the pixel pairs to compare the current output of all the pixels in strong mode.

#### E.2 SLED Auxilary Test Results

This section has more test results for the SLED test chips broken down by chip number. SLED test chips that have the prefix AIG739 have a stage active region thickness of 133nm. SLED chips with prefix IAG740 have a stage active region thickness of 266nm. Additionally, if the second part of the prefix has the letter A, it means it uses

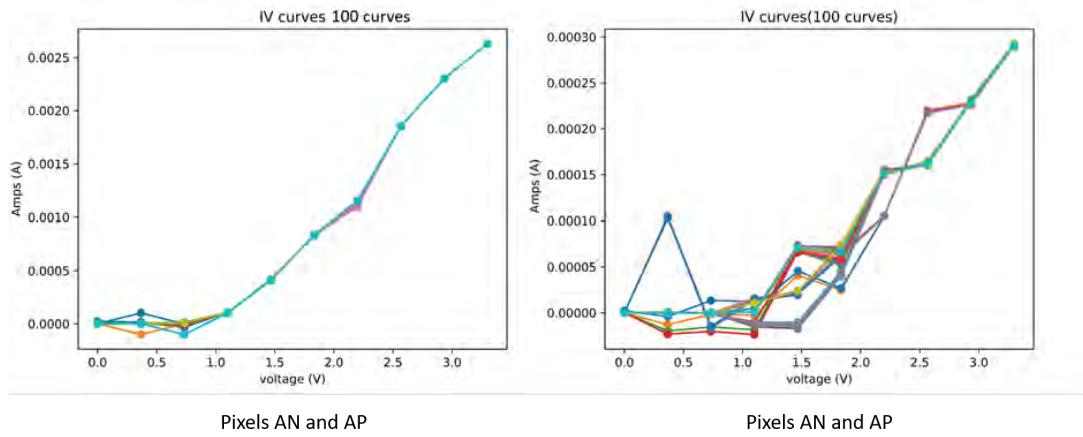


**Figure E.1:** Left: IV curves for pixel AN swept 100 times. Right: IV curves for pixel AP swept 100 times. This test prove the addressing scheme worked, as well as the analog inputs **vinn** and **vinp** can control the weak gear current output. The LED power source was set to 5V and the load used was a macro LED. Note: All 100 AN curves were collected first with AP off. Then with AN off, the 100 curves on AP were collected.

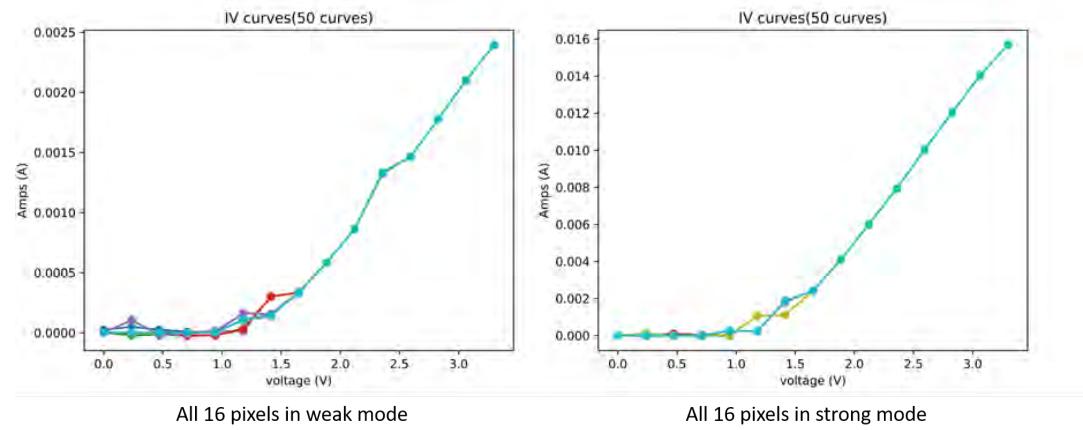


**Figure E.2:** Left: IV curves for pixel AN swept 100 times. Right: IV curves for pixel AP swept 100 times. This is the same test as figure E.1 but using the strong gear on the driver

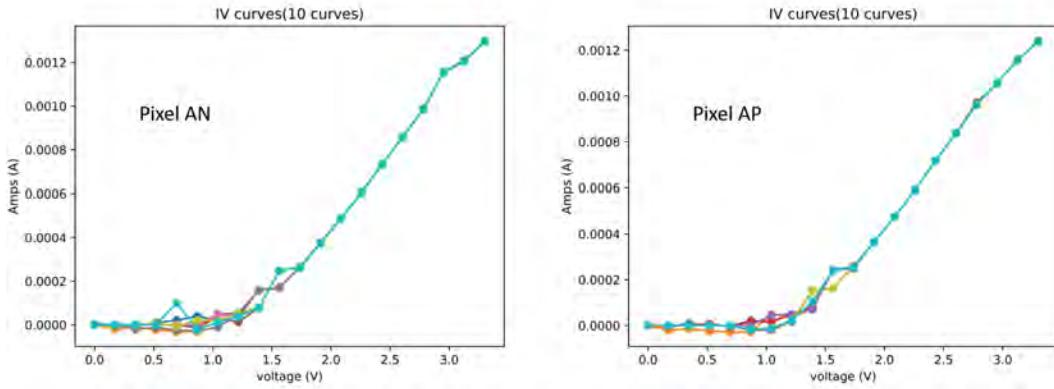
Ti/Pt/Au for the metal contacts. The chip prefixes that have a B used an experimental contact made of Pd/Ge/Au. Figures E.13 through E.17 are some of the relevant data collected during testing.



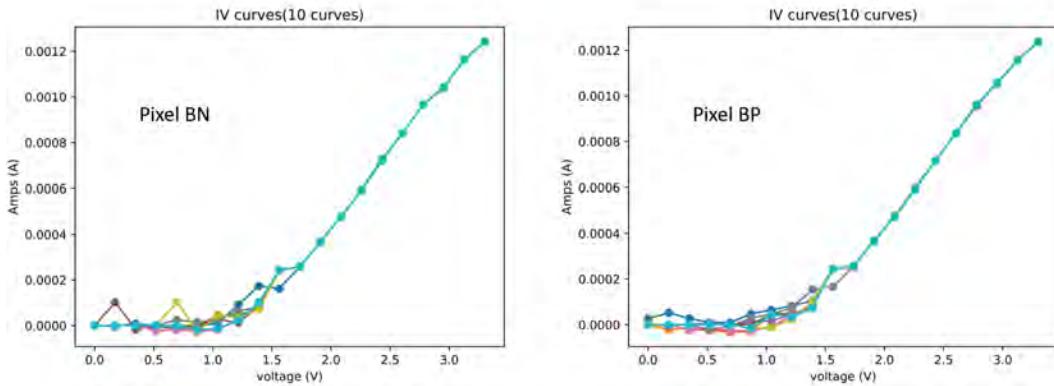
**Figure E.3:** Left: IV curves for pixel AN and AP in strong mode. Right: AN and AP IV curves in weak mode. For this test, the LED power source was set to 5V and the load were the macro LED attached to AN and AP outputs on the test chip. In this test, both AN and AP were swept simultaneously and as expected the current increased by a factor of 2X



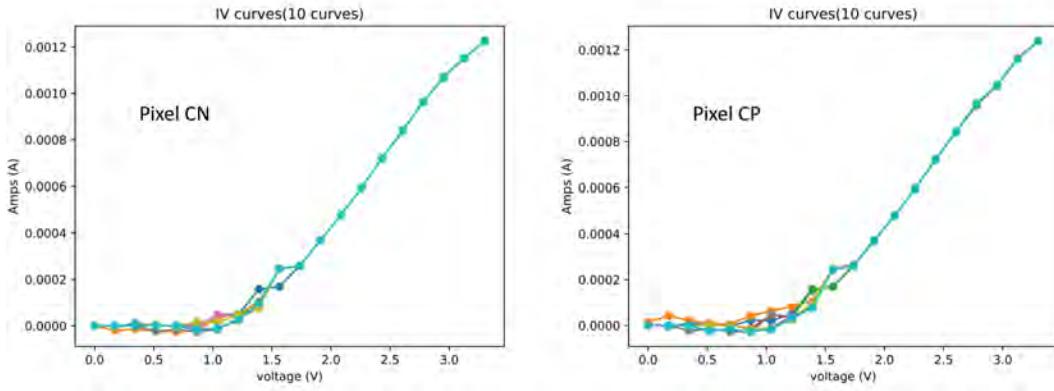
**Figure E.4:** Left: IV curves for all 16 pixels in weak mode. Right: IV curves for all 16 pixels in strong mode. LED power source set to 5V, and as a load 16 macro LEDs attached to each of the pixels in the super-pixel. All pixels were swept at the same time, thus this shows the max current used by the entire super-pixel for both gears



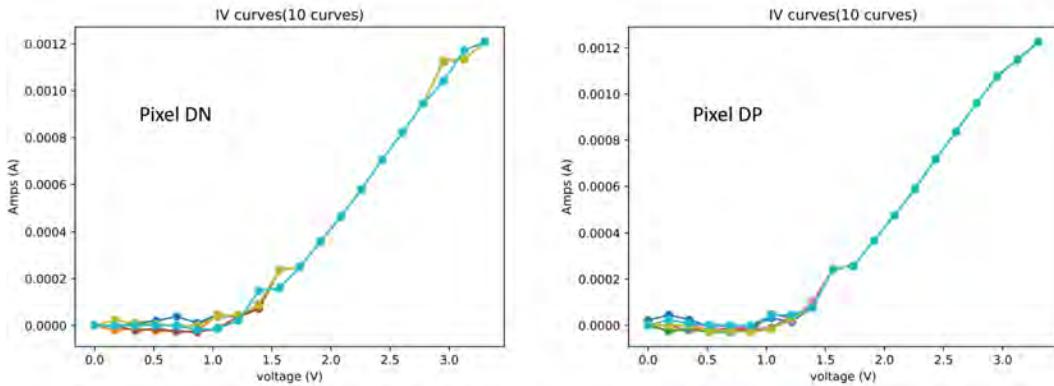
**Figure E.5:** IV curves comparing the performance of pixels AN and AP. Relative location within the super-pixel, AN is pixel (0,0) and AP is pixel (0,1).



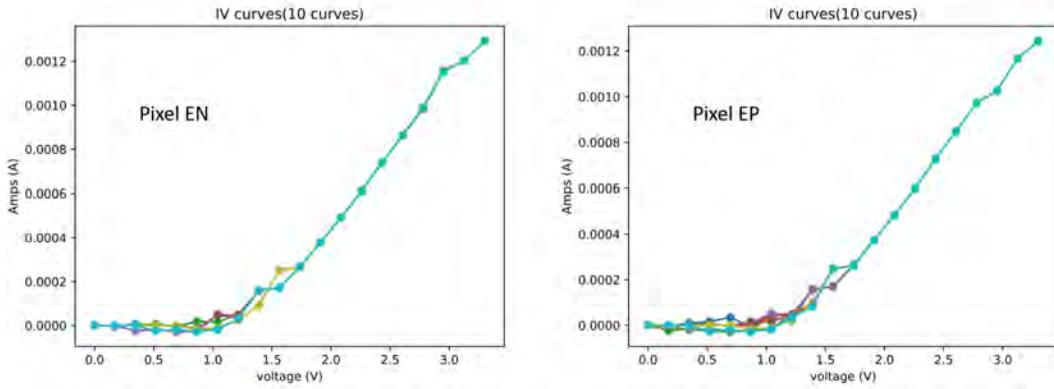
**Figure E.6:** IV curves comparing the performance of pixels BN and BP. Relative location within the super-pixel, BN is pixel (1,0) and AP is pixel (1,1).



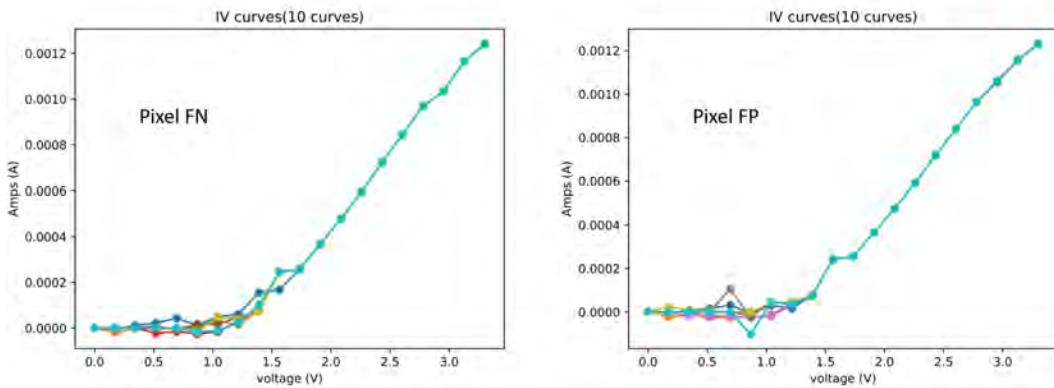
**Figure E.7:** IV curves comparing the performance of pixels CN and CP. Relative location within the super-pixel, CN is pixel (2,0) and CP is pixel (2,1).



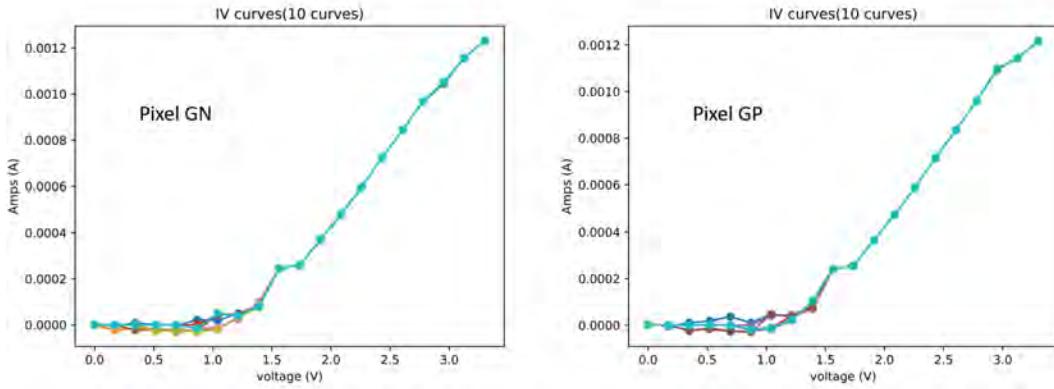
**Figure E.8:** IV curves comparing the performance of pixels DN and DP. Relative location within the super-pixel, DN is pixel (3,0) and DP is pixel (3,1).



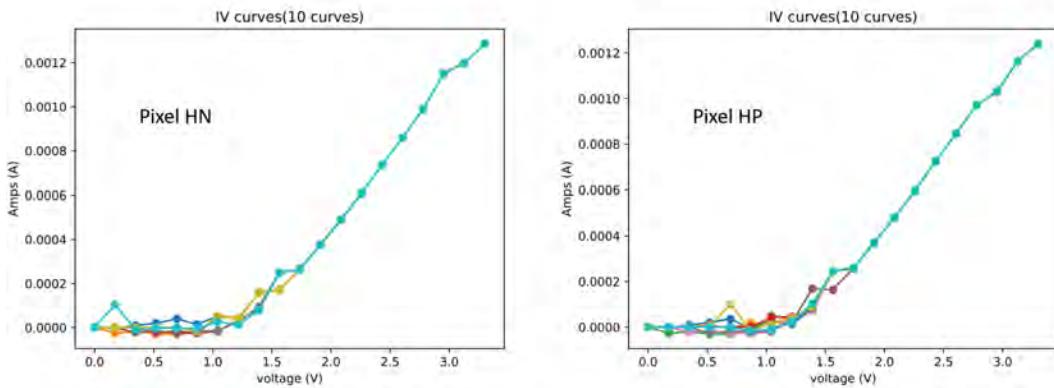
**Figure E.9:** IV curves comparing the performance of pixels EN and EP. Relative location within the super-pixel, EN is pixel (0,2) and AP is pixel (0,3).



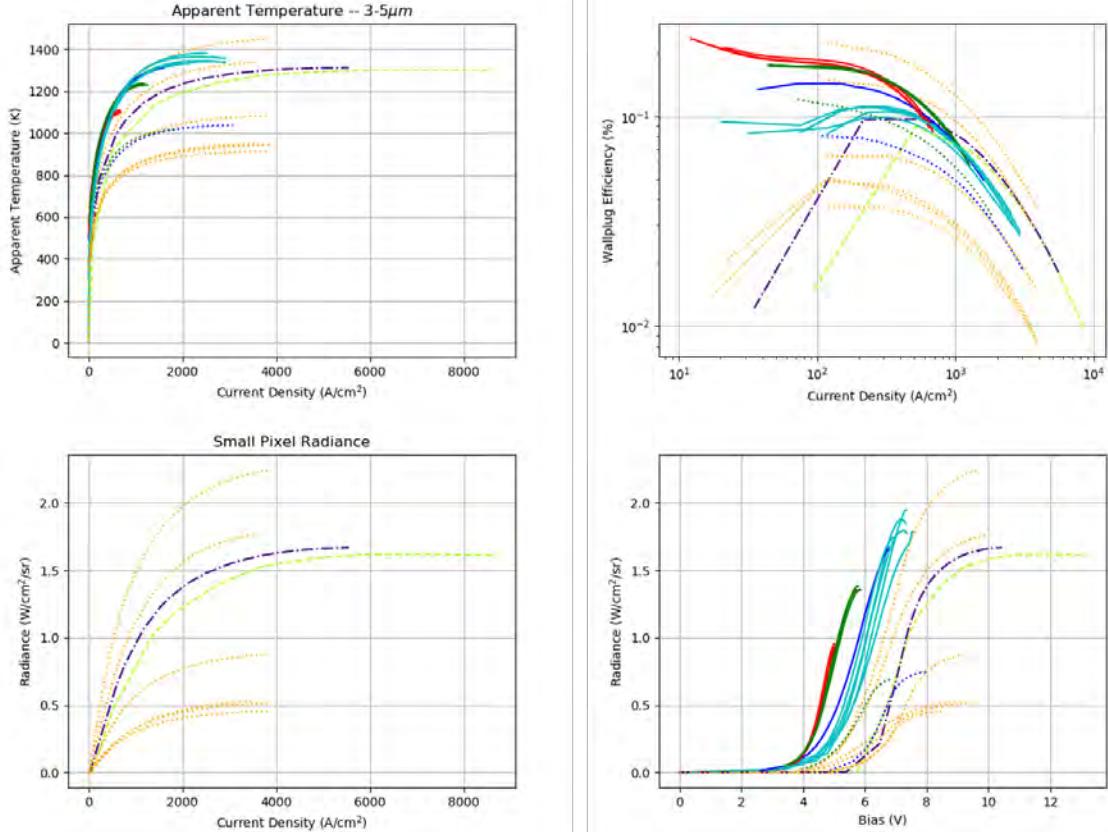
**Figure E.10:** IV curves comparing the performance of pixels FN and FP. Relative location within the super-pixel, FN is pixel (1,2) and FP is pixel (1,3).



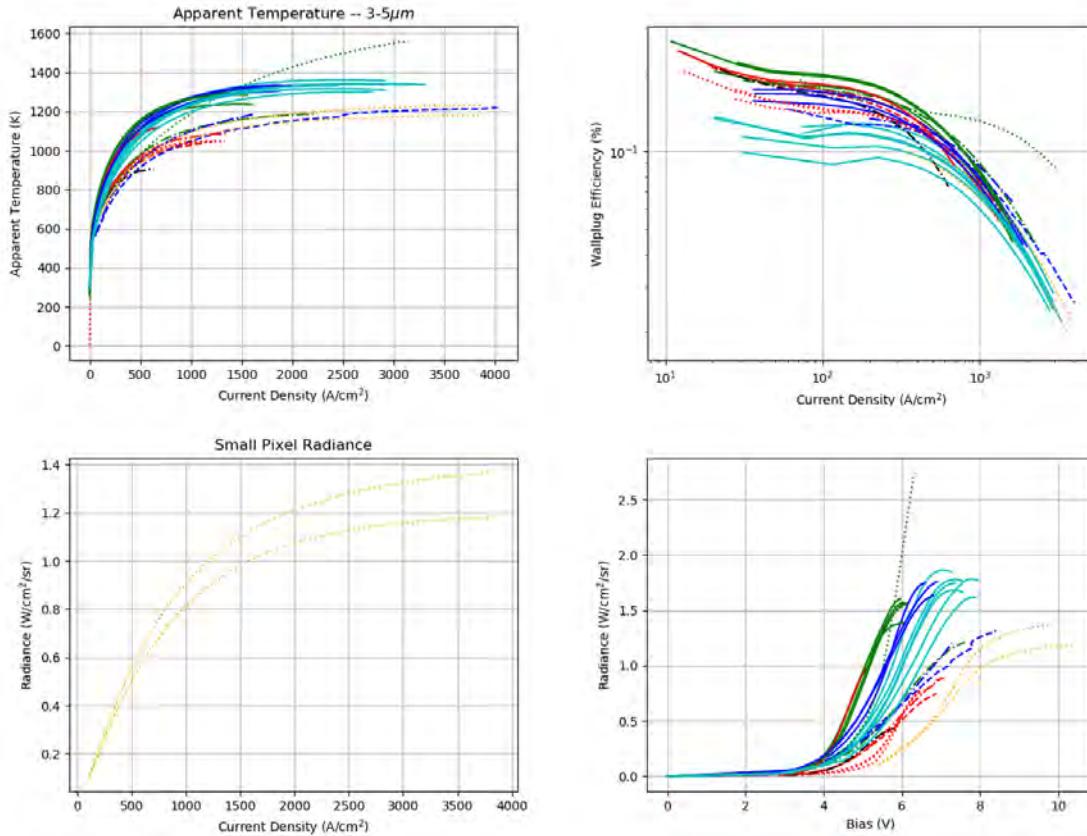
**Figure E.11:** IV curves comparing the performance of pixels GN and GP. Relative location within the super-pixel, GN is pixel (2,2) and GP is pixel (2,3).



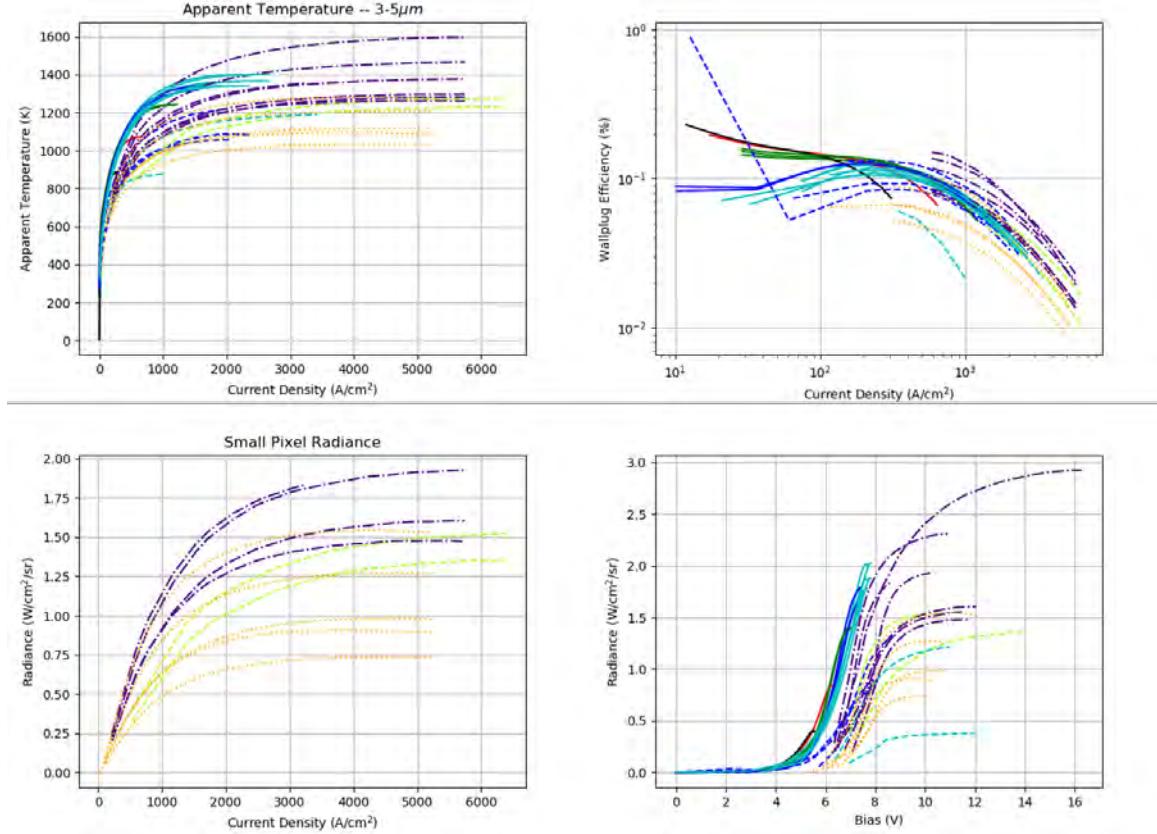
**Figure E.12:** IV curves comparing the performance of pixels HN and HP. Relative location within the super-pixel, HN is pixel (3,2) and HP is pixel (3,3).



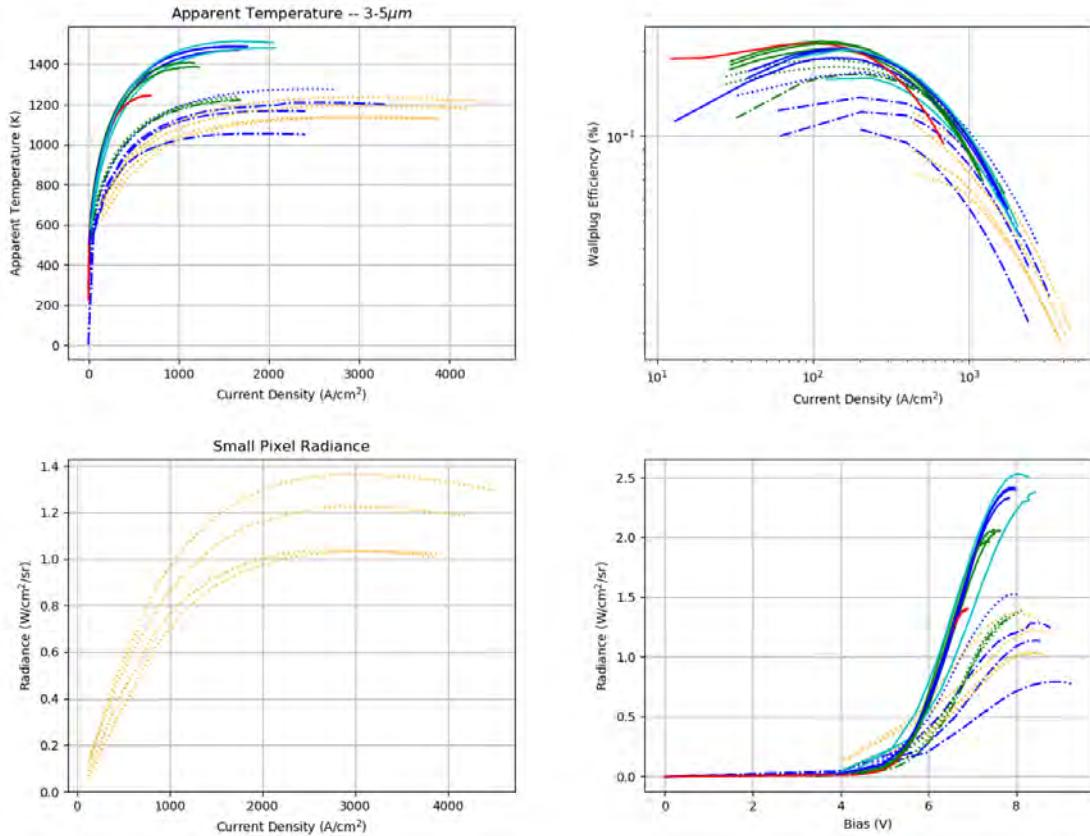
**Figure E.13:** Relevant data collected for SLED test chip IAG739-A02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage



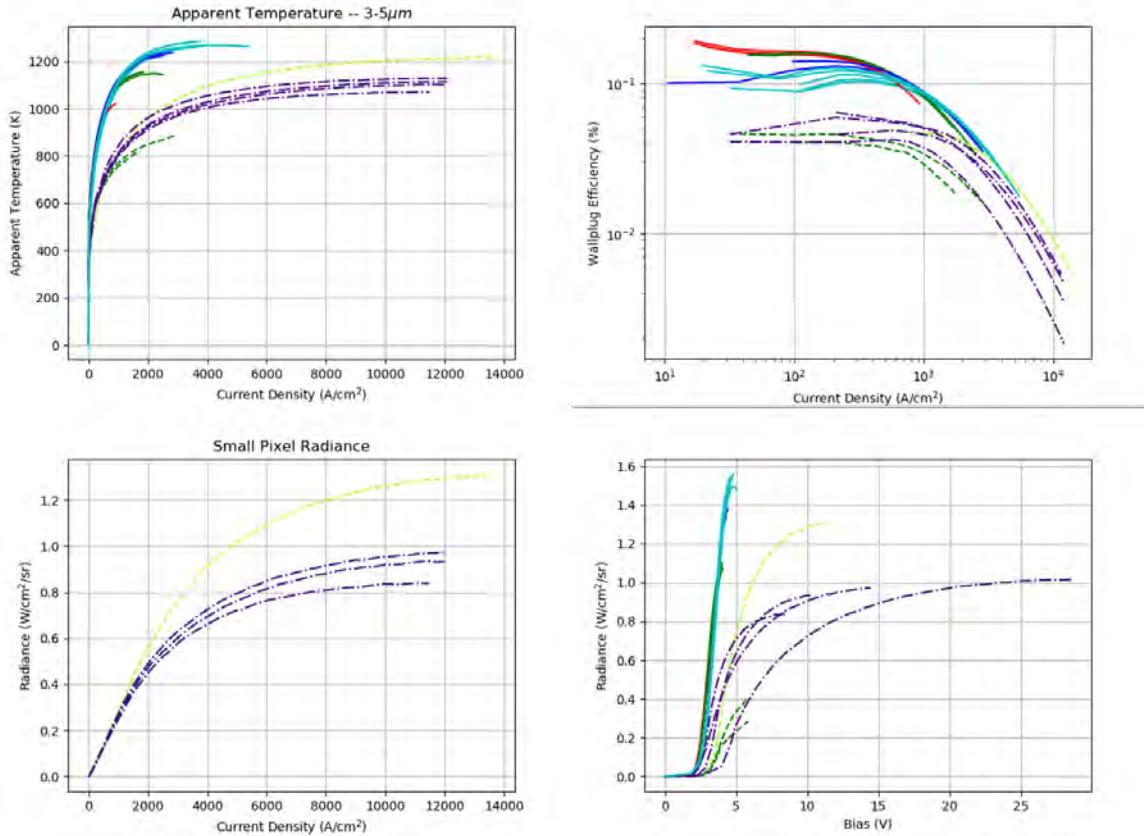
**Figure E.14:** Relevant data collected for SLED test chip IAG739-A03. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage



**Figure E.15:** Relevant data collected for SLED test chip IAG739-A04. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage



**Figure E.16:** Relevant data collected for SLED test chip IAG740-A02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage



**Figure E.17:** Relevant data collected for SLED test chip IAG739-B02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current density for small format pixels. Bottom Right: Radiance vs Bias Voltage