

**SCALABLE BOARD ARCHITECTURE DESIGN & MECHANICAL  
ADAPTATIONS FOR INFRARED SCENE PROJECTOR SYSTEMS**

by

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## **ACKNOWLEDGMENTS**

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## **ABSTRACT**

Infrared scene projectors (IRSPs) are critical laboratory tools for setup, calibration, and testing of infrared imaging systems. Projectors are progressing to handle higher resolution, faster frame rates, and improvement in thermal performance. In recent years, the progress for the development of IRSP systems has reached a point to be able to accommodate larger hybrids. By adding more Infrared Light Emitting Diodes (IRLEDs) to the hybrid array, this created the beginning of implementing the next stage in improving the hardware architecture in the rest of the IRSP system, creating the necessity to increase the amount of signal channels that are routed to the cryogenic packaging from the Close Support Electronics(CSE). The current cryogenic package being used is a pour-filled Dewar that currently houses the IRLED array and the flip-chip bonded Complimentary-Metal-Oxide-Semiconductor (CMOS) Read-In-Integrated-Circuit (RIIC). This thesis will describe a modular hardware architecture design that will let the hardware develop with the firmware and explain mechanical adaptations to allow the continued use of the current pour-filled Dewar. While also describing the current High-Definition Light Emitting Diode (HDILED) IRSP System and its components.

# **Chapter 1**

## **INTRODUCTION**

### **1.1 Motivation**

At the University of Delaware, the Complementary metal-oxide-semiconductor (CMOS) VLSI Optimization Research Group (CVORG) was founded by Dr. Fouad Kiamilev. In 2014, CVORG and the University of Iowas research group led by Dr. Thomas Boggess produced the first Infrared Light Emitting Diodes (IRLED) scene projector through SLEDs technology[2]. Since the first generation 64 x 64 Scene projector system, there have been different versions of SLEDs projectors that have been developed, such as 512 x 512, the Two Color SLED Array (TCSA), Night Glow Short Wave Infrared LED (NSLED), and the most recent development- High Definition Infrared LED (HDILED). This thesis highlights the new approach to solving the issue of hardware scalability in SLEDs IRSP systems, different projector multiple Custom Support Electronic (CSE) set ups, and compatibility of current cryogenic packages with higher formatted SLEDs systems.

### **1.2 Background**

In the Electromagnetic (EM) field, EM waves are energy that propagates though mediums and free space, emitting EM radiation. The range in frequencies can be divided into different regions; the Infrared (IR) region, which is at a 700nm to 1mm wavelength, and 300Ghz to 430Thz frequency. Infrared radiation also known as thermal radiation is emitted(syn.) by all matter that has a temperature greater then absolute zero. IR radiation is used in many different applications; such as astronomical, industrial, military, weather, medical, etc. Many various types of detectors and sensors have been developed to interpret/analysis IR data. IRSP Systems are critical

laboratory tools used to setup, test, and calibrate IR imaging systems. These projectors display radiometric video scenery in the IR spectrum. Infrared Light Emitting Diodes (IRLEDs) are a progressive emitter technology that is used for building IRSP systems. The most commonly available IRSP available on the market takes advantage of Micro-Electro-Mechanical Systems (MEMS) technology. However, this technology has limitations such as, operating at low frequency rates, having issue with emulating a non-black body spectrum, and issues with separating apparent temperatures from actual thermal temperatures[12]. To resolve the majority of these limitations, a system was developed called super-lattice light emitting diodes (SLEDs). SLEDs technology is able to perform at much higher temperatures while not damaging the system[2]. This allows the system to run at faster frame rates, provide higher resolutions, and improved thermal performance. The most recently assembled IRLED array has a resolution of 2048 x 2048, operates in the spectrum known as the mid-wave IR (MWIR) wavelength, and a 24-micron pixel pitch. This array is apart of the High-Definition Infrared Light Emitting Diodes (HDILEDs) scene projector system[9].

[2] [12] [14] [9] [1] [13] [5] [3] [10] [4] [7] [16] [11] [6] [8] [15]

## Chapter 2

### BASE IRSP FRAMEWORK

The SLEDs Projector System has a multitudinous amount of components that are used in many subsystems in order to produce simulations on the IRLED array. In order to provide the reader a better understanding of how the system works, this chapter will be divided up into sections. One section will incorporate details on the individual components. While the other will explain the subsystems of the framework and the components that are used in those systems.

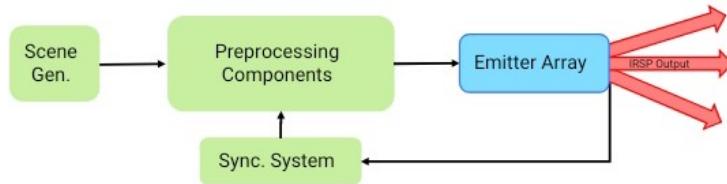


Figure 2.1: Typical IRSP system framework.

## 2.1 Individual Components in System

### 2.1.1 Pixel Overview

An individual SLED's pixel incorporates two 10V CMOS pass transistors that are responsible for transferring an analog input to the corresponding drive transistors. The pass transistor is connected in parallel to both N type and P type metal oxide field effect transistors (MOSFETs). Shown in Figure 2.2 below is a schematic of a single Read In Integrate Circuit Pixel. The job of the circuit is to let the flow of high and low voltages to pass through the circuit; with the N type passing the low voltages and the P type passing the high voltages[2].

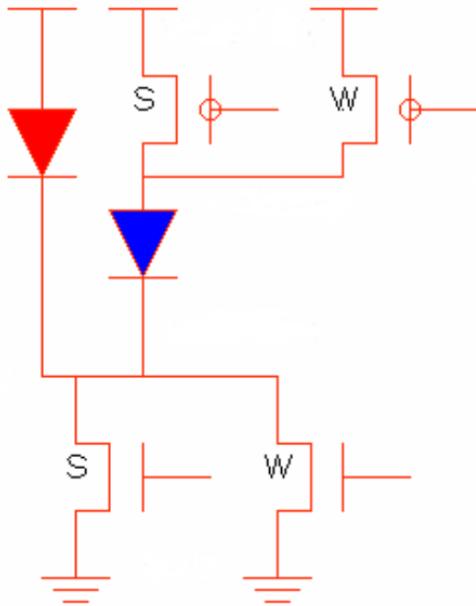


Figure 2.2: Schematic of a single TCSA RIIC SLEDs pixel[14].

### 2.1.2 Read in Integrated Circuit(RIIC)

Read-in Integrated Circuit(RIIC) is typically a CMOS ASIC that holds the circuitry used to drive and address the emitters with continuous current. Over the years there has been numerous RIIC designs such as 512x512 and TCSA, this document will only discuss the current HDILEDs RIIC. HDILED is a single color, 2048 x 2048 RIIC that has a die size of around 7cm x 7cm. The range that the current array emits at is medium wavelength infrared (MWIR). The final step is to solidify the electrical connection by hybridizing the RIIC to a GaSb SLED emitter array[9]. Displayed below in Figure 2.3 is an image of a 8" wafer that holds four HDILED RIICs in it.

### 2.1.3 Infrared Camera

The system utilizes a Forward-Looking IR(FLIR) SC8200 model camera. This model is a high speed MWIR megapixel science-grade IR camera that produces ultra sharp thermal images. It operates with a waveband range of 3.0-5.0 um with a resolution of 1024x1024; connect by a Ethernet and camera link. Controlled though a USB

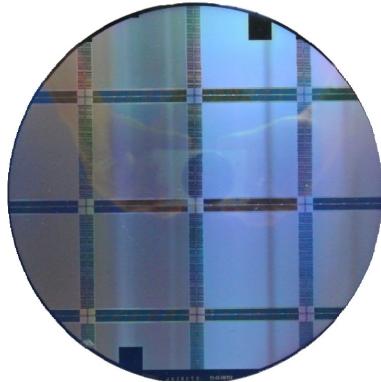


Figure 2.3: Picture of 8" wafer with 4 HDILED RIIC's[9].

and RS-232 cable[7]. However, this models software is limited to only being able to capture one frame image at a time; which is the case for most IR cameras. To simulate video multiple images are stitched together to get a video with the needed frame rate; a capture card is used to capture the video. In Figure 2.4, is the FLIR Camera secured to an optical table directed at the dewar window.



Figure 2.4: Picture of the FLIR SC8200 Camera directed at the dewar window[12].

#### 2.1.4 Non-uniformity Correction PC

In the development of IRSP systems, IRLED array technology has the potential to replace resistor array technology. IRLED arrays provide their own set of challenges, such as complex time dependencies due to thermal characteristics, unfavorable pixel temperatures, high chance of cross-talk, and high pixel non-uniformity. The Non-uniformity Correction PC system is dedicated to correct the non-uniformity amongst the pixels; so that the desired test image sent as displayed correctly, while also performing gamma correction for the non-linear LEDs on the array. In the SLEDs system

there are two techniques used to perform the correction. One of them is called the Average Pixel Linerization (APL) and Non-Uniformity Correction (NUC) software. These techniques determine the operability and correct for any differences that might occur on the array[5].

The components inside of the PC are:

- Quadro Sync Card for syncing.
- Cameralink capture cards for capturing the array to get the IR information and how the system makes images and videos.
- 2 DVI/HDMI inputs to the capture cards which are for getting loop back video from the CSE.
- NVidia M4000/K5000 GPU's.

### 2.1.5 Close Support Electronics(CSE)

The CSE houses many components inside which will be discussed in later sections and is required to run a IRSP system. The main responsibility of the CSE is to provide data, power, and control signals to the hybrid in order to drive the IR array. This unit holds the hardware and firmware required to pre-process input imagery before it is displayed on an IRLED array.



Figure 2.5: Picture of Close Support Electronics[9]

#### 2.1.5.1 Field Programmable Gate Array(FPGA)

Inside of the CSE, The signal is processed by a TB-6V-LX760-LSI Field Programmable Gate Array. This Super FPGA board is designed by Inrevium; it consist

of Virtrex 6 family FPGA XC6VLX760-2FFG1760 Device. A 16 layer board with the dimensions of 369mm x 225mm; made of FR-4 material. This device has 10 low pin count FMC connectors, giving the ability to utilize two color systems while also using 32 channels from those connectors to dispatch data to the array[8].



Figure 2.6: Picture of the TB-6V-LX760-LSI Field Programmable Gate Array(FPGA) Board[8].

### 2.1.5.2 FMCL-ZYNQ (HDMI Board)

Connected to the Super FPGA board is 2 x Custom FMCL-ZYNQ Rev 3 HDMI custom cards. Shown below in Figure 2.7, is a picture of the HDMI boards. These boards use a Xilinx ZYNQ XC 7000 series dual-core ARM Cortex-A9 MPCore with CoreSight processor, while also having 36kb Block RAM(BRAM) and 256kb on-chip RAM[15].



Figure 2.7: Picture captured of the FMCL-ZYNQ Rev 3(HDMI Board).

### **2.1.5.3 Digital-to-Analog Converter(DAC) Board**

Also, connected to the Super FPGA board are sixteen FMC-4-DAC Rev 3.2 boards. Displayed below in Figure 2.8, is a picture captured of the DAC board. These cards are highly configurable boards that can be programmed through a PIC32 programmer to convert the digital DAC signal to output an analog signal. Each DAC card manages 2 of the 32 drive channels that are sent to the array.



Figure 2.8: Picture captured of the FMC-4-DAC Rev 3.2 Board.

### **2.1.5.4 Amplifier Board**

Attached to each DAC is a FMC 4DAC Amplifier Rev 4.1 board that amplifies the various current that comes from the two analog signals received by the DAC Board. Correcting the signal to the right voltage gain and offset to drive the transistors on the RIIC[14]. These signals can be tuned using two potentiometers on each signal that control the offset and the gain of the signal. Below in Figure 2.9, is an image captured of the Amplifier Board.

### **2.1.5.5 Interface Board**

The Interface Rev 1.4 board redistributes the drive channels inside of the CSE from the FMC 4DAC Amplifier boards to the ribbon cables that lead to the cryogenic package. It is powered with 12V that is distributed to all the different components in the CSE such as; FMC-4-DAC boards, FMC 4DAC Amplifier Cards, and the RIIC.



Figure 2.9: Picture captured of the FMC 4DAC Amplifier Rev 4.1 Board.

The board also contains a circuit breaker with a controllable trip level that protects the system when too much current is drawn from the RIIC. This board is in charge of level shifting the digital address lines from 2.5V to the 5V needed by the RIIC[2]. Shown below in Figure 2.10, is a picture captured of the Interface Rev 1.4 Board.



Figure 2.10: Picture captured of the Interface Rev 1.4 Board.

### 2.1.6 Cryogenic Packaging System

The Dewar package component of the IRSP system houses the actual array. A Dewar is typically a vacuum insulated container that is used to preserve the internal temperature for a longer period of time. Currently, there are two different types of cryogenic Dewar's that are being tested for the HDILED system. One of them is a COTS Dewar and the other is a custom designed Dewar.

### 2.1.6.1 J.K. Dewar

The current packaging used in the IRSP system is a J.K. Henriksen CTS-1260 Dewar chamber which is a Commercial Off The Shelf(COTS) product that is available on the market. The responsibility of the Dewar is to keep the IRLED array cold and under vacuum. By bringing the array to cryogenic temperatures; it assists in increasing the efficiency of the IRLED's. This dewar chamber is a pour filled type that uses liquid nitrogen as the cooling agent. It uses the low heat of the vaporization to boil off nitrogen; removing the heat passively[12]. Built-in to the system is 100 transmission line signals that are used to accommodate the smaller scale SLEDs arrays but will have issues with larger format arrays due to these arrays they need to be driven by more signals directly into the array. Signals travel though 50 ohm coaxial cables that connect from the back of the dewar to the RIIC mounted board inside of the enclosure. Displayed below in Figure 2.11, is a picture captured of the J.K COTS Dewar.

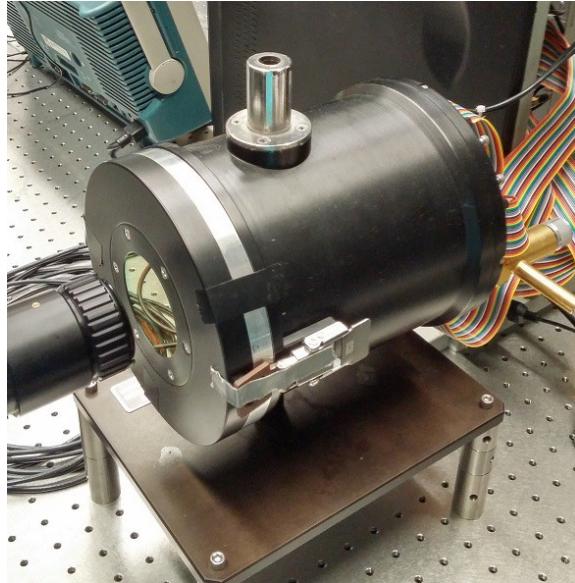


Figure 2.11: Picture captured of the J.K. Henrikson CTS-1260 COTS Dewar[12].

### 2.1.6.2 Custom Dewar

Chip Design Systems (CDS) had developed a new cryogenic packaging system with the help of Advanced Research Systems Cryogenics (ARS). The cryogenic packaging system is composed of a vacuum chamber designed by CDS, and a cold head designed by ARS. The new cryostat design, seen in Figure 2.15, is composed of a semi-custom closed loop Gifford-McMahon cryostat, and a novel vacuum chamber that incorporates a PCB into the vacuum chamber design. This design has several advantages over the previous Dewar design and the current state of the art in IRLED hybrid packaging. The main advantages are: no electrical pin limitation, improved signal integrity for electrical input/outputs, close proximity electronics, higher thermal energy removal, and customizable vacuum chamber and PCB design to properly package any IRLED hybrid.

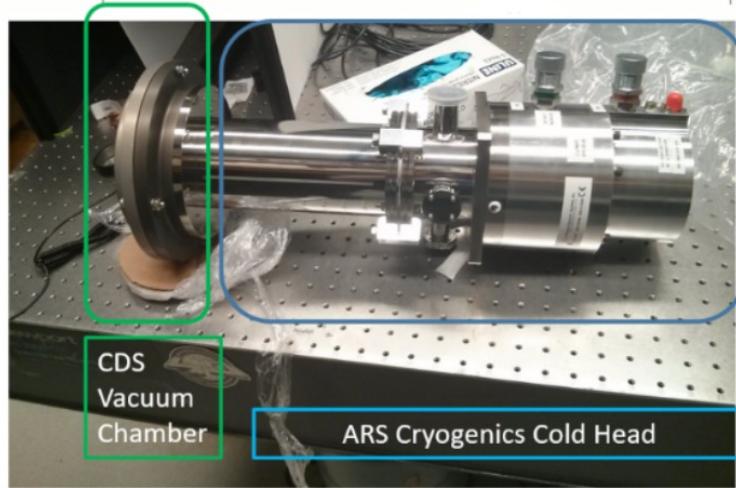


Figure 2.12: Picture captured of the real view of the custom packaging system with labels showing which part is designed by CDS and which part is designed by ARS Cryogenics[10].

By integrating the cold head and the vacuum chamber together a novel design can be created. In this design the vacuum chamber lid will be able to seal against the printed circuit board (PCB). This has the benefit of allowing for a customizable amount and design of electrical signals. These two benefits can be used to create SLEDs hybrids

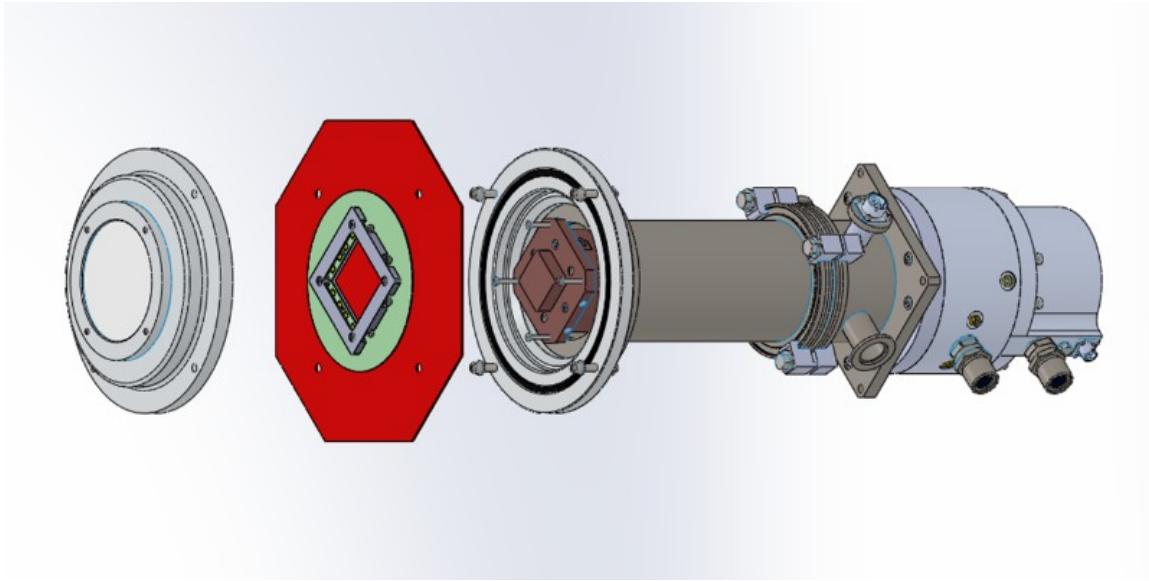


Figure 2.13: Solidwork’s schematic diagram showing the exploded parts view of the new custom ARS package. This image shows the mounting of the carrier board(Red Board)in the dewar[10].

that require more electrical input signals and create exceptionally well-matched trace impedance for improved signal integrity. The new custom cryostat design presented here eliminates many of the limitations of the previous JK CTS-1260 Dewar. The 3D CAD schematic design in Figure 2.13, illustrates the assembly with the carrier board. Other aspects of this design, including its vacuum properties, are discussed in detail in reference [16].

The vacuum chamber designed at CDS combines an interposer board (red PCB board shown in Figure 2.13 and in Figure 2.14, a metal vacuum chamber with cold pedestal, and a window. The critical innovation of this design is the ability to extend the interposer board through the vacuum chamber walls. The two metal portions of the vacuum chamber shown in Figure 2.13, have O-rings embedded in them. The O-rings are pressed against the interposer board and create a seal that can maintain the required vacuum. A vacuum of 4105 torr was measured in the vacuum chamber. It is believed that a lower vacuum can be obtained by properly baking the PCB used as an interposer and choosing a material other than glass-reinforced epoxy laminate material

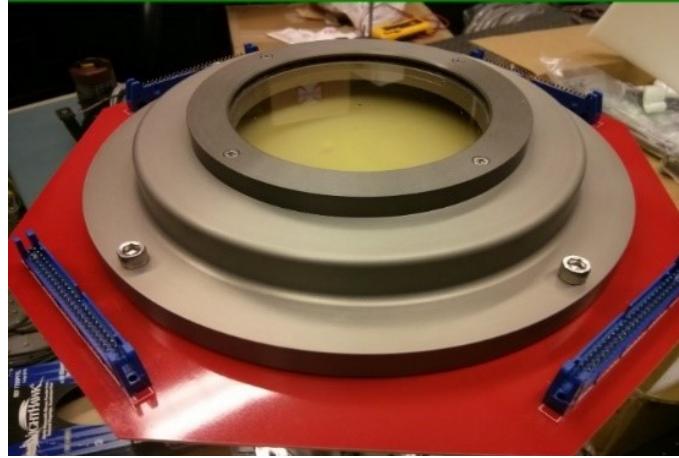


Figure 2.14: Picture of the new vacuum chamber design with interposer board installed.

(FR-4) as the interposer. However, lower pressures were not tested extensively because they are not required for IRLED IRSPs. For current IRLED IRSPs, the interposer board is a PCB that the IRLED Hybrid or any test unit is affixed or wire-bonded to. The interposer board is used to route the electrical inputs required by the RIIC to draw IR scenery into the vacuum chamber. A custom-fit vacuum chamber with an O-ring seal is placed around the IR emitter and seals directly against the interposer PCB. The vacuum chamber is a simple machined part that is inexpensive when compared to the cost of the cooling system and current Dewars. The dimensions of the cold head and vacuum chamber are seen in the schematic in Figure 2.15, measurements are shown in full detail.

The ARS cold head is a closed-circuit system comprising of the cold head, a water chiller, and a compressor. The cold head uses helium gas as a refrigerant in a single stage Gifford-McMahon Cycle refrigerator. The helium gas is used to take the heat generated by the SLED's hybrid and move it to a chilled water reservoir or flowing chilled water. The water chiller expels heat, and the compressor compresses the helium gas. This is convenient because it is a closed system and does not require a supply of new helium gas. The compressor is shown in Figure 2.16. The compressor can be placed to the side in the laboratory and up to 60 ft. of hoses can be run from the compressor to the cold head.

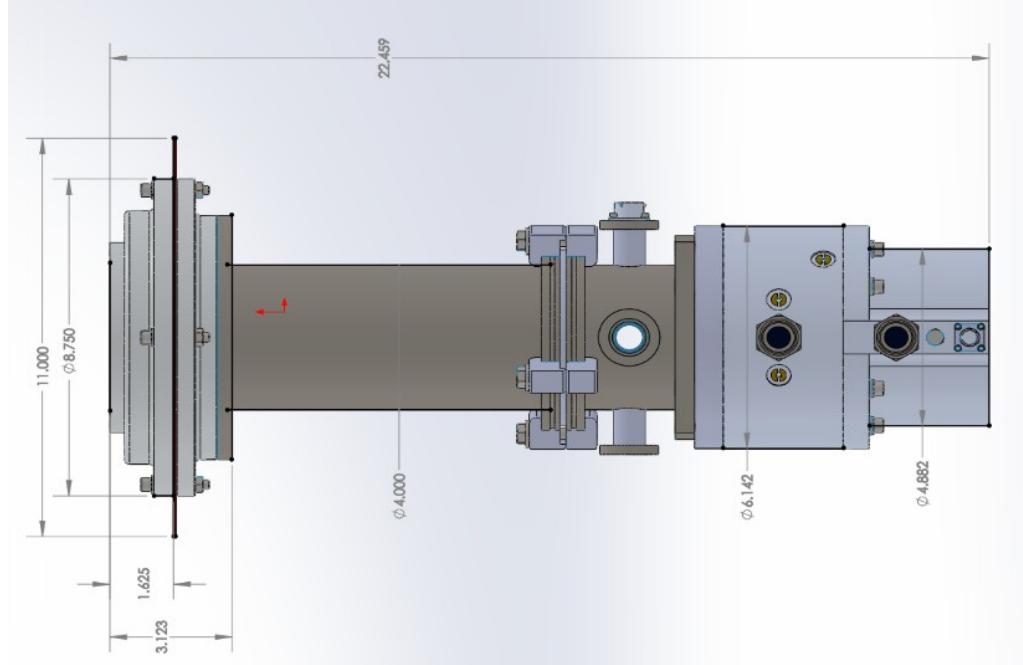


Figure 2.15: Diagram of the vacuum chamber and the cold head[10].

The dimensions of the compressor are:

- Depth: 21”
- Width: 18-7/8”
- Height: 24-5/16”
- Weight: 230 lbs.

## 2.2 Data Flow in Framework/ Framework of Systems for IRSPs

This next section will explain how the data flows through multiple systems in the IRSP framework. Shown in Figure 2.17 is a diagram of the general layout of the hardware architecture for the SLEDs IRSP system. Since the first SLED's IRSP system, there have been many different types of SLED's systems such as; 64x64, 512x512, TCSA, and HDILED's. However, this piece will mostly focus on the components in the current HDILED System.



Figure 2.16: Picture of the ARS Cryogenics Helium Gas Compressor[12].

### 2.2.1 Raw Data Collection

IRSP's displays video scenery defined by the user, such that an IR sensor can detect the image in real-time for specific end user requirements. (A scene is provided by the user through a scene generator computer). The scene generated image is then sent to the Non-uniformity Correction computer that uses the NUC Software. This NUC PC corrects the differences in the similarity between the LEDs and can operate for both single and two color arrays, while also performing gamma correction for the non-linear LEDs on the array. The computer acquires the desired frame rate and the scene data. Using two single link Digital Visual Interface (DVI) channels between the scene generator and the NUC system. Each frame is split horizontally and spatially divided into sub-frames which is received by the NUC PC; this is done to avoid cross correlation. At faster frame rates, this requires accurate synchronization to make sure that a full up to date frame is being displayed. The Graphic Processing Unit (GPU) (current GPU type need to check); then processes and corrects the image. To do this, the computer sweeps each pixel independently and generates a NUC table of coefficients based on the required drive voltage for the transistor[1]. The GPU allows the system to do this simultaneously for all of the new pixel as frames are continuously streaming in. The NUC system then works with the Synchronization System to keep the transmitted

## Hardware Architecture of SLEDs System

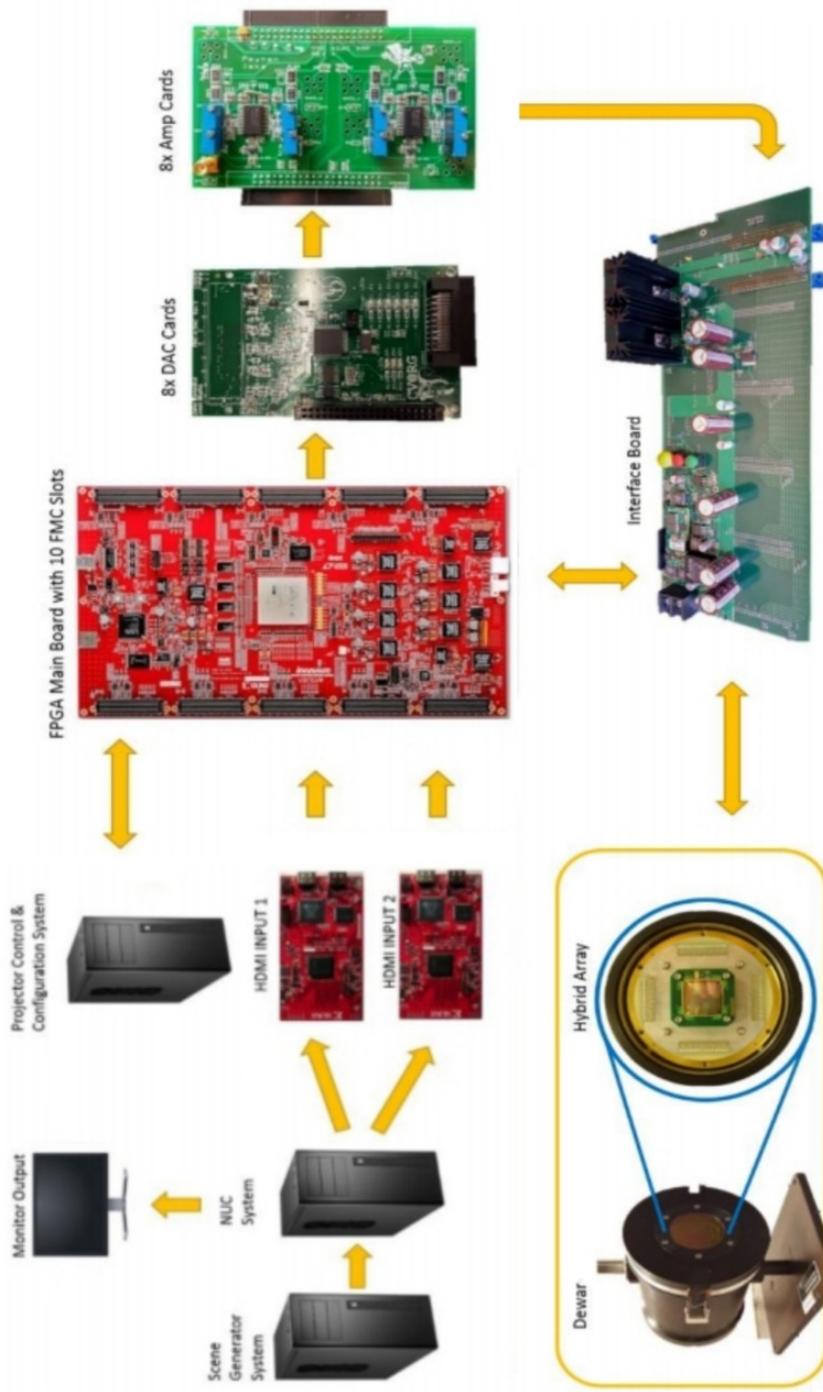


Figure 2.17: General layout of the hardware architecture for the SLEDs IRSP system[2]

data in sync with the current readings. It turns on a grid of pixels all at once and uses a grid detection algoithim to find each individual pixel and captures its radiance[14].

### 2.2.2 Synchronization System

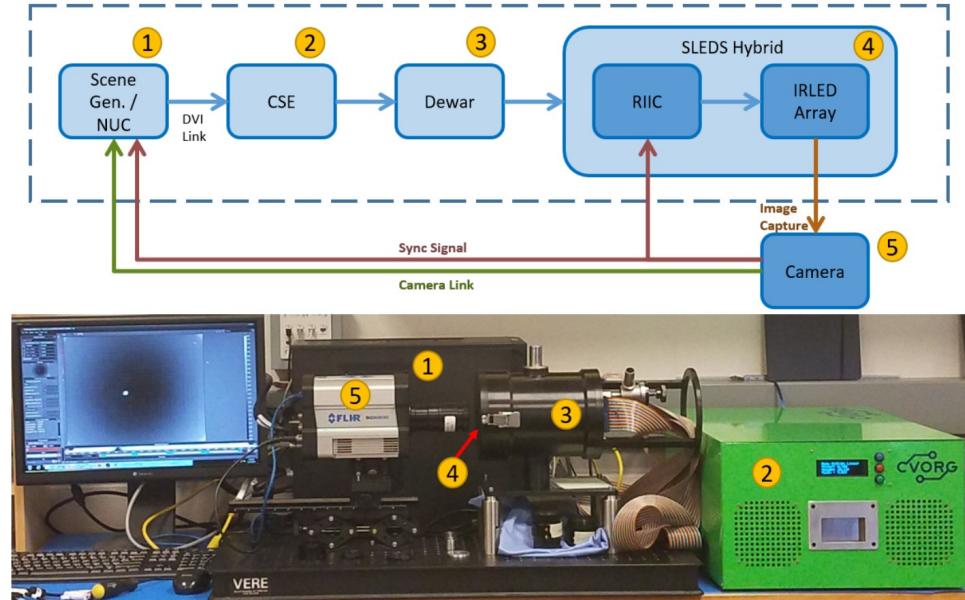


Figure 2.18: Above image is a block diagram of the synchronization setup in the IRSP system. Below image is a picture of the IRSP system[1].

At faster frame rates, this requires accurate synchronization to make sure that a full up to date frame is being displayed. In Figure 2.18 a block diagram of the synchronization layout in the system. The IR camera is used to generate a synchronization pulse that is delivered to other components in the system. The Quadro Sync cards use this pulse in combination with the GPUs to keep the DVI links in sync between the scene generator and the NUC computer. Each time the synchronization pulse occurs an input frame is fed into the projector and an image is captured from the IR camera[1].

### 2.2.3 IRSP Preprocessing System

After the desired image is corrected and bit packets, the data is then sent to the CSE to pre-process the image before being displayed on the SLED's array. Inside the CSE, the data is sent in through the two HDMI cards; where the FPGA then reads

the streaming data, unpacks the information, then loads the information to the Block RAM to be stored temporarily so that all the channels can be sent simultaneously when they are finished streaming in. The FPGA uses 32 channels to transmit data to the array. Each channel sends information for a individual pixel. These channels are digital signals that are then distributed two at a time to the sixteen connected DAC boards. Theses board are responsible for converting the digital signal on the channel to the appropriate analog signal needed; however the analog signal output from the DAC's don't have a high enough voltage. A single amplifier card is connected to each DAC to then amplify the weak analog signal coming form the DAC to the voltage needed to drive the transistors on the RIIC[14]. After the signal is converted and amplified all of the channels from the amplifier cards are rejoined on the interface board. The signals are then redistributed to four ribbon cables that are then connected to the back of the Dewar Package that houses the RIIC.

#### 2.2.4 Cryogenic Packaging System

To increase photon emission from the SLEDs, the SLEDs hybrid is cooled to 77 Kelvin in a vacuum chamber. Drive electronics are then connected to the cooled SLEDs hybrid in the vacuum chamber. In this section, both currently used and new Dewar's will be discussed because both cryogenic packages are compatible for the HDILED SLED's System. Future IRSP systems will require resolutions up to 2048 x 2048 pixels, with faster frame rates as high as 1 KHz[11]. The system uses many parallel analog input channels to transfer the scene data to the RIIC. The 1 Megapixel HDILED RIIC, for example, uses 32 analog inputs and is designed to operate at a 600Hz frame rate. At higher resolutions, the number of pixels increases dramatically and, in turn, increase the number of analog input lines required to maintain the same performance on each line. This would exceed the fixed number of I/O pins of the original cryogenic package which already constrains performance. The first HDILED array was mounted to a hybrid carrier PCB designed to fit in the original Dewar. This mounted hybrid can be seen in Figure 2.19; on the left is the board itself, inside the COTS Dewar and

on the right is the PCB layout of the hybrid carrier board.

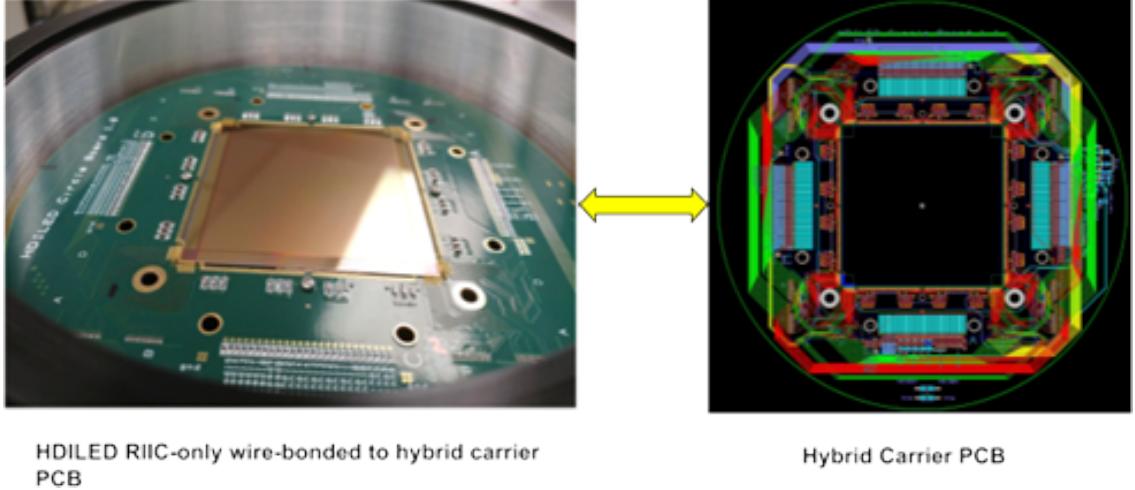


Figure 2.19: Photograph of RIIC-only wire-bonded to hybrid carrier PCB(left) and PCB layout of carrier PCB board used(right)[10].

The next piece of the IRLED packaging is the cold head and cooling system from the ARS Cryogenics. The previous type of Dewar chamber used for our IRSP's is a static, pour-filled, tank of liquid nitrogen. It takes advantage of how readily liquid nitrogen boils off, which removes the heat generated by the SLED's hybrid. The previous Dewar chambers can remove an estimated 20W of heat, and the ARS cold head can remove 200W of heat. The increased cooling capacity is because the new IRLED package uses a closed-circuit flowing helium gas system to remove heat much more effectively. The helium gas goes through several thermally conductive blocks of copper first and is pumped rather than passively boiled off – allowing for faster heat removal.

### 2.2.5 Emitter Array System

After the analog converted data stream comes in through the cryogenic package connectors to the carrier board displayed in Figure 2.19. It is then sent through the hybrid carrier PCB that is then wire bonded thru contact pads outlined along the center of the board that match the layout of the HDILED RIIC. An example of the

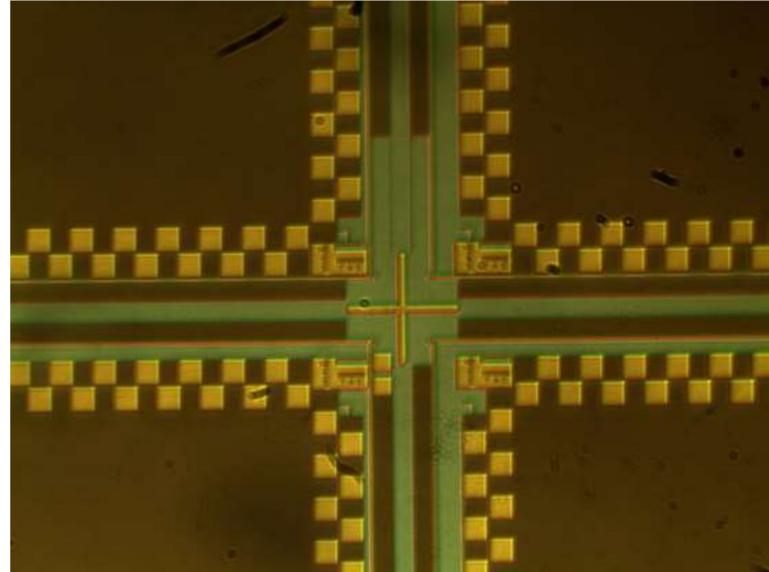


Figure 2.20: Contact pads on the corners of the full size RIIC chips on a wafer

contact pads on the RIIC that the board is wire-bonded too is shown in Figure 2.20. The hybridized RIIC and GaSb SLED emitter array forms a micro-display that emits the IR radiation of the users desired image. Attached to the board and against the array is a mounting bracket. The bracket is used to keep the array in place, protect the wire-bonds and provide the board with just enough flex to provide just the right amount of tension to hold the array in place under cry-cooled temperatures.

### 2.2.6 IRSP Output

The output of the system is a non-uniformity corrected simulation that is emitted from the SLED's micro-display, and captured using an IRLED camera. In the next figure 2.22, is imagery taken by the FLIR camera from the HDILED IRSP micro-display using NUC software cooled in the J.K Dewar.



Figure 2.21: The original star trek image on left vs raw projected image in the middle and image with APL on the right[13].



Figure 2.22: Original star trek image captured by the FLIR camera of the HDILED array running at 30Hz; using NUC correction software. The bright "T" shape in the top left quadrant are damaged pixels.

## **Chapter 3**

### **ELECTRONICS DEVELOPMENTS**

The CSE's connection to the SLEDs hybrid system uses ribbon cables connected from the interface board in the CSE to the I/O insulation displacement connector (IDC) on the back side of the dewar. The signals are then routed using the previous version of the carrier board in Figure 2.19 to the micro-display. The PCB flow chart in Figure 3.1 shows the next phase of scaling SLED hardware technology designed for high format systems, while also observing the performance and efficiency of compacting and integrating the system together. This set up will allow us to test the new carrier board design with the current working system to determine if there are any problems with signal integrity and provide the opportunity to add post-amplifiers to the analog chain.

#### **3.1 New Board Architecture Design**

As IRSP's continue to develop our group had reached a point where the current IRSP hardware has become a major performance bottleneck for the system. One solution to this is to construct new hardware to allow for the system to have room to grow for future varieties of IRSP systems. This new architecture is called the SLEDs Empire layer, shown below in Figure 3.1 is a flow chart of the next step in hardware architecture for HDILED projector's.

By improving the hardware not only will the IRSP system performance improve, the system will become more modular and adaptable to change, provide less risk of damaging system components during testing, while also allow testing to be done with various possible different projector configurations and how they affect performance.

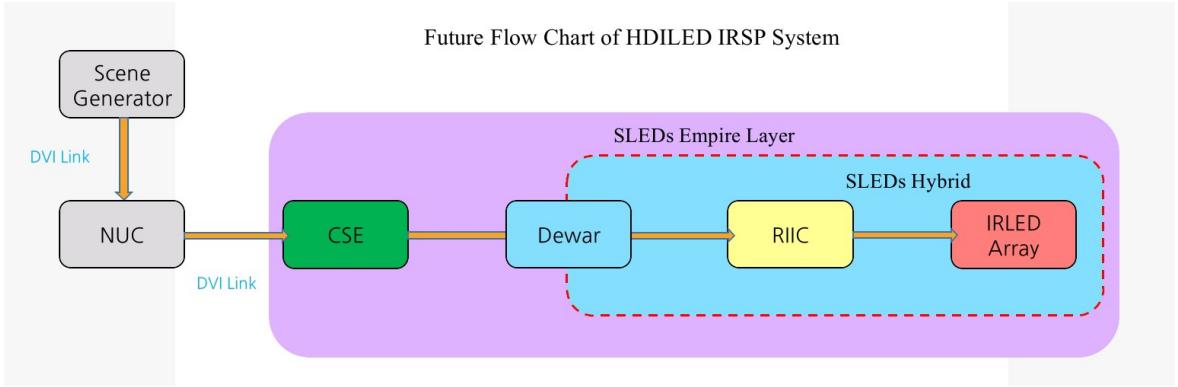


Figure 3.1: Future flow chart diagram of the HDILED IRSP System; highlighting the SLEDS empire layer.

Shown below in Figure 3.2 is a flow chart of the first phase design of the board architecture for the SLEDS Empire layer of the HDILED IRSP system. This will allow us to merge more of the systems components together to help decrease signal noise, decrease amount of physical system space; while also providing protection to the more sensitive and expensive components in the system. Allowing the systems parts to be simpler to fix, replace, or interchange for future iterations of boards. This will bring room for flexibility in the system empowering the hardware to keep up with the development of the software for the system.

### 3.2 Phase One Board Architecture

The first HDILED array is mounted to a hybrid carrier PCB designed to fit the original dewar and is, therefore, subject to the limitations thereof. This mounted hybrid can be seen in Figure 2.19. On the left is the board itself, inside the COTS Dewar and on the right is the PCB layout of the hybrid carrier board.

At the top of this diagram is the hybrid chip/micro-display that is wire bonded to the pads along the inner edges of the carrier board. The new hardware design will incorporate all the same components as the previous HDILED carrier board. However, some of the components on the previous carrier board will be shared between the new Carrier board and Mogh board. The design of these boards were done in Pulsonix PCB Design Software.

## Phase one of SLEDs Empire Layer

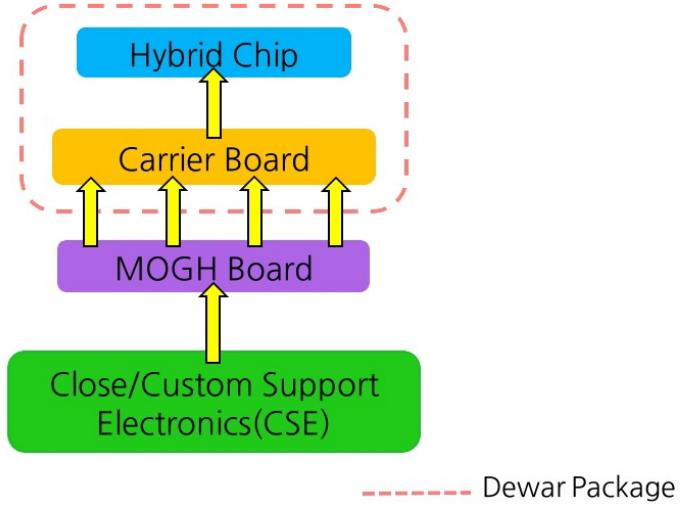


Figure 3.2: Flow Chart of the first phase in constructing the board architecture for the SLEDs Empire Layer.

### 3.2.1 Carrier Board

This new HDILED Carrier PCB provides power and signal routing from the corners of the Hybrid SLEDs array to the outside of the dewar package. The board will house the more passive components from the original carrier board. The connector used between the carrier board and the MOGH Rev.1 board is a high-speed socket type connector with a ground plane. At a voltage rating of 175 VAC, current rating of 2 amps per pin and 25 amps per ground plane. Each connector has a total of 240 + 4 signal pins and power planes. So with this board, the system can accommodate a total of 960 + 16 signal pins and power planes directly routed from the RIIC inside the Dewar enclosure to the outside. We will be able to easily iterate through electronic design without opening the vacuum chamber, including adding post amplifiers, EEPROMs, temperature sensors, and SMB connectors to further improve signal integrity.

The new carrier board can remain under vacuum while the electronics are changed outside of the enclosure enabling rapid iteration. The set up can also act as a drop-in replacement for the current dewar/carrier board/hybrid system using a

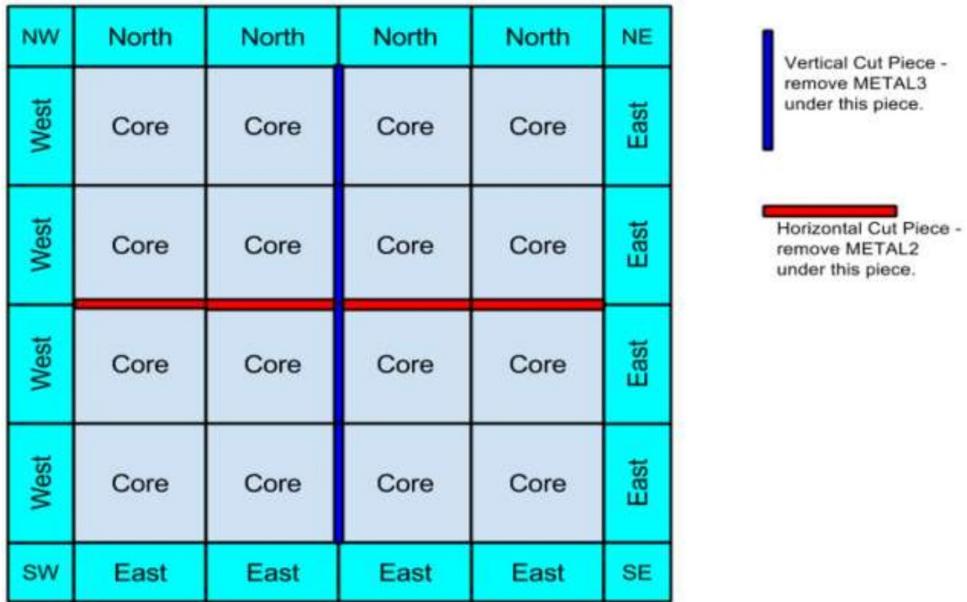


Figure 3.3: Stitching pattern for HDILED showing the pixel layout and division of the quadrants[6].

board which connects to all four quadrants of the chip. The quadrants for the pad layout of the analog signals that is used to address the pixels on the HDILED RIIC chip is shown in the stitching pattern displayed in Figure 3.3. In this previous system, the analog lines were shared such that we only needed a quarter of the analog signals at a time. This will have similar limitations as the original system except now each analog line has their own signal and the new spatial freedom of the board. The amount of signals available now has more than quadruple the number of signal pins relative to the previous model, allowing all of the mechanical components of the new system to be tested without completion of the new electronics.

The schematic of this new carrier design is found in parts in appendix A. This design was done with the assistance of Jonathon Dickason and Garrett Ejzak in order to keep the same properties as the previous carrier round board to work in the system. This board is shown in figure 2.19. In Figure 3.4, shows the new carrier board, there is a circle cut out of the orange layer. This area is restricted from having tracks on both the top and bottom layers. In the right image of Figure 3.4; the light purple layer

shows the outlines for the dimensions of the mechanical restrictions that the board has based off of the measurements observed from the lid and base of the cryogenic packages. This is to make the external layers as flat as possible to allow an O-ring to seal correctly against them. The Mogh board will convert the connectors to enable the CSE to feed all the signals to the RIIC through the four 50 pin ribbon cables used in the current system providing room to easily make improvements. Through trial and error with assembling the board which can be described in chapter 5; the group came to an agreement to have Shore Printed Circuits, Inc. assemble the board. Below are images of both the unpopulated and populated boards of the HDILED Carrier board with the RIIC only array wire-bonded to the inner cutouts edge pads.

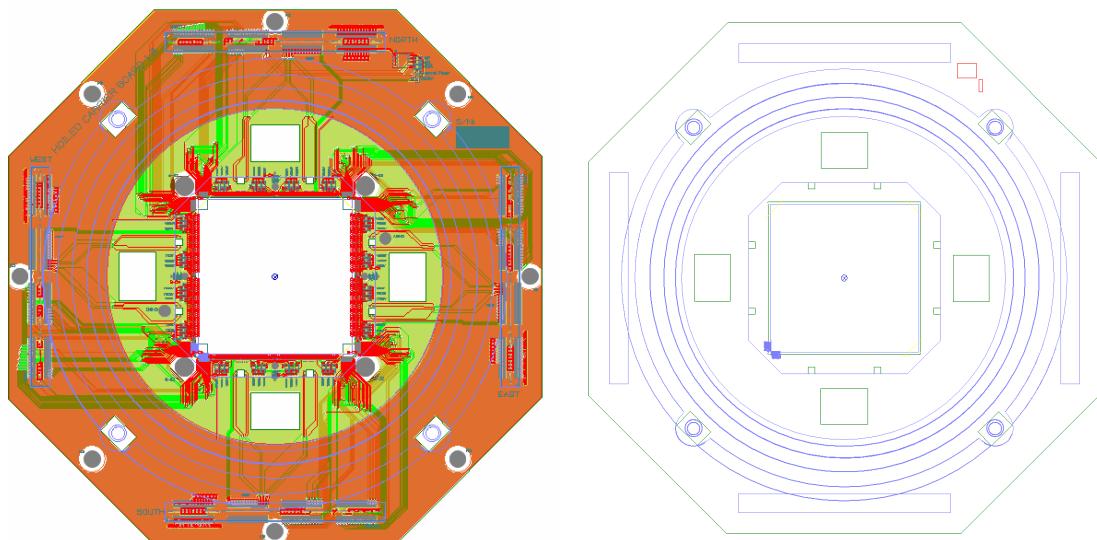


Figure 3.4: HDILED Carrier PCB layout; left is an image of all layers of PCB Layout, right is an image of the document layer and board Outline of PCB layout.

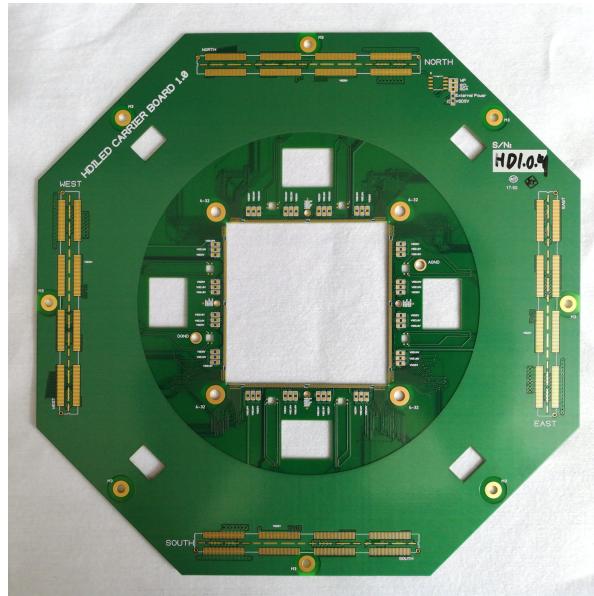


Figure 3.5: Picture captured of unpopulated manufactured carrier PCB board.

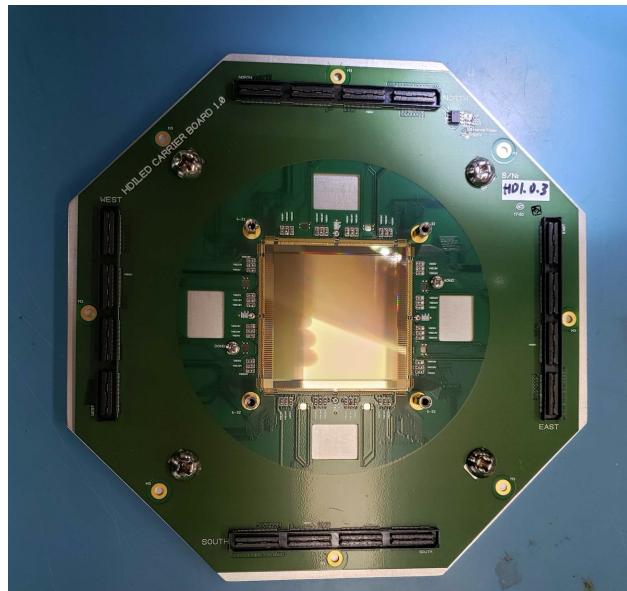


Figure 3.6: Picture captured of carrier board populated with all the board components; including the HDILED RIIC only array wire-bonded.

### **3.2.2 Mogh Board**

The Mogh board is a 4-layer passive board designed to convert the 50 pin ribbon cable headers to high-speed socket type connectors enabling the CSE to feed all the analog signals necessary to the RIIC through the four 50 pin ribbon cables used in the current system set up providing room to easily make room for improvements to the signals going directly to the RIIC. Included on this board are two layers dedicated for 6 mil tracks, one layer for ground, and one lay for 10V plane. Along with the corresponding high-speed socket type connector, NPN transistors designed for high voltage blocking, I2C-compatible EEPROM, LEDs, temperature sensor signal connectors, dip switches for testing purpose, and a combination of resistors and capacitors. The schematic of the Mogh board can be found in appendix B. The center of the board has a circular cutout to accommodate the mechanical fit against the lid of the new vacuum chamber design shown in Figure 2.15. The dimensions of the compressor are 11.32-inch x 10.62-inch. In Figure 3.7 below, the image shows the layout design of the Mogh board. E-TekNet Inc. manufactured, fabricated, and assembled the boards. The fabricated unpopulated Mogh board is shown in the picture below in Figure 3.8. A picture of the top view of the populated Mogh board can be seen in Figure 3.9.

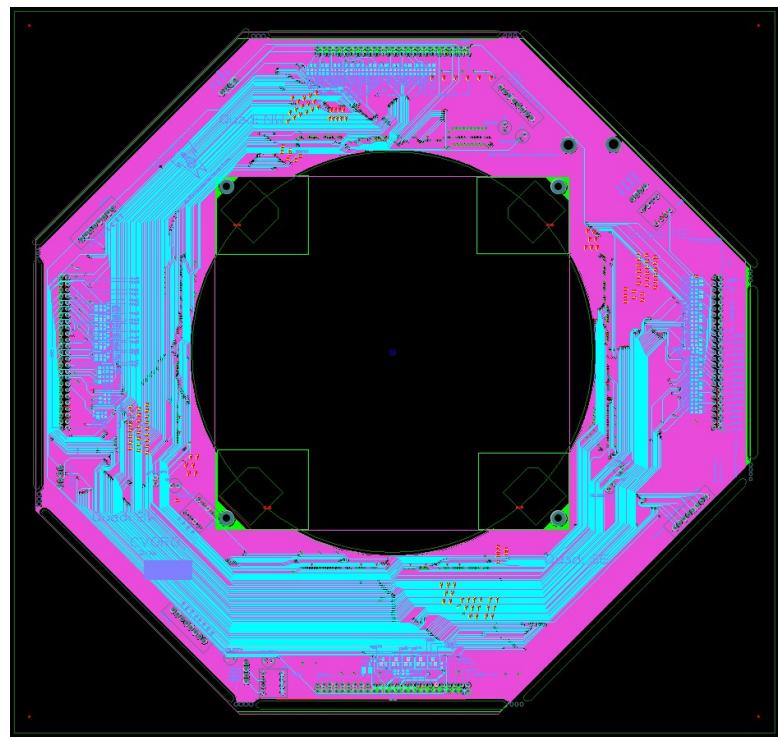


Figure 3.7: Image of the Mogh board PCB Layout.

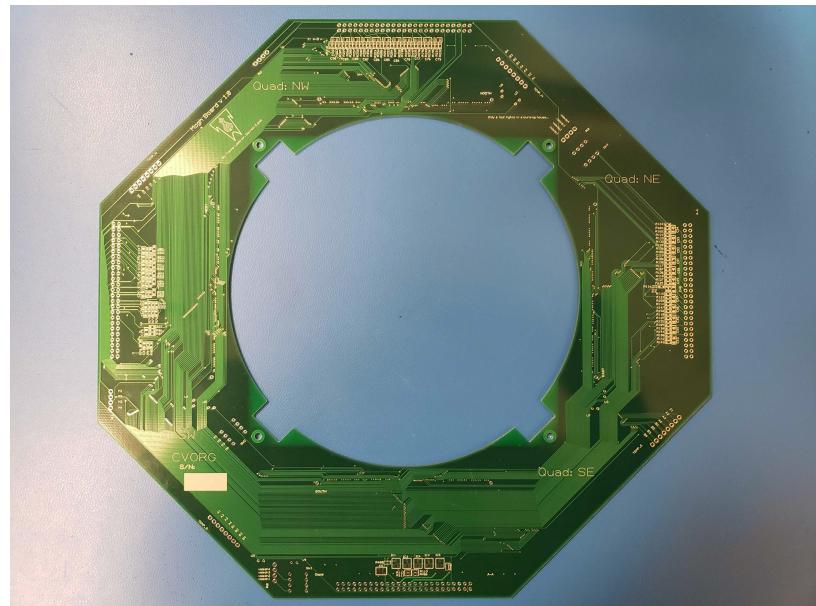


Figure 3.8: Picture of an unpopulated Mogh board.



Figure 3.9: Picture of the top view of a populated mogh board.



Figure 3.10: Picture of the bottom view of a populated mogh board.

## **Chapter 4**

### **MECHANICAL DEVELOPMENTS FOR ADAPTABILITY**

Cryogenic packages are a crucial part for cooling and protecting the SLEDs array and can be very expensive especially when they are custom made. Since the development of SLED's arrays a supporting higher formats that exceed the amount of I/O pins supported by the J.K Dewar; ideally this would make the package obsolete for those systems forcing the group to have to buy more custom Dewar packages to preform test on arrays larger the 2048x2048. A solution is to allow the group to continue utilizing the J.K Dewar was to design and make an adaptor that can fit the HDILED carrier board; while maintaining the enclosures vacuum seal. For this effort, two designs must be made and tested; one of the designs is the J.K/ARS Custom Adaptor and the engineered fit J.K Coldfinger. Both parts are made of 6061 aluminum(Al) material; this material is both cost effective and easier to cut then steel. the machining for both of the parts was done by the Coulburn machinist shop at the University of Delaware.

#### **4.1 JK/ARS Custom Adaptor**

This custom part is designed to act as an adaptor that will allow the J.K Dewars to be able to go past there pin limitations. This will make the package usable in future as the SLED's arrays resolution increases on the chip. As an added touch this design can also fit on both the J.K and the ARS Cryogenic Dewars this will permit the transport of the array between the different cryogenic packages without needing to dismantle the mounted carrier board that holds the RIIC. Providing additional protection to the expensive and sensitive SLED's array. The lid window will protect the front from any accidents such as falling objects while also preventing any undo contact on the board that could cause bending or breaking of the wire-bonds that connect to the RIIC array.

Displayed below in Figure 4.1, is the Solidwork's isometric top view image of the part; and in Figure 4.7, is the isometric bottom view of the part. The hole pattern on the top surface of the part is the same corresponding hole pattern for the ARS package lid with the appropriate O-ring groove to make a seal against the PCB; for further in depth information on test for this can be found in Zachary Marks Master thesis[12]. On the bottom of the part are the hole patterns that the screw holes to attach to the ARS dewar as well as the o-ring groove that fits the circumference of both the bases of the enclosures. The machine shop dimensions schematic can be found in appendix C. In Figure 4.1, is a picture top isometric view of the part itself; while in Figure 4.7 is a picture bottom isometric view of the part.

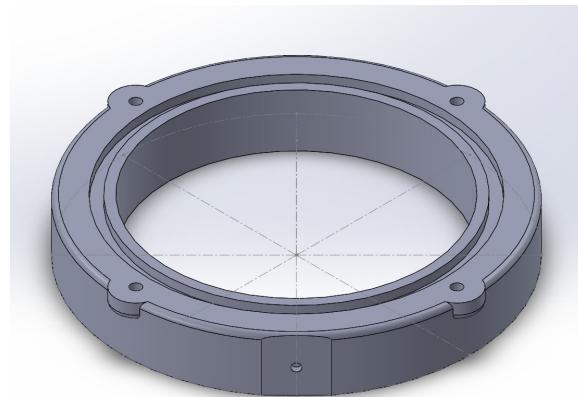


Figure 4.1: Solidwork's Isometric Top view of Dewar Adaptor.



Figure 4.2: Solidwork's Isometric Bottom view of Dewar Adaptor.

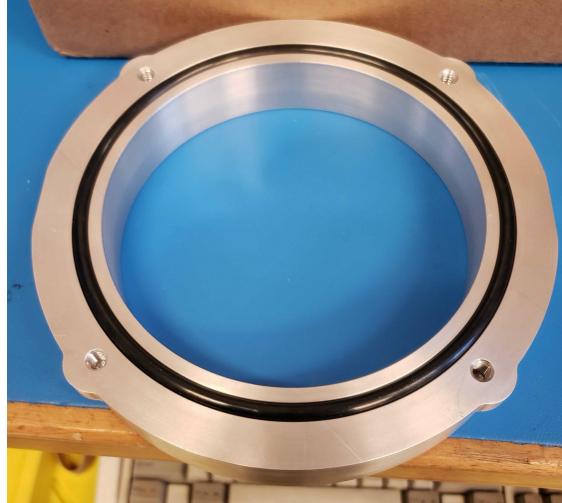


Figure 4.3: Picture captured of an isometric top view of Dewar Adaptor.

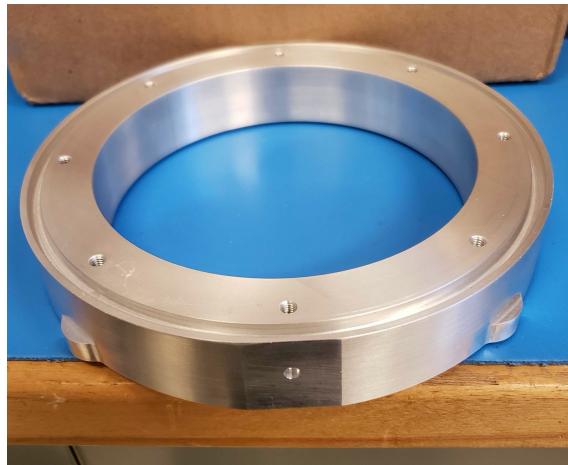


Figure 4.4: Picture captured of an isometric bottom view of Dewar Adaptor.

#### 4.2 JK/ARS Coldfinger

The J.K Coldfinger is used to evenly distribute a coolant liquid to the localized surface area of the array through a copper tungsten (CuW) plate; that is attached through epoxied and small screws to the array back of the array to the board. the SLEDs hybrid is cooled to 77 Kelvin inside the Dewar enclosure. It acts as a form of cold trap for the Dewar that will allow the LN2 to enter and leave the enclosure. This will keep the surface of the chip uniformly cooled when in operation. Due to the level of cold that can reach under cryo-cooled the coefficient of thermal expansion(CTE) or

shrinkage rate of the material has to be considered. The size of an object can change with the change in temperature; for 6061 Al the CTE is 23.6 m/m-C over the range of temperature between 20.0 - 100 C. This is tolerable and has been proven to work with previous coldfinger designs. The base of the part has four holes on the corners they serve as mounting screws from the corresponding mounting holes inside of the enclosure; these can accommodate 6-32 machine screws. The angled cuts are meant to allow easier access to the screw head for dismounting. Height was chosen to match the offset from the opening of the enclosure to the top of the adaptor; keeping in mind the thickness of the CuW as that is between the board and the top of the coldfinger. The pedestal itself at the top of the part is sized to meet the maximum contact area of the CuW plate. At the rounded square head of the part in the corners are mounting holes for standoffs that will be corresponding with the mounting bracket that holds the array in place.

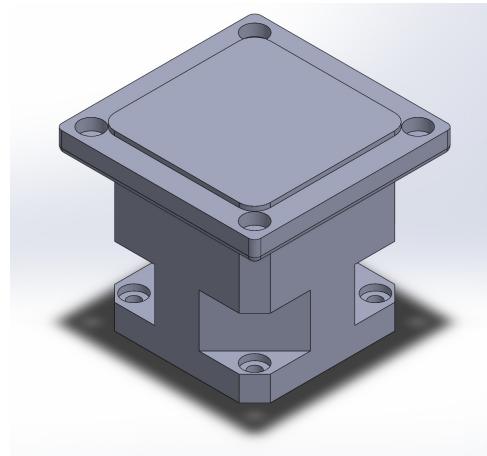


Figure 4.5: Solidwork's Isometric Bottom view of J.K Coldfinger.

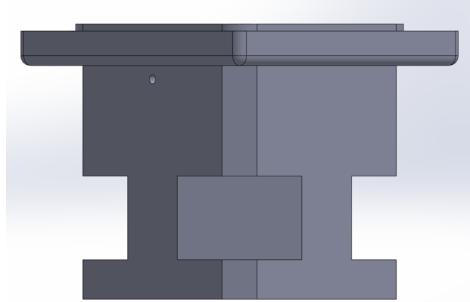


Figure 4.6: Solidwork's Isometric Bottom view of J.K Coldfinger.

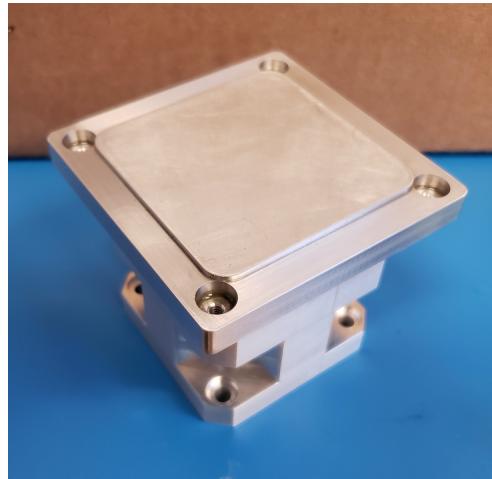


Figure 4.7: Picture of the Isometric Top view of J.K Coldfinger.

## **Chapter 5**

## **RESULTS**

This chapter will be more of a discussion section to the current progress of the development of phase one of the architecture. This will not be an explanation of the designs that can be found in the previous 3 chapters or the schematics in the appendixes.

### **5.1 Board Test Results**

Advanced Circuits manufactured the HDILED Carrier board. The outcome of the boards that they created did turn out very well; except for one flaw. When the order to the manufacture the Gerber file for the back silkscreen was lost in communication with the company and they did not put on the back silkscreen protecting the last conductive layer which is a power plane called vse10V. Therefore, we will add our own insulation to prevent metal to metal contact and board shorting from the exposed sections. An attempt was made to solder the components onto the board ; minus the SLEDs array. However, the pitch on the pins for the high-speed socket type connector were to small to be done by hand and we tried to preform re-flow soldering but were unable to keep from shorting the pins together. Through trial and error the group came to an agreement to have Shore Printed Circuits, Inc. assemble the board. The boards both pass continuity test without mounting the RIIC only array; however there was shorts found between ground and two of the main power planes. The next step was cutting away the wire-bonds from the HDILED carrier board pads. After probing the RIIC itself the shorts were found on the RIIC only die away from the board. Currently, test have been delayed until another die can be re-bonded to the board. In Figure 5.1,

below is picture of a magnified picture though the microscope of one of the wire-bonded corners.

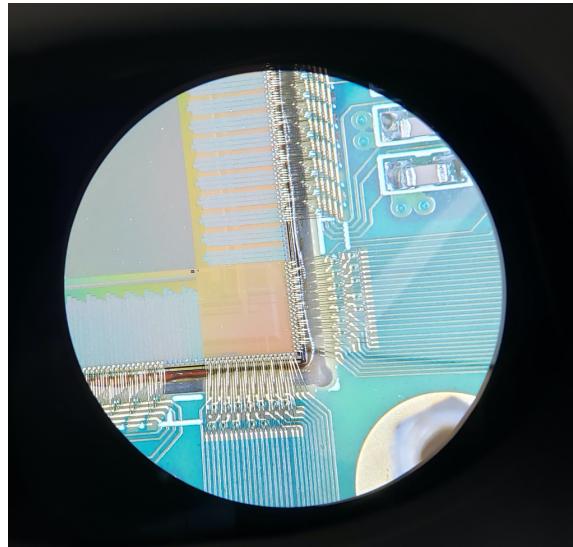


Figure 5.1: Picture of one of the corners of the wire-bonded RIIC only array on the HDILED Carrier board.

## 5.2 Mechanical Test Results

University of Delaware Machinist in the Coulburn machine shop constructed both of the part design's. The JK/ARS Dewar adapter showed promise in mechanically fitting to the J.K Dewar chamber; so did the coldfinger as well. The three seal points for the adapter held when determining the effectiveness of the adapter when assembled to the Dewar and put under vacuum; this can be shown in Figure 5.2. In Figure 5.3, is a picture of both the coldfinger and adapter assembled to the Dewar chamber. The chamber within 5 minutes, the chamber was able to vacuum down to 7.4E-4 hPa at 1500 Hz and when finished can go down to around 5.4E-4 hPa. This is more then acceptable to run the SLEDs system. The next step is to engineer fit the distance between where the coldfinger meets the copper tungsten attached to the array and the top of the adapter which will share the same surface plane as the carrier board; while also fixing minor adjustments to better fit the parts for both cryogenic packages mentioned in previous chapters.



Figure 5.2: Picture of the J.K/ARS Dewar adapter assembled and put under vacuum.

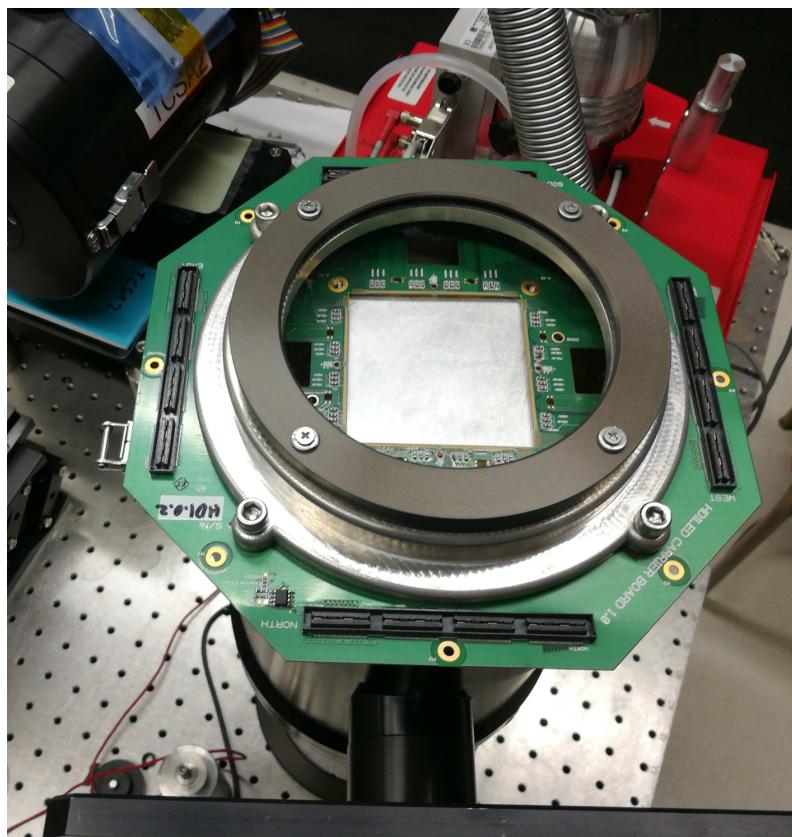


Figure 5.3: Picture of the J.K/ARS adapter and coldfinger assembled to J.K Dewar chamber.

## Chapter 6

### FUTURE BOARD DEVELOPMENT

#### 6.1 Plan for Next Step in System

In future development of IRSP as progress continues on the software side the hardware has to adapt as well to accommodate. Phase on on adapting the framework is to eliminate the bottle neck of the system which are the amount of I/O pins. As the resolutions of the SLED's array are growing larger and large, higher frame rates are needed. With phase 2 of the Empire Layer framework shown in Figure 6.1. By expanding the hardware we will provide room to test different system set ups for higher formatted arrays by creating the possibility of increasing the frame rate and increasing capacity for drive electronics. The next board to be designed for phase 2 will be called the Duras board. This PCB will be the more evolved version of the Mogh; instead of sending the input analog signals coming from the CSE to every high-speed socket connector this board will hold the same passive components to preserve signal integrity by directly routing the 4 original ribbon cable or SMB connectors from the CSE to a socket connector that will control its own quadrant on the chip. This is currently being designed while test are being preformed on the Mogh board. An example of the layout of these boards stacked on top of the yellow colored carrier board is shown in Figure 6.2. Utilizing this board in the next phase I hope to incorporate fellow graduate student Joshua Mark's post amplifier design; this will amplify the analog signals going into the RIIC. Applying an amplifier to the analog signal directly at the RIIC instead of streaming the signal over ribbon cables to the Dewar will lessen the amount of reflections, signal to noise ratio, degradation on rise time due to the cable's length, and crosstalk amongst the other signals.

Phase Two of SLEDs Empire Layer

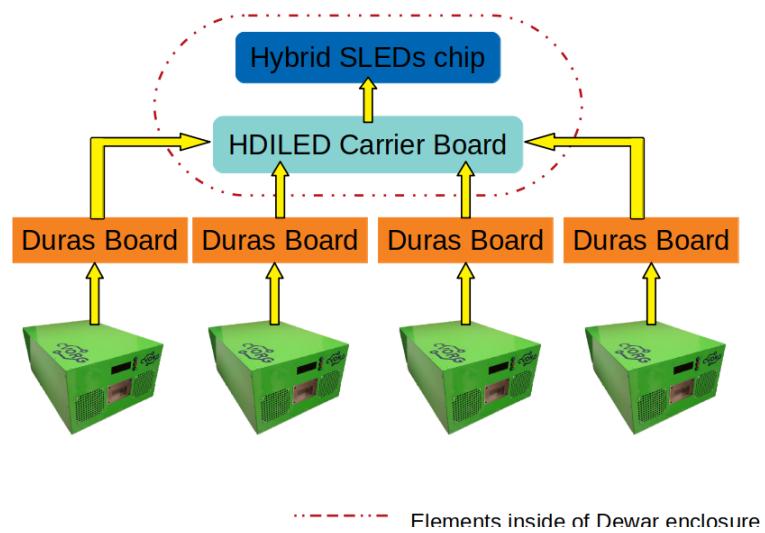


Figure 6.1: Diagram of phase 2 of constructing the Empire layer framework.

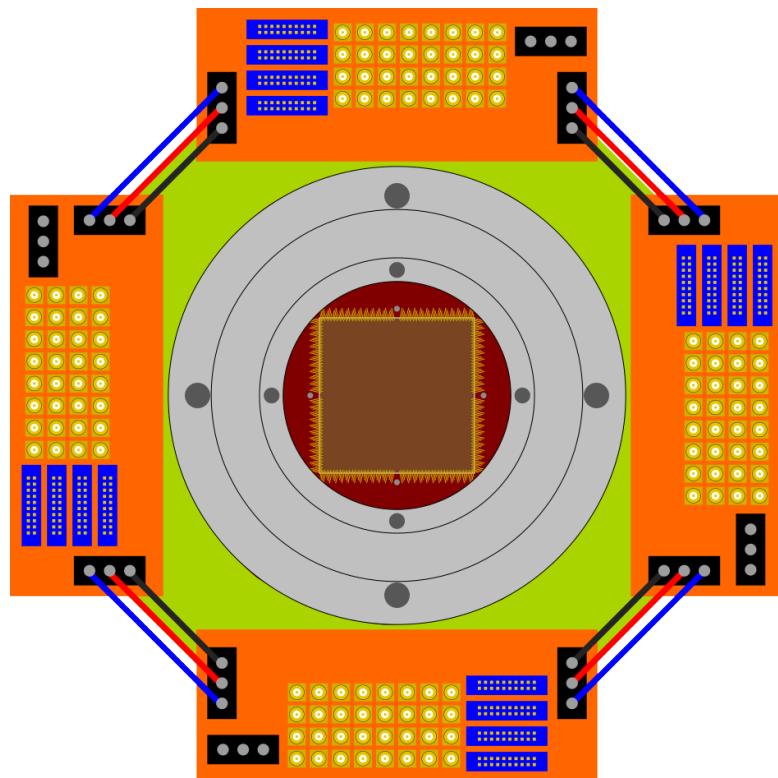


Figure 6.2: Diagram of the layout for the Duras boards.

## **Chapter 7**

### **CONCLUSION**

There are two areas that the CVORG research group will need to improve in order to progress in the development of the hardware for IRSP Systems for higher formatted hybrid arrays. As the need to incorporate higher resolution and hardware modularity with HDILEDs Systems. The SLEDs IRSP system is aimed to be designed for scalability to accommodate multiple configurations for higher-resolution and faster frame rates. In phase one of implementing the SLEDs Empire architecture; the intermediate boards presented in this thesis will assist in bridging the gap of limiting the software architecture and allowing growth for the behavior of the system. This endeavor highlights the design of these boards and the next steps that are needed to test a more direct connection to the hybrid chip signal pads. While providing the growth to test not only higher formatted pixel hybrid arrays but different drive formats for IRSP system setups. This will be a good stepping stone in making the system more compact, improve signal integrity, and improve the drive performance of the system. In the future, we hope to start testing and integrating the phases for the new SLEDs Empire hardware architecture to evaluate its integration into the system.

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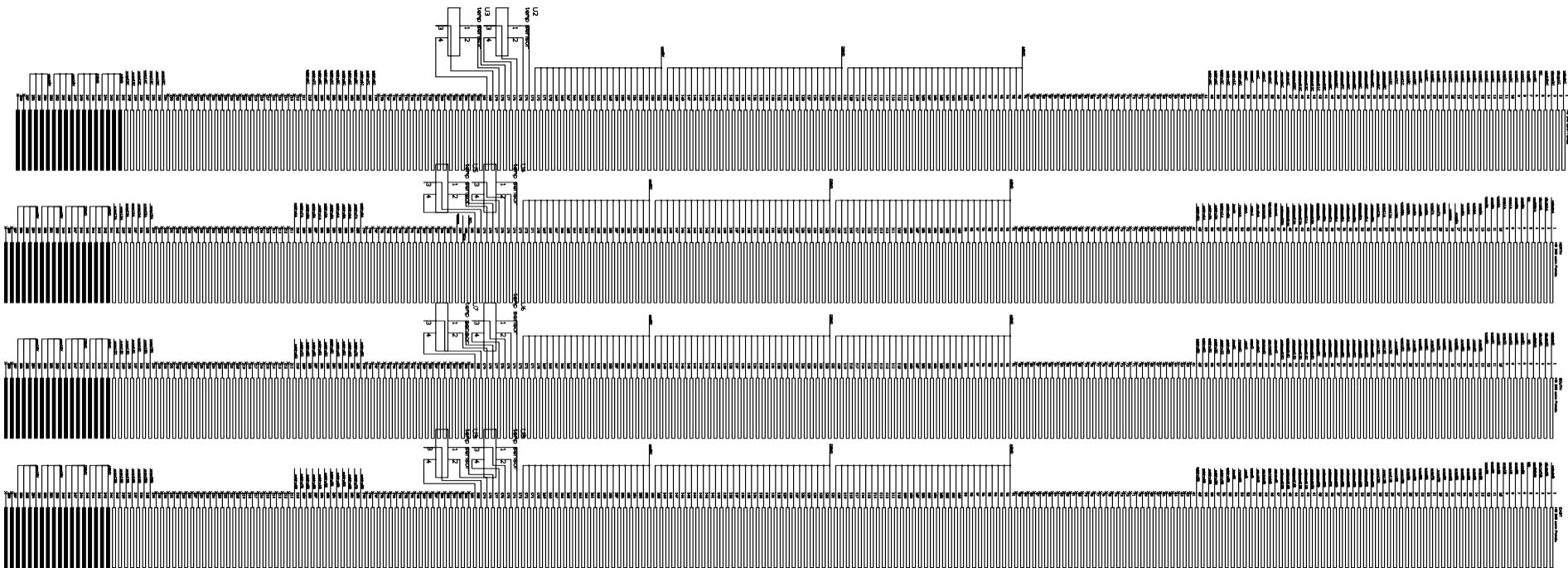
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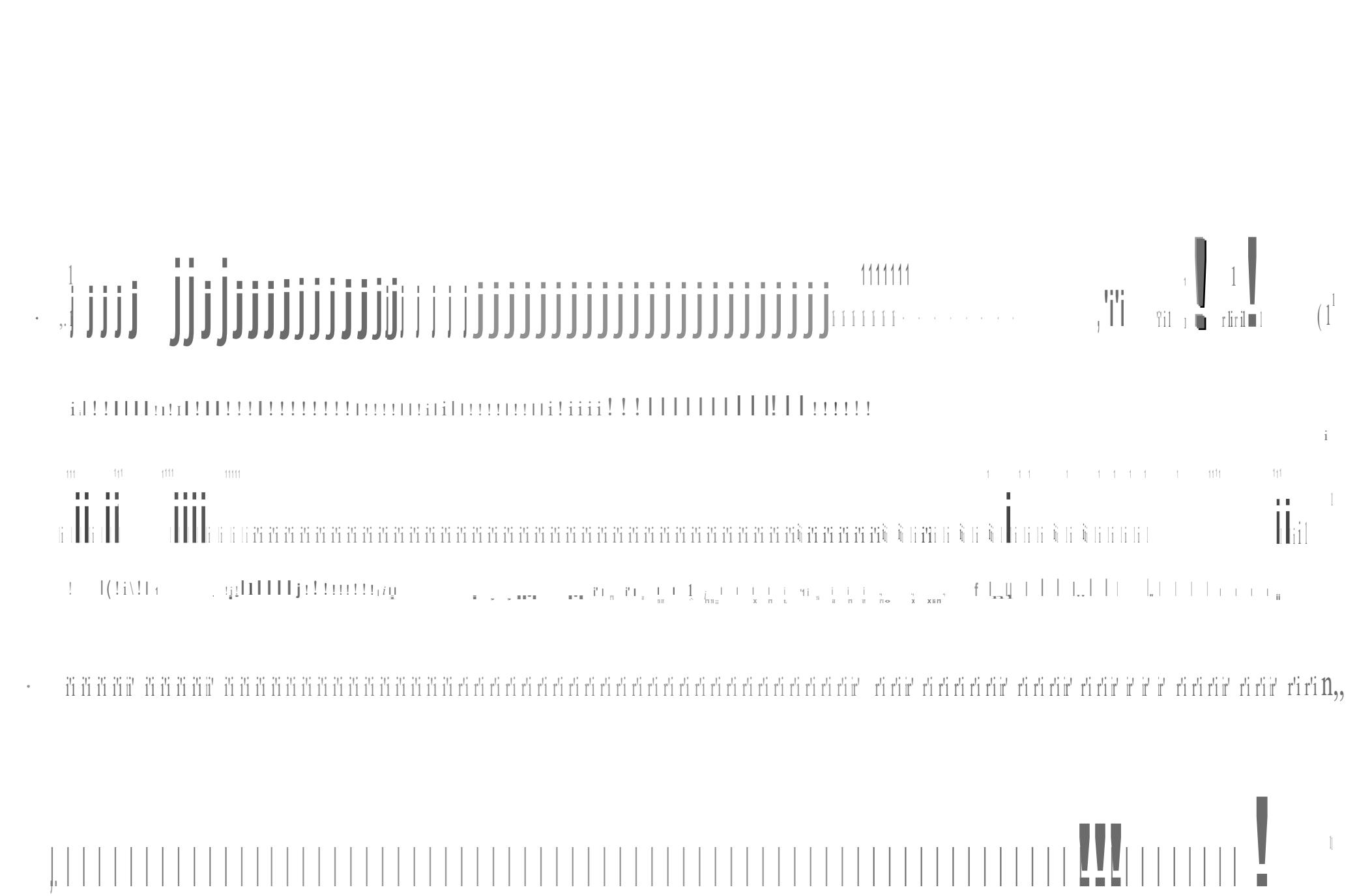
## **Appendix A**

### **HDILED CARRIER BOARD SCHEMATIC'S**

In this appendix are the Schematic's for the new HDILED SLED's Carrier Board.

1. HDILED Carrier board general schematic.
2. HDILED Carrier board schematic of corner pads.
3. HDILED Carrier board schematic of power rails.
4. HDILED Carrier board schematic EEPROM circuit.







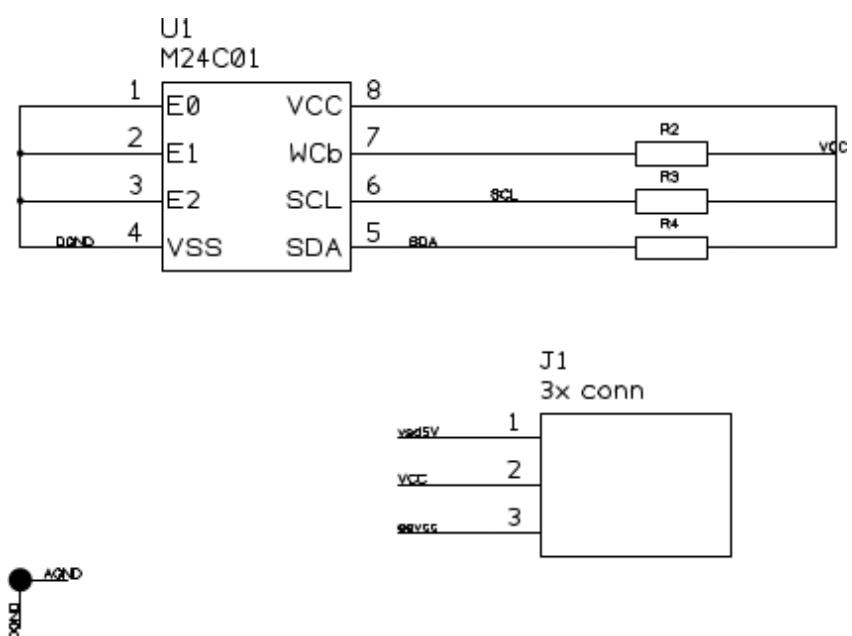
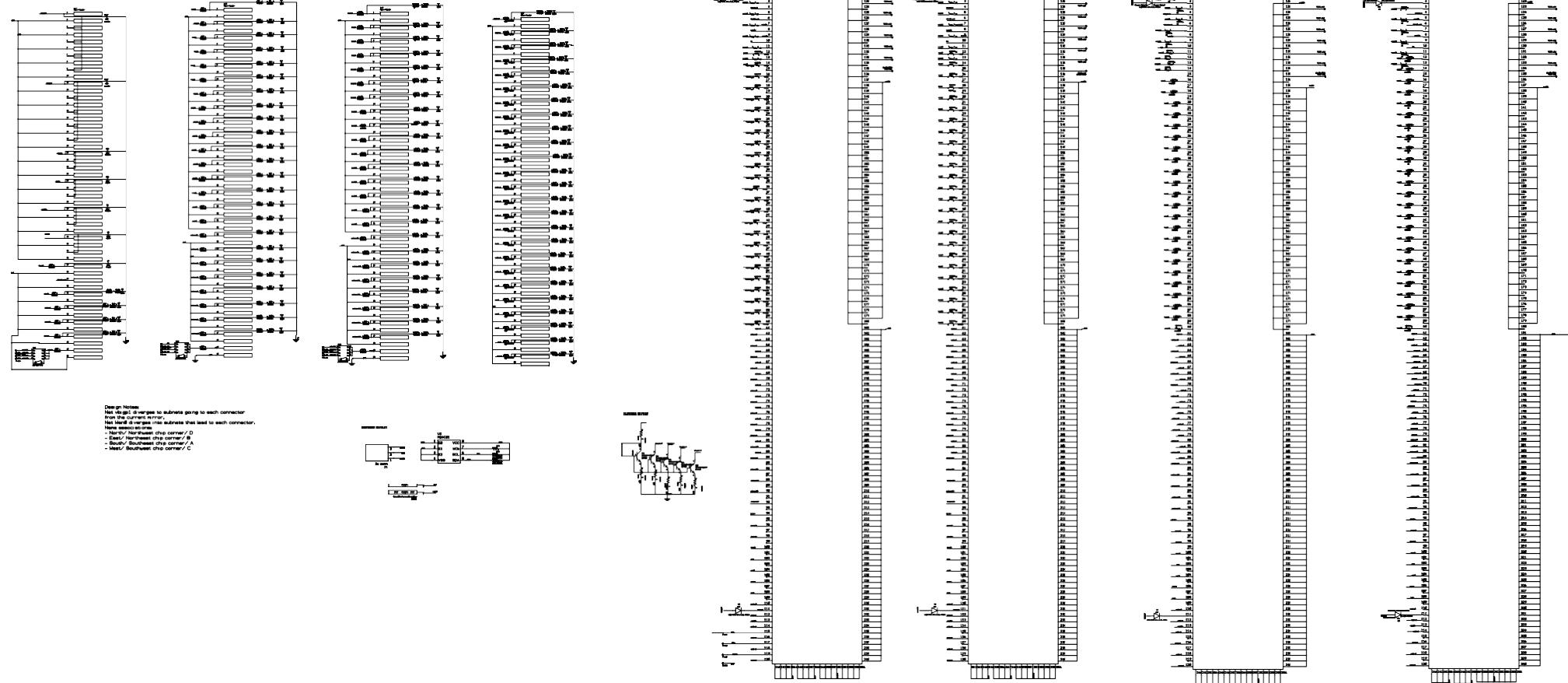


Figure A.1: HDILED Carrier Board EEPROM Schematic.

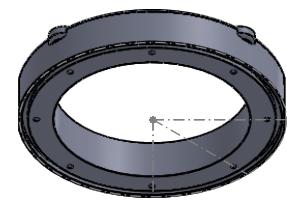
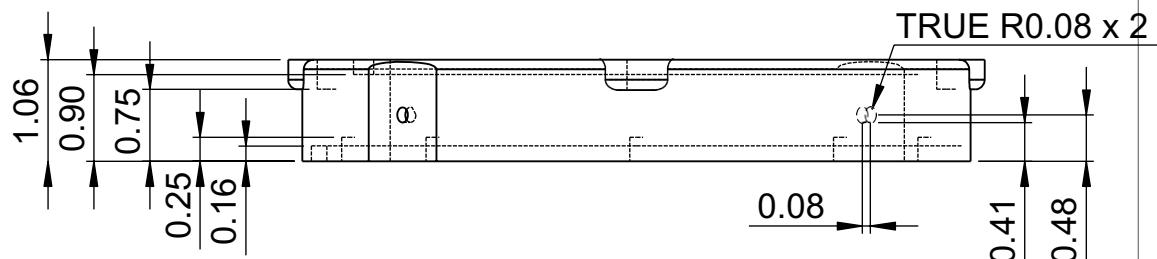
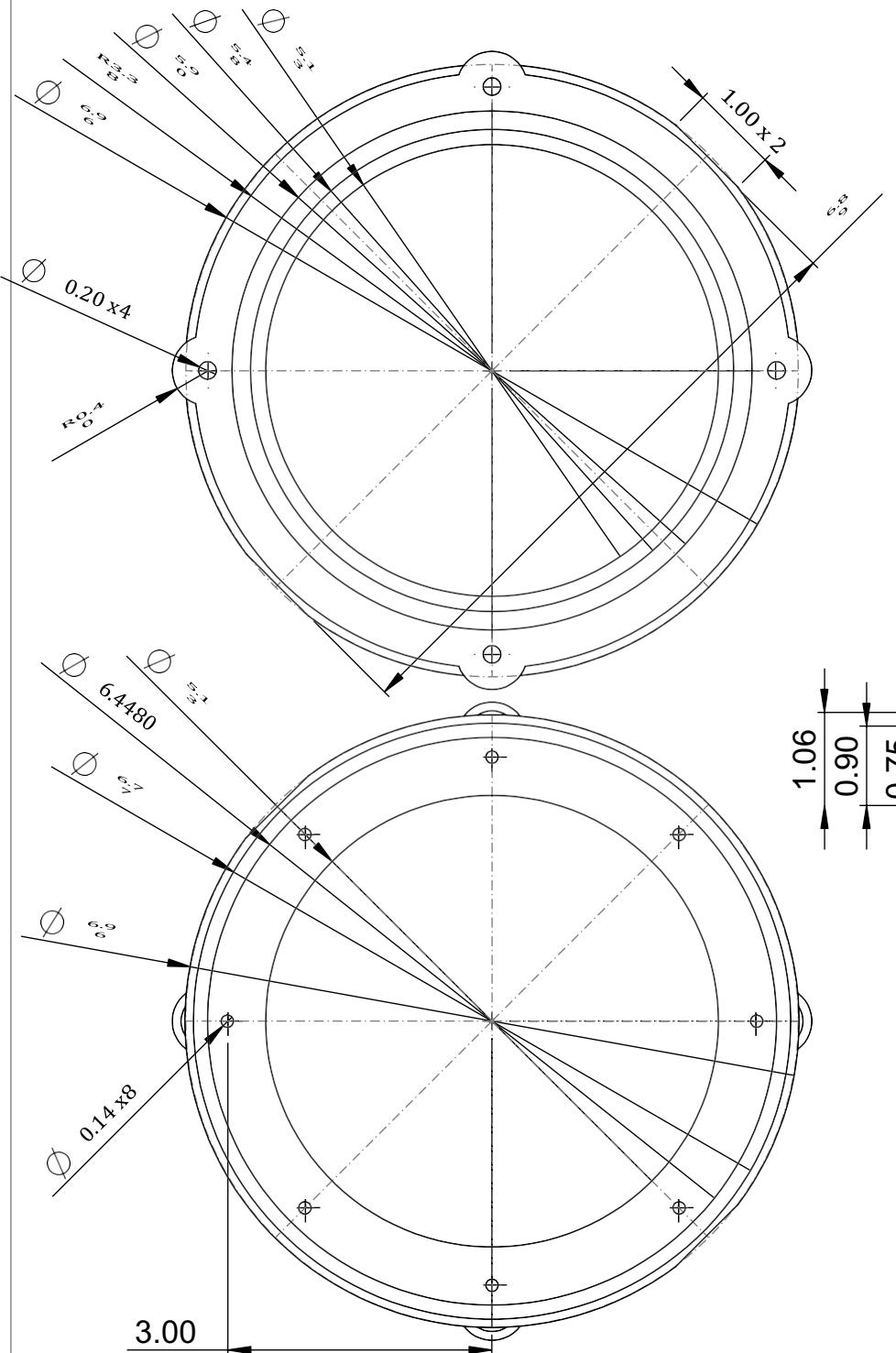
**Appendix B**

**HDILED MOGH BOARD SCHEMATIC**

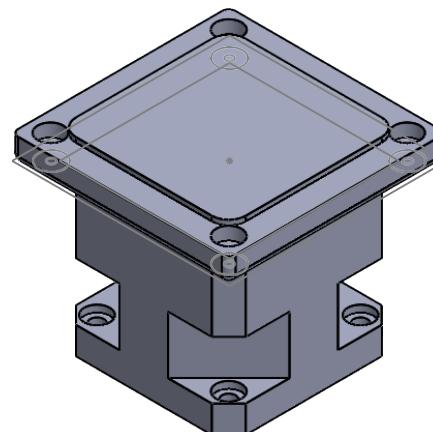
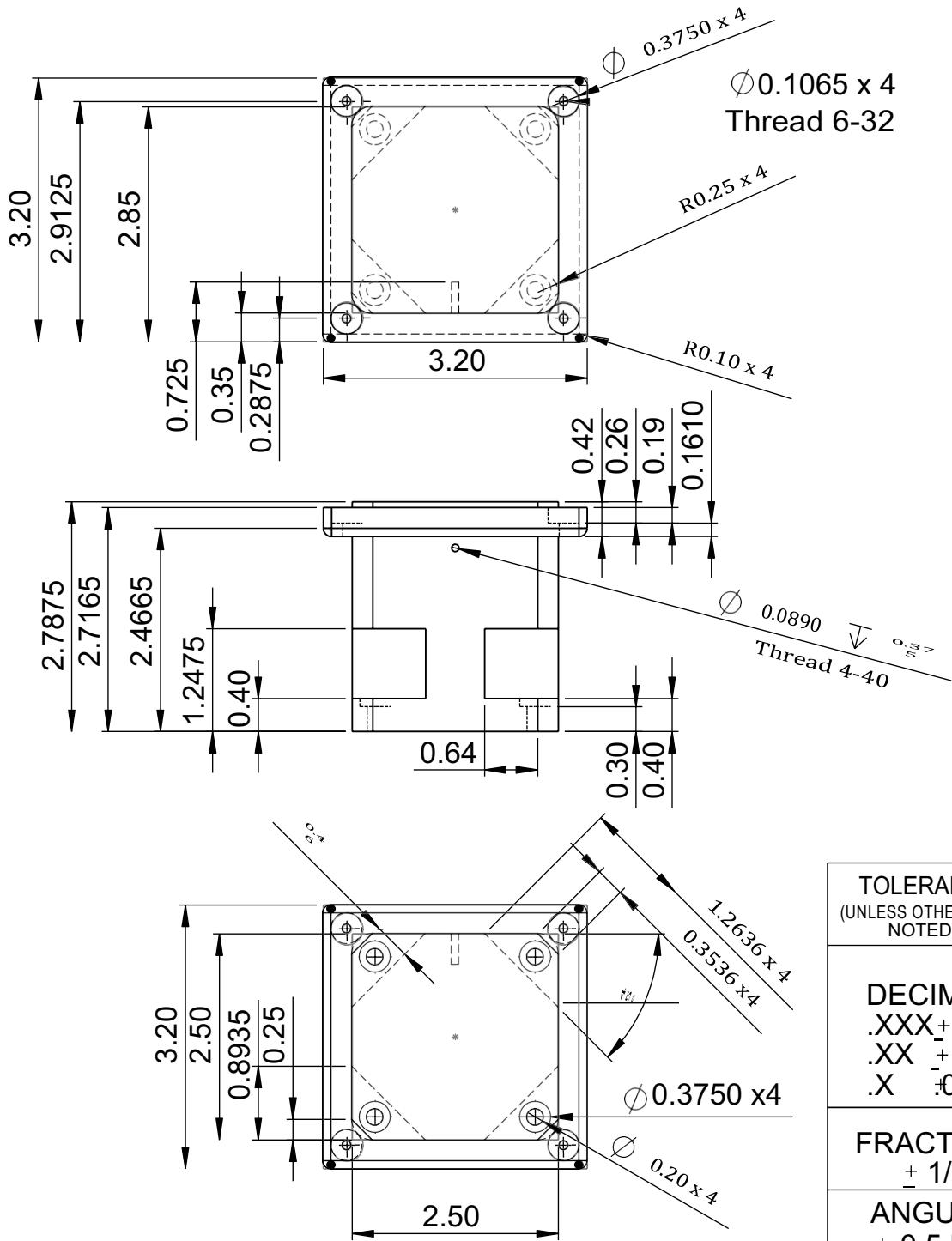
INTERFACE BOARD INPUT SIGNALS



**Appendix C**  
**MECHANICAL SCHEMATIC'S**



TOLERANCES (UNLESS OTHERWISE NOTED)	PROJECT OR CLASS: CVORG - SLEDs	
DECIMAL .XXX .005 .XX ± .010 .X + .050	DRAWING TITLE: JK/ARS Dewar Adaptor v1	DATE:
	DRAWN BY:	DATE:
	CHECKED BY:	DATE:
FRACTIONAL + 1/32	APPROVED BY:	DATE:
ANGULAR ± 0.5 DEG	MATERIAL:	QUANTITY:
	SCALE:	DWG NO:
	BILLING ACCOUNT:	



TOLERANCES (UNLESS OTHERWISE NOTED)	PROJECT OR CLASS: CVORG - SLEDs	
DECIMAL .XXX + .005 .XX + .010 .X + .050	DRAWING TITLE: JK coldfinger v1	DATE:
	DRAWN BY: Tianne Lassiter	DATE:
	CHECKED BY:	DATE:
FRACTIONAL + 1/32	APPROVED BY:	DATE:
	MATERIAL:	QUANTITY:
ANGULAR + 0.5 DEG	SCALE:	DWG NO:
	BILLING ACCOUNT:	