

**DESIGNING A MODULAR TESTING PLATFORM FOR
DIGITAL-TO-ANALOG SIGNALS**

by

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Semester Year

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ACKNOWLEDGMENTS

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ABSTRACT

Chapter 1

INTRODUCTION

1.1 SLEDs Background

Infrared imaging and detection is used in various industries and services around the world. Since infrared light exists outside the human-visible light spectrum, it requires specialized hardware and testing procedures to ensure proper performance. Infrared applications generally require high speed and precision, which means that testing infrared systems is a vital step in ensuring their success.

A system must be "statically" and "dynamically" calibrated with an accurate infrared source. A static calibration only requires scientific test equipment to measure radiance. Dynamic calibration is much more involved and requires a thorough understanding of the system in question. To dynamically test, the system is placed under more realistic and changing conditions, such as having to react appropriately to moving objects or images. A common solution for this need is the Infrared Scene Projector (IRSP) which can be used to project infrared images and video to test a desired device.

IRSPs display realtime IR scenes that simulate true IR signals for their targets. Since infrared depends on physical information (temperature), simulating this as a signal requires specialized hardware. This hardware is used to turn commands from the users into analog display signals as well as read feedback from the display device and adjust its own parameters accordingly. This "hardware-in-the-loop" approach can allow a system to accomodate for various physical effects or issues within the display. Since infrared displays are analog devices, they cannot be precisely analyzed without some sort of readback and processing to view output. A typical system design is shown below.

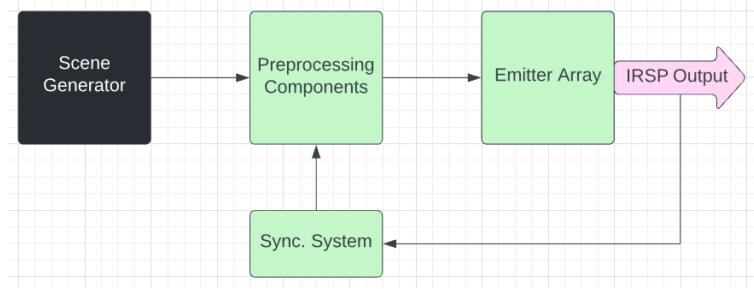


Figure 1.1: General IRSP architecture

Testing is one of the most important aspects of any system design, as it is the bottleneck for how many reliable systems can be built & validated. This work consists of a new approach to manually test the high-speed analog amplifier circuits within the system, as well as considerations & redesigns for the next generation of these devices.

1.2 Motivation

IRSPs can be characterized by multiple factors, of which two of the most important are frame rate and output temperature range. Frame rate can be described as the number of discrete outputs from the display device per second. The frame rate is directly tied to the rise time of individual pixels, which is fully dependent on the display architecture and physical properties. The temperature range represents different "colors" or ranges of IR light that the projector can display. An ideal device has both high refresh rate and high max temperature to overcome the challenges of temperature-based projection. [7]

Much of the IRSP market is dominated by resistor array devices. By heating up resistors (mapped to each pixel) to specific points with controlled current input, the device can simulate temperature output for an infrared image. The use of resistors limits the benefits of this approach, however. [3] Resistor arrays depend on raising temperatures to the actual desired temperature of the projected image. While innovative, resistors cannot dissipate heat quickly, limiting their rise time. The characteristics of the resistors are a hard limit on refresh rate, forcing most designs to stay under 500Hz. Additionally, higher projected temperatures will further increase the rise time, since

the resistors will have to physically cool down from this temperature level. By limiting the max temperature output, designers can ensure that pixel rise time will consistently stay within a certain range.

Since 2008, CVORG has been at the forefront of developing an Infrared LED-based IRSP with a full suite of custom hardware and software control. [1] The success of the current iteration of the system has allowed us to continue researching improvements and changes to the system that would further expand on the technology's potential. Our technology is now targeting a 1024 x 1024 display at 2KHz.

After successfully developing the technology to a certain point, it was considered stable enough to reproduce and iterate on. The process of building and testing each component of the system provides one with an intimate knowledge of the functions and requirements of individual hardware components, as well as limitations to be targeted later.

One of the most important links in the system's chain consists of the digital-to-analog conversion and subsequent amplification. These amplified analog signals are used to drive the display, making their functionality and speed a top priority. [6] As such, it was imperative to create reliable testing procedures for such components. The relevant systems, components & design methodology for this portion of the system will be described in detail below.

Chapter 2

SYSTEM OVERVIEW

Using a combination of digital commands and analog signals users can precisely command and utilize the display at the high frequencies required by the application. The system has been developed over the years to be user-friendly and configurable for many different applications. The associated technologies will be briefly explored below.

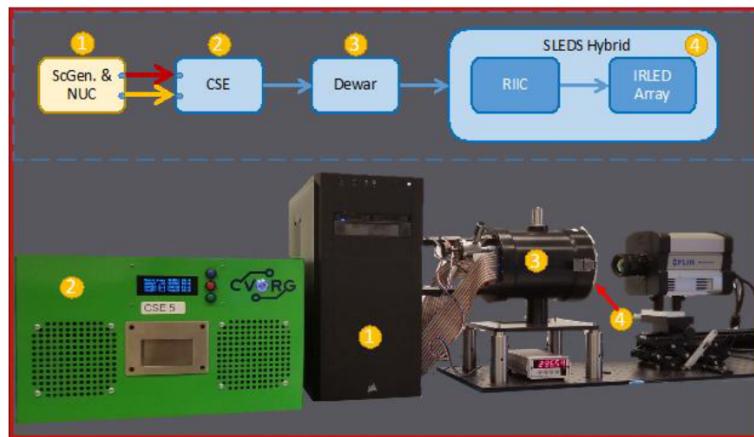


Figure 2.1: SLEDS IRSP Overview

2.1 SLEDS Array

As mentioned before, infrared projection requires high-speed analog signals and full user control. The LED array itself is hybridized to a Read-In Integrated Circuit (RIIC), a 10V chip which is digitally instructed by a close-support unit. This hybridized unit in its temperature-controlled enclosure is referred to as the Dewar. The first iteration of this LED array named SLED (Superlattice Light-Emitting Diode System)

was constructed in 2008 with a resolution of 68 x 68 pixels. In this early stage, no driver had yet been developed to control the RIIC. [5]

To drive such a complex analog device, specialized electronics and communication are required to turn human commands into infrared signals. The first drive system for the SLED array was developed in 2011 and helped lay the groundwork for the next iteration of SLEDS, consisting of a 512x512 display and 48 micrometer pitch size.[5]

Further versions of SLEDS were created over the years to fulfill different requirements. TCSA (Two-Color SLEDS Array) was developed in 2016 and capable of driving the LEDs at two separate wavelength bands. NSLEDS (N3 Superlattice LED System) was also developed around this time. This array was capable of driving a 1024x1024 display for the first time. The next advancement, HDILED (High-Definition Infrared LED) was the first 2048x2048 display in the world when it was finished.

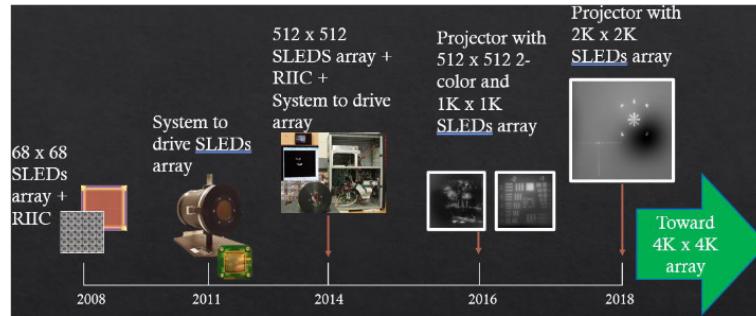


Figure 2.2: SLEDS Timeline

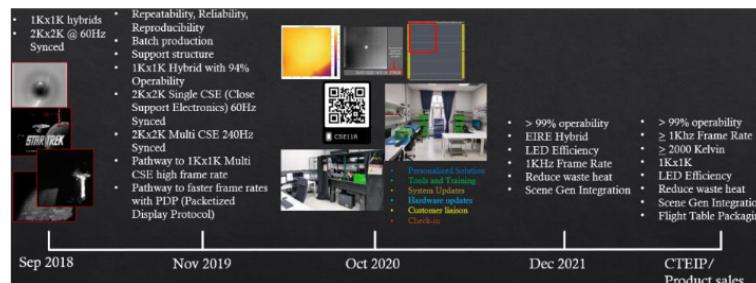


Figure 2.3: SLEDS Timeline, Part 2

2.2 RIIC Overview

The RIIC is a 10 volt IC that is hybridized with an array of IRLEDs to directly drive them using CMOS logic. A dual-circuit system allows the array to display at different dynamic ranges, a "weak gear" and "strong gear". Each pixel is driven by a

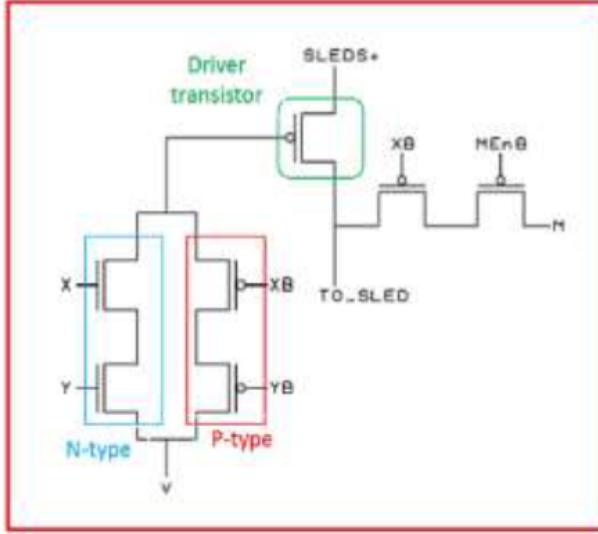


Figure 2.4: Single Pixel RIIC Schematic

strong/weak pair of NMOS transistors, which do not take up as much space as PMOS and allow for greater resolution as a result.

The RIIC is divided into four quadrants that can be individually commanded. Due to the nature of the driver firmware that will be discussed later below, this quadrant approach allows great control over the display. [4] Each quadrant has 2-32 input channels depending on the desired configuration. Configuration is performed using an SPI register on the RIIC, shifting in data when commands are received.

2.3 CSE Overview

The RIIC/LED hybrid is driven by a close-support electronics system, or CSE. While the CSE was a response to the need for a RIIC driver, it is also the culmination of many years of work and development. The system architecture consists of an FPGA, DACs, Amps, and I/O boards. This array of hardware completes the loop from a user on any PC to the IRLED array, making the projector a viable product. This hardware

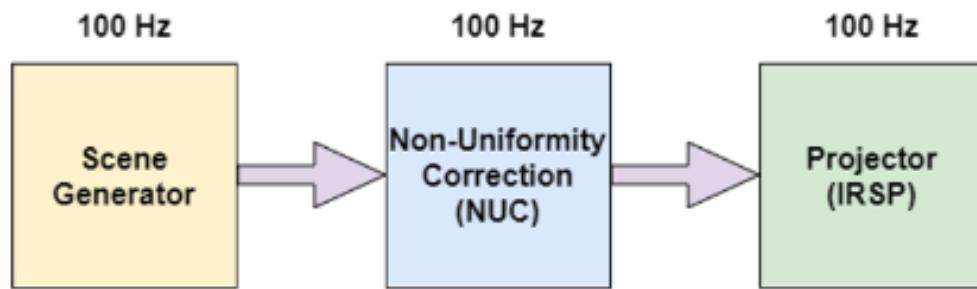
has been redesigned and iterated on for years, and is now being fully upgraded to a second revision consisting of smaller components and more efficient signal integrity strategies.

2.4 Scene Generation and NUCPC

The final ingredient necessary in the IRSP chain is the Scene Generator. While scene generation technology is far beyond the scope of my work, a general overview is necessary to understand the system. A scene generator is to the projector what a media player is to a television. Most of these scene generators are proprietary black boxes, documented by the creators to be sold to end users [5] Scene generators can communicate over nearly any physical interface, but the standards must be agreed upon between the manufacturer and user. A common display protocol is DVI, as it is fairly well documented and easy to understand. HDMI is another possible choice, but it is a more complex and less openly documented standard.

To generate a scene, a GPU is usually necessary to create images and transmit them over the chosen display protocol. The generator will use frames created on the GPU to send over to the IRSP. The next step is called "Non-Uniformity Correction," which is the process of analyzing predetermined output from the IRSP to determine radiance properties of each pixel. Pixel data is placed into a table used by the scene projector and used to accomodate for irregularities in the LEDs. These irregularites are nonlinear which is why they require analysis and writeback rather than simple algorithmic correction. Once the NUC process is complete, the desired images can be projected onto the display device.

Since our research group did not have access to a proprietary scene generator, they developed a pseudo-scene projector using what was dubbed a Non-Uniformity Correction PC (NUCPC). This NUCPC is connected to the CSE through HDMI, and image data is generated by an Nvidia graphics card[5].



All components of this process operate at the same speed and resolution.

bandwidth	$= \text{resolution} * \text{bits} * \text{fps}$
<i>resolution</i>	: number of pixels (including blanking)
<i>bits</i>	: number of bits per pixel
<i>fps</i>	: frames per second
bandwidth	: bandwidth requirements in bits per second

Bandwidth requirements of a scene projector using a traditional display protocol.

Figure 2.5: Example scene generator in IR system

Chapter 3

PDP VS. CONVENTIONAL DISPLAY PROTOCOLS

3.1 DVI & HDMI

Early scene generators used the DVI protocol, which is a simple and well understood standard. Unfortunately, they are also quite large connectors that did not fit well into the CSE design. For this reason, HDMI was chosen as the display protocol for NUCPC to CSE. HDMI uses the same electrical levels as DVI which kept it compatible with preexisting scene generator technology.

While they are good solutions, these display protocols are also rather limited. They are forced to remain compatible with even older protocols such as VGA. An example of typical display function is shown below. Video data is sent in sequential horizontal lines. Once the boundary of the display is reached, a "blanking period" is entered to reset the device's row/frame. The blanking period is recognized by a sync signal, which means that bandwidth is required for non-video data. If blanking periods were able to be reduced, it would inversely increase the potential frame rate.

Fixed frame-rate display protocols are also inherently limited. If a new frame is not necessary, the last frame will be retransmitted. Bandwidth is static which is useful for the reliability of consumer products, but less useful for a high-speed infrared projector. As such, utilizing the potential bandwidth of HDMI became a top priority and the foundation for the CSE firmware.

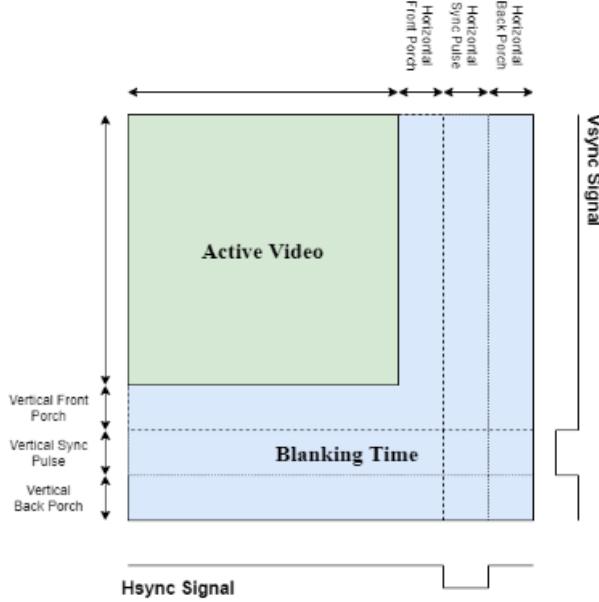


Figure 3.1: An example of timing in display protocols

3.2 PDP

The Packetized Display Protocol (PDP) is the communication protocol for the CSE to LED array. The initial vision for PDP consisted of a "physical layer agnostic method of pixel data transmission capable of providing and addressing latency guarantees while maximizing bandwidth utilization" [2]. Unlike traditional display communication protocols, PDP does not operate on entire display frames, and instead splits any projected scene into regions known as sub-frames. These sub-frames can be written to individually, greatly increasing bandwidth utilization and allowing for high frame rates beyond any traditional HDMI connection.

Sub-frames are marked by the PDP firmware with packets denoting their x and y coordinates. PDP communication packets will then consist of a packet header for draw location followed by the desired data. This divide-and-conquer strategy allows the NUCPC to only send frames when they require updates and therefore update relevant subframes at much higher frame rates than normally possible [5]. IRSP is an incredible application for this concept, as many scenes only have small regions that require updates. An example scene may contain a subframe changing at 200Hz,

another at 50Hz, and yet another remaining static. Over a traditional display protocol, displaying any of these regions at the appropriate rates would be impossible due to the entire frames being sent at preset intervals. PDP, however, allows the NUCPC to utilize far more HDMI bandwidth to only send packets relevant to the subframes.

Table 1 Examples of PDP Packets

Name	Type ID	Type Specific Fields					
Ignored	0x0						
Draw Region	0x1	X start	X end	Y start	Y end	Data	
Array Reset	0x2	Quad mask					

Figure 3.2: Brief example of PDP Packet

PDP can be used in two modes. The method of splitting and refreshing subframes is known as "streaming mode". Users may also opt to use it in a typical display mode where the entire frame is sent at a fixed refresh rate. This is known as "backwards compatibility mode". While there is nothing innovative about this mode, it is necessary to maintain compatibility with existing scene generation technology.

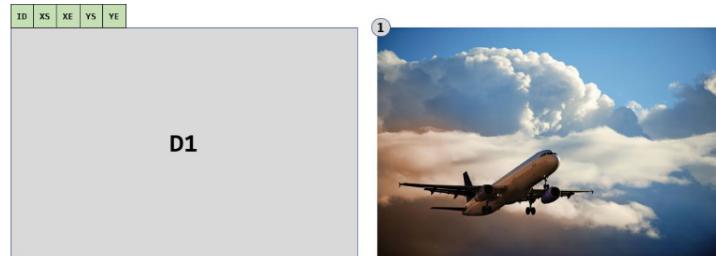


Figure 7 PDP Backwards Compatibility Mode

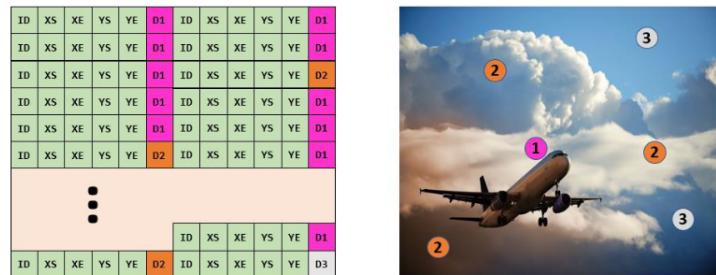


Figure 8 PDP Stream Mode

Figure 3.3: Example of packet organization in each mode

PDP was previously described as being "physical layer agnostic" [2]. The protocol can theoretically be implemented over any physical medium such as DVI or ethernet. The initial implementation utilized HDMI to maintain compatibility with existing technology, but a future revision is moving the physical medium to SFP+. Improvements to the CSE hardware will be briefly discussed in a later section.

Chapter 4

CSE ARCHITECTURE

4.1 CSE Hardware Overview

The CSE is comprised of two gigabit-speed input cards, a mainboard powered by an FPGA, eight DACs connected to the FPGA, eight amplifier cards (one for each DAC) and a pair of interface boards [5]. The input interface cards have HDMI I/O ports and connect to the NUCPC or external scene generator to receive input. Each interface card is connected to the main FPGA via FPGA Mezzanine Card (FMC) slots. The FPGA is host to a MicroBlaze soft processor and uses its eight remaining FMC slots for DACs. Each DAC outputs to an amplifier card, creating the analog driving inputs for the RIIC. All amplified signals are routed out through the interface board to be connected to the RIIC through ribbon cables.

4.2 Datapath

Once the scene generator provides video input, the HDMI cards decode and send the video stream to the FPGA. Since the FPGA uses a soft processor, it can be interfaced with in C to control registers [5]. The processed data is then distributed amongst the eight DAC slots in accordance with the packets defined by PDP. Each DAC card holds two dual-channel DAC components for a total of 32 channels. Once the digital input has been converted to analog, the amplifier cards boost the output and send it through the interface boards. Each interface board has power input from a PSU and power output for the DACs and Amps, and also contain boost components to convert the 2.5V amplified output to 5V for the RIIC to read.

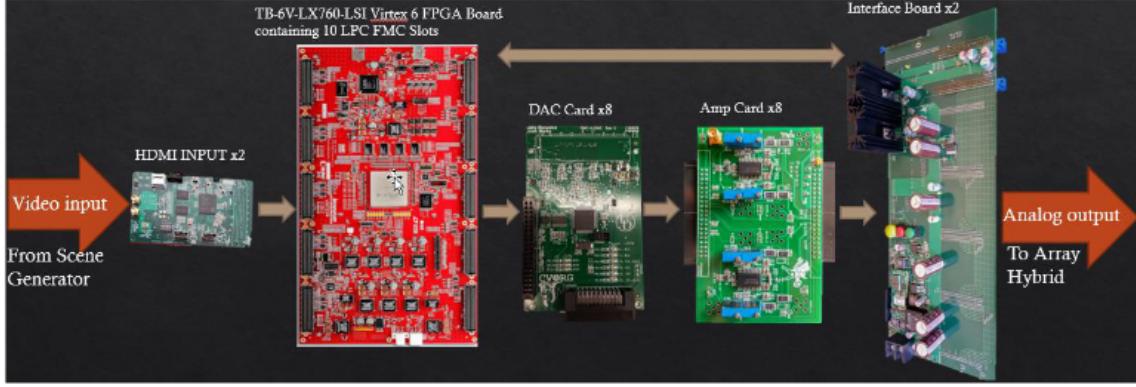


Figure 4.1: CSE Architecture Overview

4.3 Hardware Revisions & System Upgrade Plans

After many years of development, the CSE reached a level of maturity to be considered a cohesive product (internally dubbed Nessie). Due to ever-increasing requirements from customers and breakthroughs in the technology, the group has moved to target a multi-CSE platform capable of each driving a quadrant of an array (now known as Nessie2). By increasing the number of output machines, frame rates can be quadrupled and resolution can be doubled [5]. To compare, the previous system (CSE + SLEDS) would effectively be one quarter of this entire setup. The main challenge facing the system architecture is proper synchronization, as this is vital to ensure all quadrants are being controlled in the same time domain.

Another major change coming to the system architecture is the placement of all analog systems onto the Dewar enclosure rather than inside the CSE. This means the CSE will only handle digital video conversion, and send these values to amplifiers directly on the Dewar. The overall datapath will remain the same with a scene generator interfacing with the FPGA through an SFP+ interface. The FPGA will distribute video data amongst the DACs and then routed outside to the Dewar to be amplified and read. Plans for the Nessie2 amps based on lessons learned from the Nessie1 amps will be discussed later.

Chapter 5

CSE ANALOG COMPONENTS

5.1 Analog Circuit

In order to develop a better testing procedure for the current amplifier circuits as well as begin development of the next generation, some exploration of the initial designers' writing was required. Analog output from the CSE was addressed to each pixel of the IRSP. Due to the sensitive nature of digital-to-analog communications and the unique load requirements of the system the entire system architecture had to be measured and mapped out. To do so, the system was split into various sections representing gain and load stages. [7]. The first stage (DAC Buffer) was responsible for terminating the differential output of the DAC and turning it into a single-ended signal. The next stage was the Cable Driver, a gain stage which was responsible for driving interface board communication and ribbon cable signals. This stage provides some, but not all of the voltage gain required to drive the RIIC from 0-5V. The ribbon cables would output to the final stage known as the Dewar Driver. This stage provides the remainder of the gain required to drive the RIIC at 5V. The Dewar output stage was a 10nF load and required a 0-10V swing from the amplifiers.

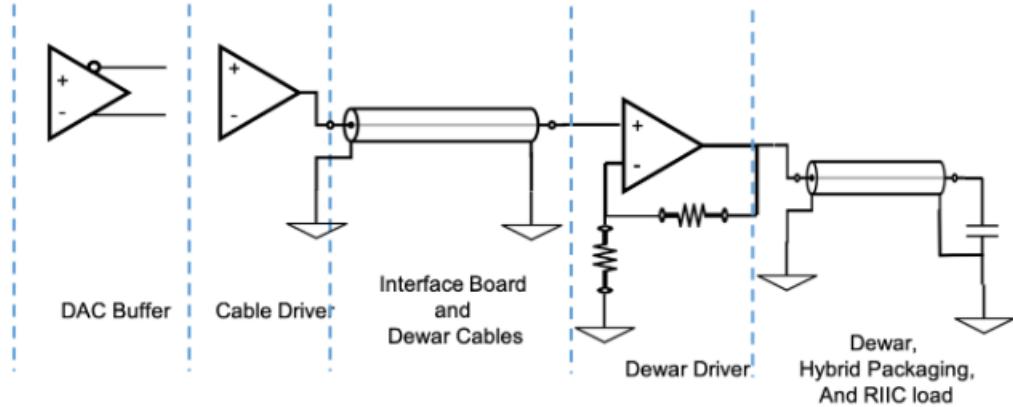


Figure 5.1: High-level schematic of the analog gain & impedance stages

5.2 Understanding the Requirements

To properly test, validate and repair the amp cards, one requires an understanding of the card's place in the system. The card was responsible for passing digital-to-analog converted signals with 16-bit resolution at high speeds, and any issues would be directly visible in the projected video. The amp card received inputs from a 16-bit DAC with a 250 Megasamples per second output [7]. For digital information to be properly decoded as an analog signal, the converter must settle on values at an acceptable speed with negligible margin of error. As bit resolution increases, the margin of error should decrease.

5.3 Settling Time

In any digital-to-analog system, designers must account for physical characteristics of electronics. Every DAC has a delay between input and response, known as Delay Time. The DAC then enters a Slewing period, where it tries to approach the target current or voltage output as fast as possible (current level in the case of our specific DAC). As the DAC approaches the target, slope decreases and the DAC oscillates between over- and under-estimates of the value until finally settling on a DC output. While an ideal DAC will settle on a precise output, most DACs will continue to oscillate between values if it is unable to discern their mean, especially in practical situations. The mathematical account of this phenomenon is called the Error Band.

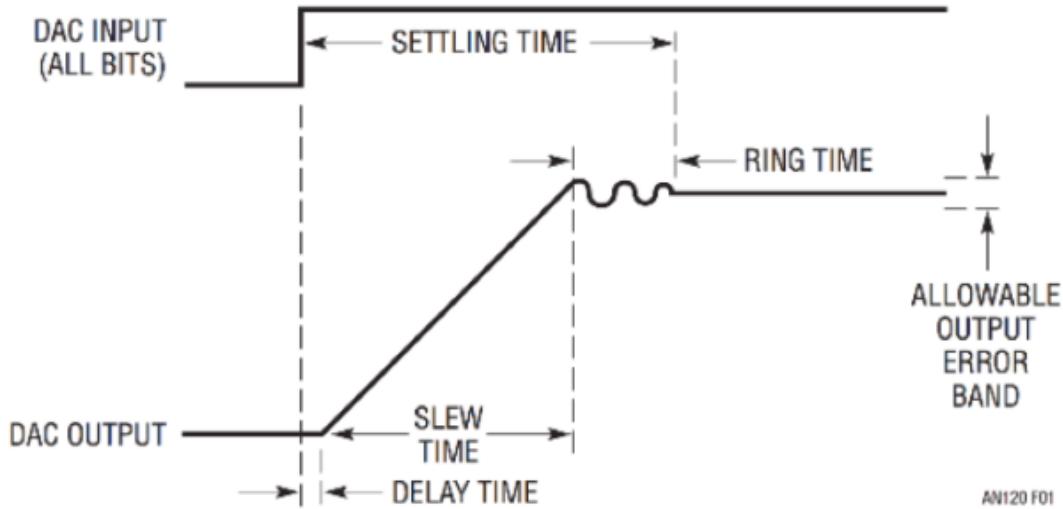


Figure 5.2: Example DAC output

5.4 Error Band

The maximum acceptable error band is notated as $\frac{V_{out}}{2^n}$ where V_{out} represents the maximum voltage output of the device and N represents the desired bit resolution. An 8-bit system with 4V max output, for example, has an error band of $\frac{4V}{2^8} = 0.0156V$. The settling time is the time it takes for our analog system to be bounded by this error band. A smaller error band makes calculating the final value more difficult for the device.

5.5 PCB

The amp card was designed to encompass the first and second stages (DAC Buffer/Cable Driver). Prototype and final PCB layouts are attached below. The load and bandwidth requirements meant that the amplifiers had to have a high slew rate (reflected as rise time in the Dewar) and bandwidth. These design choices were the basis for the v2 redesign which will be discussed later. Each amp card contained two amplifiers, and each amplifier had their own ground planes which were unified at the DAC input and interface board output connectors. This is a common design choice

meant to eliminate cross-talk between ground planes of sensitive analog components at high speeds. Each amplifier component was a quad amplifier, but only the first two were used in the design. While this decision was also made out of concern for cross-talk, the unused pins wasted quite a bit of space and were one of the first motivations for a new PCB in Nessie2. The amplifier card was initially designed as a 2-layer PCB which proved to be insufficient for power delivery and signal integrity [7]. The board was redesigned to a 4-layer version and extensively tested to ensure the previous concerns were fixed.

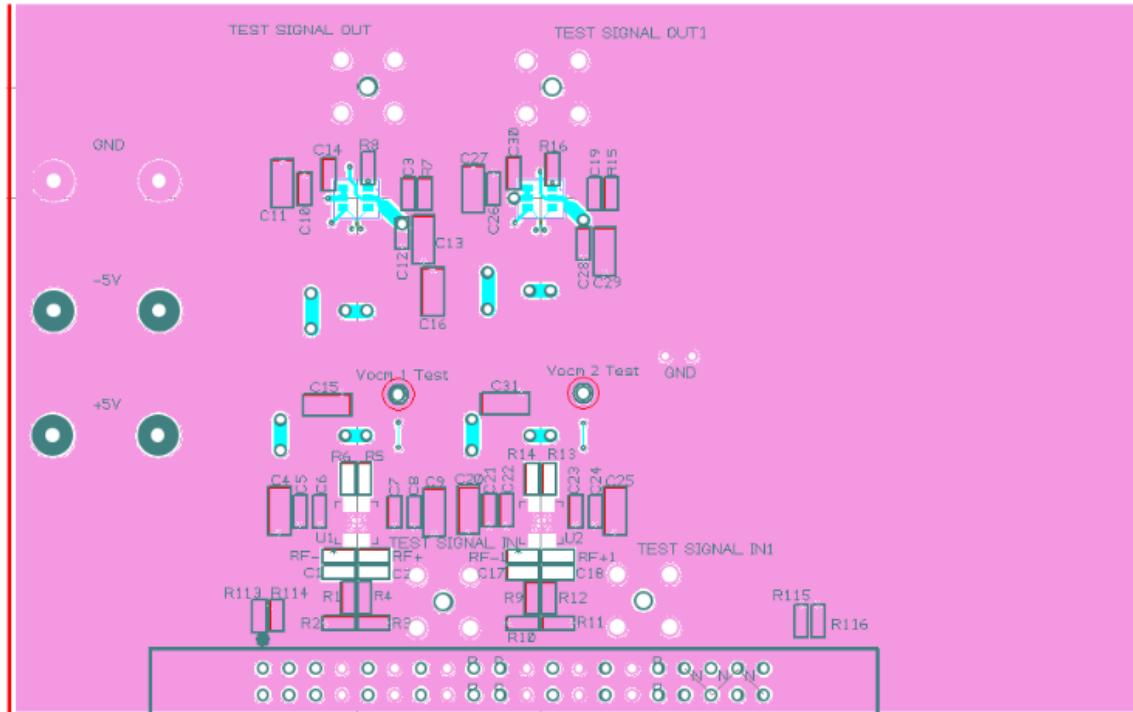


Figure 5.3: Prototype Amp Layout

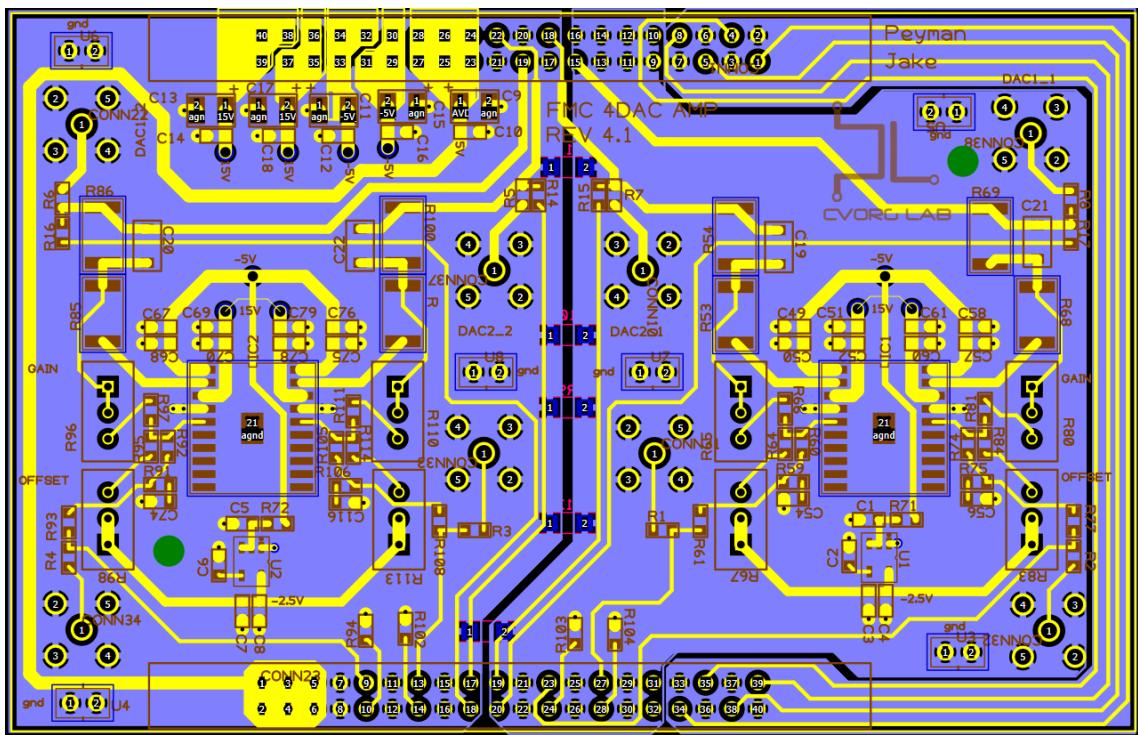


Figure 5.4: Final Amp Layout

Chapter 6

FIRST ITERATION OF AMPLIFIER TESTING

The first version of the test setup and procedure was not well documented or maintained. Due to hardware changes that were too costly to warrant a complete re-fabrication, every amp card had to first be electrically reworked. The post-rework test was a simple continuity and resistance check with a multimeter to make sure all new connections were stable. Amps were then hooked up to a function generator and power supply using jumper wires from their connectors. Input and output were viewed on an oscilloscope to ensure proper amplification. While this was supposed to be a sufficient emulation of their requirements in the system, the entire procedure was loosely documented and not well-enforced enough to ensure long term reproducability and reliability.

6.1 Electrical Rework

One of the first tasks I was given upon entering the group was to help rework each amp. The first issue was that the amplifier power rails (+15V/-5V) were not connected by default. Each amplifier's power rails had to be soldered to the power output using jumper wires. This first step already provided too much room for error, as jumper wires for power distribution would not necessarily be a better choice than simply integrating power lines into the PCB. Adding a person's hand solder in between increased the risks of cold solders or accidental shorts which are completely unacceptable for power pins.

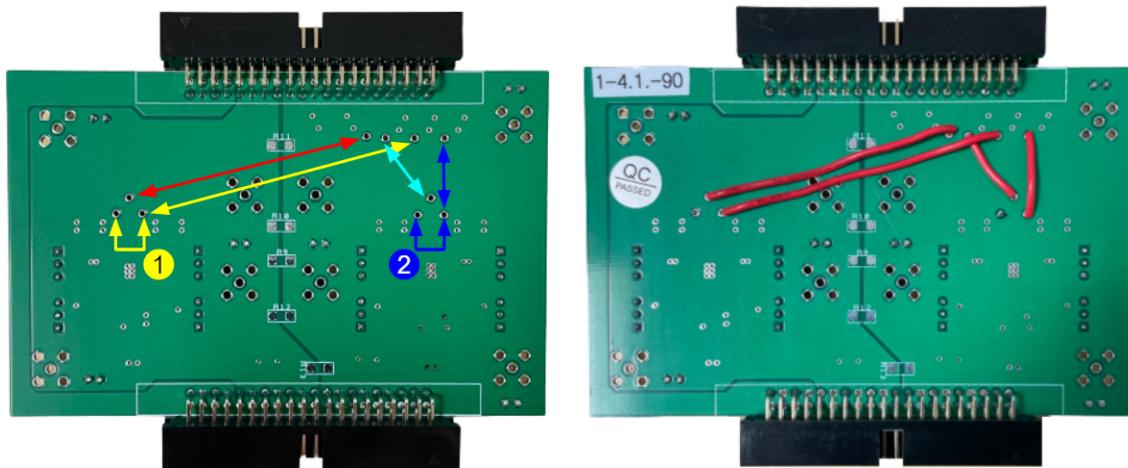


Figure 6.1: Rework of the power rails

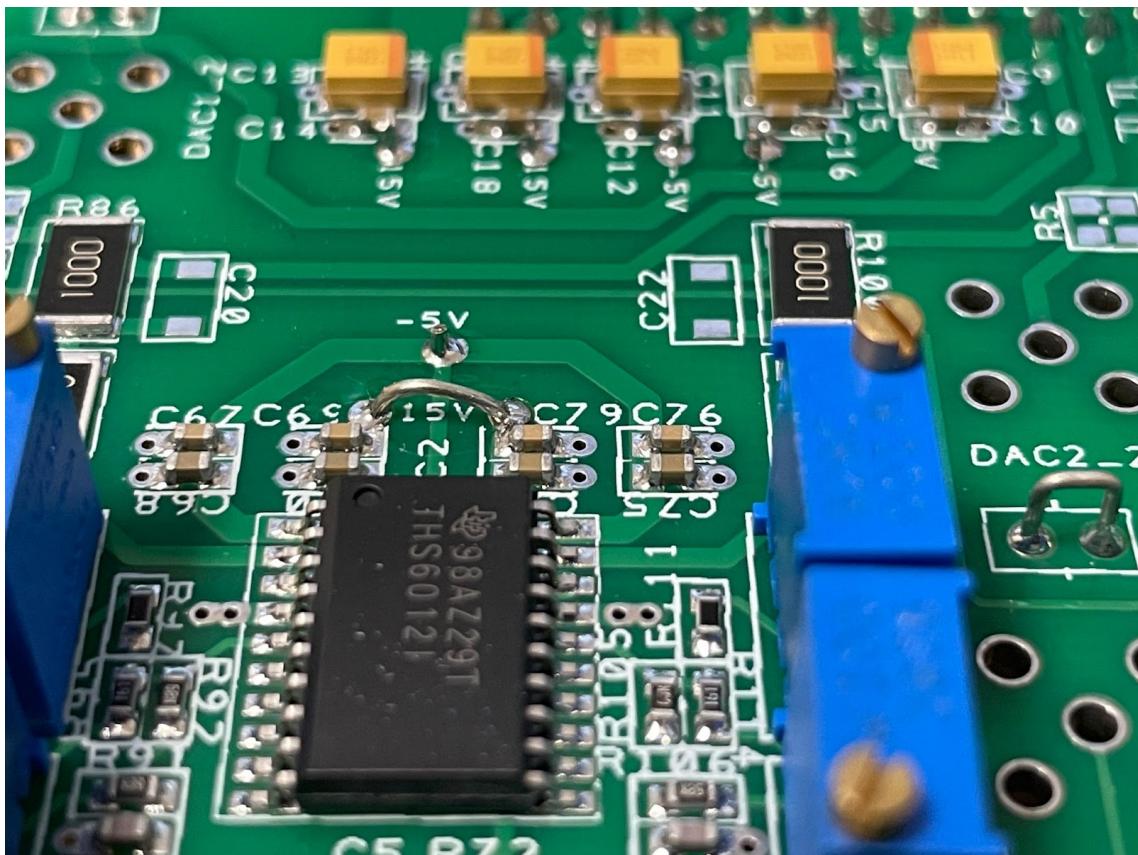
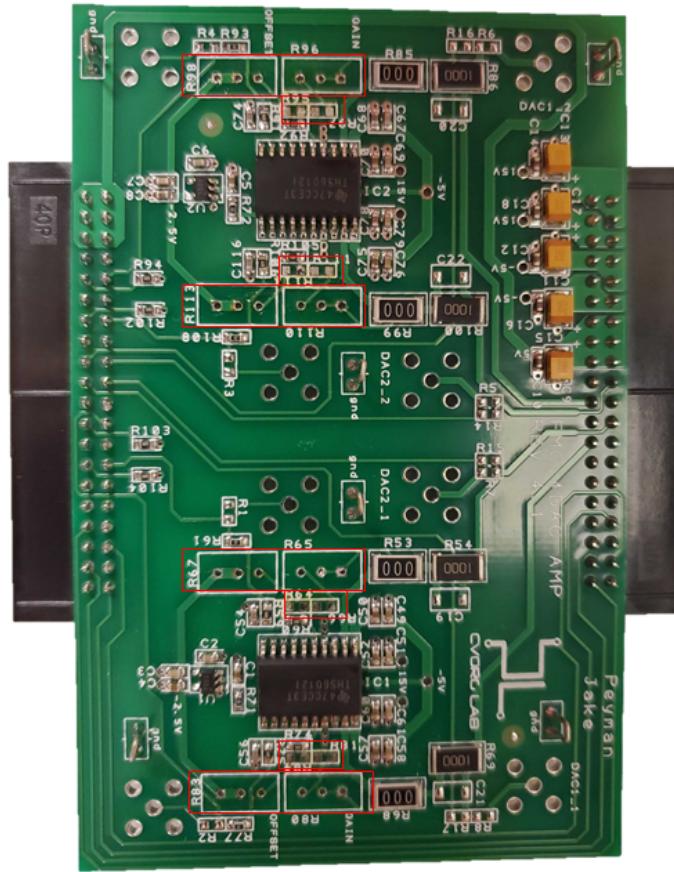


Figure 6.2: Power rails post-rework

6.2 Component Replacement

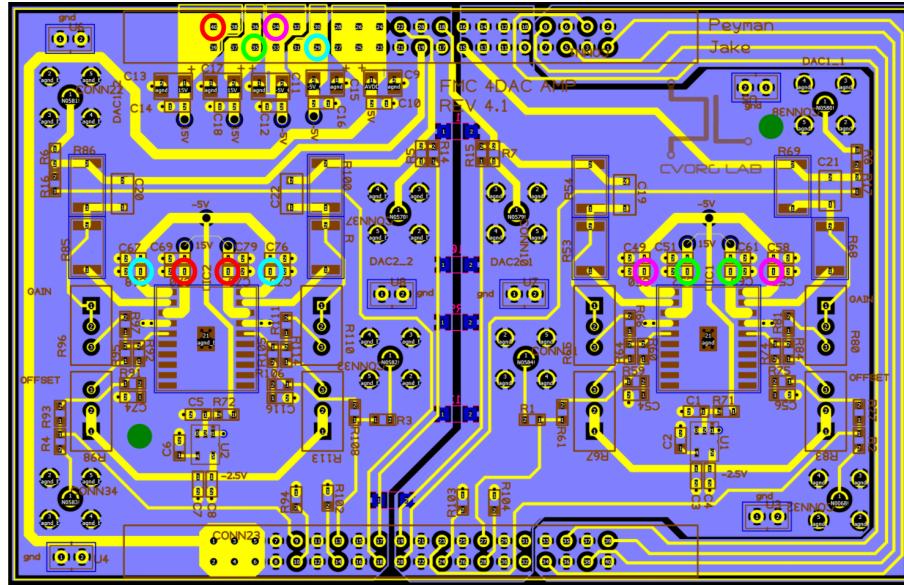
After bridging the power planes on the board, potentiometers and resistors had to be removed and replaced. The potentiometers were initially 100 ohms and used to control gain and offset of the amplified signals. These were replaced with 10 ohm potentiometers which was meant to allow more fine-tuned control over these values. The replaced resistors were also changed to new values to increase signal integrity. Once the rework was completed, it was to be given a brief electrical test (mentioned in the overview) to check the quality of all connections. While the continuity and resistance checks served their purpose, they were not sufficient for fully judging quality of the rework or identifying other issues early.



The room for human error in this whole process proved to be a massive detriment. Despite a number of group members being experienced solderers, it was impossible to rework such a high volume of boards at a consistently high level of quality. The rework process introduced so many faulty cards that every post-rework card had to be “quality checked” by a senior group member to make sure the rework was acceptable. As usual, adding another intermediary step decreased the reliability of amps and the pool of boards we had available.

6.3 Electrical test

The first stage of the electrical test consisted of the electrical checks mentioned above. There was no enforced procedure beyond following instructions on a document, and a less experienced group member ran the risk of not fully understanding what they were testing. Without detailed instructions or an intimate knowledge of the purpose of the amp, this electrical check proved to be less and less useful.



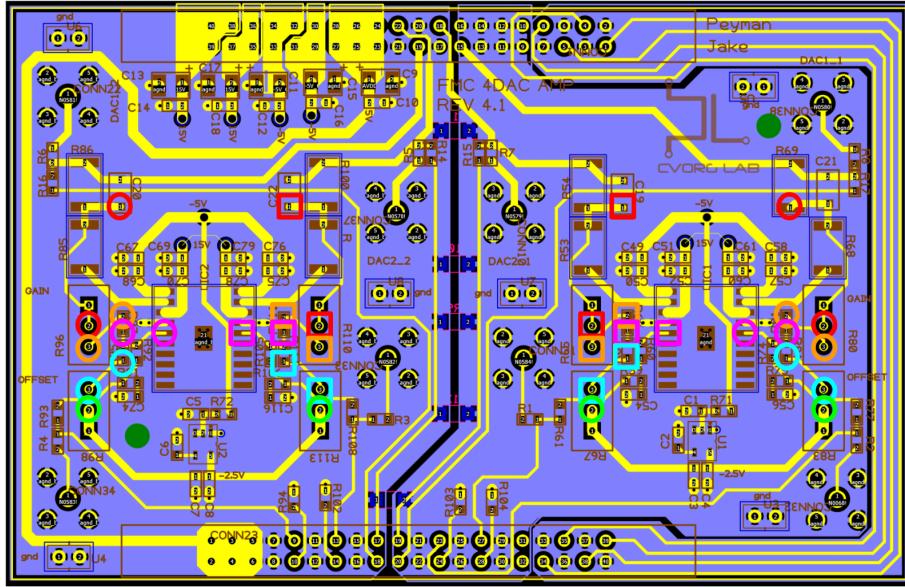


Figure 6.5: Official documentation for checking replaced components

bit. Simple breakout boards were hand-soldered for the amp connectors. Inputs were on the bottom connector and plugged into a function generator. Outputs were on the top connector and included pins for power connections (+15/-5) as well as output to the oscilloscope.

6.3.1 Function generator

The function generator settings used in the test were rather generic and barely modeled a realistic input for the amps in our system. Input was configured as a 1MHz square wave with an amplitude of 363mV and offset of 318mV. This function was also connected to an oscilloscope to compare against output. Using a high-speed square wave input was definitely a good idea, as a functional amplifier would output an equally square wave. Faulty components would not be able to replicate such sharp rise and settling time. The major downfall of this approach was that the function generator had to be individually tied to each of the card's four input channels, greatly increasing the amount of time a tester had to spend on moving pins and connectors. Having to manually set the wave up was also not the best idea, as this just added another area for the tester to make a mistake.

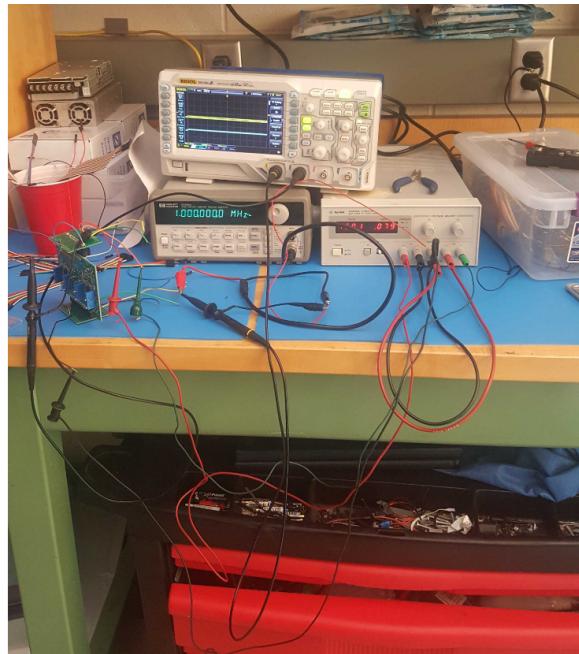
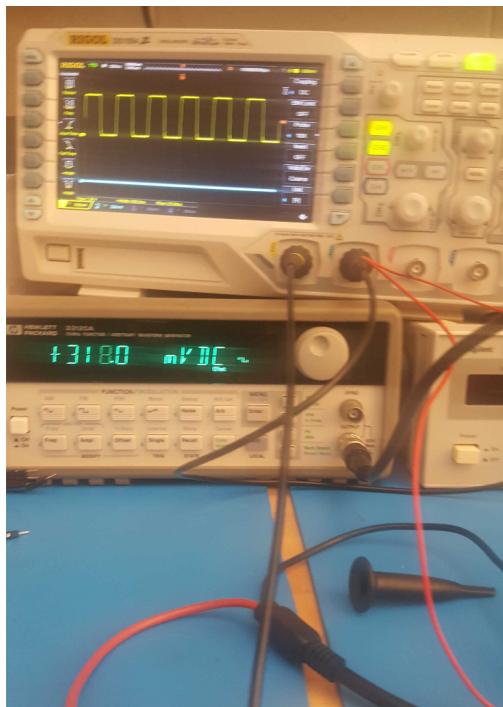
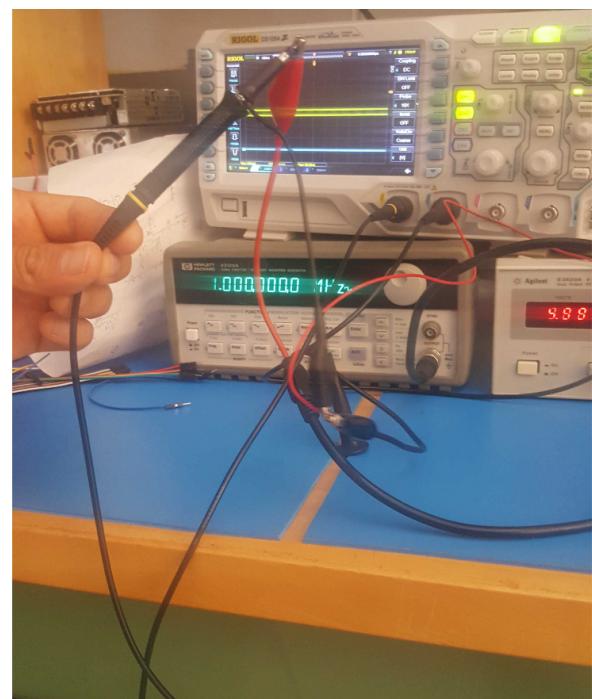


Figure 6.6: One of the only official pictures for a completed test setup



(a) Function generator settings



(b) Function generator to scope

Figure 6.7: Official documentation for setting up the function generator. Insufficient to teach anybody new how to use the equipment.

6.3.2 Power supply

Setting up the power rails was a little bit less involved. The user only needed to attach +15V, -5V, and GND to the top breakout board. Connections were still made using extruding jumper wires and alligator clips, yet another point of concern when testing a large number of amps. There were hardly any examples of what a correct setup would look like in the testing document at this point.

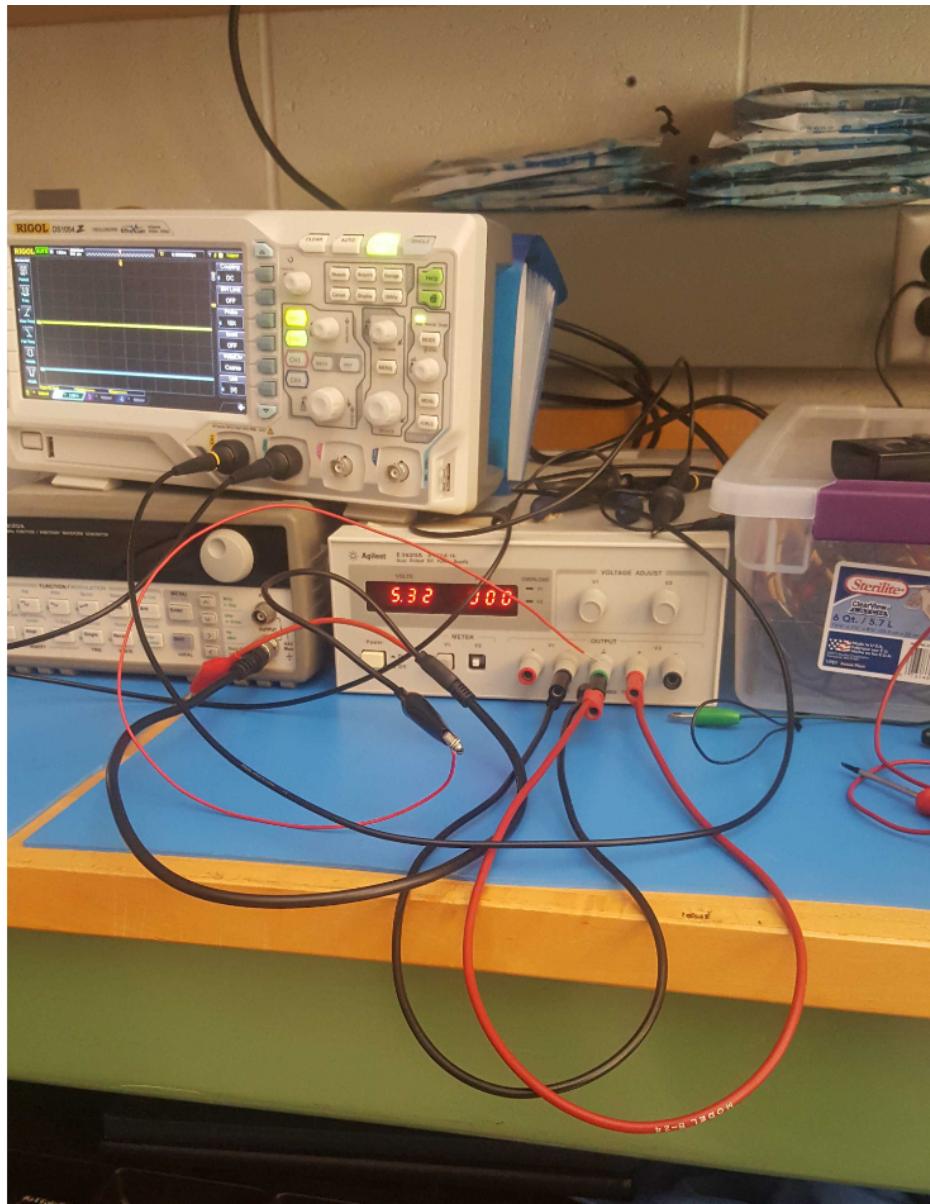


Figure 6.8: Official reference image for the amp power supply

6.3.3 Measuring Output

As mentioned before, output would be measured on an oscilloscope. Amplitude of input and output could be easily compared by human eyes and the next channel would be connected. This was a slow process that involved manually re-attaching input and output alligator clips. If gain or offset needed to be tweaked, the tester was to turn their respective potentiometers and observe output. The move to 10 ohm potentiometers greatly decreased their effect on the circuit at all and ended up being more of a nuisance than a useful control signal.

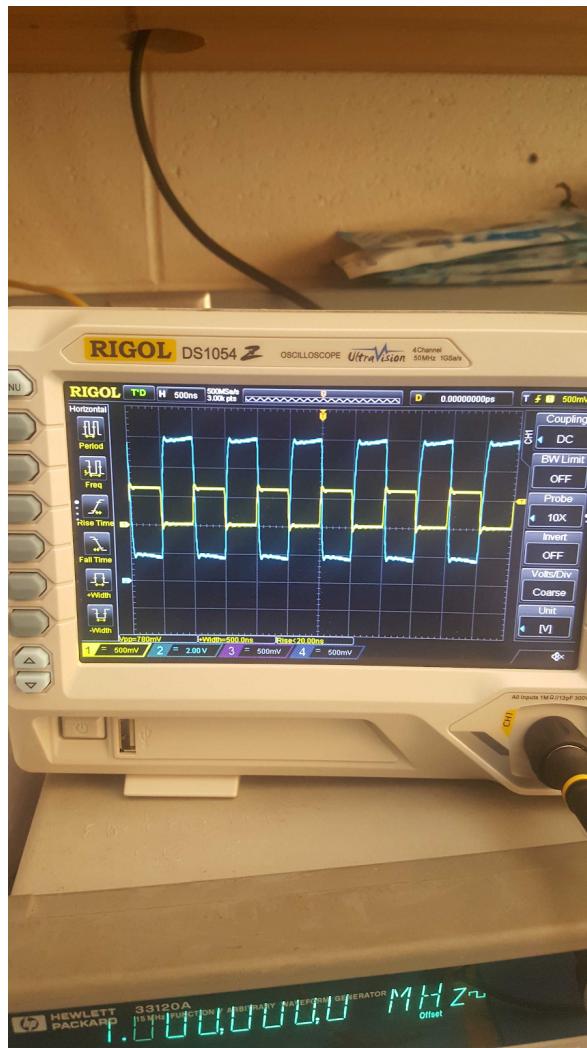


Figure 6.9: Official example of oscilloscope output. Yellow=input, blue=output

6.4 Lessons Learned

In conclusion, learning and using the amplifier rework and test procedures was a difficult task that left far too much room for interpretation or error. The amplifiers were crucial to the system's integrity but were not thoroughly tested or maintained. The process was slow, tedious and quite disconnected from the functionality of the system. Poor documentation meant that only a few group members truly understood the purpose and functionality of all steps involved. Swapping cards under test required disconnecting the card from its breakout boards that were already precariously grasped by alligator and probe clips from the instruments. The breakout board pins were not even labeled, so it was difficult to determine if issues were due to the user or hardware. This procedure may have filled its need when first conceived, but proved to be unsustainable as the project scaled up. A careful re-examination was required to understand what needed to be tested and what could be improved.

Chapter 7

DEVELOPMENT OF A FORMAL TESTING PROCEDURE

7.1 Initial considerations

The new procedure was to be a direct response to the previous one. Based on complaints and difficulties from all who had to use the setup, we compiled a list of the biggest concerns and focused the procedure design around them. These included:

- Manually changing input/output channels was slow and introduced too many steps
- Input & output were connected through a flimsy probe clip
- No way to separate amp power rails
- No indication if the amps were receiving sufficient power
- No data collection for comparison between cards
- No standards or documentation for gain/offset potentiometer tweaks

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Appendix A

TITLE OF APPENDIX

This is the information for the first appendix, Appendix A. Copy the base file, appA.tex, for each additional appendix needed such as appB.tex, appC.tex, etc. Modify the main base file to include each additional appendix file.

If there is only one appendix, then modify the main file to only use app.tex instead of appA.tex.