

**ABUTTED IRLED INFRARED SCENE PROJECTOR DESIGN AND
THEIR CHARACTERIZATION**
A TALE OF STRIFE AND SEMICONDUCTORS

by

Joshua Marks

A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical and Computer Engineering

Spring 2019

© 2019 Joshua Marks
All Rights Reserved

**ABUTTED IRLED INFRARED SCENE PROJECTOR DESIGN AND
THEIR CHARACTERIZATION**

A TALE OF STRIFE AND SEMICONDUCTORS

by

Joshua Marks

Approved: _____
XXXX XXXX, Highest Degree
Chair of the Department of XXXX

Approved: _____
XXXX XXXX, Highest Degree
Dean of the College of XXXX

Approved: _____
Douglas J. Doren, Ph.D.
Interim Vice Provost for Graduate and Professional Education

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Xxxx Xxxx, Highest Degree
Professor in charge of dissertation

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Xxxx Xxxx, Highest Degree
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Xxxx Xxxx, Highest Degree
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Xxxx Xxxx, Highest Degree
Member of dissertation committee

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

LIST OF TABLES	xi
LIST OF FIGURES	xii
ABSTRACT	xxii
Chapter	
1 CONTRIBUTIONS OF THIS DISSERTATION	1
1.1 Summary of Contributions	1
1.2 Goals of this Dissertation	1
2 INTRODUCTION	2
2.0.1 Dynamic IRSP Projection	4
2.0.2 Commonly Used IRSPs	5
2.0.2.1 Resistor Arrays	5
2.0.2.2 Digital Micro-mirror Device / Deformable Mirror Device	6
2.0.2.3 Liquid Crystal	9
2.0.2.4 Scanning Lasers	10
2.0.2.5 Superlattice LEDs	10
3 IR SENSOR TECHNOLOGY DEVELOPMENT	11
3.1 Introduction	11
3.2 Infrared Sensor Development	14
3.2.1 Early History (1800 - 1857)	14
3.2.1.1 Discovery of Infrared	14
3.2.1.2 Seebeck Effect	14
3.2.1.3 Peltier Effect and Thomson Effects	16

3.2.1.4	The Thermocouple and the Thermopile	17
3.2.2	The Bolometer	18
3.3	Pre-Quantum Mechanics Period (1857 - 1900)	19
3.4	Quantum Mechanics Period (1900 - 1929)	20
3.5	Military Application Period (1929 - 1970)	20
3.6	Types of Infrared Sensors	22
3.6.1	Photonic Sensors	23
3.6.2	Thermal Sensors	24
Part I	IRLED IRSP CHARACTERIZATION	25
4	IRSP AND IR SENSOR MODELS	26
4.1	Sensor Model	26
4.2	Ideal IRSP Model	27
4.3	Realistic IRSP	29
4.3.1	Frame Time	29
4.3.2	Bit Resolution	30
5	RISE TIME OVERVIEW	31
5.1	CVORG IRLED IRSP Analog Signal Model	31
5.2	Measurement Methodology	32
5.2.1	How Oslo Architecture IRSPs Draw	33
5.2.2	Pixel Write Cycle	34
5.2.3	Conceptual RIIC Pixel Schematic	36
5.2.4	Pixel Write Timing	37
5.3	Actual Pixel Write Cycle	38
5.4	System Rise Time Measurement Method	39
5.5	Analog Signal Transmission Line Effects	41
5.6	System Rise Time Experiment	43

6 RISE TIME EXPERIMENTS	44
6.0.1 Fast and Slow RIIC Channels	46
6.0.1.1 Analog Input Circuitry Overview	46
6.1 Rise Time Results	49
6.2 Slow and Fast Channel Cause Investigation	52
6.3 IRLED and RIIC rise time vs System Rise Time	54
6.4 System Bit Resolution	56
6.4.1 System Bit Resolution Results	59
6.5 Thermal Effects on Rise Time	64
6.6 Conclusion	64
7 ANALOG CIRCUIT IMPROVEMENTS FOR INCREASED RISE TIME	65
7.1 Introduction	65
7.2 Architecture Overview	65
7.3 Load Characterization	66
7.3.1 SPICE Model Description	66
7.3.2 Vector Network Analyzer and Signal Generator Sweep	67
7.4 Component Choices	69
7.4.1 OPA695	69
7.4.2 ADA4932	69
7.5 Architecture Design	69
7.6 SPICE Simulation	70
7.7 PCB Construction	72
8 SETTLING TIME MEASUREMENT	76
8.1 Analog System Performance Metrics	76
8.1.1 Accuracy and Precision Review	76
8.1.2 Settling Time Definition	78

8.1.3	Examples of Different Bit Resolutions	79
8.2	Measuring Settling Time	83
8.2.1	Settling Time Instrument Conceptual Overview	88
8.2.1.1	Overview and Inspiration	88
8.2.2	Settling Time Instrument Conceptual Overview	93
8.3	CSE Analog System Overview	95
8.4	Settling Time Circuit Mathematical Model	97
8.4.1	Unit Cell Overview	97
8.4.2	System Simulation	101
8.4.3	System Bit Resolution	104
8.5	SPICE Simulation	104
8.5.1	Electronic Component Choices	104
8.5.1.1	Operational Amplifier	104
8.5.1.2	Clamping Diode	107
8.5.1.3	Common Base Transistors	107
8.5.1.4	Other Components	108
8.5.2	SPICE Simulation	109
Part II ABUTTED IRLED HYBRID DEVELOPMENT	112
9 AIREA OVERVIEW	113
9.1	Summary	113
9.2	Introduction	114
9.2.1	IRLED Hybrid Overview	115
9.2.2	Problems Associated with IRLED Production Beyond 4 Megapixels	116
9.2.3	AIREA Goals	120
9.2.4	Methods, Assumptions, and Procedures	121

10 AIREA RESULTS AND DISCUSSIONS	123
10.1 IRLED Work	123
10.1.1 AIREA SLED Pixel Design	123
10.1.2 AIREA SLEDs Wafer Overview	126
10.1.3 AIREA SLEDs Wafer Growth	128
10.1.4 AIREA SLEDs Wafer Fabrication	131
10.1.5 AIREA SLEDs Wafer Indium Bump Fabrication	142
10.1.6 SLEDs Wafer Trench Etch Overview.	147
10.1.7 SLEDs Wafer Trench Results	150
10.2 RIIC Work	153
10.2.1 AIREA RIIC Overview	153
10.2.2 RIIC Pixel Testing	157
10.2.3 Oslo RIIC Design Update	160
10.2.4 AIREA Wafer Layout.	168
10.2.5 Die Stitch Design.	171
10.2.6 Wafer Testing	174
10.2.7 Silicon RIIC Wafer Etch Die Singulation Overview	177
10.2.8 SLED Wafer and Abutted Hybridization Overview	180
10.2.9 Final Assembly	182
10.2.10 AIREA Etch Die Singulation Design	183
10.2.11 TEOS Oxide Etch Experimental Results	186
10.2.12 TEOS Oxide Etch and Through Substrate Etch Test Wafer Results	190
10.2.13 RIIC Wafer Die Singulation Etch Complications	191
10.2.14 RIIC Wafer Die Singulation Etch Attempted Solutions	195
10.2.15 RIIC Singulation: Dicing Method	202
10.3 Hybridization Process	205
10.3.1 Indium Bump Deposition	205
10.3.2 Hybridization and Fly-Cutting	206
11 CONCLUSION	209
REFERENCES	211
REFERENCES	212

Appendix

A TITLE OF APPENDIX	217
A.1 Current Gating vs Voltage Gating	217
A.2 Oscilloscope Overdrive	217
A.3 DAC Board	217
A.4 AIREA Wafer Analysis	217
A.5 Dewar Impedance Measurement	217
A.6 RIIC Analog Signal Architecture	217
B LABORATORY REPORTS	218
B.1 21:1 Board Testing:	218
B.1.1 Initial results:	218
B.1.2 Circuit Update	222
B.1.3 Straight Post-amp Testing:	229
B.1.4 Bit Resolution:	234
B.1.5 5V operation	236

LIST OF TABLES

5.1	NSLEDs WEN settings for different frame rates.	39
6.1	List of DACMODES and their function	48
9.1	Overview of the IRLED IRSP program and the associated cost per wafer of the RIIC component (excludes fixed NRE cost of making masks etc inherent in CMOS production. This cost can be between \$10K and \$120K).	119
10.1	RIIC die count for shared HDILED/AIREA RIIC wafer.	168
10.2	Etch Recipe	196
10.3	Etch Recipe	197

LIST OF FIGURES

2.1	Laboratory setup showing all optical components for IR Scene Projection.	4
2.2	DMD Diagram.	8
3.1	Example Planck's Law Curves for black-bodies at various temperatures.	12
3.2	Infrared image of a tea kettle with hot water in it.	12
3.3	Flir,. FLIR SC8200 Imaging F18 With Afterburner At Close Range.. 2016. Web. 8 Mar. 2016.	13
3.4	Diagram of a Thermocouple [16]	15
3.5	M. Melloni's Thermomultiplicateur [3]	18
3.6	Fundamental optical excitation processes in semiconductors: (a) intrinsic absorption, (b) extrinsic absorption, (c) free carrier absorption.[38]	23
5.1	Analog signal timing constraints.	32
5.2	A diagram showing the four quadrants of the Oslo RIIC and the addressing for the first and last pixels.	34
5.3	A diagram showing which pixels are written to in which pixel write cycle.	35
5.4	A diagram showing a high level overview of the internal circuitry of a RIIC pixel.	37
5.5	Timing diagram for writing to a pixel.	38
5.6	39

5.7	IRSP and camera timing diagram.	40
5.8	vpaddac0 - analog voltage at RIIC pad with ringing, vrowdac0 - analog voltage on DAC row line, capn2, capn - analog storage node in the pixel. Ringing is filtered by RIIC.	42
6.1	Rise time measurements using custom firmware that allows for WEN durations below 6 ticks (30ns for the current system).	45
6.2	Rise time measurements using custom firmware that allows for WEN durations of 1, 2, 3, and 4 ticks.	45
6.3	Super Pixel Inputs	47
6.4	RIIC Segmented Row Architecture	48
6.5	Slow channel rise time measurements with WEN custom firmware showing reasonable agreement with stock firmware.	50
6.6	Fast channel rise time measurements with WEN custom firmware showing reasonable agreement with stock firmware.	51
6.7	Effect of WEN Delay on rise time of fast channels.	53
6.8	Effect of WEN Delay on rise time of fast channels.	53
6.9	Difference between 32x32 grid spacing and 33x33 grid spacing for rise time measurements. The results show the rise time of the system and the rise time of just the RIIC and the rise time of the IRSP System.	55
6.10	Difference between 32x32 grid spacing and 33x33 grid spacing for rise time measurements. The results show the top portion of the curves for rise time of the system, and the rise time of just the RIIC and the rise time of the IRSP System.	55
6.11	One bit system.	57
6.12	Two bit system.	58
6.13	Fast Channel NSLEDS1 vs NSLEDS3 Rise Time with Bit Resolution.	60

6.14	Slow channel rise time for both NSLEDS1 and NSLEDS3 with bit resolution levels overlaid. The plot attempts to quantify the performance decrease of the epoxy attachment vs. the epoxy and indium bump attachment.	61
6.15	Fast channel rise time measurements showing the difference in rise time for strong and weak mode.	62
6.16	Slow channel rise time measurements showing the difference in rise time for strong and weak mode.	63
7.1	Overview of the Analog Electronics Architecture	66
7.2	Carrier Board SPICE Model.	67
7.3	SPICE settling time results for all three amplifier stages.	68
7.4	SPICE schematic of the three stage amplifier architecture.	71
7.5	SPICE settling time results for all three amplifier stages.	71
7.6	Schematic for first and second stages of the new amplifier topology.	73
7.7	Layout for first and second stages of the new amplifier topology. . .	74
7.8	Layout for the Dewar Driver Board.	75
8.1	Analog System Settling Time Definition	77
8.2	Analog System Settling Time Definition	79
8.3	1 Bit System	80
8.4	2 Bit System	81
8.5	4 Bit System	82
8.6	Oscilloscope AC Coupling Setting.	84
8.7	Oscilloscope AC Coupling Setting.	85
8.8	High pass filter and corresponding frequency response.	86

8.9	Decomposition of analog signal into settling component and DC component.	86
8.10	False Sum Node historically used to measure settling time.	87
8.11	False Sum Node historically used to measure settling time.	87
8.12	False Sum Node historically used to measure settling time.	88
8.13	Prototype of Jim Williams' 18-bit Settling Time Instrument.	90
8.14	iPhone 5S Logic Board.	91
8.15	iPhone 5S Shielded Logic Board.	92
8.16	Unit Cell block diagram.	93
8.17	Settling Time Instrument Conceptual Diagram.	95
8.18	CSE Analog System Overview	95
8.19	Block Diagram of Settling Time Mathematical Model Unit Cell . .	97
8.20	Block Diagram of Settling Time Mathematical Model Unit Cell . .	98
8.21	Input signal and output signal showing the effects of the subtraction and the multiplication steps together.	99
8.22	Input signal and output signal showing the effects of the subtraction and the multiplication steps together.	100
8.23	Unit Cell Python Code.	100
8.24	The final system output is shown along with the corresponding upper and lower limits of the error band. The error band is shown by the dashed red lines.	102
8.25	Frequency Response of the LMH5401.	105
8.26	Frequency Response of the LMH5401.	106
8.27	Frequency Response of the LMH5401.	108

8.28	Frequency Response of the LMH5401.	110
8.29	Frequency Response of the LMH5401.	111
9.1	Cross Section View of an IRLED Hybrid.	115
9.2	A plot of the RIIC yield percentage vs. the RIIC die area.	118
9.3	Wafer yield vs. die size for D=0.002.	119
10.1	Left side shows current AIREA/HDILED superpixel design. Right side shows proposed AIREA/HDILED superpixel design. A superpixel is a 48-micron square and integrated four 24-micron square pixels. The current design has 8 indium bumps and the proposed design.	124
10.2	Identification of common single anode contact and four cathode contacts for each super-pixel.	124
10.3	Plan view of the super-pixel with critical dimensions indicated. . .	125
10.4	AIREA SLEDS Wafer Map.	126
10.5	Hybridization Alignment Marks.	127
10.6	A high resolution X-ray diffraction scan off the deliverable structure, showing good alignment of the zeroth order super-lattice peak and quaternary layers to the substrate peak.	129
10.7	A 20x optical profilometry image of the boundary between a V-flux deficient (right side) and V-flux supported (left side) region. The sharpness of the boundary and its localization to a corner of the wafer lends itself to the interpretation of V-flux design.	130
10.8	Exploded view of gold electrical connections.	132
10.9	IAG577 etch mask after etching. Etching caused roughening of the mask.	132
10.10	Etch mask on TSI1648 after etching no roughening occurred when the etched was pulsed at a low duty cycle to prevent heating. . . .	133

10.11	Deliverable IAG581, after the RIE ICP etch. This creates the topography of the wafer, forming the four mesas surrounding the common cathode in between.	135
10.12	Deliverable IAG581, bottom metal near the edge of the array where the development was better, resulting in a more uniform coverage of gold in the channels between the mesas.	136
10.13	Deliverable IAG581, bottom metal deposition near the center of the array. The development did not progress as much here as it did near the edge of the wafer so it is visible that the metal didn't cling as well in the channels, especially near corners.	137
10.14	Deliverable IAG581, the alignment markings near the edge of the wafer. There is the gold markings from the first metallization being matched to markings from the bottom metallization which are more difficult to see. The alignment is excellent.	138
10.15	Image of a completed AIREA wafer. This wafer is ready for indium bumping and dicing.	139
10.16	(a) Light-Current and (b) Apparent Temperature curves for a 24x24 um ² device across the 3-5um band.	139
10.17	Pictures of the etch and top metal contacts on IAG616.	141
10.18	General shape of an indium bump on the left and the location of the indium bumps for both the SLEDs die and the RIIC die on the right.	142
10.19	Microscope Inspection Image of AIREA SLEDS Wafer.	143
10.20	Microscope Inspection Image of AIREA SLEDS Wafer.	144
10.21	Edge bead bubbles and cracks during lithography bake on the cleaved edge.	144
10.22	Finished Indium bumps on the SLEDs die.	146
10.23	Rough abutted vertical sidewalls.	148
10.24	SLEDs Wafer Trench Etch.	148
10.25	SLEDs Wafer Trench Etch.	149

10.26	Zoomed in view of the 50 micron deep trench and overview of the fly cut procedure.	149
10.27	Melted Indium bumps from the ICP trench etch.	151
10.28	Overview of all defects observed on the AIREA SLEDs die.	152
10.29	AIREA CMOS RIIC.	154
10.30	Architectural overview of the AERIA RIIC.	155
10.31	Architectural overview of the AERIA RIIC.	156
10.32	Architectural overview of the AERIA RIIC.	156
10.33	Strong drive transistor I-V sweep.	158
10.34	Weak drive transistor I-V sweep.	159
10.35	Selstrong circuitry.	161
10.36	Standby current vs supply voltage.	162
10.37	Simulated standby current vs supply voltage.	163
10.38	Top image shows the old layout of the digital IO section before adding pull-down resistors. Bottom image shows updated digital IO section with pull-down resistors.	165
10.39	Top image shows the old layout of the address decoder section. Bottom image shows updated address decoder section. The added logic is an OR gate that computes load = (load or reset) - this additional logic forces entire pixel array to reset during power on.	166
10.40	Plot of the shared HDILED/AIREA wafer stitch. The two AIREA 1Kx1K RIICs on the left edge of the wafer are not usable because their corners extend past wafer edge.	169
10.41	AIREA Final CMOS wafer design.	170
10.42	Die Stitch Process.	172
10.43	Cut Piece Error Example.	172

10.44	The wafer holder "claw" marks are circled in red.	173
10.45	Bad pixel curves and good pixel curves overlaid on a plot.	175
10.46	Physical location of bad pixels shown in yellow. Tested pixels shown in green. Untested pixels shown in blue.	176
10.47	AIREA Silicon wafer dicing cuts and etch window.	178
10.48	Cross-section view of Silicon wafer and the region to be etched. . .	179
10.49	Cross-section view of Silicon wafer and the region to be etched. . .	179
10.50	50 um etched trench in the center of the SLEDs array.	181
10.51	Hybrid without vertical sidewall exposed.	181
10.52	Assembled AIREA hybrids.	182
10.53	The side view of the region to be plasma etched by TSI.	184
10.54	The AIREA RIIC wafer after TSI has plasma etched through the TEOS layer and deposited the positive photoresist.	185
10.55	The AIREA RIIC wafer after die singulation.	186
10.56	First etched sidewalls.	187
10.57	A second attempt with improved results.	188
10.58	A view of the other edge in the second attempt.	189
10.59	Comparison between sawn edge and etched edge.	191
10.60	RIIC wafer etch for AIREA hybrids.	193
10.61	Aluminum stress relief structure.	194
10.62	Overhead view of the aluminum test structure and height profile. .	194
10.63	SEM image of a test piece and a side view of the height profile for the aluminum test structure.	195

10.64	D1 Top Right Corner.	199
10.65	C1 Bottom Right and D1 Bottom Left.	200
10.66	C1 Top Right and D1 Top Left.	201
10.67	Close up view of chip out produced by dicing method.	203
10.68	Close up view of dicing method.	204
10.69	Indium bumps deposited on both the SLEDs and the RIICs.	206
10.70	Ideal hybridization.	207
10.71	Actual hybridization system caused by natural bow of the RIIC pieces.	208
10.72	Rabbit ears after fly-cutting.	208
B.1	Post-amp circuit with 21:1 divider circuit. Resistors R32 and R31 form the 21:1 divider.	219
B.2	220
B.3	221
B.4	223
B.5	224
B.6	225
B.7	226
B.8	227
B.9	228
B.10	Post-amp circuit without 21:1 divider circuit.	230
B.11	231
B.12	232

B.13	233
B.14	235
B.15	237

ABSTRACT

Chapter 1

CONTRIBUTIONS OF THIS DISSERTATION

1.1 Summary of Contributions

1. Mathematical framework for understanding the importance of system rise time and settling time in IRSP.
2. Measurement methodology for measuring IRLED IRSP system rise time.
3. Settling time measurement instrument
4. First Abutted IRLED Hybrid

1.2 Goals of this Dissertation

We have a habit in writing articles published in scientific journals to make the work as finished as possible, to cover up all the tracks, to not worry about the blind alleys or describe how you had the wrong idea first, and so on. So there isn't any place to publish, in a dignified manner, what you actually did in order to get to do the work.

—Richard P. Feynman, Nobel lecture 1996

This thesis seeks to push the boundaries of Metrology science in the area of Infrared Light Emitting Diode (IRLED) Infrared Scene Projection (IRSP). It also seeks to provide future graduate students in the CVORG Laboratory a guide to designing analog circuits, and measuring their response. So that they may not find the lab as I did – full of equipment and projects long past, but no one to show them how to use the equipment. In a small way I hope that this Dissertation will live on and be useful after I am gone.

So, like Dr. Feynman says I will include the blind alleys and the wrong paths I took to arrive at the designs presented in this Dissertation. These will be included in an Appendix in the form of laboratory reports.

Chapter 2

INTRODUCTION

Infrared (IR) imaging systems have found many use cases in academic, medical, industrial, and military applications, as the various IR imaging system technologies have matured over time. This is due to the importance of imaging the unique IR signatures emitted by hot objects in these application fields. More use cases are found as the IR imaging technologies become more sensitive and able to resolve finer grained details of hot objects. This increase in uses of IR imaging systems requires accurate testing and calibration using IR sources. Calibration of both the static and the dynamic performance of the IR imaging systems is required.

Static performance calibration can be done with the use of Scientific Test Equipment that approximates an ideal black-body radiance curve for the spectral band and temperature range of interest. Dynamic calibration is a more complex task and requires a more intricate test setup.

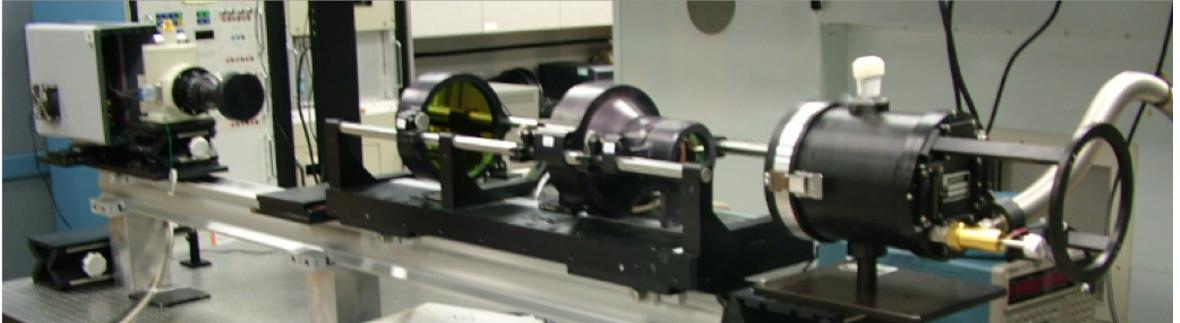
Infrared Scene Projectors (IRSPs) are tools designed to dynamically test IR imaging systems. IRSPs display a 2-D real time IR scene. Under certain conditions, the projected IR scene is a good approximation of reality, and the sensor's response can be equivocated to it's response to a similar scene created by an actual physical event. Sometimes imagery is projected onto the IR imaging system and the response is noted. Sometimes feedback is taken from the IR imaging system and used to alter the projected scene. The latter type of testing is called hardware-in-the-loop. Hardware-in-the-loop systems can test real-time IR imaging systems.

The most ubiquitous IRSP technology used since the 1980s are arrays of thin film black-body emitters (resistors). The arrays of resistors are used to create the 2-D

image that is displayed to the IR imaging system. This IRSP technology is colloquially known as a Resistor Array. Resistor Array technology is still being actively researched and developed [25][13][41][24]. Resistor Arrays are limited in their frame-rate and temperature range [33]. These limitations are due to the Resistor Arrays utilizing black-body emitters. Black-body emitters must achieve the actual desired temperature required in a IR scene. The frame-rate limitation is because the resistor emitter pixel can only change value as quickly as thermal energy can be added or removed from the pixel. This effectively forms a negative exponential curve similar to a resistor-capacitor (RC) curve. Where R is the thermal impedance seen looking into the pixel resistor element and C is the Heat Capacity of the material used in the resistor element. Just as an RC circuit has a time constant that limits how quickly the voltage on the capacitor can change the resistor emitter has a time constant that limits how quickly the temperature of the resistor element can change. The temperature range is ultimately limited by the range of temperatures the resistor elements can be safely heated to. Higher temperatures exacerbate the frame-rate limitation further.

To overcome these limitations development work on improved IRSP technologies has been and currently is being conducted [49][29][20][10][28][19]. Of particular promise and interest to this dissertation are the systems based around infrared light-emitting-diodes [29][20][10] [19]. IRSPs using LED arrays have shown the ability to display temperatures greater than 1400 K in a narrow spectral band (3-5 μ m) [21]. An array of superlattice LEDs (SLEDs) hybridized to a Read-In Integrated Circuit (RIIC) is used to make these IRSPs. Proper control electronics are required to display and project imagery in SLED based IRSPs [22]. A 68×68 SLED array was demonstrated in 2009 [9]. More recently, a 512×512 SLED array with elements made up of sixteen cascaded indium-arsenide/gallium-antimonide (GaSb) type-II superlattice structures was reported [12]. This array had an apparent temperature of up to 1350 K [33].

Figure 2.1: Laboratory setup showing all optical components for IR Scene Projection.



2.0.1 Dynamic IRSP Projection

Infrared Scene Projectors are called Projectors because of the requirement that the image the IRSP produces be recreated at the focal plane of the Unit Under Test (UUT). This requirement stems from the fact that the UUT must be tested under conditions similar to real life conditions. The image must also be collimated to ensure that it is not distorted when it arrives at the UUT focal plane. Figure 2.1 shows a laboratory setup with a collimator and appropriate lenses for accurately projecting the light from the IRSP to the UUT. On the left in the picture is the UUT. On the right in the picture in the black cylinder is an IRLED array based IRSP. The optical setup in the middle are collimators used to properly project the IRSP generated image to the UUT.

It is required that the image projected onto the UUT focal plane closely simulates radiometrically, spectrally, spatially, and temporally a real life application. Owen Williams [46] presents six performance criteria for a good IRSP. These six criteria are summarized here and broken down into more succinct points to help guide the discussions about characterization and the performance of IRSPs in this dissertation.

1. The infrared projector must project radiance so that the UUT focal plane is uniformly filled with the projected radiation over the entire entire field-of-view. Overfilling of the field-of-view may be required for HWIL applications.
2. Pixel radiance must be Lambertian over all viewing angles of the UUT.
3. The projected irradiance at the UUT entrance pupil must be spatially incoherent.

4. The projected radiance should be unpolarized.
5. The projected radiance should be temporally incoherent.
6. The IRSP must operate fast enough to ensure the UUT responds similar to the way it does in real world applications.
7. Image artifacts created by the IRSP should be minimized to the point that they will not cause the UUT to respond to them. Imaging artifacts include: flicker, aliasing, fixed pattern noise.

2.0.2 Commonly Used IRSPs

2.0.2.1 Resistor Arrays

Most currently in use thermal pixel arrays are based on the suspended membrane resistor technology developed at the Honeywell Technology Center. The invention is credited to Cole and Han in US patent US5600148A. The thermal pixel is made up of a thin-film of Silicon Nitride suspended over the RIIC by support legs and vias[46]. The suspended membrane resistor is fabricated through the use of sacrificial layers. The sacrificial layers lie in between the resistor material and the RIIC. The sacrificial layers are removed in an etch step and the resistor is left free standing. In a vacuum the gap between the resistor element and the RIIC provides excellent thermal isolation. It also allows for fine control of the impedance of the thermal element because the width and length of the support legs can be changed, thus changing the electrical resistance. These devices provide a wide-band emission spectrum due. The wide-band emission is a product of Planck's Law for hot bodies. Hot bodies inherently emit a wide-band.

The emitters are fabricated on top of a RIIC. The RIIC has CMOS electronics that control addressing, pixel brightness, and delivery of power and ground. Coles 1998 paper Large area Micro-Emitter Arrays for Dynamic Scene Projection is an excellent source for more information on this topic.

Currently, Santa Barbara Infrared (SBIR) is the sole source for IRSP systems based on resistor arrays. SBIR licensed the Honeywell Resistor array technology and continue to produce systems using that technology. SBIR has produced several different versions of their IRSP system that offer different pixel resolutions, cryogenic operation,

RIIC features such as snap-shot mode and constant current drive, and higher temperature range thermal pixel elements. SBIR reports that 1500K was demonstrated under their Ultra High Temperature Program [23].

The growth potential of resistor arrays is limited by the trade-off between power, speed, and radiance [47] in the design of the thermal pixel element. At an array level the technology is limited by the amount of current, and power required to fully illuminate arrays of higher resolution and higher radiance.

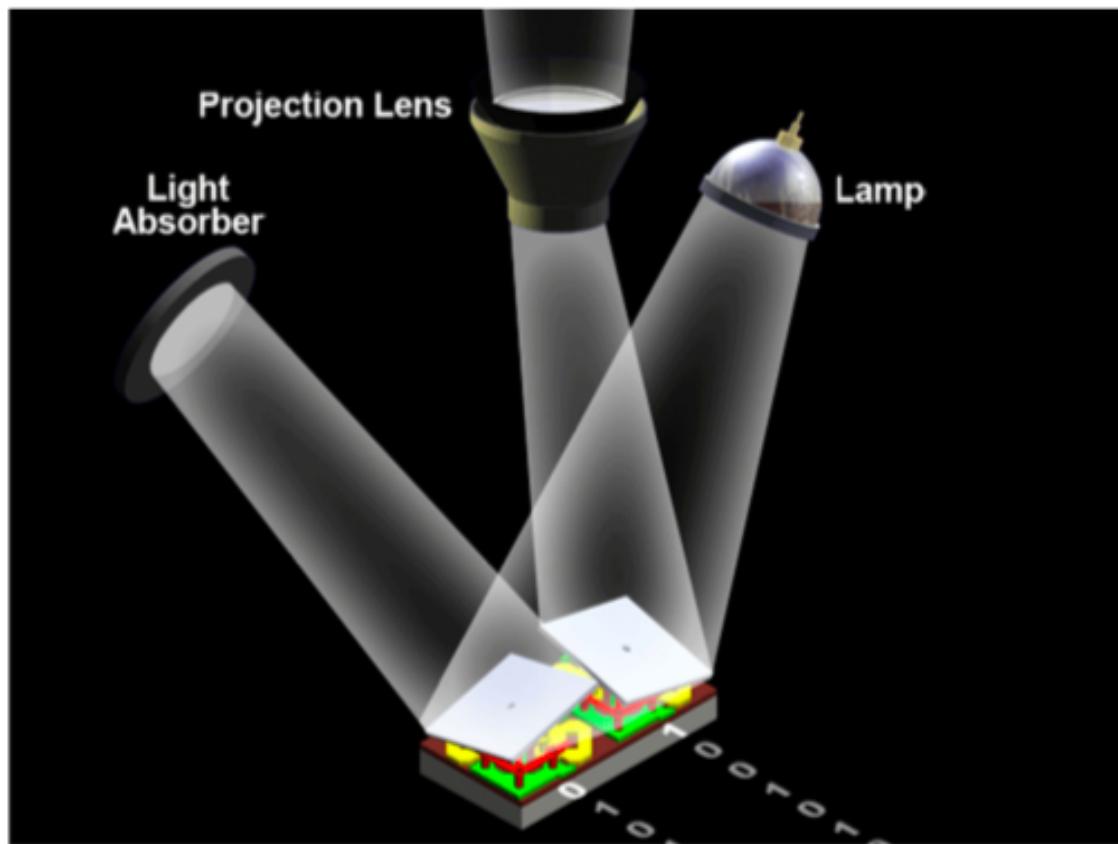
2.0.2.2 Digital Micro-mirror Device / Deformable Mirror Device

A digital micro-mirror device (DMD) is an electro-optic-mechanical device. This device utilizes Micro-Electro-Mechanical (MEMs) fabrication technology to fabricate small electronically controlled mirrors. These mirrors are small enough that they can be considered pixel elements and are able to be individually controlled to project arbitrary images. The general goal of a DMD device is to use the pixel unit cell mirrors to reflect an illumination source either out of the system aperture or onto a heat sink that prevents the light from escaping from the system. The pixel mirrors have two stable states – one that points in the direction of the aperture and one that points in the direction of the heat sink [26]. These two states are shown in the Figure 2.2.

The pixel unit cell is constructed out of a micro-mirror, torsion hinge, a via used for connecting the micro-mirror to the torsion hinge, and two spring tips [26]. The micro-mirror is attracted to either spring tip by electrostatic fields generated from the memory state of the CMOS memory circuit that lies underneath the micro-mirror [39]. Greyscale imagery is created by modulating the mirror between its On state and its Off state. Mirror transit time is on the order of $10 \mu s$ [39]. In visible light systems integration of the modulated light output from each pixel is done by the observers eye. For IRSP applications the requirements for the modulation rates are more stringent because the observer is an imaging system and not a human. An imaging system is able to detect much higher frequency modulations than the human eye.

This observation leads to the primary two drawbacks of DMD IRSPs. The first is the limited scene contrast and the second is the tradeoff between the frame rate and the grayscale bit-depth due to the need to modulate the micro-mirror state to achieve different grayscale values [32]. The modulation is called a Pulse-Width Modulation (PWM). In an IRSP application an IR source of a desired wavelength is used as the illuminator. The wavelength of the illuminator causes the second drawback of a DMD system. The wavelength of light for Mid-Wave IR (MWIR) and Long-Wave IR (LWIR) is large enough that it causes optical aberrations between pixels due to diffraction limits. This limits the contrast that is achievable between neighboring pixels. Unfortunately, these drawbacks have caused DMD projectors with a 10 bit output to have an output frame rate of around 40 Hz [39].

Figure 2.2: DMD Diagram.



2.0.2.3 Liquid Crystal

Liquid Crystal IRSP technology started with Liquid Crystal Light Valve technology developed at Hughes Aircraft. This technology used a visible light image projected onto a photoconductor array with a liquid crystal layer. When the visible light image is incident on the photoconductor array an electrostatic field is applied to the liquid crystal molecules in the pixels. The electrostatic field causes the liquid crystals to rotate within a pixel cell and the rotation of the molecule causes light of a certain polarization to be blocked or transmitted. By modulating the rotational state of the molecule imagery can be created. A polarized IR source must be passed through the liquid crystal in order to produce an IR image on the output.

This technology was superseded by Liquid Crystal on Silicon (LCoS). In an LCoS system the liquid crystal is directly applied to a CMOS IC. An IR transparent window is placed on top of the Liquid Crystal layer. This forms a sandwich structure where the CMOS IC is the base the Liquid Crystal is in the center and the IR transparent window is on top. The CMOS IC generates electrostatic fields that cause the rotation of the Liquid Crystal and thus the reflection or no reflection of the incident polarized IR light. The amount of voltage the CMOS IC generates directly controls the how much rotation the liquid crystal undergoes. The rotation of the liquid crystal determines the amount of phase retardation the incident IR light experiences. This in turn directly controls the amount of light that is reflected towards the output aperture of the LCoS IRSP [27].

The main design trade-off for LCoS systems is the thickness of the Liquid Crystal layer determines both the speed at which Liquid Crystal relaxes and the efficiency in which light is transmitted through the Liquid Crystal layer. The two are indirectly related to one another. Making the choice of Liquid Crystal thickness a very important design parameter.

2.0.2.4 Scanning Lasers

2.0.2.5 Superlattice LEDs

Infrared Light Emitting Diode (IRLED) displays have been demonstrated in a 512 x 512, a 1024 x 1024, and a 2048 x 2048 pixel resolutions. These IRLED displays have utilized Superlattice LED (SLED) devices. The reported IRLED displays have three major components: the SLED array, the Read-In-Integrated-Circuit (RIIC), and the Close Support Electronics (CSE). The SLED array is fabricated from cascaded InAs/GaSb Type-II superlattice segments that are coupled together with tunnel junctions [34]. Both $48 \mu m$ and $24 \mu m$ pixel pitch has been demonstrated. The SLED array is hybridized to the RIIC using an indium bump process. This gives the RIIC control over individual SLED pixels. Meaning arbitrary images can be drawn on the SLED array. The CSE takes input scene data and converts it into control signals and data to draw arbitrary scenes on the SLED array. Pixel radiance is controlled by the amount of current allowed to go through the SLED device. The more current the higher the output radiance of the SLED device is.

IRLEDs show great promise as an IRSP technology because of their inherent fast switching speed, and high in band radiance. Also the ability for the IRLED arrays to be cryo-cooled makes them a contender to replace resistor array technology eventually. Currently, there is a large wall-plug efficiency problem with IRLEDs. They have shown a less than 1% wall-plug efficiency.

Chapter 3

IR SENSOR TECHNOLOGY DEVELOPMENT

3.1 Introduction

The infrared spectrum consists of electromagnetic wavelengths from 700 nm to 1mm [43] . This is a useful part of the electromagnetic spectrum because hot objects display unique IR signatures. The spectral radiance of a hot object that is opaque and non-reflective (commonly called a black-body) is based on Plancks Law. Plancks Law describes the spectral density of the emitted electromagnetic radiation of a black-body that is at thermal equilibrium with the surrounding environment for a given temperature. Mathematically Plancks law is:

$$B_{\lambda}(\lambda, T) = \frac{2hc^2}{\lambda^5} \frac{1}{\exp \frac{hc}{\lambda k_B T} - 1},$$

This equation describes the spectral density, which is the amount of power in each wavelength of the observed signal. The equation shown above is the spectral density per wavelength of the signal. The spectral density is a function of temperature, T, and wavelength, λ . Some typical black-body curves for given temperatures are shown in Figure 3.1. The black-body curves for different temperatures have peak values at different wavelengths.

An object, such as a tea kettle like the one shown in Figure 3.2 has clearly distinct regions of higher and lower amounts of infrared radiation. These characteristics can be used to identify the tea kettle as a tea kettle. Some examples of information that can be learned from the image are that there is a hot liquid exiting the tea kettle. The heat transferred from the hot liquid is transferred to the tea kettle body and the shape of the tea kettle can be seen. The fact that there is a reservoir of hot liquid in

Figure 3.1: Example Planck's Law Curves for black-bodies at various temperatures.

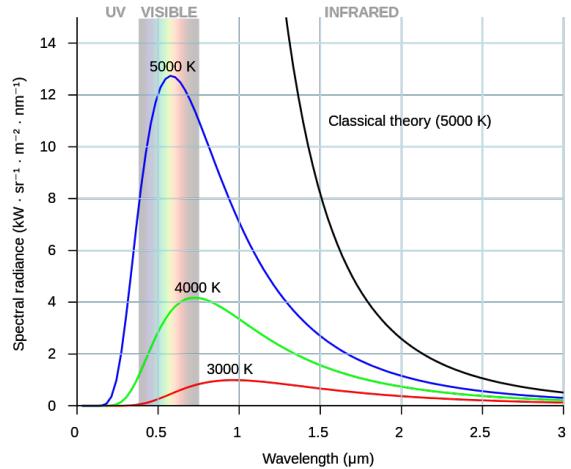
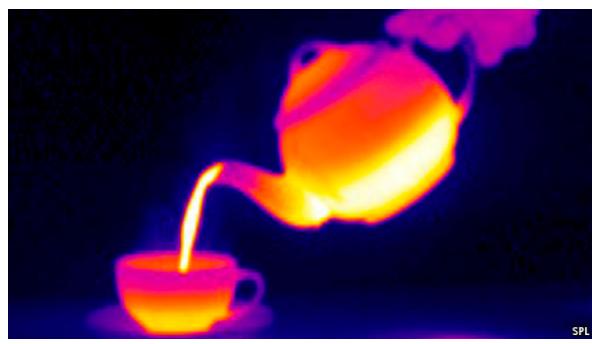


Figure 3.2: Infrared image of a tea kettle with hot water in it.



the bottom can be seen as well. All of these can be used to algorithmically determine that the object being viewed is a tea kettle. If only visible light data were used the knowledge that the object contained a hot liquid would be lost. And with it some knowledge about the function of this object.

A more complicated object to view in the infrared that yields a wealth of information is an aircraft. In Figure 3.3 an F18 is imaged with a FLIR SC8200. The most striking feature visible is the hot plume from the afterburner. Another feature in the image is the hot spot near the front of the aircraft. These features like the features of the tea kettle could be used to discriminate this aircraft from the background.

A review of the historical uses of infrared sensors is valuable to the reader to give some context about the importance and many uses of infrared sensors.

Figure 3.3: Flir,. FLIR SC8200 Imaging F18 With Afterburner At Close Range.. 2016. Web. 8 Mar. 2016.



3.2 Infrared Sensor Development

3.2.1 Early History (1800 - 1857)

3.2.1.1 Discovery of Infrared

Infrared light was discovered by William Herschel (17381822) on February 11th 1800.[38] He used a prism to split sunlight into different wavelength components. He marked on a piece of paper every quarter inch. In each quarter inch segment he placed a thermometer and measured the temperature rise over time. The existence of energy in the visible spectrum was readily apparent because it could be directly observed. The last quarter inch segment had no visible light, however Herschel noticed that a thermometer placed in this region also measured an increase in temperature over time[15]. He wrote in his paper to the royal society of London about this event:

”It being now evident that there was a refraction of rays coming from the sun, which, though not fit for vision, were yet highly invested with a power of occasioning heat[...]" [15]

This marked the first time that infrared light was measured and found to exist. The early stages of infrared scientific discovery revolved around using thermometers. Thermometers are inherently broadband devices because they absorb energy from a large portion of the infrared and visible light spectrum. This does not make them especially accurate scientific instruments for analysis of small wavelength bands.

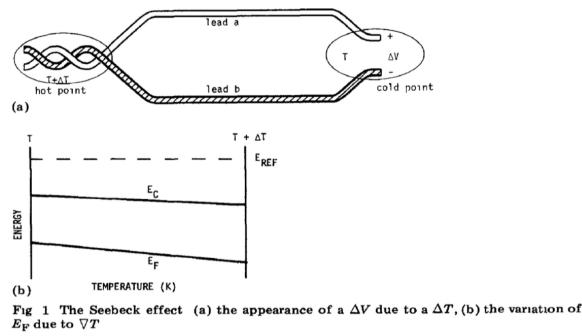
3.2.1.2 Seebeck Effect

It was not until 1821 when Thomas Johann Seebeck discovered what is now called the Seebeck Effect, which later became a part of the Thermoelectric effect, that a more accurate method of measuring infrared radiation was invented. The Thermoelectric effect is when two metal conductors are joined together and that joint is heated. Here I will call this the hot point. There is a corresponding cold point, which is spatially distant from the hot point. The two wires are not joined together at the cold point. A space is left for a voltmeter to be inserted into the circuit formed by the metal wires. A voltage is then observed between the two cold point wire leads. Usually two

dissimilar metals are used when constructing a thermocouple. For example Seebeck used Antimony and Copper [38].

The observed voltage at the cold point is proportional to the difference between the temperature at the hot point and the cold point [14]. The observed voltage is not inherently due to the junction because the Seebeck Effect is a phenomena related to the bulk material properties [14]. The two dissimilar metals increase the voltage seen because one metal conductor will cause a positive voltage and the other metal conductor will cause a negative voltage. Together the voltage drop across the two metals will be greater than the separate components. The voltage observed across a metal conductor in the Seebeck effect is on the order of $\mu V \setminus K$ [38].

Figure 3.4: Diagram of a Thermocouple [16]



In general, the mechanism by which the Seebeck Effect causes a voltage to appear across the two conductors is that at an atomic level the thermal energy input enables electrons from the material with a lower Fermi Energy to migrate to the material with a higher Fermi Energy. The electron migration and the increase in the energy level of the electrons that migrate causes a electromotive force [14][40].

Different materials have different Seebeck coefficients and create varying amounts of voltage across them for different temperatures applied to them. The importance of this effect for this dissertation is that for the first time in history thermal energy was able to be converted directly into electrical energy.

This new found ability opened the door many years later on to the possibility of using electronic systems to detect thermal changes.

3.2.1.3 Peltier Effect and Thomson Effects

Jean Charles Athanase Peltier (J. Peltier), discovered the second thermoelectric effect [38]. In his experiments, he found that passing an electric current through a bismuth-antimony thermocouple junction caused heating or cooling depending on the direction of the current flow[36]. The heat or lack thereof generated by this effect was known as the Peltier Heat. J. Peltier found that the the Peltier Heat was proportional to the magnitude, I, and the duration, dt. This is expressed in the following equation:

$$dQ_p \propto Idt \quad (3.1)$$

$$= \pi_a b I_a b \quad (3.2)$$

$$= \pi_a b q \quad (3.3)$$

Here $\pi_a b$ is a proportionality coefficient and called the Peltier coefficient, and q is the charge transported. This gives us a way to calculate the amount of heat per charge that can be added or removed from a system. In this equation $dQ_p > 0$ means that heat is being absorbed by the system [48]. One point to note is that the Peltier heating and cooling effects oppose the generation of Seebeck voltages. This is important to maintain energy conservation because otherwise the two effects would add in a positive feedback loop.

J. Peltier reported these findings in his 1834 paper, "Nouvelles expriences sur la caloricit des courants lectrique", submitted to the Annales de Chimie et de Physique. He also reported the close relationship of the Peltier coefficient and the Seebeck coefficient. Peltier observed that for a given externally applied current the rate of absorption or liberation of heat at a thermoelectric junction depended on the value of the Seebeck coefficient of the junction. [48]. This was later proven analytically by Thomson in 1854.

Thomson used the first and second laws of thermodynamics to analyze a thermoelectric circuit. He arrived at the following equation:

$$\dot{q} = -K \mathbf{J} \cdot \nabla T \quad (3.4)$$

In this equation it is shown that the Seebeck coefficient and the Peltier coefficient are related by a simple proportionality constant. Thomson also went on to predict and show that a material can have a Seebeck coefficient that is not constant in temperature. When an electric current is passed through such a material the gradient of the Seebeck coefficient must be taken into account. This requires an integration and creates a continuous solution [42].

The thermoelectric equations all together are:

$$\mathbf{J} = \sigma(-\nabla V - S \nabla T) \quad (3.5)$$

$$\dot{e} = \nabla \cdot (\kappa \nabla T) - \nabla \cdot (V + \Pi) \mathbf{J} + \dot{q}_{ext} \quad (3.6)$$

$$-\dot{q}_{ext} = \nabla \cdot (\kappa \nabla T) + \mathbf{J} \cdot (\sigma k^{-1} \mathbf{J}) - T \mathbf{J} \cdot \nabla S \quad (3.7)$$

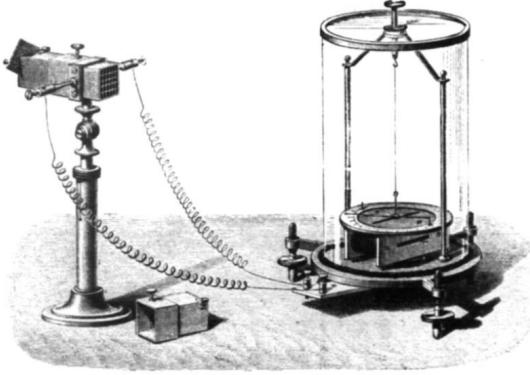
3.2.1.4 The Thermocouple and the Thermopile

Thermocouples and Thermopiles use the Seebeck effect to detect Infrared radiation. As noted in the previous section the Seebeck effect creates an electromotive force that is proportional to the temperature difference between the hot point and the cold point. A Thermocouple is a single Seebeck effect joint, while a Thermopile is several Thermocouples connected in series with one another. The series connection of the thermocouples creates a higher output voltage, which is easier to measure [17]. These devices were the first infrared detectors [17].

Thermocouples and Thermopiles were first invented in the 1830s by L. Nobili and M. Melloni [38]. L. Nobili invented the thermocouple based on Seebecks work, and later M. Melloni invented the thermopile by connecting bismuth-copper thermocouples in series [38]. At the time M. Melloni called his instrument a thermomultiplicateur

[3]. The thermomultiplicateur consisted of a series of thermocouples and an astatic galvanometer connected to the output to measure the voltage of the combined thermocouples. M. Melloni's thermopile used bismuth and antimony rods that were 1mm thick, 2mm wide, and 20 mm long. The sensitivity of the instrument was estimated as being some forty times greater than that of a sensitive liquid-in-glass thermometer, and was sufficient to indicate the radiation from a person at a distance of 25-30 ft. [3]. Finally, 30 years after Herschel discovered Infrared light a more sensitive measurement instrument was developed.

Figure 3.5: M. Melloni's Thermomultiplicateur [3]



3.2.2 The Bolometer

Samuel Pierpont Langley invented the bolometer in 1880. The bolometer is a thermal energy sensing device that deserves some explanation due to its continued use in infrared camera systems.

The bolometer uses an absorbing material that increases in temperature at a well known rate for a given incident radiant power, P . The temperature increase of the absorbing material is measured with a electrical resistance thermometer. The absorbing material is placed in contact with a thermal reservoir of constant temperature. When radiation is incident upon the absorbing material it increases the temperature of the absorbing material above the temperature of the reservoir tank at a well known constant

rate. This rate is defined as: $dT_B/dt = P/C$. Where P is the incident radiant power, T_B is the temperature of the absorbing material, and C is the heat capacity of the material [37]. Eventually T_B reaches a steady state value of: $T_B = T_S + P/G$ [37]. Where T_S is the temperature of the heat sink and G is the thermal conductance of the material attaching the absorbing material to the heat sink reservoir [37]. Bolometers are still used today in modern camera designs. Modern bolometer based camera systems use micro-bolometers arrays typically constructed out of Vanadium Oxide or amorphous Silicon resistors [30]. In the early history of infrared sensor design scientific exploration motivated the advancement of sensor technology. In the early 1900s the focus shifted to two main areas of interest: infrared spectroscopy and military applications.

3.3 Pre-Quantum Mechanics Period (1857 - 1900)

Smith reported on the first photonic effect, photoconductive effect, in a short note in the February 20th 1873 edition of the journal Nature. He reported that he purchased some Selenium bars and measured their resistance while they were in a closed container and then when he opened the container the resistance changed drastically [1].

The discovery of photonic effects continued with the discovery of the photovoltaic effect. W.G. Adams and A.E. Day showed in 1876 that illuminating a junction between selenium and platinum has a photovoltaic effect [?]. Hertz showed the phenomena of photoemission in 1887 when he used to ultraviolet light to illuminate a coupled coil in a spark gap experiment. The experiment consisted of two coils coupled. A spark was generated in the primary coil and the time delay was observed in the secondary. Illuminating the secondary coil caused a change in the nature of the spark produced in the secondary [6]. A photoelectric effect caused by visible light was discovered by Elster and Geitel in 1889 when they observed an alkali metal being illuminated [?] In 1900 Rayleigh and Jean developed the Rayleigh-Jean Law. This law related spectral radiance for a blackbody to wavelength. This law fit the data well for low frequencies, but not for high frequencies. It was not until Planck theorized the packetization of

energy and wrote Plancks law that all wavelengths could be accurately described by an equation.

3.4 Quantum Mechanics Period (1900 - 1929)

Max Planck resolved the Ultraviolet Catastrophe by deriving a spectral density formula based on an electrically charged oscillator in a cavity that could only change its blackbody radiation by discrete value. This view of energy as having a smallest unit or quanta ushered in what I am calling here the Quantum Period.

Coblentz a few years later used thermopiles to survey 110 stars and starts the infrared astronomical spectroscopy field [38]. In 1905 Einstein showed that light is also quantized into photons. Some of the first military applications are conducted by Theodore W. Case in 1917.

Theodore W. Case found performed a large assay of materials looking to empirically determine which materials were photoconductive. He reported his findings in his 1917 paper Notes on the Change of Resistance of Certain Substances in Light. In the paper he reports that sulphide salts were photoconductive. Two specimens which show remarkable action are acicular crystals of bismuth sulphide (bismuthinite), and a granular lead antimony sulphide [7]. This sparked the interest of the military during World War I and lead to the military funding Case to develop covert signalling technology. Case eventually constructed an apparatus with a thallous sulfide detector that was able to transmit a message 18 miles [18]. His project was eventually defunded due to the thallous sulfide detector having many issues. This however was just the beginning of the military interest in Infrared Detector technology.

3.5 Military Application Period (1929 - 1970)

During the first world war the British military were interested in detecting the hot surfaces of aircraft to detect them. This work was done on a smaller scale in parallel with the radar research being conducted by the British at that time. The research was primarily conducted by Reginald Victor Jones (R V Jones). The research

team mostly consisted of just Jones. He eventually built a prototype consisting of an infrared detector, a telescope, signal amplifiers, and a galvanometer. This prototype was able to detect single engine aircraft up to two miles away. It was inferior to radar due to a lower range, and lack of ability to detect the range of the aircraft [18]. This idea of detecting aircraft with infrared detectors would be revisited when detector technology improved.

In America, Robert J. Cashman started working in 1935 to extend Cases work and produce a more stable detector. He eventually succeeded and the National Defence Research Counsel (NDRC) funded a production run of 6800 of the sensors [18].

At about the same time as Cashmans work the Radio Corporation of America (RCA) developed a Infrared Imaging tube and mass produced it. An imaging tube connects a near-IR cathode to visible phosphors. This converts the response of the near-IR cathode to visible light that a human can see. Effectively, letting a user see infrared light. The RCA Imaging tube was called the 1P25 image converter. The 1P25 was produced in 1942 and was used in the Snooperscope and Sniperscope as early night vision [38] for night time operations.

In 1941, an important discovery was made Russel Ohl of Bell Laboratories. He discovered both the p-n junction and the photovoltaic properties of the p-n junction. This discovery would lead to solar cell creation, and modern electronic IR cameras [35].

In Germany, the lead sulphide detector was heavily researched and developed. Research started when Edgar W Kutzscher at the University of Berlin started to study PbS detectors in 1932. Infrared research in Germany was more exploratory and innovative than in either Britain or America. The Kiel IV was the first successful airborne infrared system. It had a much greater range than the British counterpart [18]. The greater sensistivity and success of the Kiel IV was most likely due to the Germans greater study of thin film deposition techniques and other manufacturing techniques [38]. In America, Cashman also studied lead sulphide detectors after producing a refined and more robust thallic sulfide detector.

In the 1950s an application of note was the Sidewinder heat-seeking infrared

guided missile. The Sidewinder used PbS, PbSe, and InSb detectors over their service lifetime. Initially, the detectors were uncooled and later they were cooled to decrease self generated noise in the detector material [38]. The imagers in the Sidewinder used scanned single-element detectors and linear arrays in the MWIR (3 - 5 microns) region.

The 1950s and 1960s saw the an explosion in material research in extrinsic detectors. These new detectors were narrowband and used materials in the III-V, IV-VI, II-VI systems. In 1959 the HgCdTe alloys were discovered. With the HgCdTe alloys it was possible to perform bandgap engineering and select many different sensitivity ranges. The 1960s also saw the first production of the first Forward Looking Infrared (FLIR) system. It operated in the Long Wave Infrared (LWIR) and used a Hg-doped germanium linear array. The 1960s also saw the first research being conducted on Si detectors.

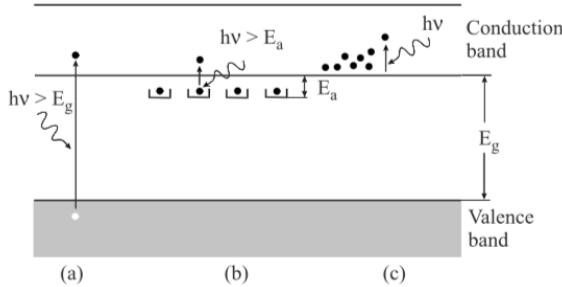
The Vietnam War put pressure on the military to develop imaging systems that could detect vehicles, people, and buildings. At present work is focused on multi-spectral, higher frame rate,

3.6 Types of Infrared Sensors

There are many types of Infrared Sensors. [38] has a succinct list of the different infrared sensor technologies. "[...] thermoelectric power (thermocouples), change in electrical conductivity (bolometers), gas expansion (Golay cell), pyroelectricity (pyroelectric detectors), photon drag, Josephson effect (Josephson junctions, SQUIDs), internal emission (PtSi Schottky barriers), fundamental absorption (intrinsic photodetectors), impurity absorption (extrinsic photodetectors), low dimensional solids [superlattice (SL), quantum well (QW) and quantum dot (QD) detectors], different type of phase transitions, etc."

Given all of these different technologies for sensing infrared radiation there are really only two broad categories of infrared sensors. There are photonic sensors and thermal sensors. Photonic sensors are characterized by their use of the photoelectric effect to convert infrared radiation into proportional electric signals [8].

Figure 3.6: Fundamental optical excitation processes in semiconductors: (a) intrinsic absorption, (b) extrinsic absorption, (c) free carrier absorption.[38]



3.6.1 Photonic Sensors

Photonic detectors work through optical excitation of a semiconductor material. Photons enter the material and elevate electrons from the valence band to the conduction band. The change in energy distribution can be measured with electronic circuits and the amount of incident radiation on the material can be calculated from the change in energy distribution.

There are also some photonic sensors that use internal photoelectric effects in a photovoltaic cell to detect incident light energy [8]. These work in a similar manner to the previously mentioned photonic sensors, but the electrons being elevated to the conduction band are inside of the bulk material rather than on the surface.

Photonic detectors have several advantages, chief amongst them are good signal-to-noise performance and a very fast response time [38]. Photonic sensors have some limitations as well. The chief limitation is that they are spectrally band limited. A photonic sensor is not a broadband device. It will respond to specific wavelengths of light, but not to wavelengths of light outside of its band. It is also important to minimize the thermal generation of carriers in a photonic sensor because this will create noise on top of the desired signal. Normally, photonic sensors are cooled to cryogenic (77 Kelvin) temperatures to mitigate this issue.

3.6.2 Thermal Sensors

A thermal detector is a broadband device that absorbs thermal energy in an absorbing material. The absorbing material temperature increases as more energy is incident upon it. The temperature of the absorbing material is read with a thermocouple or some other device that converts temperature into a proportional electric signal. Thermal sensor devices differ greatly from photonic sensors because their response does not depend on the spectral content of the radiant power [38]. These devices consist of an absorbing material that is attached to a supporting structure. A digital thermometer is integrated into the design to read the temperature of the absorbing material.

Part I

IRLED IRSP CHARACTERIZATION

Chapter 4

IRSP AND IR SENSOR MODELS

4.1 Sensor Model

The simplest model for a sensor is a delta function convolved with the time series of the input radiation on the detector. The delta function lets the sensor sample the input time series at discrete intervals like a real sensor would do. Mathematically it would look like this:

$$CameraResponse = [Rad * \delta][n] = \sum_{k=-\infty}^{\infty} Rad[m]\delta[n - m] \quad (4.1)$$

In Equation 4.1 the *Rad* function is the input time series of the Radiation incident upon the sensor. The *Rad* function is convolved with a delta function to produce a sampled *CameraResponse* output function. Sampling frequency can be increased by decreasing the difference between index values, *n*. The faster the input time series is sampled the higher the frequency of observed signals is possible. This is due to sampling theory as described by Shannon.

Unfortunately, the ideal sensor described here can only view one point in space at a time. Arrays with pixel elements made up of ideal sensors called staring arrays or focal plane arrays (FPAs) have been made that sample multiple points in space at a time. An array of ideal sensor elements can be described with a matrix where each

element in the matrix consists of an ideal sensor with a corresponding CameraResponse function denoted here as Z .

$$\begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & \dots & Z_{1a} \\ Z_{21} & Z_{22} & Z_{23} & \dots & Z_{2a} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ Z_{b1} & Z_{d2} & Z_{d3} & \dots & Z_{da} \end{bmatrix} \quad (4.2)$$

This model makes several assumptions in order to remain simplistic. These assumptions are listed below.

1. The sensor is sensitive to a certain spectrum.
2. The sensor has a uniform response across the spectrum.
3. The sensor has a linear output.
4. The sensor does not require an integration period.
5. The sensor data can be read instantaneously.

4.2 Ideal IRSP Model

An Infrared Scene Projector (IRSP) seeks to accurately represent the infrared emission of an actual physical hot object. An IRSP is a two-dimensional array of pixels that emit in the infrared spectrum. These pixels are used to display infrared scenes to an infrared sensor. The goal of the IRSP is to approximate the infrared emission of an actual hot object in order to simulate an actual scenario involving one or more hot objects.

Referring back to Owen William's sixth point an ideal IRSP must operate fast enough to ensure the sensor under test behaves as if it would in a real scenario. Frame time is a useful measure of an IRSP temporal performance because it is a property of how the IRSP functions. An IRSP receives video data and then draws and displays each frame of the video one at a time. The faster the frames of the video can be drawn and displayed the higher the frequency that can be accurately observed by the sensor.

An ideal IRSP would have zero latency between projected image frames. The physical world contains continuous systems, and thus can be sampled at any point in time and receive new data. Another way of looking at this is that there is a constant flow photons leaving physical hot objects and not discrete steps larger than the Planck constant.

An ideal IRSP can be conceptualized as having pixel elements that can be commanded to higher or lower radiance based on a control signal. Assuming the control signal is a voltage level that directly corresponds to projected radiance, in the simplest case every pixel would have its own digital-to-analog converter (DAC) that would create the control signal. This situation would have the least amount of update time for a new frame because the frame update would be limited by the time it takes the DACs to reach the desired values. This would yield a frame update rate given by Equation 4.3. Where settling time is the time it takes the DAC to reach the desired value. Settling time is discussed more in depth in Chapter 8.

$$T_{(DAC_settling_time)} \quad (4.3)$$

We now have a case where if $T_{(DAC_settling_time)}$ is at least twice as fast as the sampling rate of the ideal sensor the ideal sensor would view the IRSP image as indistinguishable from the actual hot object. An IRSP and sensor under test where the IRSP has a frame rate at least twice as fast as the sampling rate of the sensor can be run in an un-synchronized manner. This means that the IRSP and the sensor can operate completely independent of one another. This offers a potentially easier test setup and the ability to simply treat the IRSP imagery as a physical scenario, but places a heavy requirement on the IRSP to achieve very fast frame rates.

A synchronized system offers the ability to have the same frame update rate on the IRSP and the ideal sensor. This is possible because the IRSP and the sensor operation are synchronized. When the IRSP finishes updating the projected image the sensor then will sample the image. The operation of the two devices are controlled with the same clock signal. This is why it is called a synchronized system.

4.3 Realistic IRSP

4.3.1 Frame Time

In the ideal model of an IRSP there is a DAC for every pixel in the IRSP array. This is not a feasible design goal because IRSP resolutions typically range from approximately 200,000 pixels to over 4 million pixels. The number of DACs required to individually drive each pixel would be cost prohibitive and un-manageable. A simple realistic IRSP would have one DAC that is used to sequentially drive every pixel in the array. The desired pixel must be selected by addressing circuits. Then the DAC is commanded to the desired value to produce the desired brightness. The output signal from the DAC must first reach the RIIC pixel over a transmission medium. This gives rise to another time constant, $T_{transmission}$. This gives a frame time of:

$$Frame_time = number_of_pixels \times (T_{Address_time} + T_{transmission} + T_{DAC_settling_time}) \quad (4.4)$$

This will be a significantly longer frame time than the ideal IRSP. Luckily, this frame time can be reduced with the use of a multiplexing architecture and multiple DACs. If it were possible to write to two pixels at once the frame time would be reduced by half. The more DACs that are added the lower the frame time becomes and the closer the ideal IRSP is approximated. With a multiplexing architecture N DACs can be written at once. This yields an equation for frame time that looks like this:

$$Frametime = \frac{(number of pixels)}{(NDACs)} * (T_{address_time} + T_{transmission} + T_{DAC_settling_time}) \quad (4.5)$$

These equations are not quite correct yet as they do not account for the rise time of the pixel elements. The pixel element rise time is defined as the time it takes a pixel element to reach the desired radiance after power is applied to the pixel element. The DAC settling time and the pixel element rise time can be combined into a system level

measurement that will be called the optical rise time. The optical rise time determines the amount of time required to write to an individual pixel. This is called the pixel time. The pixel time is related to the frame time by multiplicative factor, which is simply the number of pixels in the frame. Accurately knowing the optical rise time determines the minimum frame time that is achievable. The optical rise time also determines at what rate the sensor can sample while maintaining a good approximation of a physical hot object.

4.3.2 Bit Resolution

Hot objects emit radiation in a continuous spectra. Unfortunately, a digital system is limited to discrete values. The number of values that a digital system can represent is called the bit resolution. Equation 4.6 is an equation that relates the number of bits to the number of possible represented states in a system. In this equation, n is the number of bits. An example, is a 2-bit system that has 4 states.

$$\text{number_of_states} = 2^n - 1 \quad (4.6)$$

The higher the bit resolution of an IRSP the more accurately the IRSP can approximate the continuous output spectra of a hot object.

The next few sections are concerned with presenting methods that were used to measure the system level optical rise time, and the DAC settling time. These metrics were used to characterize the electronic hardware being used to drive the thermal pixel elements in an IRLED Scene Projector and determine their accuracy. The simple models here are used to understand measurement results obtained from experiments that measure the optical rise time and bit resolution of the IRLED IRSP under development in the CVORG laboratories. Chapter 5 discusses the optical rise time measurements and experimental setup used to obtain the measurements. Chapter 8 discusses how to measure settling time and system bit resolution.

Chapter 5

RISE TIME OVERVIEW

From Chapter 4 we have a basic model describing the time it takes to write one frame of a simplistic IRSP with some physical constraints accounted for in a non-multiplexed architecture. That equation is:

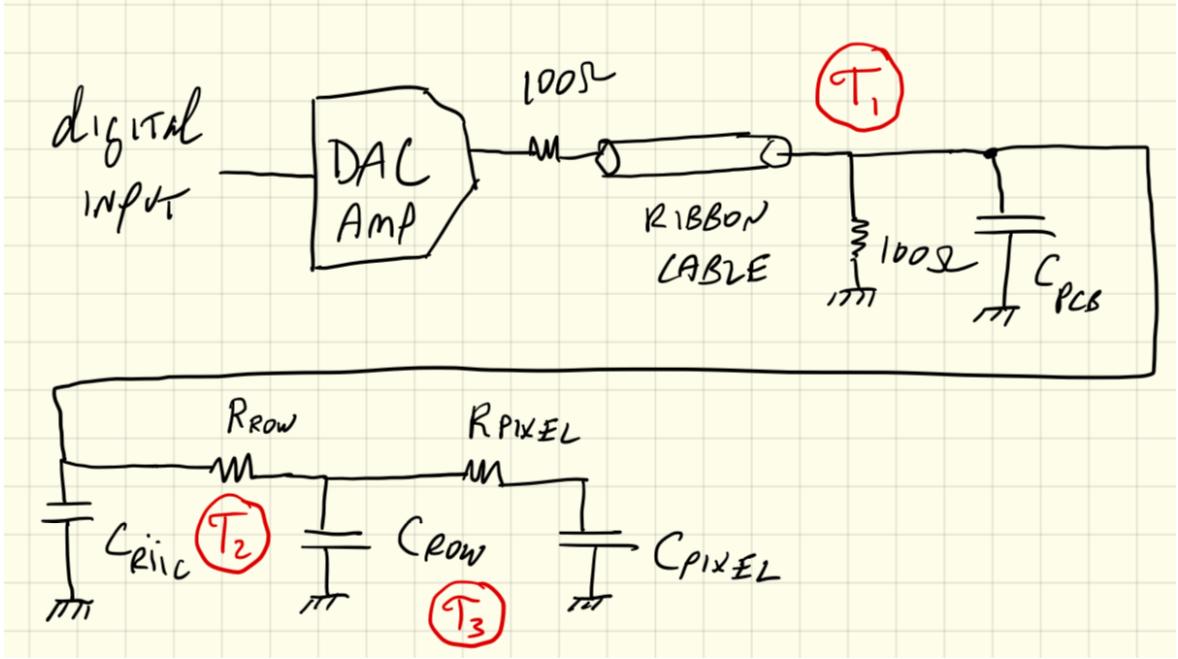
$$Frame_time = number_of_pixels \times (T_{Address_time} + T_{transmission} + T_{DAC_settling_time}) \quad (5.1)$$

This simple model is made even more realistic in this chapter by including timing constraints that are specific to the IRLED IRSP being developed in the CVORG Laboratories. Only the analog signal timing constraints are explored here because they were determined to dominate the relatively instantaneous digital addressing time constants. This chapter also goes on to describe a method for measuring optical rise time with the CVORG IRSP, the measurement results of these experiments, and the a discussion of the meaning of the results.

5.1 CVORG IRLED IRSP Analog Signal Model

In Figure 5.1 there are the three time constants labeled T_1 , T_2 , and T_3 . T_1 describes the time required for the signal to reach maximum value given the resistance (R) and capacitance (C) of the termination network, and the impedance caused by the transmission line that transmits the signal from the output of the DAC to the RIIC. T_2 describes the RC time constant caused by the decoder logic used for addressing individual pixels in the RIIC. T_3 describes the internal node RC time constant of a RIIC pixel. Each of these time constants adds to the overall rise time of an individual pixel in the IRLED IRSP. The time constants are listed in equations 5.2, 5.3, 5.4.

Figure 5.1: Analog signal timing constraints.



$$T_1 = (100\Omega || 100\Omega)(C_{PCB} + C_{RIIC}) = 50\Omega [C_{PCB} + C_{RIIC}] \quad (5.2)$$

$$T_2 = R_{Row}C_{Row} \quad (5.3)$$

$$T_3 = R_{Pixel}C_{Pixel} \quad (5.4)$$

These equations ignore the possible effects on the signal from the inductive transmission lines used to transmit the signals to the RIIC. To assess the effect of ringing caused by the transmission lines a simulation was conducted that extracted layout parasitics of the RIIC. The simulation is detailed in Section 5.5.

5.2 Measurement Methodology

In general, the measurement methodology used to measure optical rise time was to vary the length of time that the capacitive storage node in the pixel was written to. A longer time writing meant that the storage node would have a voltage applied

to it for a longer period of time. This is conceptually similar to charging a simple RC circuit. The longer the voltage is applied the higher the voltage on the capacitor.

While, the measurement methodology is conceptually simple to actually perform the measurement with the IRLED IRSP a thorough understanding of how the components in the analog signal pathway work is required. The next section describes how the Oslo RIICs in general operate.

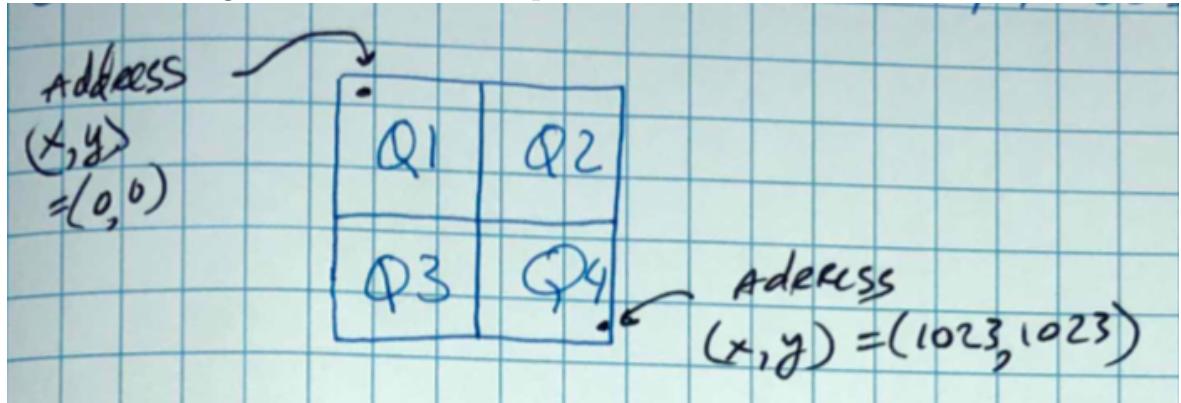
5.2.1 How Oslo Architecture IRSPs Draw

There are four quadrants in a RIIC. Each quadrant consists of an individual 512 x 512 RIIC. Smaller 512 x 512 RIICs that are connected together are used instead of one large monolithic RIIC for ease of layout and design, and due to the limit of photolithography mask sizes.

Due to input / output pin limitations in the Dewar the 512 x 512 quadrants are connected in parallel and four special control signals are used to choose which quadrant is being addressed. This special pin is:

1. WEN0 - write to Q1
2. WEN1 - write to Q2
3. WEN2 - write to Q3
4. WEN3 - write to Q4

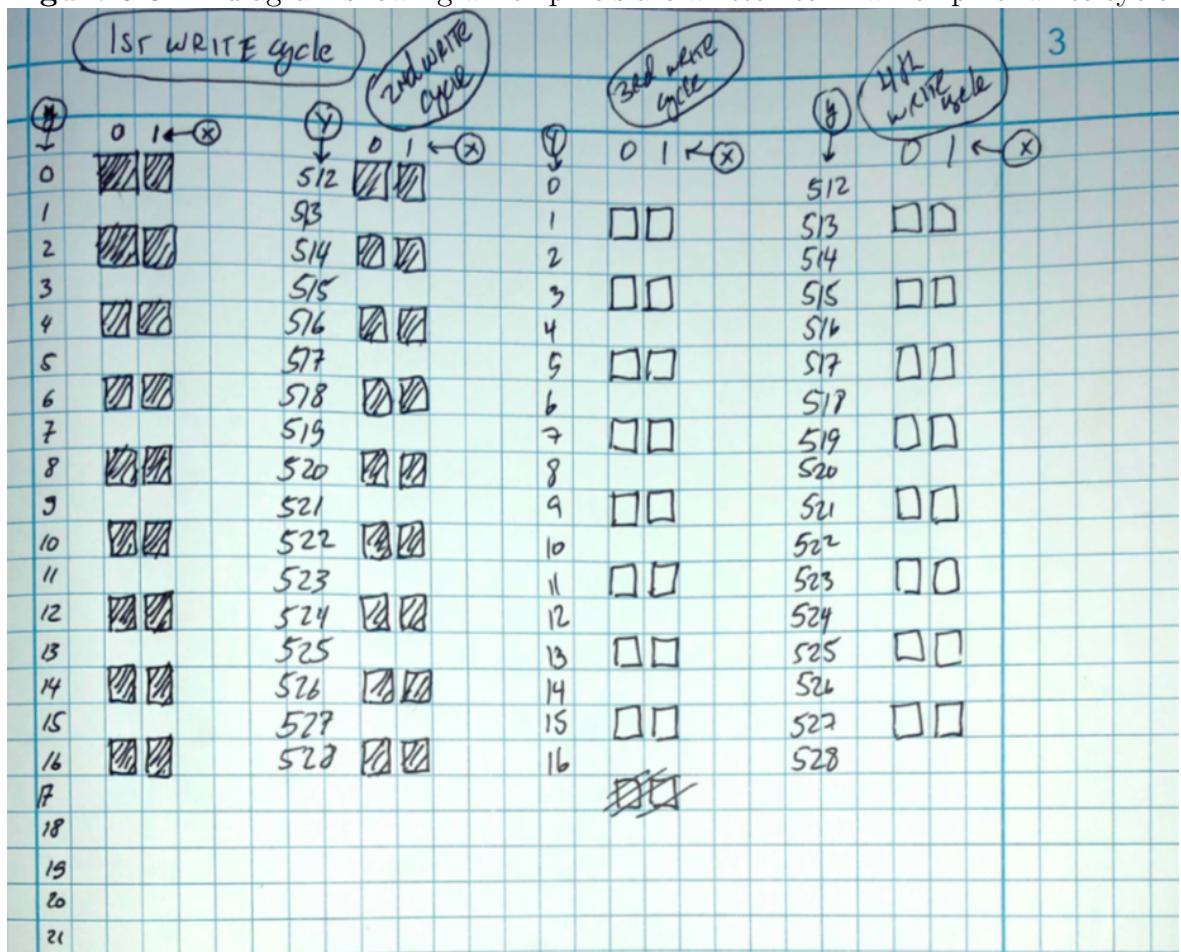
Figure 5.2: A diagram showing the four quadrants of the Oslo RIIC and the addressing for the first and last pixels.



5.2.2 Pixel Write Cycle

In the Oslo RIIC Architecture 32 pixels in a column are written at the same time. A one time write of a set of 32 pixels is called a "pixel write cycle." Figure 5.3 shows that in the "First Write Cycle" 32 pixels in the first quadrant of the RIIC are written to in parallel. The "Second Write Cycle" shows that the same 32 pixels that were written to in the "First Write Cycle" are written to in the second quadrant. The "Third Write Cycle" and "Fourth Write Cycle" are not shaded because the Y values for the third and fourth quadrant of the RIIC are in the 512 - 528 range.

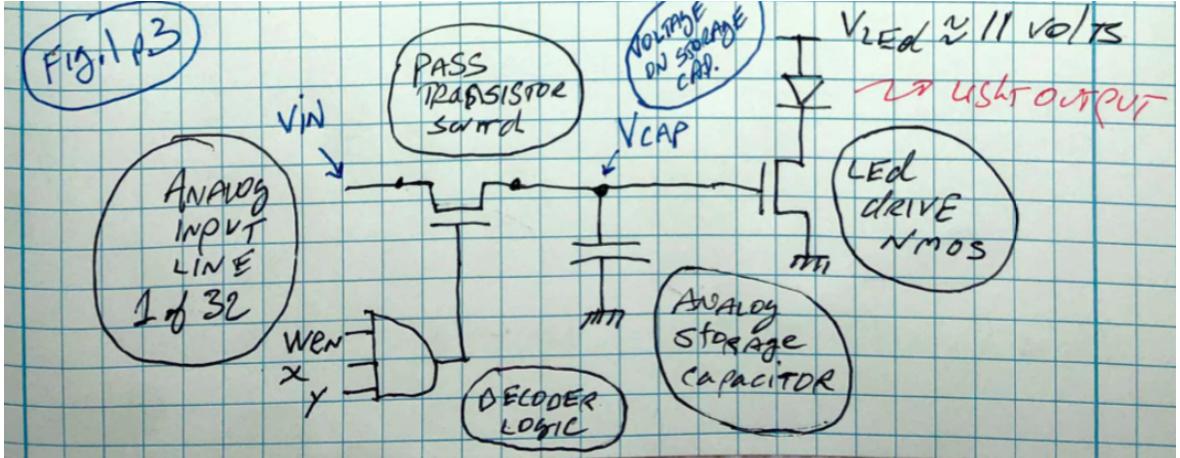
Figure 5.3: A diagram showing which pixels are written to in which pixel write cycle.



5.2.3 Conceptual RIIC Pixel Schematic

Figure 5.4 in the simplest case the process to write to a pixel is to set the analog voltage that is desired. The analog voltage then charges the capacitive node on the pass transistor switch. The address bits are set and the circuit awaits the appropriate WEN signal to latch the analog voltage into the pixel capacitive node. The internal pixel capacitive node is labeled " V_{cap} ".

Figure 5.4: A diagram showing a high level overview of the internal circuitry of a RIIC pixel.



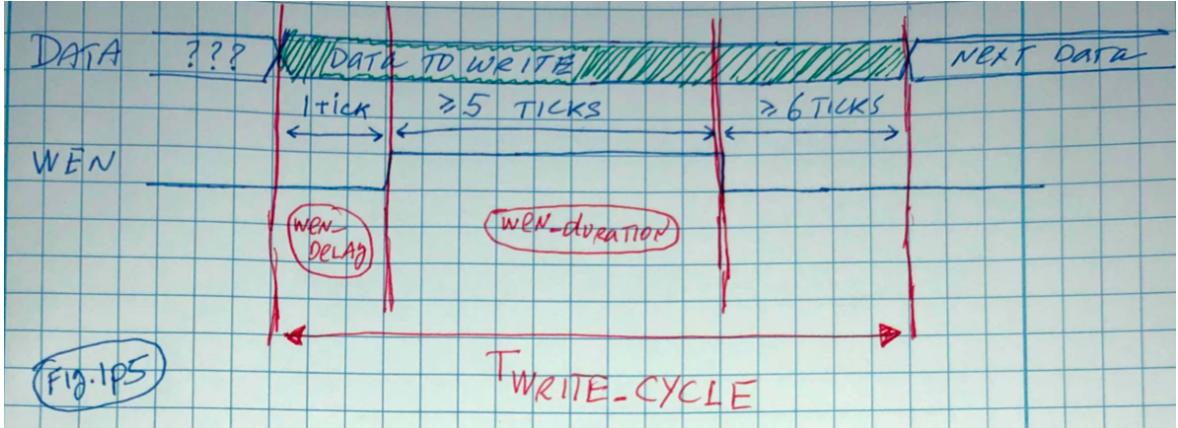
5.2.4 Pixel Write Timing

In Figure 5.5 a timing diagram for a single pixel write is shown. Time is given in units of ticks, which correspond to one clock cycle of the CSE FPGA. The CSE FPGA currently runs at 200MHz. This makes one tick equal to 5ns. The diagram shows the WEN pulse duration, the WEN delay, and the data being written.

The total duration of the pixel write cycle is determined by the frame rate and the array resolution. For example, for 100Hz and 1 Megapixel, there is a time budget of 10 mSec to write 10^6 pixels. The ideal pixel write cycle can be determined by dividing the time budget by the number of pixels in the array and then multiplying that result by the number of RIIC analog inputs. For the example given above this yields equation 5.5.

$$IdealPixelWriteCycle = 32 \times \frac{10ms}{10^6} = 32 \times \frac{10 \times 10^{-3}}{10^6} = 320ns \quad (5.5)$$

Figure 5.5: Timing diagram for writing to a pixel.



5.3 Actual Pixel Write Cycle

The IRLED IRSP uses standard HDMI decoder ICs that adhere to the HDMI standard. The HDMI standard protocol incurs several fixed time costs that shorten the actual Pixel Write Cycle. The HDMI protocol requires the use of a front porch and a back porch. The front porch and the back porch separate pixel drawing signals from the sync signals required to demarcate the end of a horizontal line and the end of a frame.

Figure 5.6 shows the timing diagram for the IRLED IRSP operation with the front porch and the back porch overlaid on top of the other timing information. Figure 5.6 shows plots for array Data, Frame VSync, Camera Integration Time, and Array Reset. During the Front Porch the camera integrates and the IRLED array is reset.

At 100Hz operation and with 1 MegaPixels the actual Pixel Write Cycle is 45 Ticks or 225ns. At 400 Hz operation and 1 MegaPixels the Pixel Write Cycle is 11 Ticks or 55ns. As can be seen the Pixel Write Cycle shortens dramatically as frame rate increases. This places a heavy demand on the electronics used to address and set the values of each individual pixel element.

For NSLEDs the WEN Delay is chosen as 5 Ticks, and the WEN Duration is

Figure 5.6:

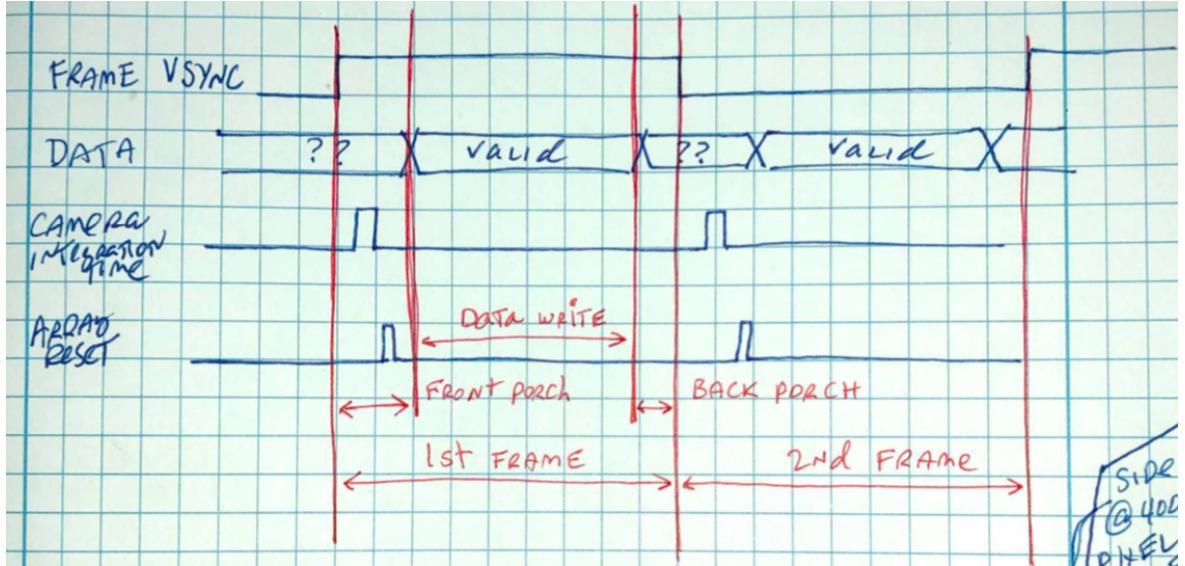


Table 5.1: NSLEDs WEN settings for different frame rates.

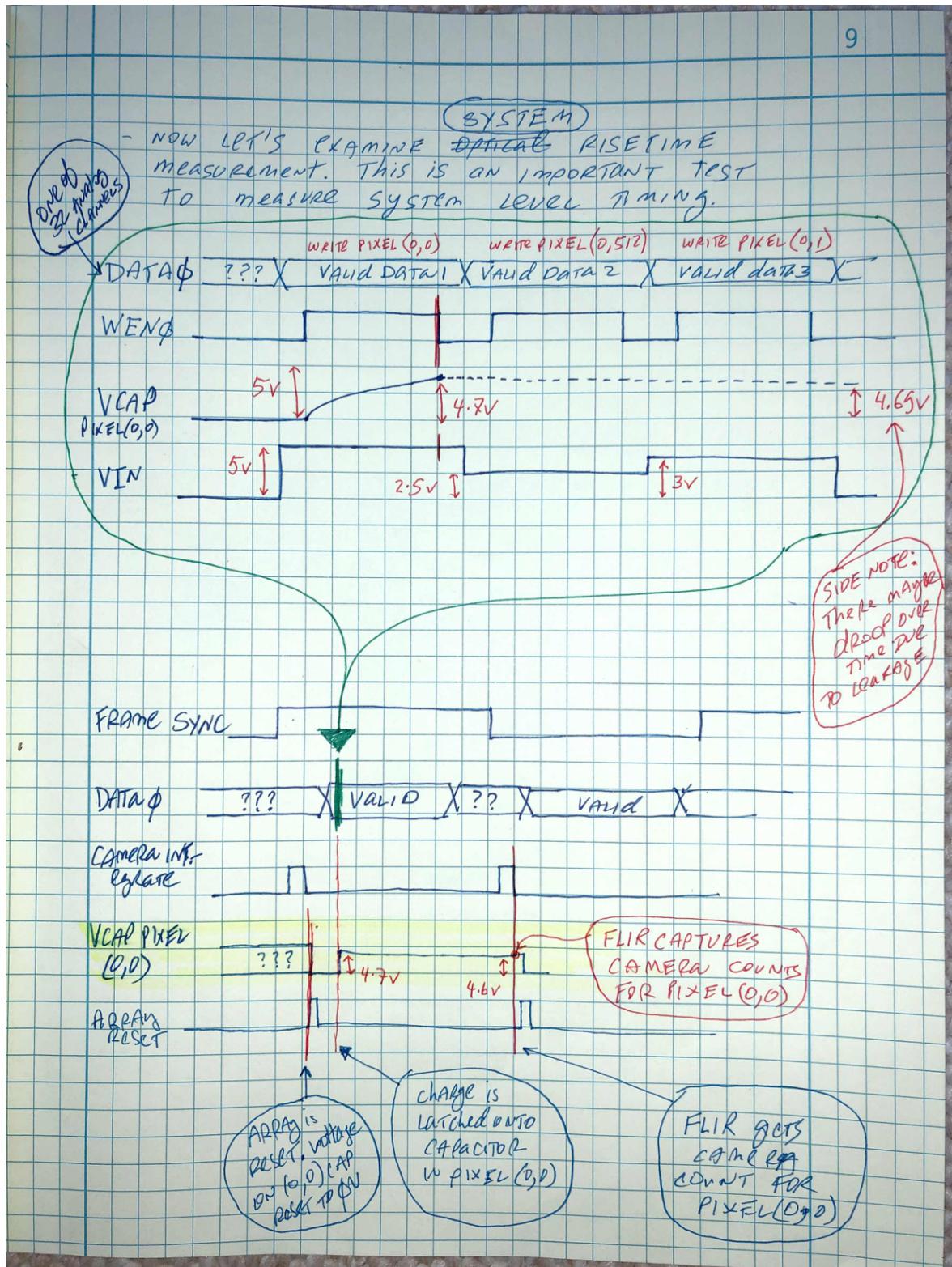
Frame Rate, MP	WEN Duration (Ticks)	WEN Delay (Ticks)
100Hz, 1MP	30	5
400Hz, 1MP	5	1

chosen as 30 Ticks at 1 Megapixel and 100Hz operation. At 400Hz and 1 Megapixel operation the WEN Delay is chosen as 5 Ticks, and 1 Tick. These values are summarized in Table

5.4 System Rise Time Measurement Method

In Figure 5.7, the top half shows the timing diagram for the IRSP. The Data, WEN, pixel analog storage node (VCAP), and the input analog voltage (VIN) are shown. The data is written and pixel (0,0) in this case is chosen. The VIN signal is set by the analog electronics. The WEN signal transitions and loads the VIN signal onto VCAP. VCAP rises to full value with time constant T_3 . The data selecting the

Figure 5.7: IRSP and camera timing diagram.



next pixel is written and a new VIN voltage is set and latched into the next pixel to be drawn to.

The plots in the bottom half show the same events from the cameras perspective and add additional information about camera functions. Here the array is first reset. Then the IRSP selects the pixel and sets the voltage on VCAP. VCAP droops a small amount due to leakage on the analog storage capacitor. The camera then integrates right before the next frame starts.

5.5 Analog Signal Transmission Line Effects

This simulation was done in Cadence Virtuoso with the Spectre package. A ringing signal was input into the RIIC at the RIIC bond pad. The output is taken at the gate of the current drive transistor used to power the IRLED in the pixel.

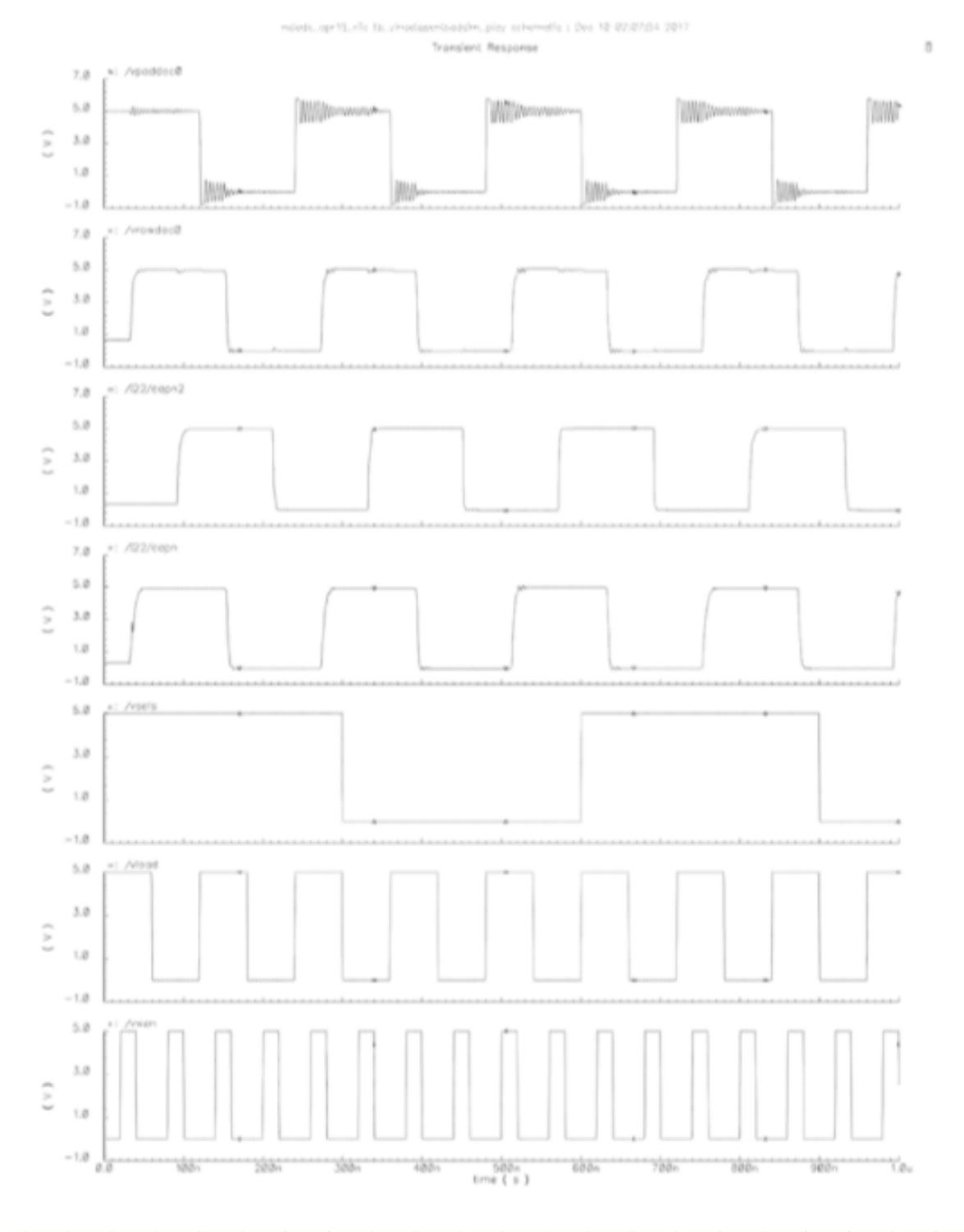
The plots in Figure 5.8 first show the input signal, which is labeled as vpad-dac0. The input signal has large ringing component. The inductance used to create the ringing signal in the simulation was made to be much much greater than the expected inductance of the ribbon cables, dewar, and carrier PCB for the RIIC. Several attempts were made to measure the impedance of these IRSP elements. These attempts are detailed in Appendix A.5. It was ultimately determined that it is not possible to accurately measure the combined impedance of these IRSP components with the available scientific equipment. A time domain reflectometer could be used to make these measurements, but was beyond the financial means of this researcher.

The second plot in Figure 5.8 shows the voltage at the row line in the RIIC. This is a storage node on the addressing decoder logic of the RIIC. RIIC architecture for the analog signal is described in detail in Appendix A.6. At the row decoder level most of the ringing has already been filtered out.

The third plot in Figure 5.8 shows the voltage at the capn2 which is *****

The fourth plot in Figure 5.8 shows the voltage at the storage node in the pixel. At this point most of the ringing has been filtered out. The remaining noise can be attributed to noise from the control signal lines: vsels, vload, and vwen.

Figure 5.8: vpaddac0 - analog voltage at RIIC pad with ringing, vrowdac0 - analog voltage on DAC row line, capn2, capn - analog storage node in the pixel. Ringing is filtered by RIIC.



From the simulation results it can be seen that the system response results exhibit the qualities of a low-pass RC filter. This is important because it means that the system response can be modeled with a simple RC filter and the transmission line effects can be ignored.

5.6 System Rise Time Experiment

It would be good to know what values of WEN Duration and WEN Delay cause the maximum value on VCAP in the shortest amount of time. WEN Duration and WEN Delay can be changed independently. This allows measurement of system pixel rise time. Several experiments were done at cryogenic temperatures and room temperatures. These experiments varied the values of WEN Duration and WEN Delay for different frame rates.

At 100Hz there is 225ns available of available time for a whole frames worth of operations. From Figure 5.3 we see that 6 ticks are needed before the next write. This leaves 195ns available to write to the pixel. With 195ns available VCAP will reach 99% of the VIN value.

At 400Hz operation a WEN Duration of 5 ticks and a WEN Delay of 1 tick cause the system to operate without any race conditions and still achieve the desired frame rate. This creates a pixel write period of 30ns. A 30ns write period unfortunately does not cause VCAP to reach the full value of VIN by the next pixel write cycle.

The next chapter details a set of rise time experiments that led to some notable conclusions that have characterized the system performance. The first is a firm understanding of the system rise time. The second is the revelation that there are fast and slow analog input channels that are caused by the RIIC architecture. The third is a measurement of bit accuracy for the system.

Chapter 6

RISE TIME EXPERIMENTS

Using the measurement method outlined in the previous chapter rise time measurements were taken over a period of time. The measurement method was refined to a point where custom firmware was developed that could have a WEN pulse duration smaller than 6 ticks (30ns). This increased the temporal resolution of the measurement, and showed some interesting results.

In Figure 6.1 a fast channel rise time and a slow channel rise time are both shown. The reason for fast and slow channels is discussed in Section 6.0.1. These channels are called fast and slow because the fast channel has a faster rise time response than the slow channel. The plot shows good agreement between data that was collected with stock firmware down to a resolution of 30ns and the new firmware that allowed measurement results in 1 tick (5ns) steps down to 0ns. This proves the new firmware is operating similarly to the stock firmware.

Another important result from this plot is that the rise time plots of both the fast and slow channels has the characteristic of a single pole low pass RC filter. Prior to this measurement it was not known whether the settling time of the analog system or the inductive nature of transmission lines used to transport the analog signal to the RIIC would cause ringing within the first 30ns of the system rise time. Simulations were performed that were detailed in the previous chapter that suggested ringing would be filtered by the capacitance in the RIIC, but there had been no experimental proof until this experiment was performed.

A further refinement of the firmware was created that allowed for WEN durations of 1, 2, 3, and 4ns. The results are similar to the previous plots results.

Figure 6.1: Rise time measurements using custom firmware that allows for WEN durations below 6 ticks (30ns for the current system).

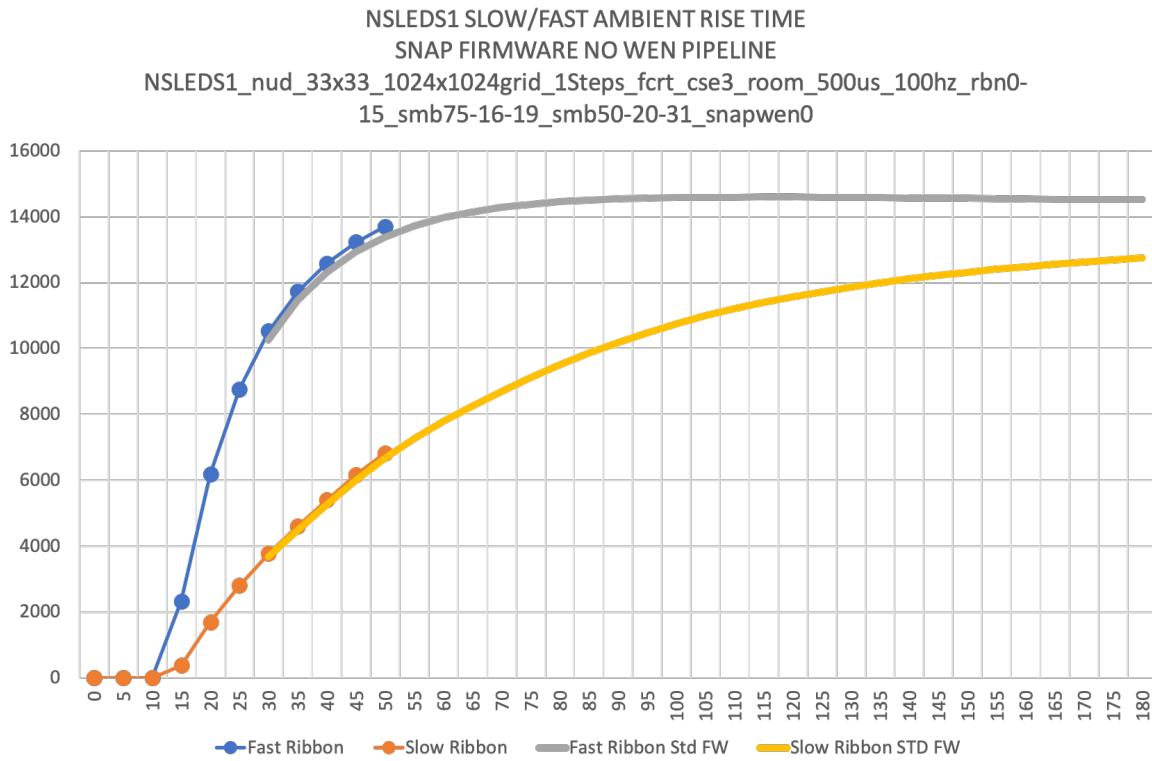
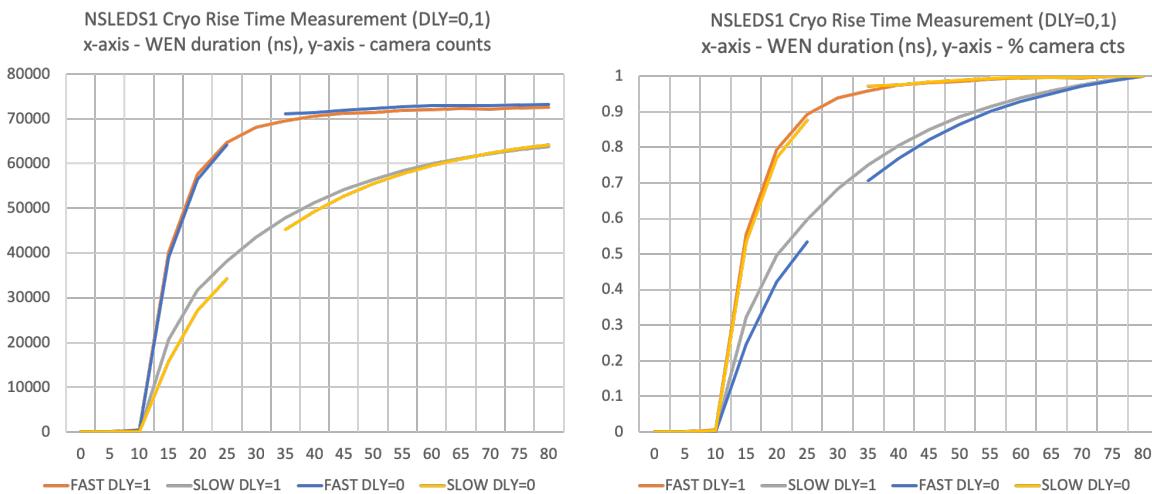


Figure 6.2: Rise time measurements using custom firmware that allows for WEN durations of 1, 2, 3, and 4 ticks.



6.0.1 Fast and Slow RIIC Channels

Measurement of the rise time of different pixel elements in the IRSP revealed a loose bimodal distribution of rise times. Some rise times were very fast and some were much slower. These results were later attributed to the fanout capacitance of the analog inputs to the RIIC. A brief overview of the analog input circuitry is useful to understand why this occurs.

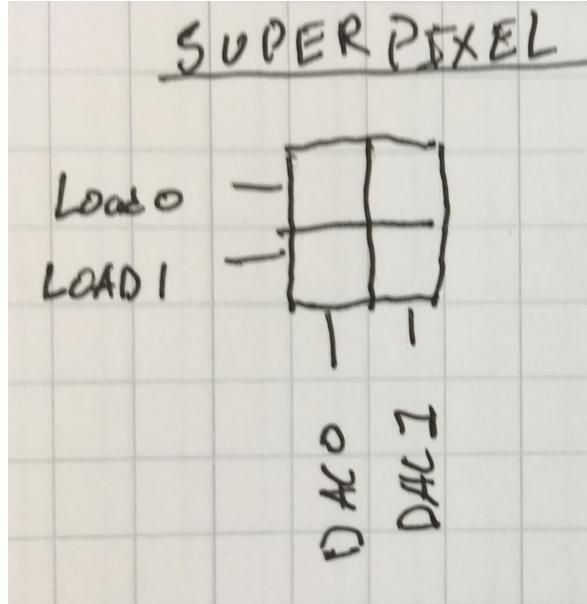
6.0.1.1 Analog Input Circuitry Overview

The basic unit cell of the Oslo RIIC architecture is called a Super Pixel. A Super Pixel is a unit that includes four pixels. The four pixels are space multiplexed and time multiplexed. The space multiplexing is possible because two of the pixels are written in parallel with two different DACs. The time multiplexing is controlled by a LOAD signal. The signal is used to switch which pair of pixels the two DACs are writing to. A diagram showing the inputs into a super pixel is shown in Figure 6.3.

The Oslo RIIC has several modes that affect how many analog inputs are required in order to drive the IRSP. These are called DACMODES. The Oslo RIIC DACMODES are listed in table 6.1. The DACMODE is set with a control register and controls how many DACs are required to drive the RIIC. Analog input channels 0 and 1 are used in every DACMODE. Analog input channels 2 and 3 are used in DACMODE2 and up. This trend continues until all DACMODES have been accounted for. Analog input channels are always connected to the number of rows required to operate the RIIC in the lowest number DACMODE. For example, analog input channels 0 and 1 are always connected to the 256 rows even if a high number DACMODE is selected.

The Oslo RIIC is a segmented row based architecture. This architecture sought to solve the high input capacitance of the 512×512 SLEDs IRSP by using a large pass transistor to hide the capacitance from the pixels of the rows not being currently addressed. This limits the capacitance seen by an analog input signal to the pixels in the row being addressed and the row pass transistors of the other rows. This greatly reduces the capacitive load seen by the analog input signals, and increases the rise time

Figure 6.3: Super Pixel Inputs



of the analog input signals compared to the previous RIIC. The row based architecture is illustrated in Figure 6.4.

Specifically, the fanout capacitance is caused by the capacitance of the row pass transistor of each row that the analog input is connected to. The rows are connected in parallel to the analog input, which causes the capacitance to add. This makes analog input channels 0, and 1 have the largest fanout capacitance of 256 row pass transistor capacitances. Channels 0, and 1 also have the Serial Programmable Interface (SPI) attached to them. The SPI is also required to drive the whole array. This doubles the fanout of these channels to 512.

The fanout of the remaining channels are determined from just the number of row pass transistors that they are connected to. The fanout for the different channels is summarized in table 6.1.

Figure 6.4: RIIC Segmented Row Architecture

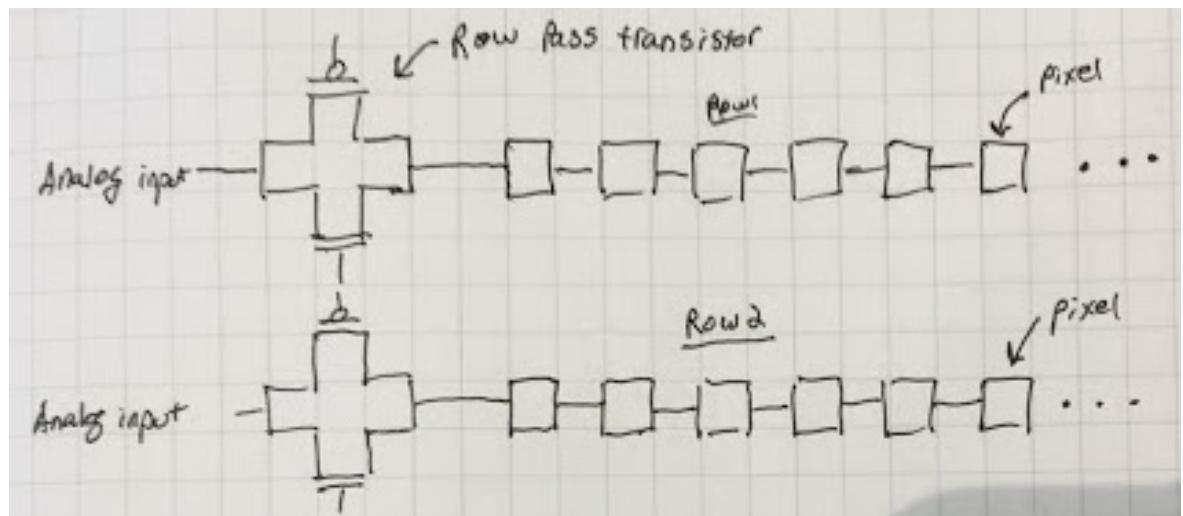


Table 6.1: List of DACMODES and their function

DACMODE #	DACs Used	Fanout
DACMODE0/1	0, 1	512
DACMODE2/3	0, 1, 2, 3	128
DACMODE4/5	0, 1, 2, 3, 4, 5, 6, 7	64
DACMODE6/7	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	32

6.1 Rise Time Results

General results room temp what is our 10 - 90 risetime? cryo 10 - 90

33 vs 32 grids system rise time vs RIIC + emitter rise time

Proof that fanout capacitance causes fast and slow channels Moving integration buckets Fast channel no effect Slow channel effect

From Figure 6.5, slow channel 10 - 90% rise time at cryogenic temperatures is 75ns or 39 ticks. For the fast channels 10 - 90% rise time at cryogenic temperatures is 30ns or 6 ticks. Room temperature results are less accurate than cryogenic results because of thermal effects, so they are not included here.

Figure 6.5: Slow channel rise time measurements with WEN custom firmware showing reasonable agreement with stock firmware.

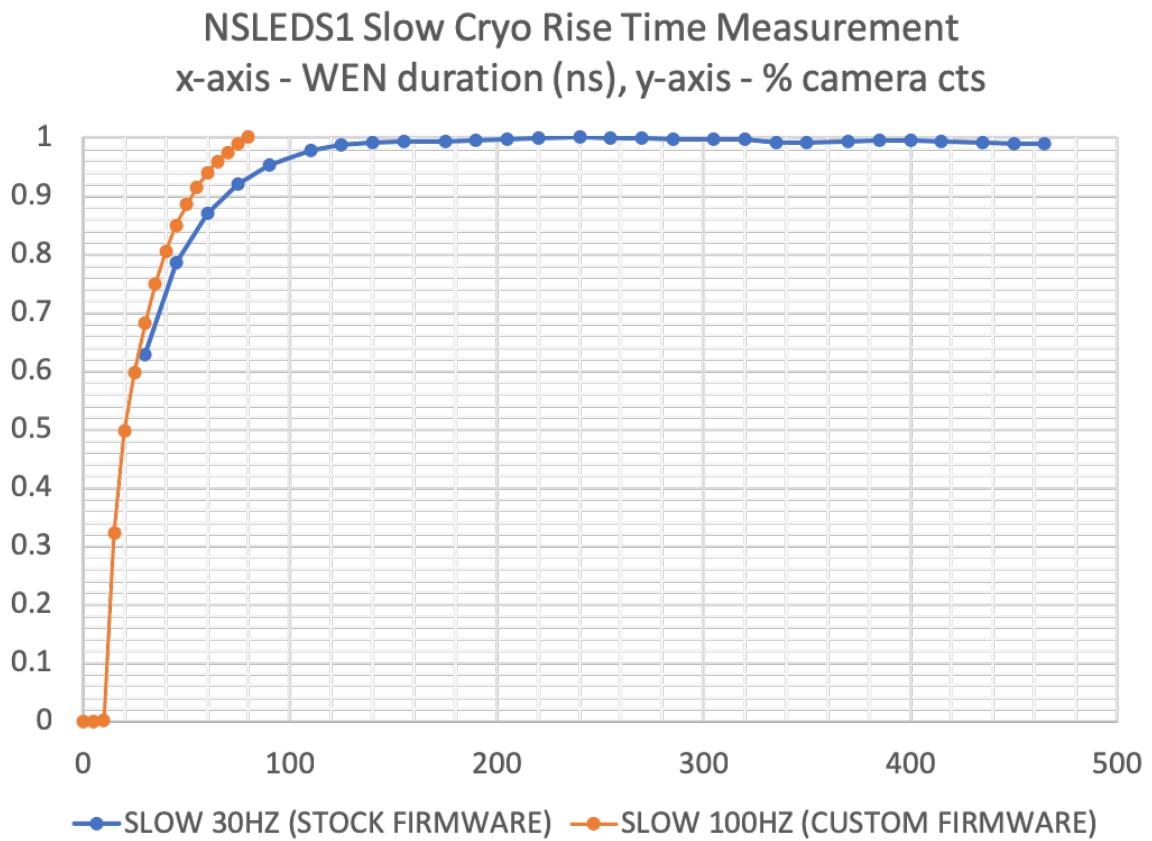
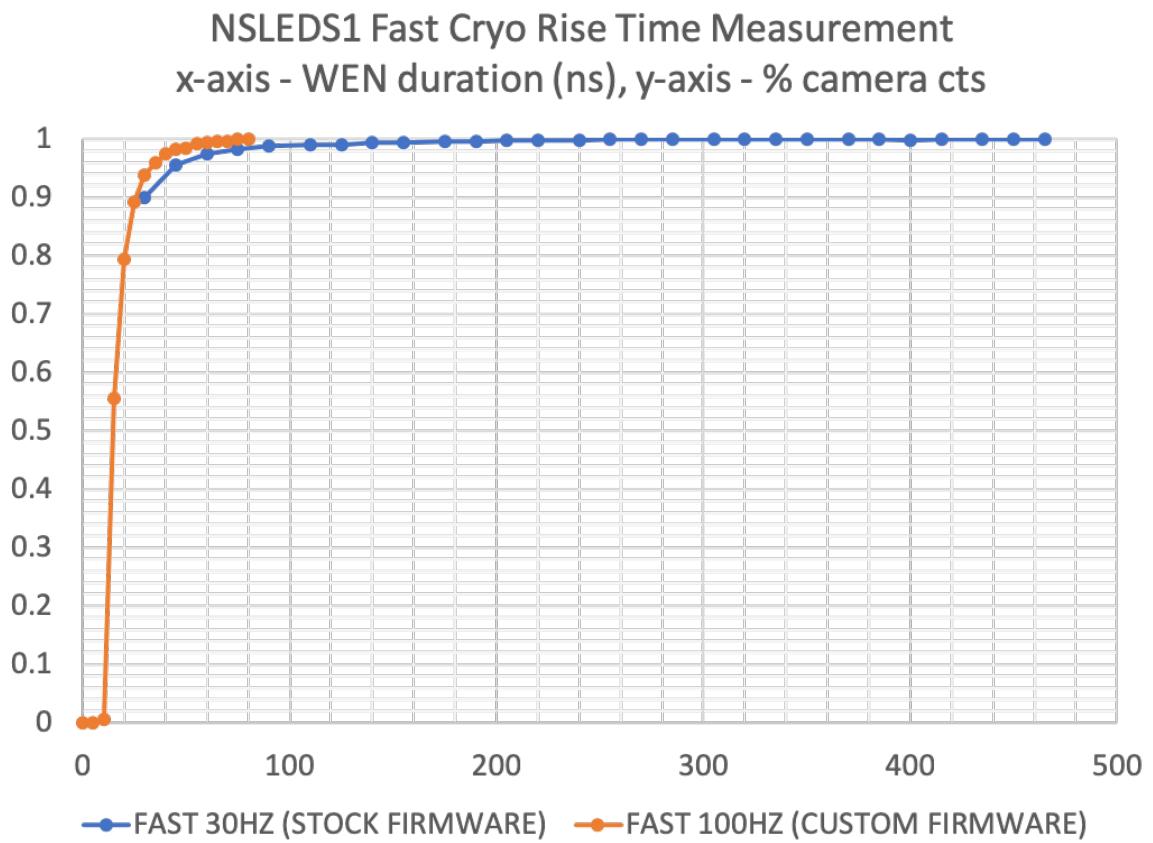


Figure 6.6: Fast channel rise time measurements with WEN custom firmware showing reasonable agreement with stock firmware.



6.2 Slow and Fast Channel Cause Investigation

Fanout capacitance of the different analog input channels was suspected to be the cause of the slow and fast channel phenomena. To prove this an experiment was designed where the start of the WEN pulse would be varied and the results for both the slow and fast channels would be recorded. The WEN pulse determines how long the analog inputs will charge the analog storage node in a pixel. This can be thought of as an integration window. The longer the analog signal writes to the analog storage node the closer the voltage on that capacitor approaches the desired value. By starting the WEN pulse earlier it is possible to start charging the analog storage node before the analog signal has completely settled.

Given that the electronics are similar and comparable between the analog input channels the results of this experiment should show if the fanout capacitance of the RIIC has an effect on the rise time of the analog input signals. As the fanout is believed to be the only difference between the analog input channels.

The results are shown in Figures 6.7 and 6.8. The results show that for the fast channel it is not possible to see the analog rise time because the analog rise time is too fast. For the slow channels it is possible to see different RC curves based on the fanout capacitance of these lines. These results shed some light on the cause of the fast and slow analog channels.

Figure 6.7: Effect of WEN Delay on rise time of fast channels.

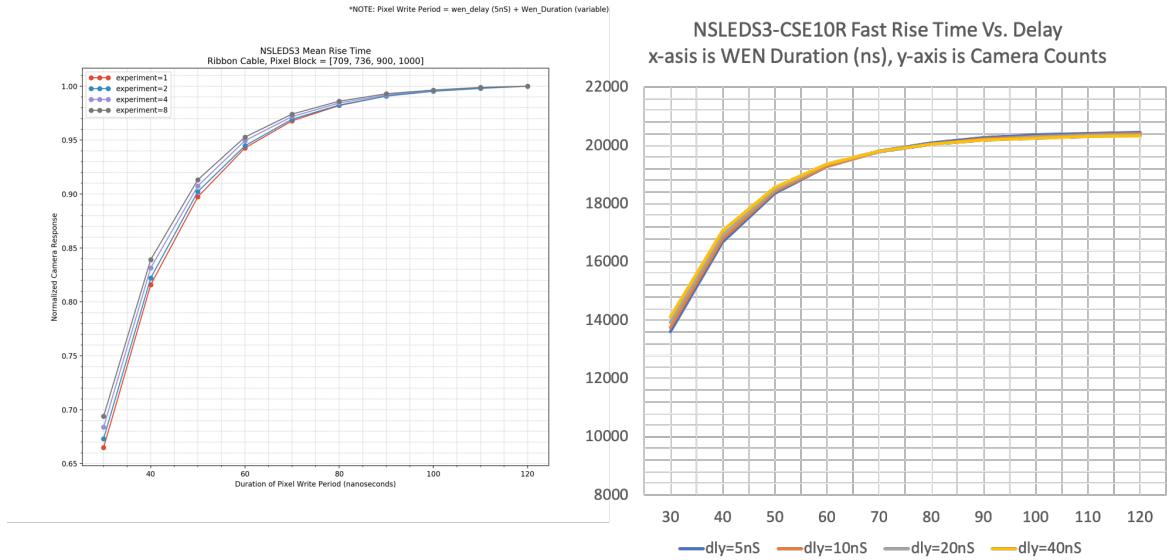
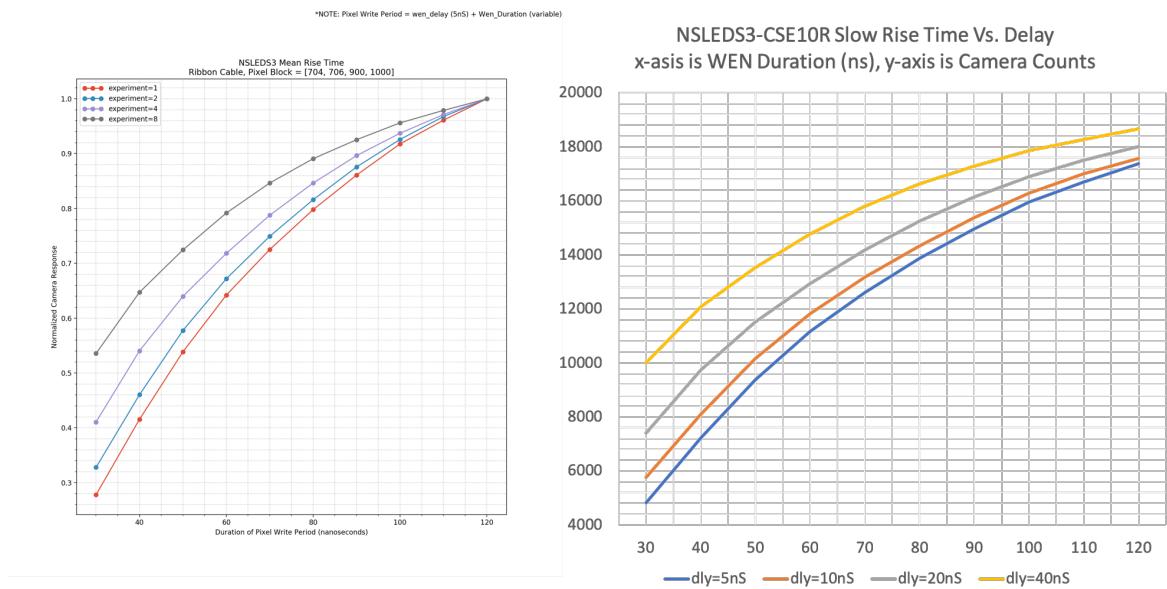


Figure 6.8: Effect of WEN Delay on rise time of fast channels.



6.3 IRLED and RIIC rise time vs System Rise Time

Initially, data for rise time was collected using a grid of pixels with a spacing of 32 pixels between them. A grid of pixels is used to get a statistically significant data set. A statistically significant dataset is required because pixel characteristics vary by a fair amount and to understand the full range of responses from the pixels requires a large enough dataset to apply statistical approximation methods, such as the median, mean, and variance.

The spacing of 32 presented an interesting result when compared to a grid spacing of 33 due to the way the Oslo RIIC draws an image. With a spacing of 32 pixels the same DAC is used to write to all pixels. There are 16 DACs available and the DACs are interlaced amongst each other. For example, DAC0 will be used to write to Row 0 then DAC1 to Row 1 etc. Eventually, at Row 15 DAC0 is used again. DAC0 is again used at Row 31. By using the same DAC for all pixels the DAC rise time is excluded from the measurement of the optical rise time. Figures [6.9](#) and [6.10](#) both show that the measured rise time for a spacing of 32 is much faster than the measured rise time for a spacing of 33. The interesting result is that the rise time of the RIIC and the IRLED can be separated from the total system rise time with this method.

Figure 6.9: Difference between 32x32 grid spacing and 33x33 grid spacing for rise time measurements. The results show the rise time of the system and the rise time of just the RIIC and the rise time of the IRSP System.

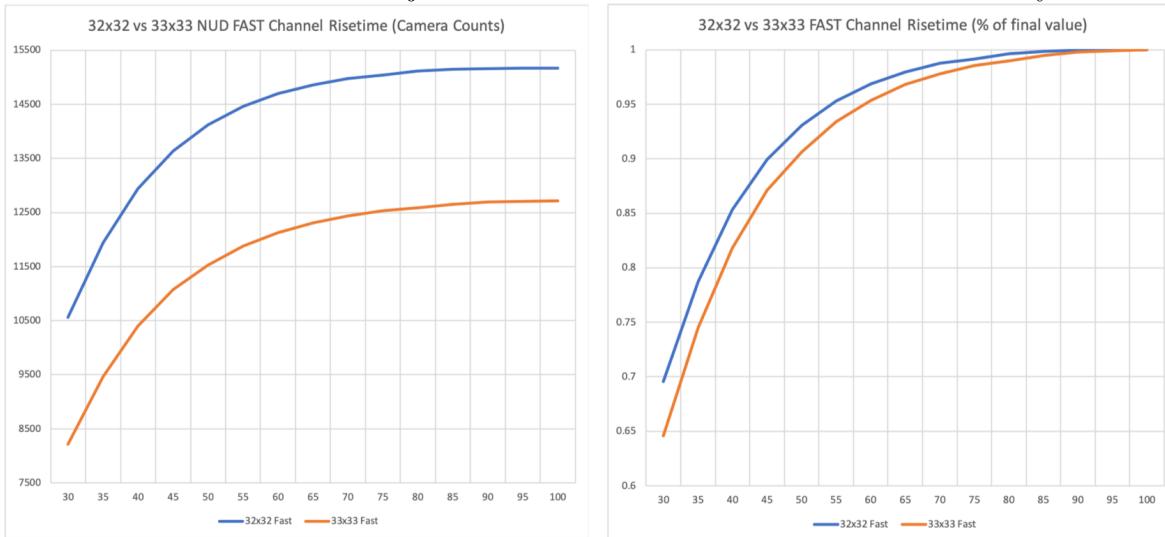
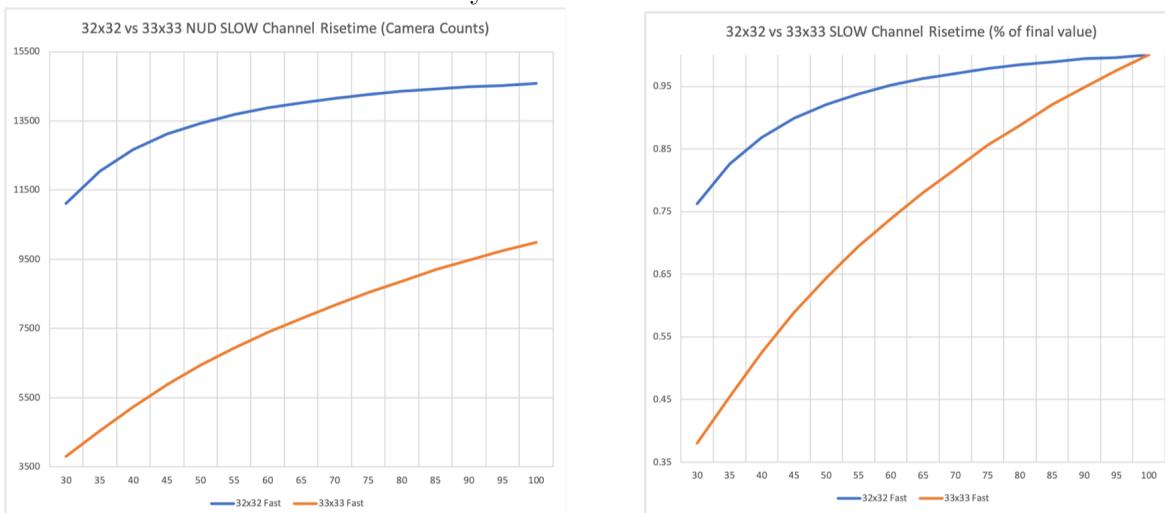


Figure 6.10: Difference between 32x32 grid spacing and 33x33 grid spacing for rise time measurements. The results show the top portion of the curves for rise time of the system, and the rise time of just the RIIC and the rise time of the IRSP System.



6.4 System Bit Resolution

System bit resolution is defined similarly to the bit resolution in Chapter 8 for Settling Time measurements. The idea of error bands is used again. A small recap is presented here to understand the experimentally derived plots. In Figure 6.11, a one bit system is presented. This system has the bit threshold set at half of the maximum value. Here we see that the measured value is above the bit threshold and the system will report that. However, a one bit system is not able to determine if the measured value is equal to the desired value because both the measured and the desired values are above the bit threshold. More bits are required to make finer selections of the Y-Axis of the plot.

A two bit system is shown in Figure 6.12. The two bit system has a finer selection of the Y-Axis than the one bit system and is able to discriminate between the measured value and the desired value.

Figure 6.11: One bit system.

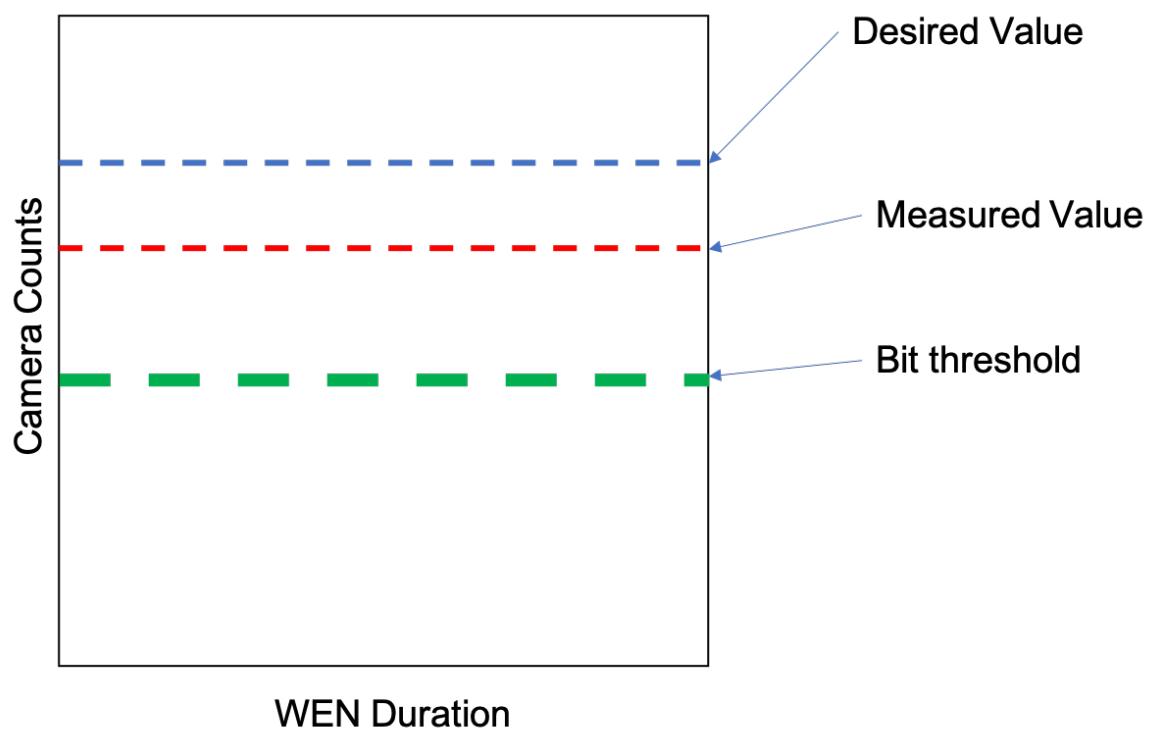
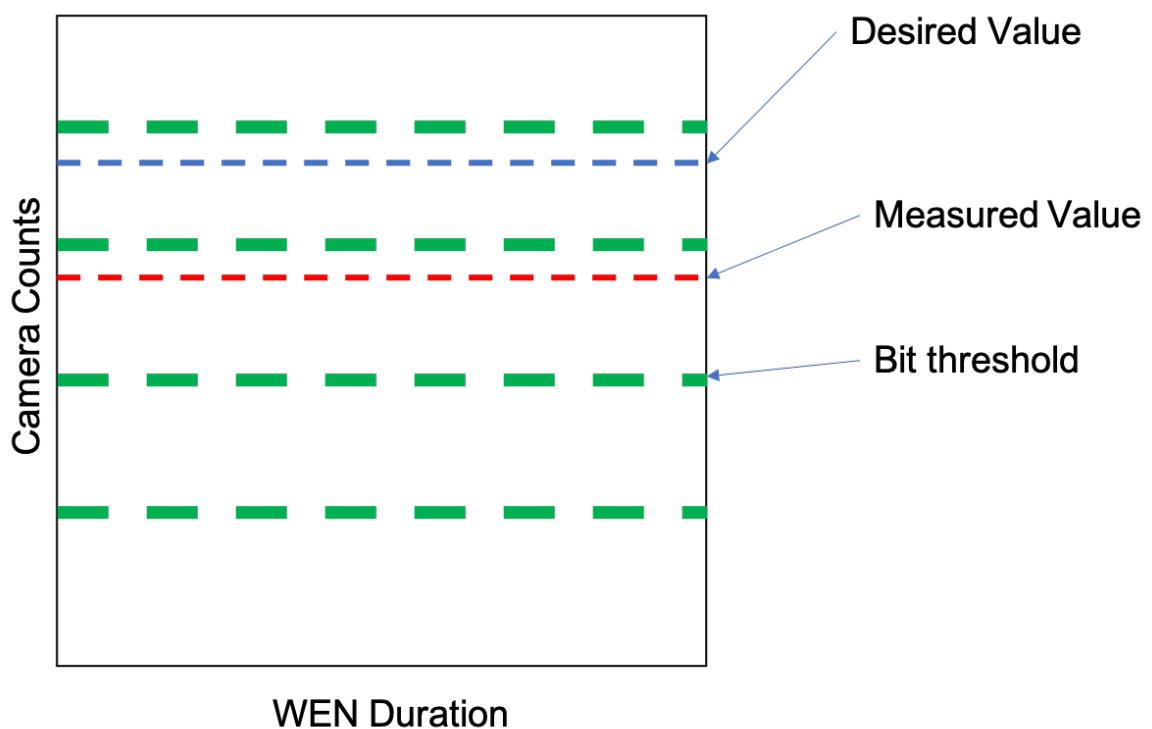


Figure 6.12: Two bit system.



6.4.1 System Bit Resolution Results

In Figure 6.13 The bit thresholds are overlaid on top of a rise time plot that is normalized and zoomed in on the top portion of the two signals. The two signals are the fast rise times for NSLEDS1 and NSLEDS3. It can be seen that NSLEDS3 settles to within a smaller error band faster than NSLEDS1. The reason for the difference in rise time between NSLEDS1 and NSLEDS3 is described in Section 6.5.

In Figure 6.14, an un-zoomed in version of the bit resolution plot for the slow channels of NSLEDS1 and NSLEDS3 is shown. It is again noted that NSLEDS3 has a faster rise time.

Figure 6.13: Fast Channel NSLEDS1 vs NSLEDS3 Rise Time with Bit Resolution.

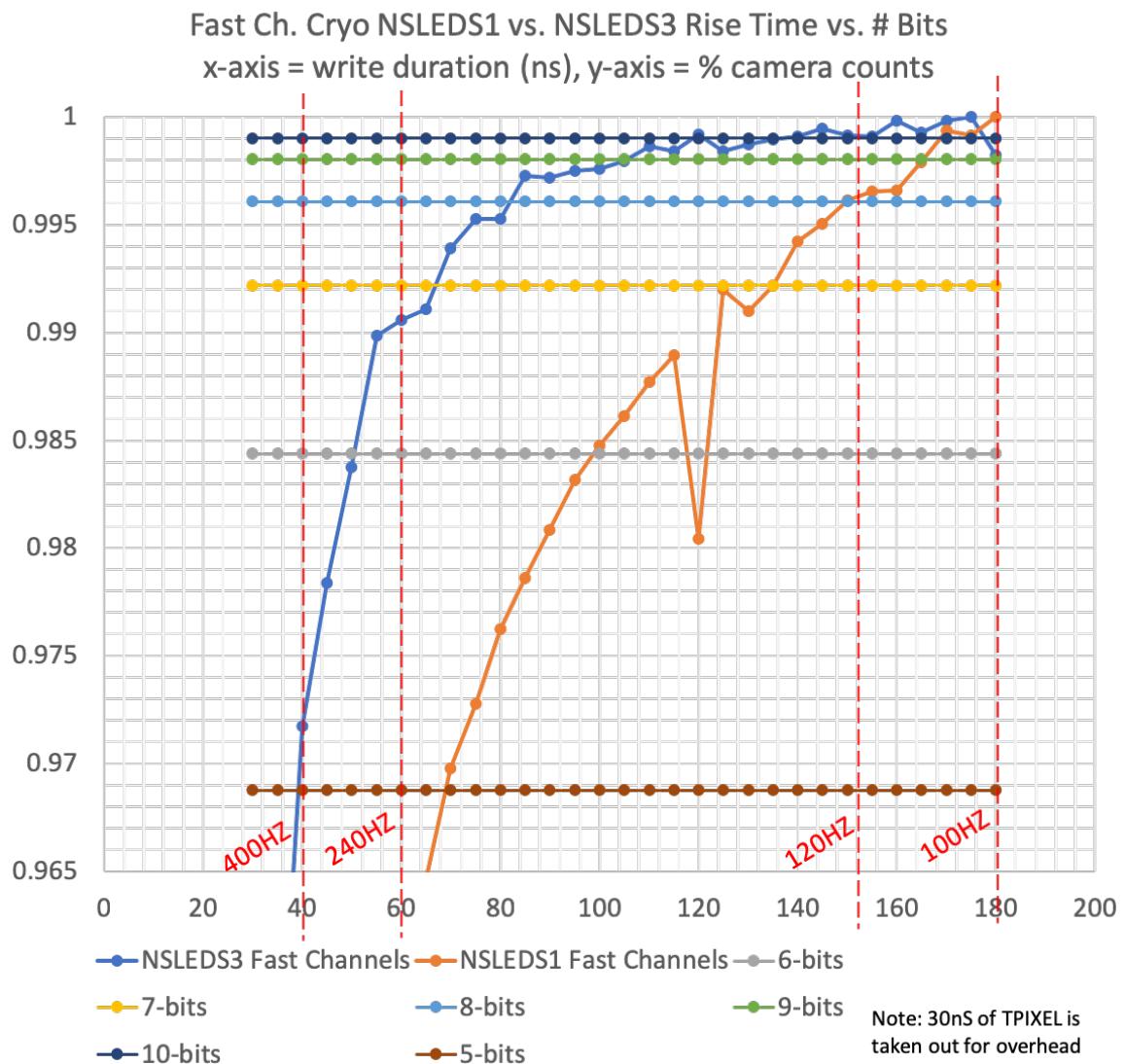


Figure 6.14: Slow channel rise time for both NSLEDS1 and NSLEDS3 with bit resolution levels overlaid. The plot attempts to quantify the performance decrease of the epoxy attachment vs. the epoxy and indium bump attachment.

AMBIENT NSLEDS1-CSE3 v. NSLEDS3-CSE5 Room Temp Fast vs Slow Rise Time in 33x33 NUDs
x-axis is WEN Duration (ns), y-axis is Camera Counts (Frame Rate vs. # Bits)

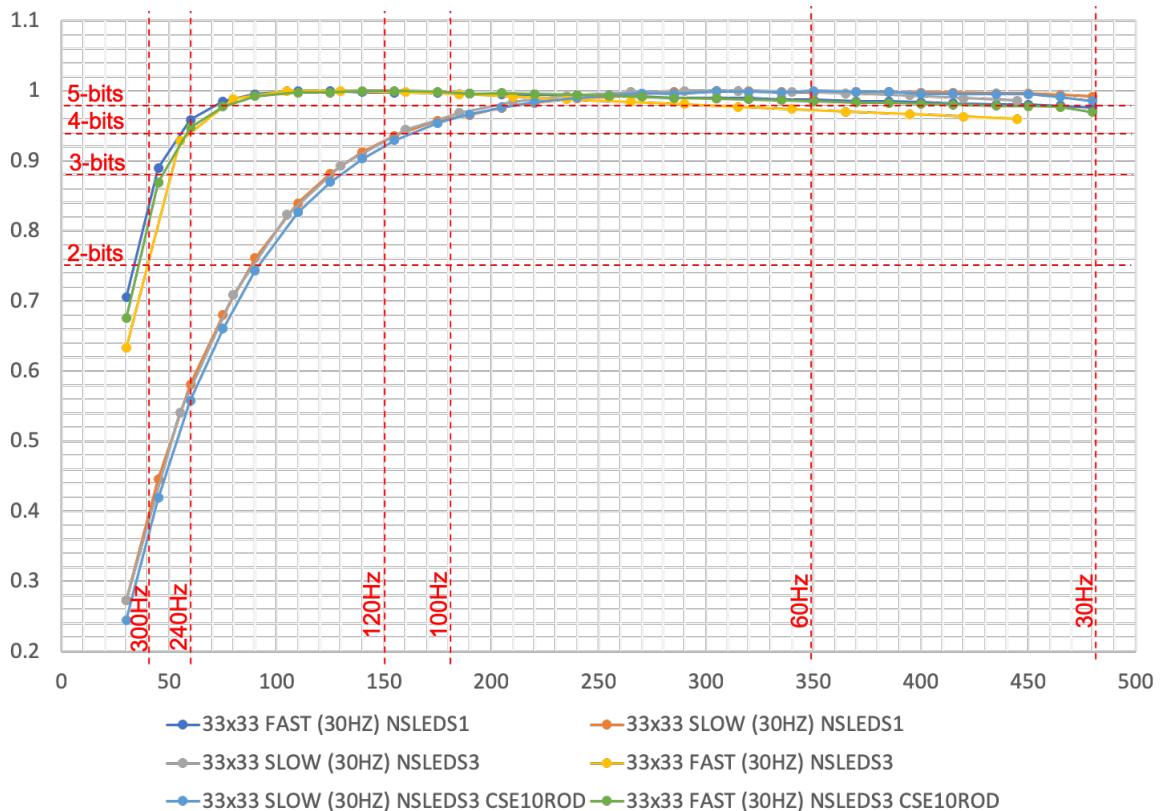


Figure 6.15: Fast channel rise time measurements showing the difference in rise time for strong and weak mode.

NSLEDS1 Fast Cryo Rise Time Measurement
x-axis - WEN duration (ns), y-axis - % camera cts

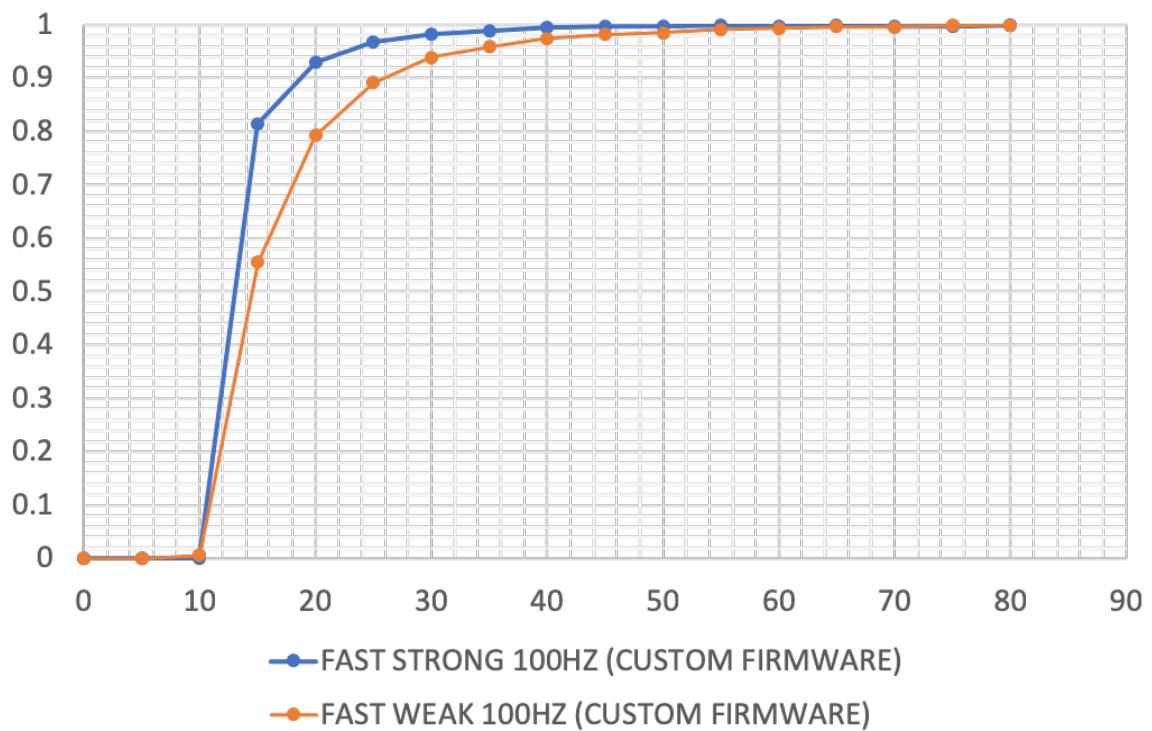
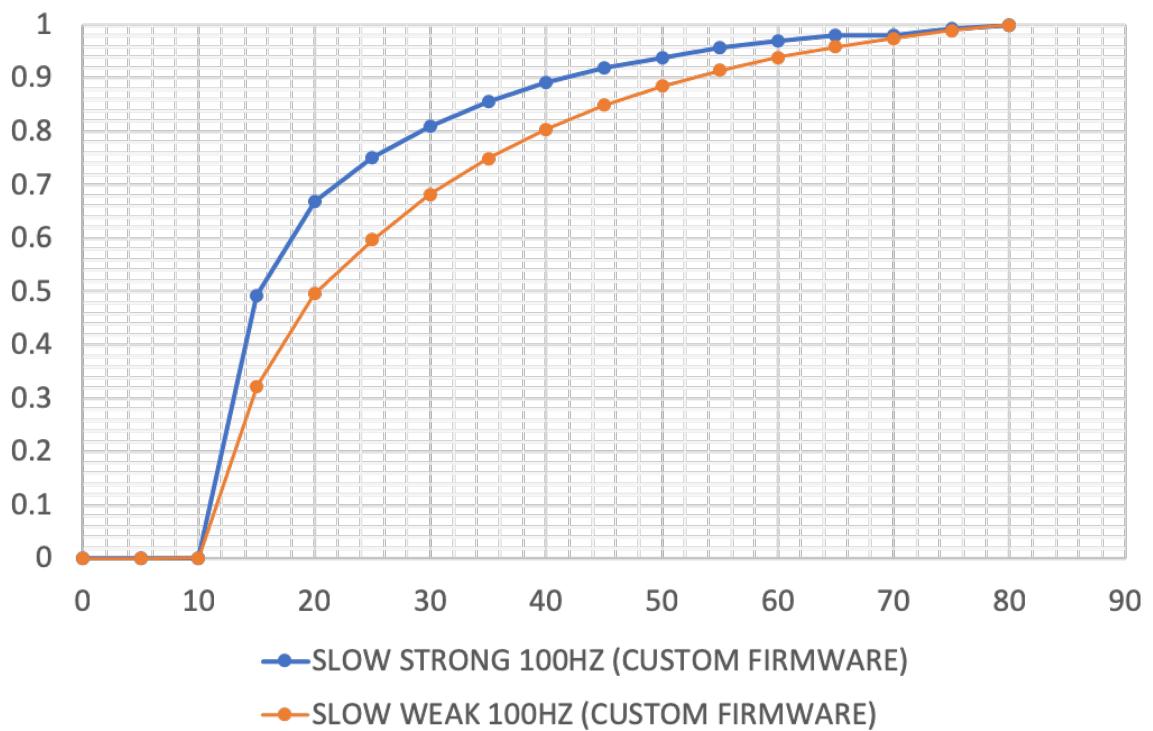


Figure 6.16: Slow channel rise time measurements showing the difference in rise time for strong and weak mode.

NSLEDS1 Slow Cryo Rise Time Measurement
x-axis - WEN duration (ns), y-axis - % camera cts



6.5 Thermal Effects on Rise Time

NSLEDS1 and NSLEDS3 have different attachment methods between the IRLED Hybrid and the Copper Tungsten heat sink plate. NSLEDS1 only uses epoxy, while NSLEDS3 uses epoxy with indium bumps. The indium bumps provide a higher thermal conductivity path than the epoxy. The higher conductivity path helps remove heat from the RIIC and preserve the performance increase caused by cooling the CMOS semiconductors to 77K.

6.6 Conclusion

Resistor Array rise time dominated by resistor element heating

Chapter 7

ANALOG CIRCUIT IMPROVEMENTS FOR INCREASED RISE TIME

7.1 Introduction

The 512 SLEDS IRSP CSE heavily influenced early versions of the newer generation IRLED IRSPs. In the version of the RIIC used with the 512 SLEDs IRSP there was a large capacitive loading due to the RIIC architecture. This required a power amplifier that could handle at least a 10nF load over a 10V swing. These kinds of requirements limited the available amplifiers. Eventually, an amplifier that had been developed for driving long cables for the television industry was chosen. This amplifier was able to drive the approximately 10nF load of the RIIC, but did not have a very fast rise time.

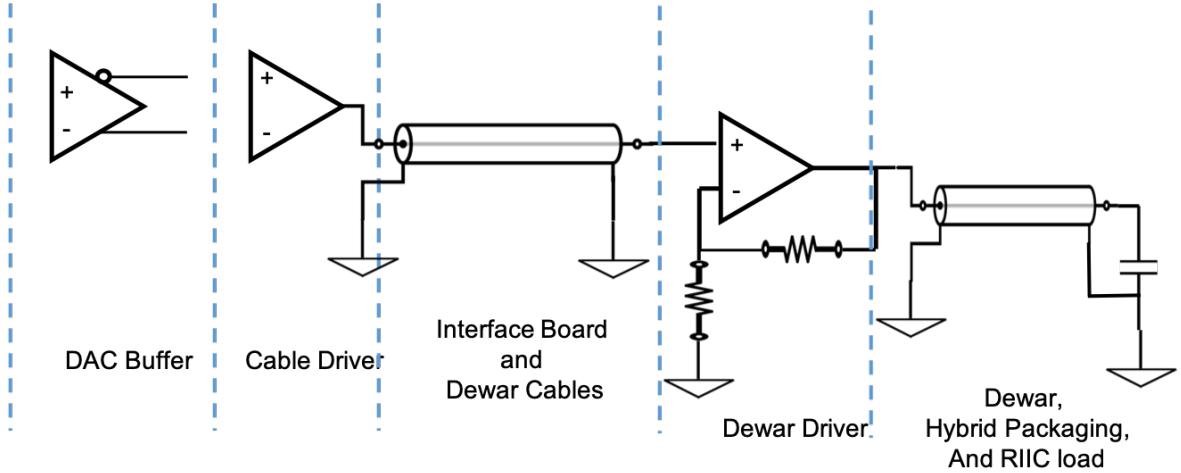
Looking towards the future, it was decided that a new amplifier architecture that could deliver faster analog circuit rise time was desired. The design of the new amplifier system proved to be an interesting problem. The design process can be broken down into load characterization, component selection, and physical design of the components.

7.2 Architecture Overview

An overview of the architecture that was eventually chosen is given here to give some context to the reader before explaining why the architecture was chosen.

Figure 7.1 shows the general overview of the architecture chosen for the new generation of CSE. A three stage amplifier chain was chosen. The amplifiers have been given the names of: DAC Buffer, Cable Driver, and Dewar Driver. The different transmission lines the signal must go through have been labelled on the diagram.

Figure 7.1: Overview of the Analog Electronics Architecture



7.3 Load Characterization

To design an analog amplifier system the load the amplifiers would be driving had to be better understood. Several approaches were undertaken to achieve that understanding. Ultimately, due to the lack of a Time Domain Reflectometer and other required experimental equipment an electromagnetic simulation of the PCB that the IRLED Hybrid is wire bonded to produced the best results. This model was converted into the SPICE circuit simulation language and used when designing the amplifier circuits in SPICE.

7.3.1 SPICE Model Description

The software package "Arbitrary Transmission Line Calculator" (ATLC) was used to simulate the traces on the Carrier Board. The simulations extracted the impedances for both a micro-strip and a strip line trace configuration on the Carrier Board. A rough circuit diagram was created by visually identifying whether sections of the analog signal traces were in a micro-strip or a strip line configuration. The visual identification was tabulated in a spreadsheet. This information was then used

Figure 7.2: Carrier Board SPICE Model.

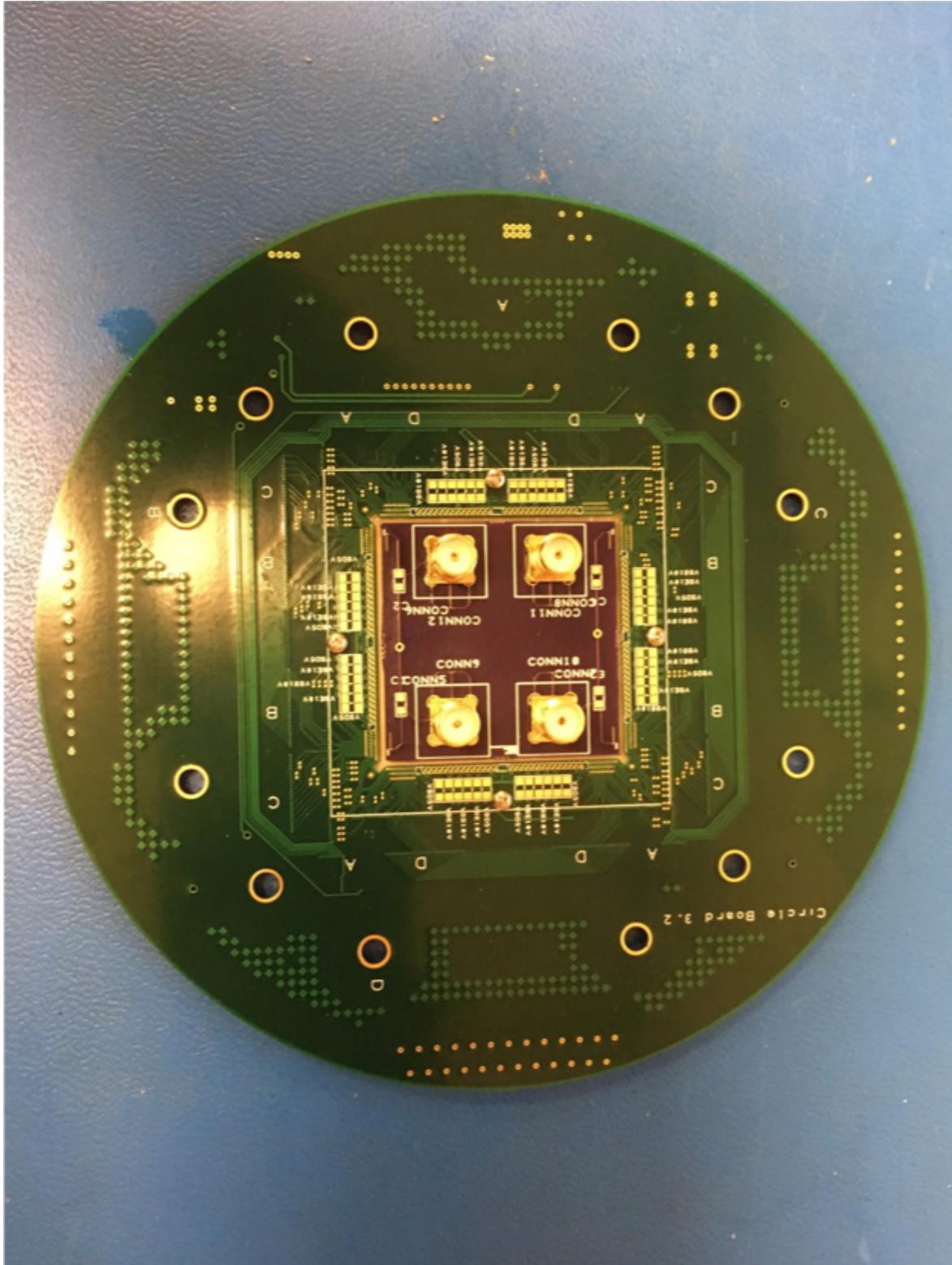
to construct the SPICE model. The values ATLC generated were used for the different transmission lines in the SPICE models. This model was then used to design the amplifier circuits in SPICE.

7.3.2 Vector Network Analyzer and Signal Generator Sweep

A direct measurement of the impedance of the Dewar and the Carrier was attempted using a Vector Network Analyzer (VNA) and a signal generator where the input voltage was measured and the output voltage was measured across a large frequency range.

These efforts proved to be not fruitful because the VNA was not able to measure to a low enough frequency for this application. And it was not possible to extract phase information easily with the signal generator. This eliminated the complex impedance information.

Figure 7.3: SPICE settling time results for all three amplifier stages.



7.4 Component Choices

7.4.1 OPA695

The OPA695 was chosen because it has a high bandwidth and a slew rate of $4300-V/\mu s$. These features combined with the low input voltage noise for additional precision made the OPA695 a good choice for the new amplifier architecture.

The OPA695 has one issue. The data sheet lists the voltage swing as $\pm 4.2V$. The RIIC requires a 0-5V swing to use the total range of the drive transistors in the pixels. The data sheet also lists the maximum operating voltages as $\pm 6.5V$. An experiment was conducted to see whether a 0-5V output could be had from the OPA695. By setting both of the supplies to the maximum operating voltages it was possible to produce a 0-5V output.

The OPA695 was used for both the Cable Driver and the Dewar Driver.

7.4.2 ADA4932

The 512 IRSP CSE did not have a buffer amplifier for the output of the DAC. It is often needed to have a buffer amplifier that takes the differential output of the DAC and converts it into a single ended signal. Assuming that the system is single ended and not differential. The buffer amplifier ensures that both outputs of the DAC are terminated into the same impedance and separate the parasitics of the rest of the system from the DAC.

The ADA4932 was chosen due to its high -3dB bandwidth of 560MHz and 0.1dB of flatness across a 300MHz frequency range. The flatness and low distortion is important for a buffer amplifier because the job of a buffer amplifier is to reproduce the signal accurately.

7.5 Architecture Design

Initially, a single stage architecture was attempted. This was the architecture used in the 512 IRSP CSE. A single amplifier was used to drive all of the traces, cables, and loads in the analog signal chain. The different transmission lines present in the

system have different impedances. If it were possible to split these transmission lines and properly terminate each one the overall system performance would be increased. This idea was used to conceive the three stage architecture use for the new analog electronics.

The first stage is a buffer stage that properly terminates the DAC outputs and converts the differential output of the DAC into a single ended output that is compatible with the existing cabling.

The second stage is a gain stage that provides part of the gain required to achieve the voltage swing required by the IRSP. The function of the second stage is also to drive the traces on the Interface board, and the Ribbon Cables that goto the Dewar. These are lumped together as one transmission line in this system because it is not convenient to split them with the current CSE architecture.

The third stage is another gain stage that provides the rest of the required gain to achieve the 0-5V swing required by the IRSP. The function of this stage is also to properly terminate the first transmission line (Interface board and Ribbon Cables) from the second transmission line consisting of the: Dewar coaxial cables, the Carrier Board traces, and the capacitive load of the RIIC.

7.6 SPICE Simulation

A SPICE simulation was conducted that involved the three stage amplifier architecture, and the modeled load of the Carrier Board and RIIC.

It was discovered that it was not possible to properly terminate the first transmission line and remove the reflection caused by the impedance mismatch. This was solved by realizing that the analog system is a discontinuous system. The analog system writes to a pixel for a certain period of time. Then it waits for the next pixel write cycle to begin. During the waiting period it is ok to have signal distortions present on the analog signal line because it the value is not being sampled. By choosing a cable length that caused the reflection to return when the CSE is not drawing allowed a high quality signal to be present at the input of the third amplifier stage.

Figure 7.4: SPICE schematic of the three stage amplifier architecture.

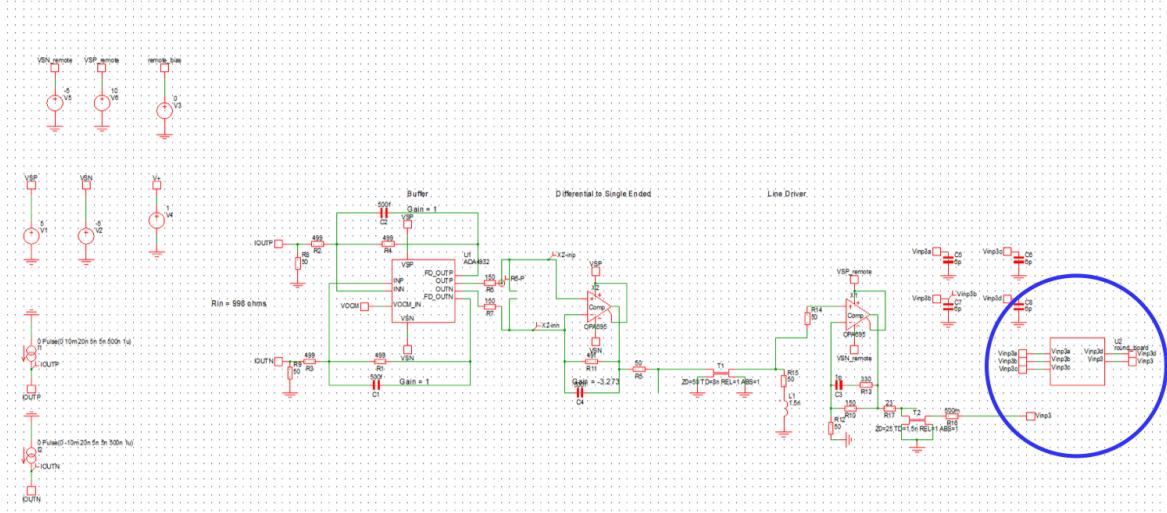
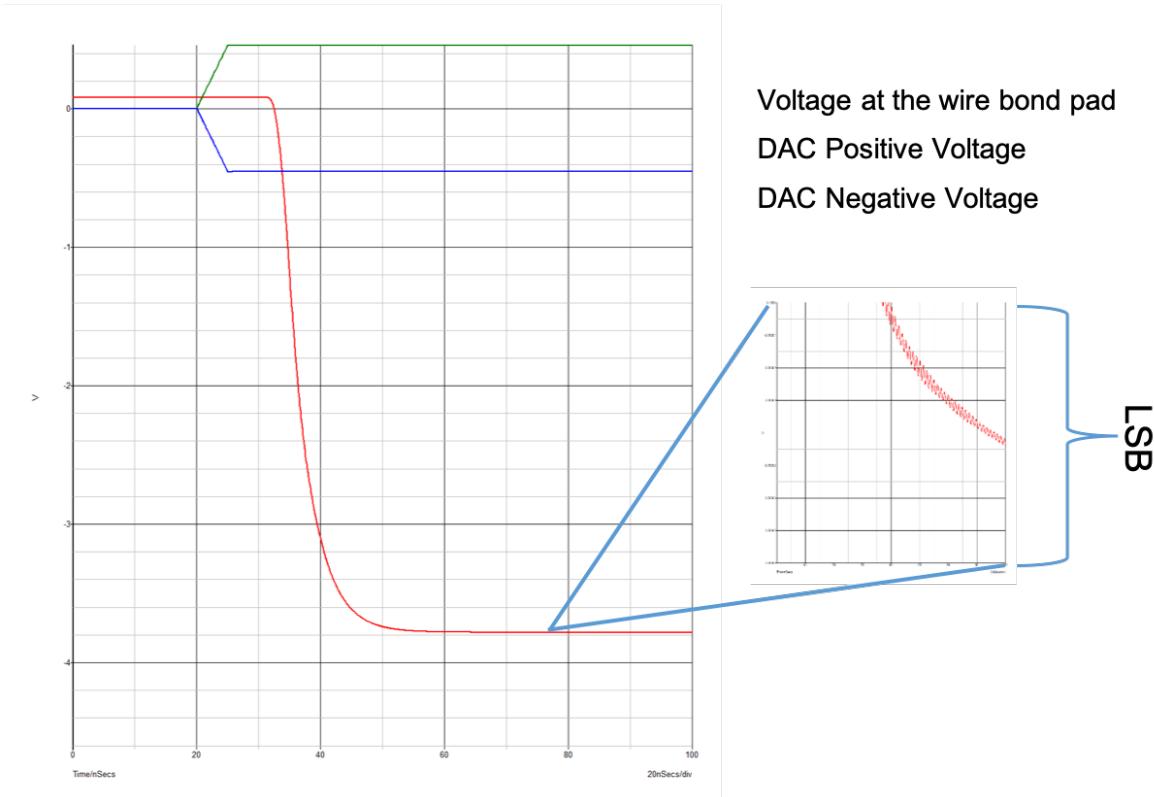


Figure 7.5: SPICE settling time results for all three amplifier stages.



A transient simulation was run that inputted a high speed pulse with a 20ns rise time. This pulse represents the DAC output in this system. A settling time, to a 16 bit LSB, of 76ns was calculated during the simulation.

7.7 PCB Construction

A PCB was designed for the first and second stage amplifiers. This PCB was used to test whether the circuit design operated correctly.

Several PCB designs were also done for the Dewar driver. At first a 2 layer PCB was designed. The first PCB layout is shown in Figure 7.8. This board was redone with a 4 layer board to improve power delivery and signal integrity. Several test boards were constructed in order to achieve a final design that did not have signal integrity problems. Appendix B.1 provides an in-depth lab report about this testing and the results.

Figure 7.6: Schematic for first and second stages of the new amplifier topology.

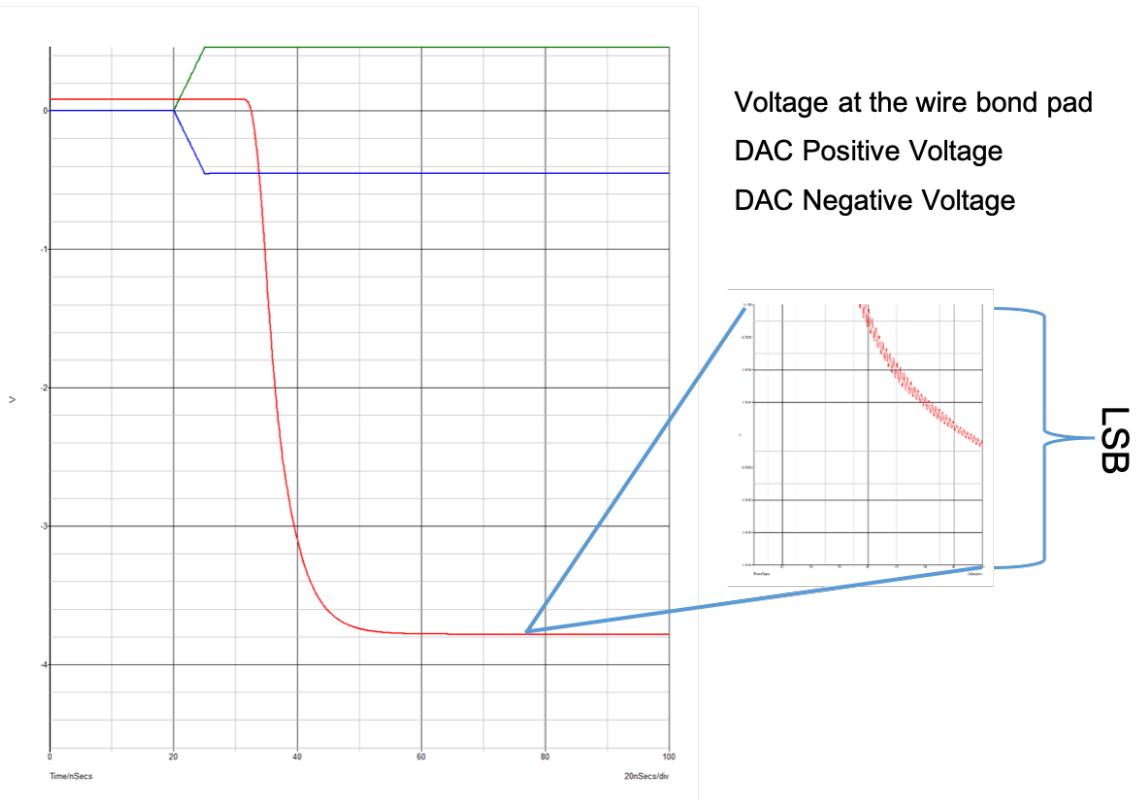


Figure 7.7: Layout for first and second stages of the new amplifier topology.

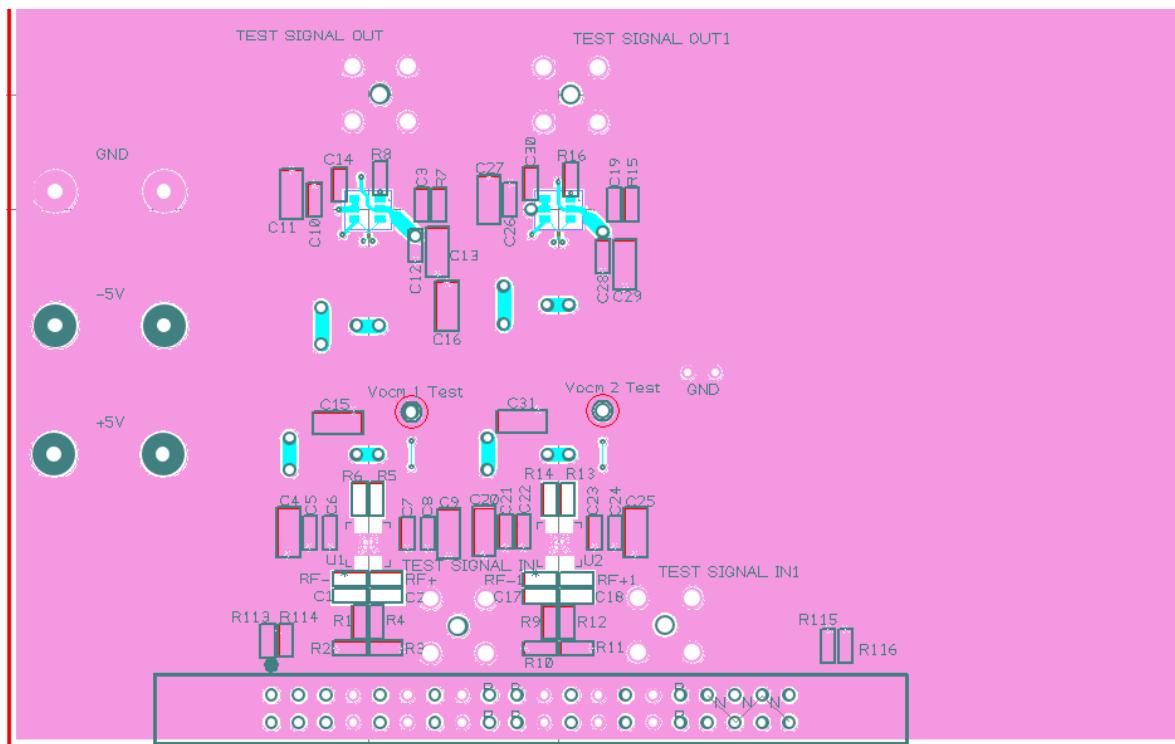
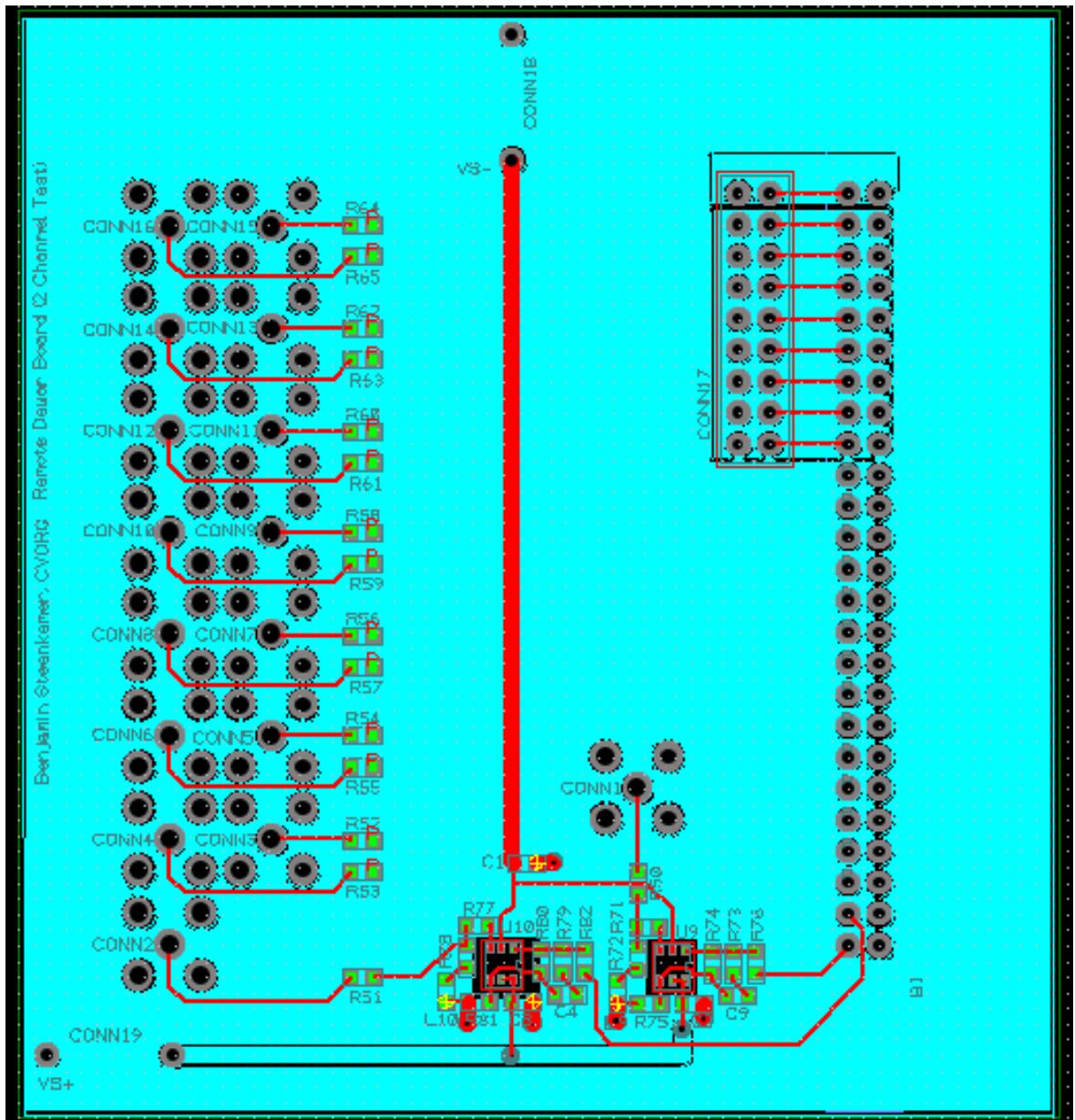


Figure 7.8: Layout for the Dewar Driver Board.



Chapter 8

SETTLING TIME MEASUREMENT

8.1 Analog System Performance Metrics

Remember the measurand!

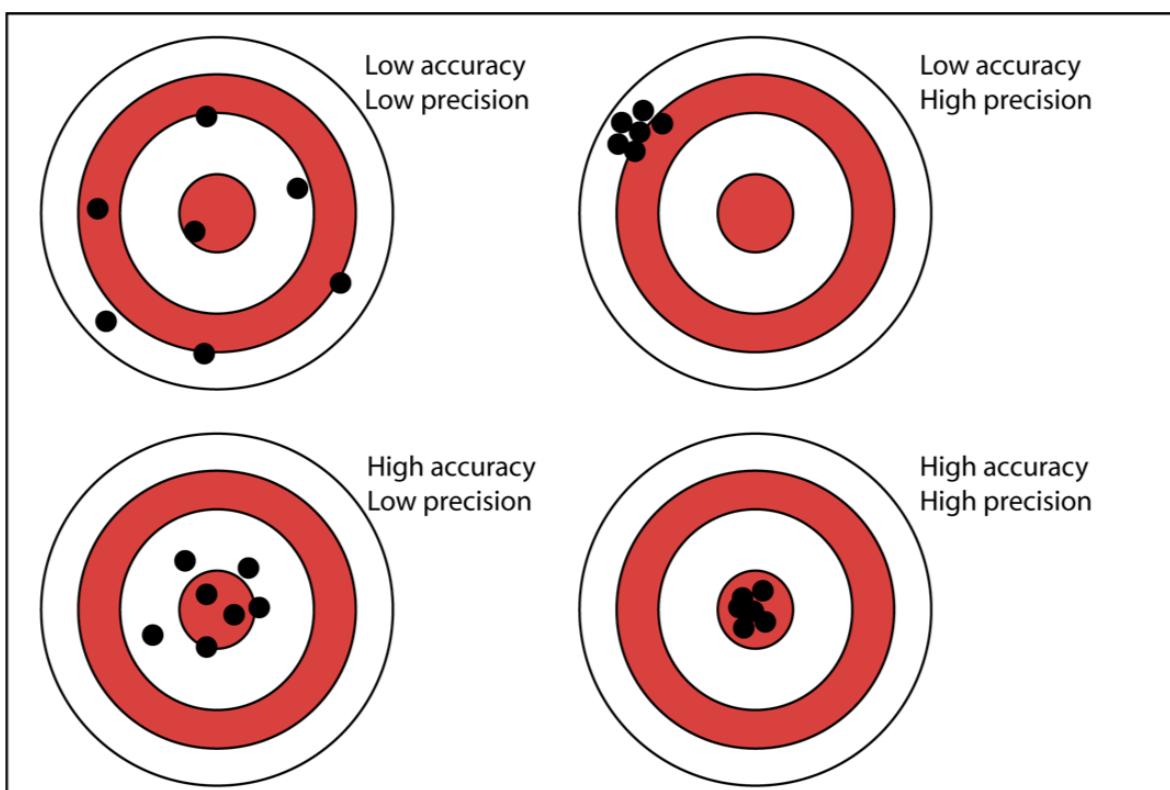
—Dr Alasdair Mac Arthur, 2016 NAROM Summer School

8.1.1 Accuracy and Precision Review

Precision is a function of random errors. It is a measure of statistical variation. In the Low accuracy High precision plot in the upper right corner the black dots are closely grouped together. If the locations of the black dots were plotted in a histogram the width of the histogram would be small. This indicates a low statistical variation in the data. Precision is an important metric of the analog system because every time the analog system is set to the same digital value the measured output voltages should have a small statistical variation.

Accuracy is a measure of how close to the truth the measured value is. In this case the measured values are the black dots. The high accuracy plots show that the black dots are close to the center of the Bulls Eye diagram. The center of the Bulls Eye diagram being the true value of this plot.

Figure 8.1: Analog System Settling Time Definition



8.1.2 Settling Time Definition

8.2 shows the different sections of a signal as it approaches the desired value. First, the DAC is loaded with the desired digital value. There is some delay time between inputting the value and the DAC starting to change its value. This is labeled Delay Time. The DAC then begins what is called Slewing. This is the time that the DAC is moving towards the desired value as fast as possible (biggest slope value). The DAC then approaches the desired value and enters a period of overshooting the value and then undershooting the value. At this point it is hunting for the value and should eventually settle to a DC value at the correct value indicated by the digital input value. In a practical situation however, the DAC may never settle to one distinct DC value. The DAC may keep oscillating between two values unable to settle to the mean of these two values.

In order to determine the final bit resolution of a DAC that is oscillating between two values the idea of an error band is introduced. The allowable output error band is determined by the bit resolution desired from the analog system. To convert bit resolution to voltage the formula:

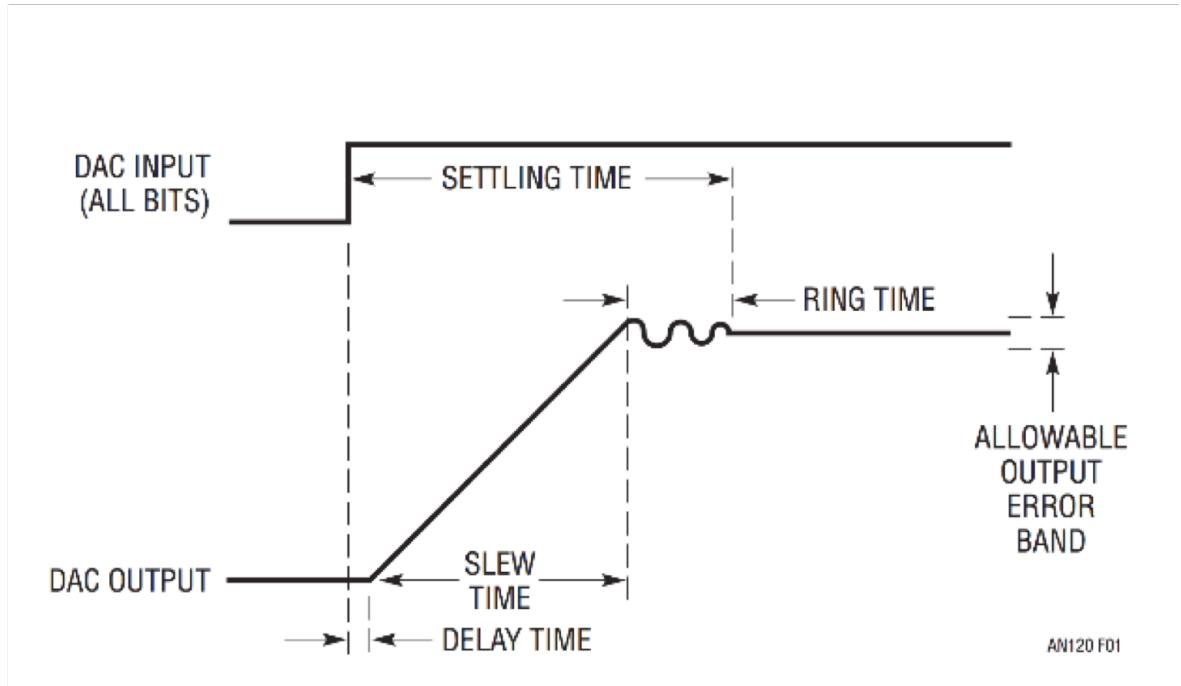
$$\frac{\text{maxvoltage}}{2^n} \quad (8.1)$$

Where n is the number of bits the desired analog system should have. As an example, for an analog system with a maximum output value of 5V and bit resolution of 4 bits the error band is:

$$\frac{5V}{2^4} = 0.3125V \quad (8.2)$$

The time it takes the analog system to be bounded by an error band that is 0.3125V in height is the settling time of the analog system to four bits. As the number of bits is increased the error band decreases. The smaller the error band is the more challenging it is for the analog system to reach a final value.

Figure 8.2: Analog System Settling Time Definition



8.1.3 Examples of Different Bit Resolutions

Some examples of different bit resolutions and their corresponding error bands will help give a more full understanding of the idea of error bands. First is shown a 1-bit settling time. This is essentially whether the signal is on or off. [8.4](#) shows a 2-bit system. In this system, the shaded area is about 7V. The 2-bit system is able to determine whether the signal has settled between 7 and 14 volts. This is not exceptionally useful. The third figure [8.5](#) is a 4-bit system. In this system the shaded area is about 1 volt. The system can determine that the final value is between 9.5 and 10.6 volts. This is more useful than the 2-bit system in determining the final settled value.

Figure 8.3: 1 Bit System

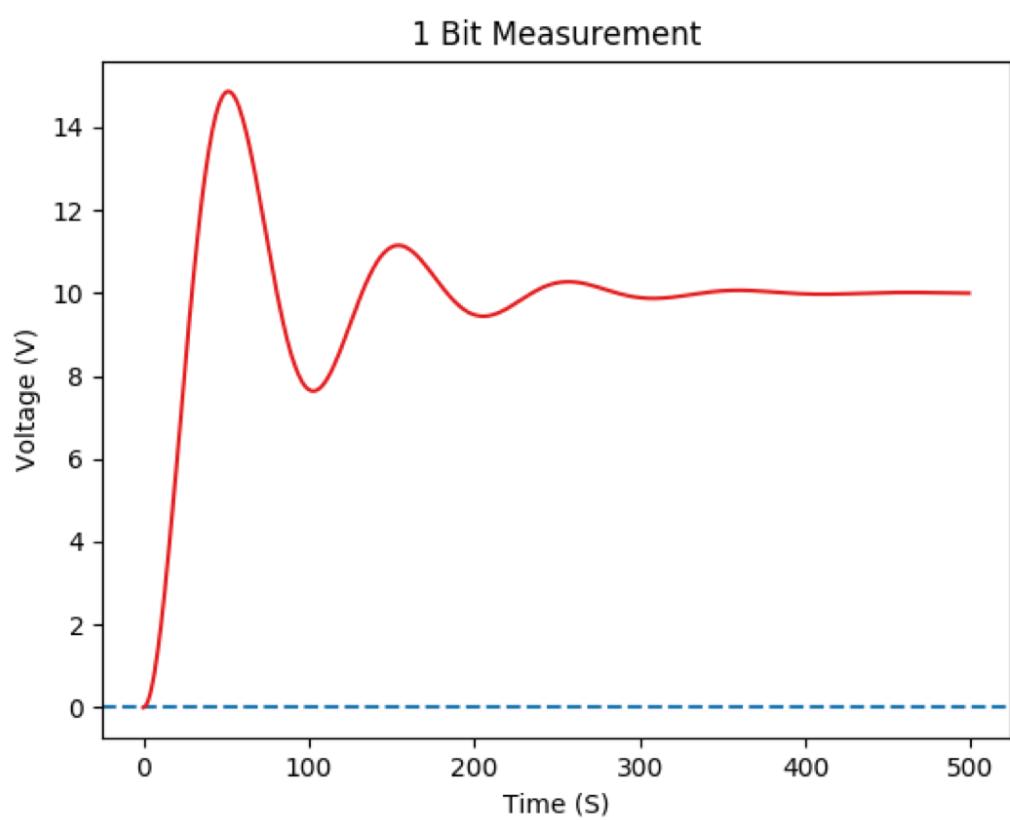


Figure 8.4: 2 Bit System

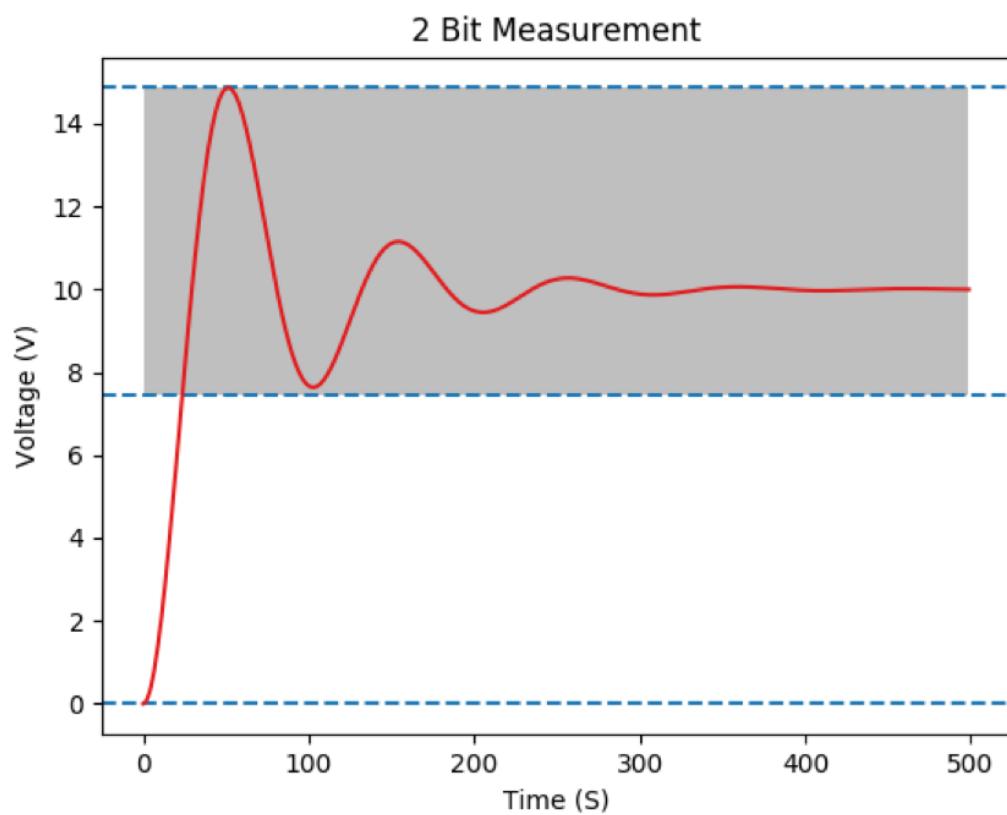
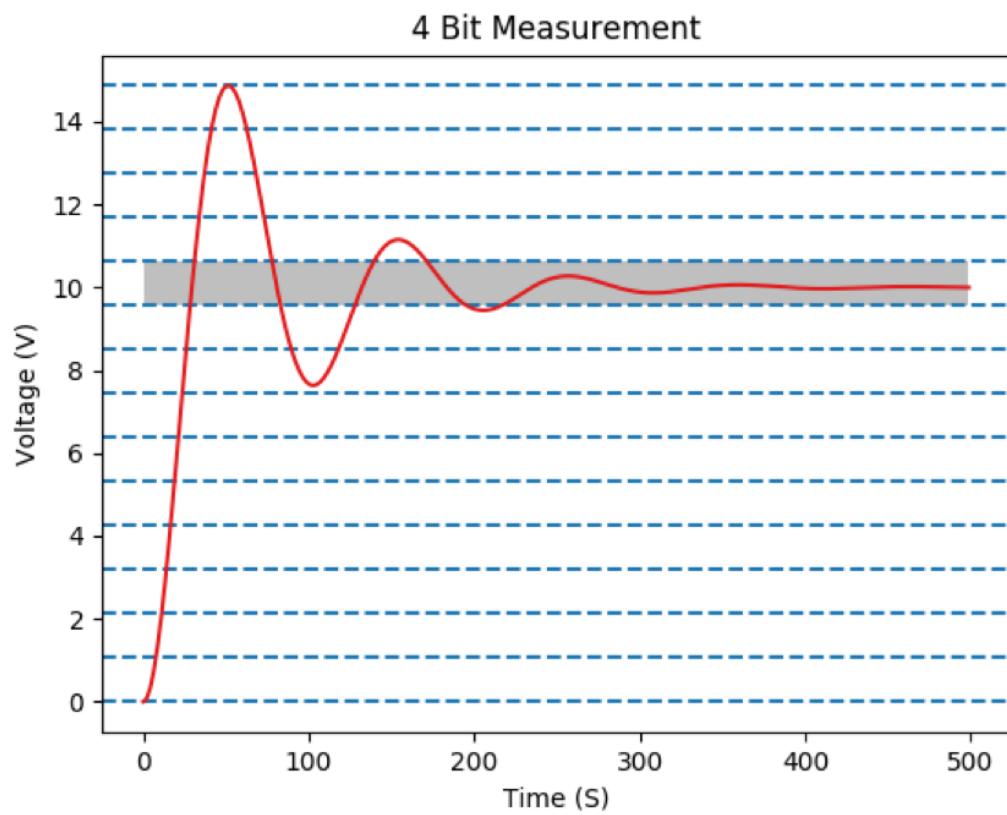


Figure 8.5: 4 Bit System



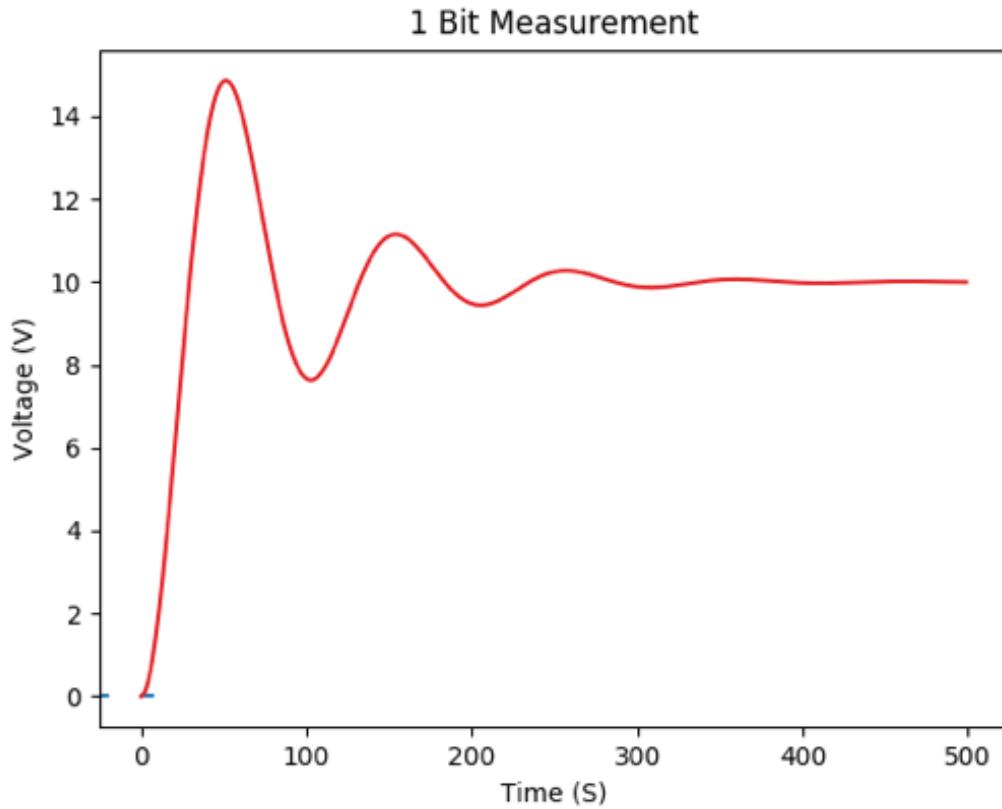
8.2 Measuring Settling Time

The settling time signal is a small AC signal that is superimposed on top of a large DC signal. Figure 8.9 is useful for visualizing this idea. On the left side we see a red AC signal centered around 0V. On the right side we see a 10V DC signal. When these signals are added they combine to form a signal that looks like the one in 8.6. It would be advantageous if we could separate these two signals and view only the small AC signal. The first order answer would be to simply move the waveform on an oscilloscope down with the vertical axis control. This would center the top of the whole waveform in the center of the oscilloscope screen. Then it would be simple to adjust the gain and zoom in on the AC settling signal. However, there is a major problem with this approach. The issue is called oscilloscope overdrive. Overdrive occurs when a signal extends off of the oscilloscope screen. This causes a nonlinear oscilloscope response. A full discussion of how oscilloscope overdrive occurs is included in A.2.

It is required that the two signals be separated. Another first order solution is to use a filter like the AC coupling option on an oscilloscope. Figure 8.7 shows the AC coupling setting on an oscilloscope. This setting uses a high pass filter to remove the DC signal on an input signal. A high pass filter and its corresponding frequency response is shown in figure 8.8.

Historically, a false summing node technique has been used for settling time measurement [45]. The false sum node technique is shown in figure 8.10. In this circuit configuration the a positive input pulse is fed into an amplifier under test (AUT). The output of the AUT will be $-V_{in}$ when an input pulse is fed into the AUT. The clamping diodes constrain the voltage range of the output to plus or minus the forward voltage drop of the diodes (typically 400mV for a Schottky diode). The circuit has some limitations. Chiefly, that if gain will be used in the oscilloscope then the voltage range the limiting diodes allow will still cause oscilloscope overdrive during the slew time of the AUT in some gain settings. This will lead to measurements that are not correct. The resistor divider causes another issue when an oscilloscope probe is attached to the output of the circuit. An oscilloscope probe has a fair amount of capacitance

Figure 8.6: Oscilloscope AC Coupling Setting.

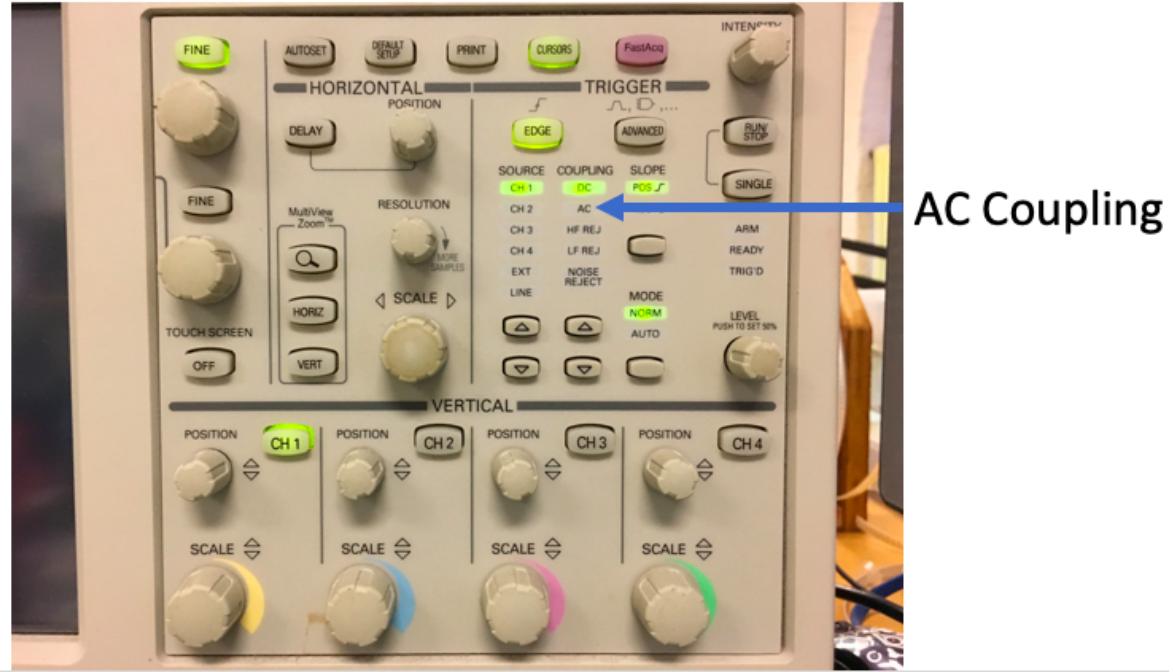


(10 - 12pF). Combining the probe capacitance with the resistor values creates an RC filter at the output of the circuit. This distorts the settling time signal and makes it impossible to recover all of the settling time information from the AUT. This circuit is also dependent on the input pulse being well behaved and settling quickly. The input pulse settling time and the settling of the of the AUT will be indistinguishable from each other – making it impossible to measure the settling time of the AUT.

Jim Williams describes a solution that is inspired by the Classic Sampling Oscilloscope [45]. He proposes a conceptual circuit that is shown in figure 8.11.

This circuit has a number of advantages over the standard false sum node circuit. Most importantly, the output is sampled in time in this circuit. The time sampling

Figure 8.7: Oscilloscope AC Coupling Setting.



is accomplished through the use of a switch and a delayed pulse derived from the input pulse. The time sampling ensures that while the amplifier is slewing it is not being inputted into the oscilloscope. This removes the risk of causing an oscilloscope overdrive event during the slewing portion of the signal and enables the use of all gain modes on the oscilloscope. This circuit also includes a current step input rather than a voltage step input. This is because it is easier to control a current than it is to control a voltage (see Appendix A.1 to understand why).

Ten years later, in a paper published in 2010 [44] Jim Williams supplies a conceptual circuit diagram for a circuit that is able to measure the settling time of an 18-bit DAC. This is shown in figure 8.12. This circuit is almost the same as the previously published circuit, but now includes a preamplifier for the oscilloscope to ensure that there is enough gain in the system to properly view the small 18-bit signal. The circuit also uses a DAC instead of a pulse generator. The reason for using a DAC being a difference in purpose of the papers.

Figure 8.8: High pass filter and corresponding frequency response.

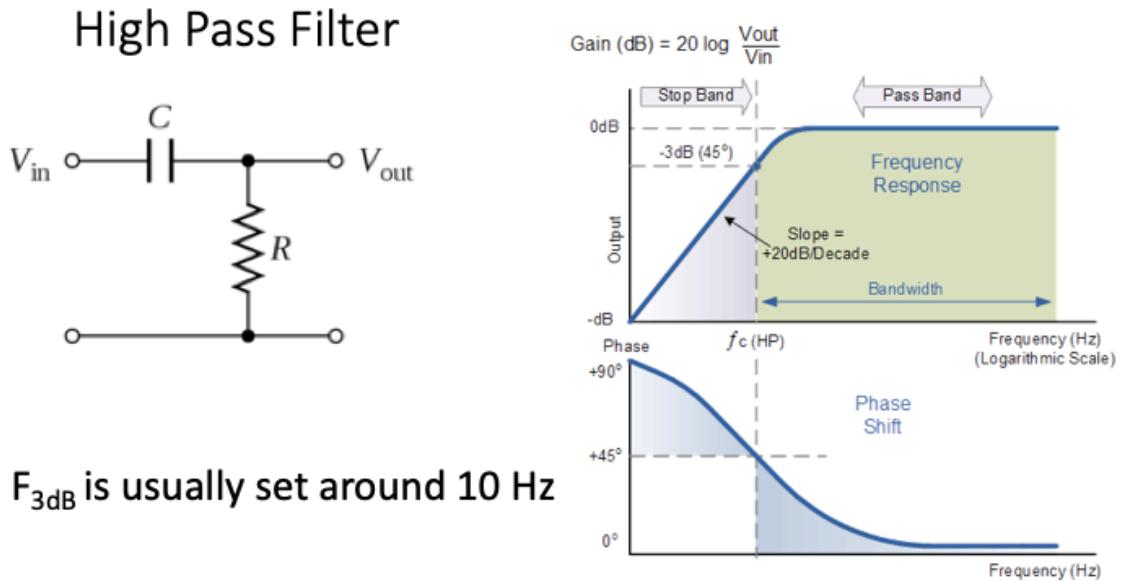


Figure 8.9: Decomposition of analog signal into settling component and DC component.

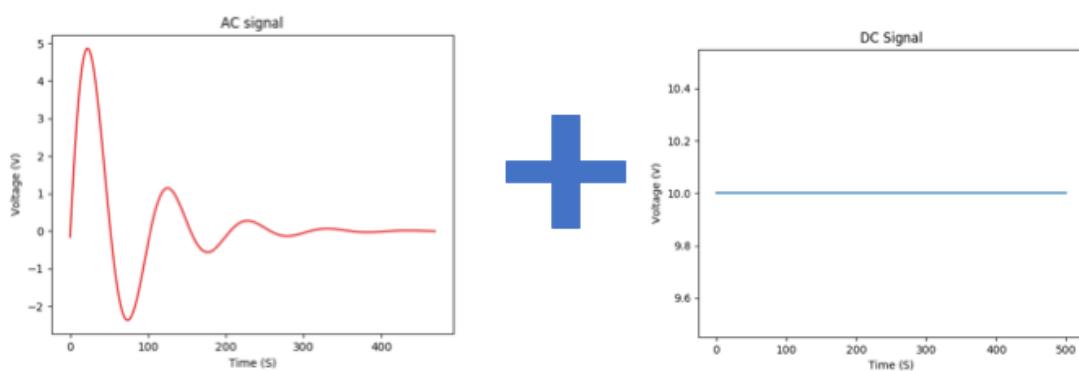


Figure 8.10: False Sum Node historically used to measure settling time.

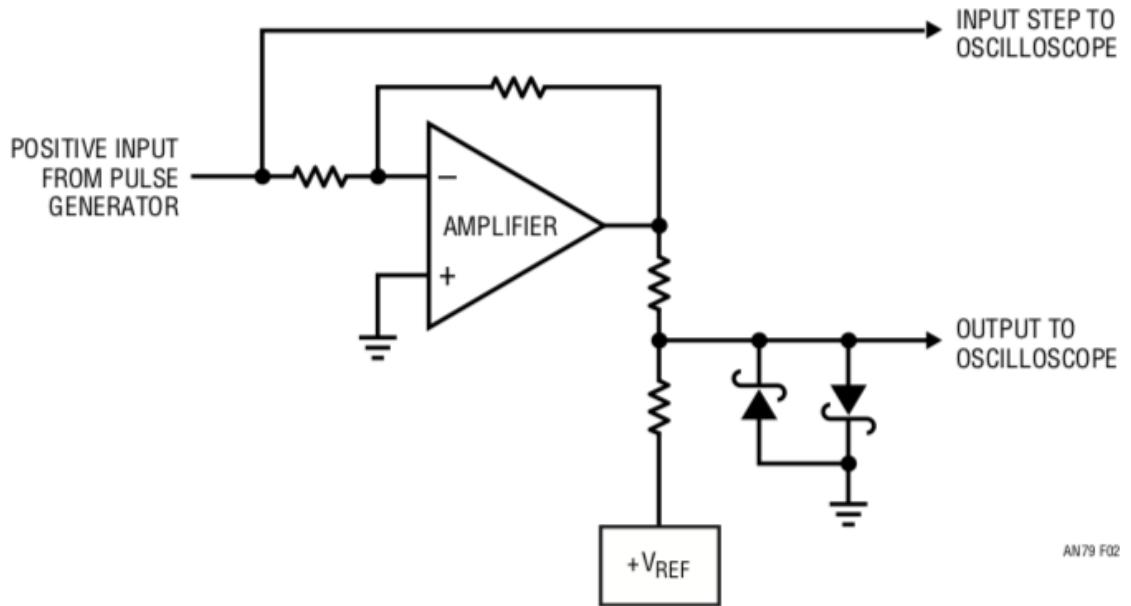
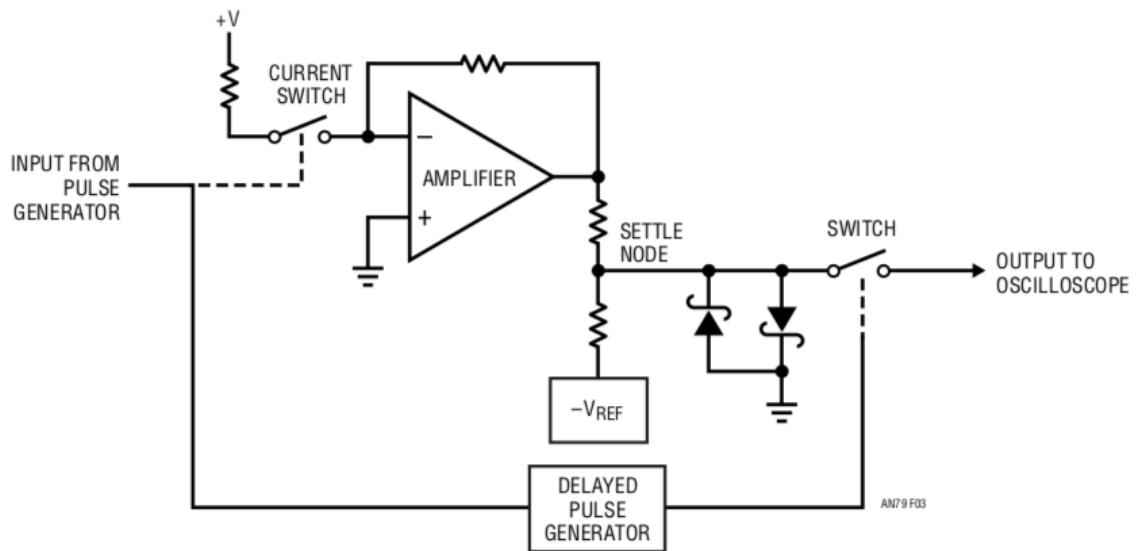
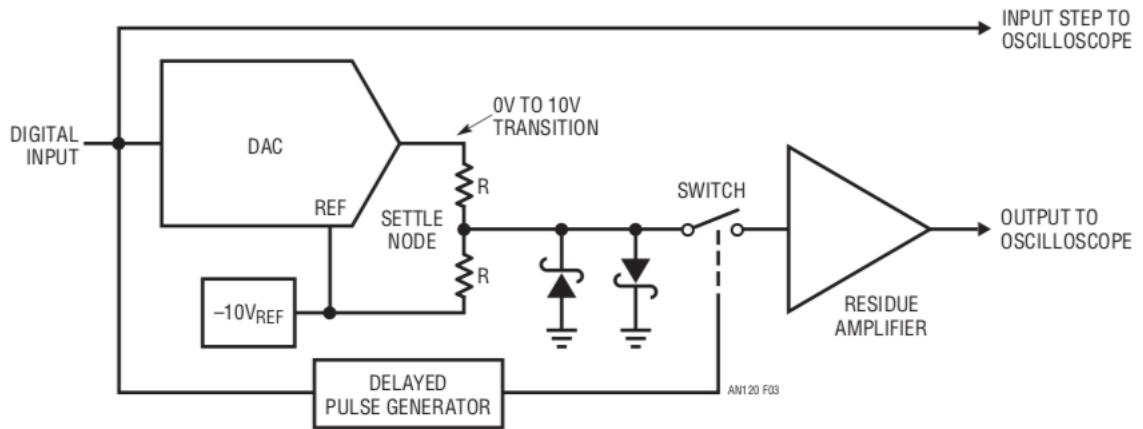


Figure 8.11: False Sum Node historically used to measure settling time.



In both circuit designs the design of the time sampling switch is important because it should not cause a distortion of the settling signal information. The switch can cause distortion by decreasing the bandwidth of the total circuit and by introducing feedthrough artifacts into the settling signal from the command signal. Feedthrough is primarily caused by parasitic capacitance that makes an AC connection between the command signal and the settling signal.

Figure 8.12: False Sum Node historically used to measure settling time.



In general, the concept of both circuit architectures is to limit the voltage range that can be seen by the oscilloscope with clamping diodes. Then only input a signal into the oscilloscope after slew time has occurred to ensure that no voltages large enough to cause overdrive are inputted into the oscilloscope. The design of these circuits using real components and the actual physical construction of the circuit is non-trivial. In both papers [45] and [44] Jim Williams describes in great detail his choices of components and construction techniques.

8.2.1 Settling Time Instrument Conceptual Overview

8.2.1.1 Overview and Inspiration

The settling time circuit described in this section was heavily influenced by the work of Jim Williams in his papers [45] and [44]. The circuits he describes in these

papers were described in detail in the previous section of this dissertation. The two main challenges Jim addresses with his circuit are:

1. Oscilloscope overdrive
2. Proper signal probing

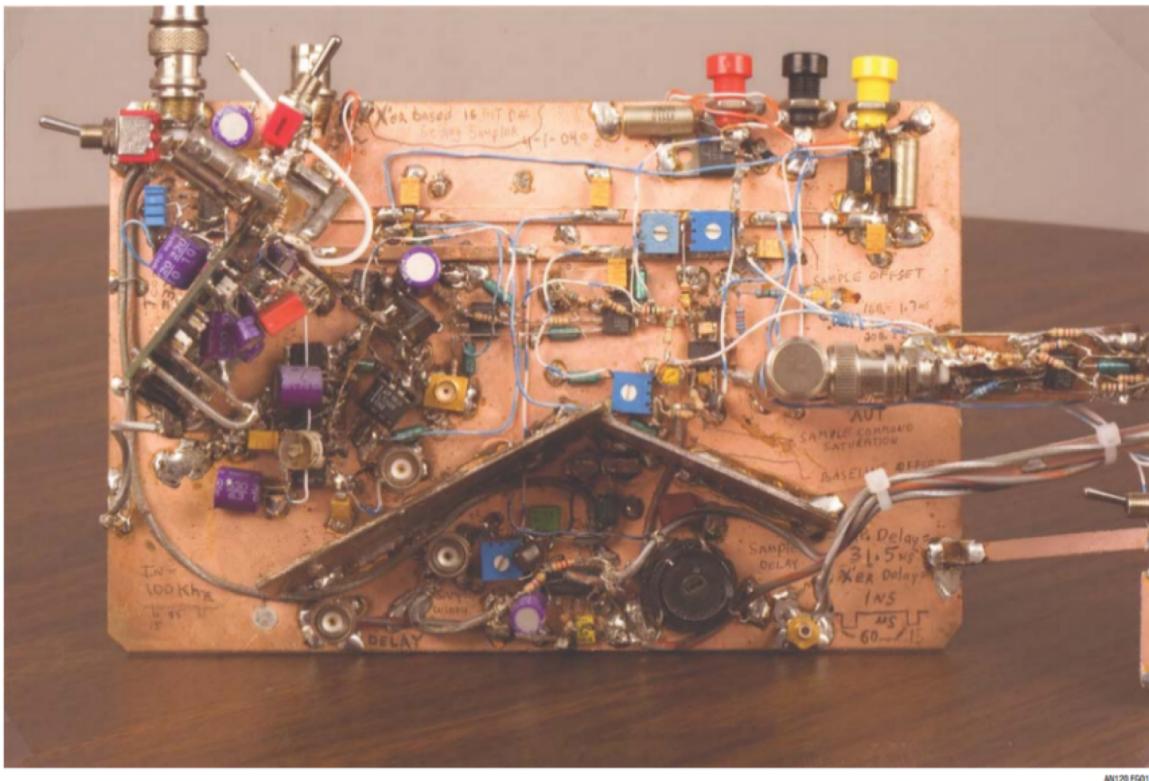
The conceptual overview of his circuit architecture is to design a circuit that limits the output voltage range of the circuit, and the output of the circuit can be sampled in time to ensure that the slew rate of the output signal is not transmitted to the oscilloscope. Both of these design goals were chosen to eliminate the risk of overdriving the oscilloscope. The proper signal loading is handled by the addition of the time-sampling switch. The oscilloscope probe capacitance no longer directly connects to the resistor divider and does not create an RC time constant.

Initially, it was planned to simply reproduce the circuits that were offered in these papers and use them for our own settling time measurements. Unfortunately, the experience required to properly layout the circuits was non-trivial. Figure 8.13 shows Jim Williams finished prototype. In this circuit every wire and component has been deliberately oriented a specific way. Not having the benefit of a long career in the electronics industry it was thought that construction of the circuit would be difficult and the instrument could not be trusted. It was chosen to attempt to design a circuit that would be:

1. Easier to construct and reproduce.
2. Easily expandable bit depths for increased measurement resolution.

Initial inspiration for the basic architecture of the settling time circuit came from observing the iPhone 5S logic board. Figure 8.14 shows the logic board with no shielding and Figure 8.15 shows the logic board with shielding. The logic board has clearly defined sections that are individually shielded to prevent interference from external sources and from cross-talk amongst themselves. Connections between sections are done with carefully planned transmission lines. If an iPhone could be built in

Figure 8.13: Prototype of Jim Williams' 18-bit Settling Time Instrument.



this manner could a settling time measurement instrument also be constructed in this manner?

It was decided to construct the settling time instrument out of repeated unit cells that could be individually shielded and linked together with controlled impedance transmission lines. This would be a similar construction as that of the iPhone logic board. The unit cell construction is also convenient because it allows more unit cells to be easily added to the design depending on the bit resolution desired. Each unit cell would have a gain of four, which would yield two bits of resolution.

Figure 8.14: iPhone 5S Logic Board.

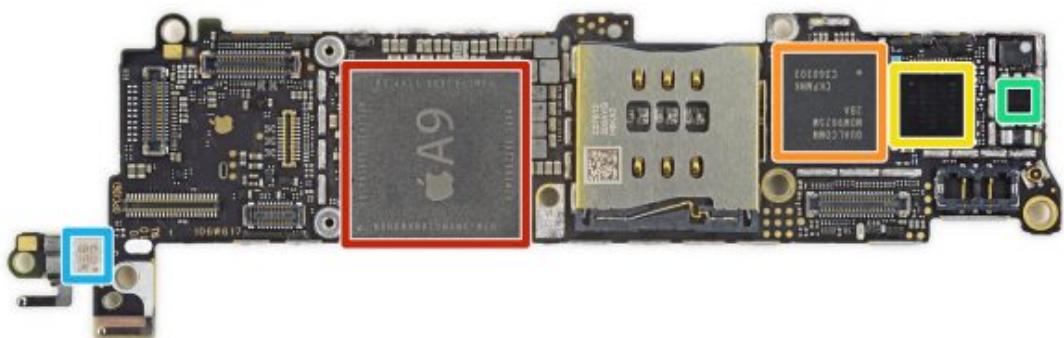
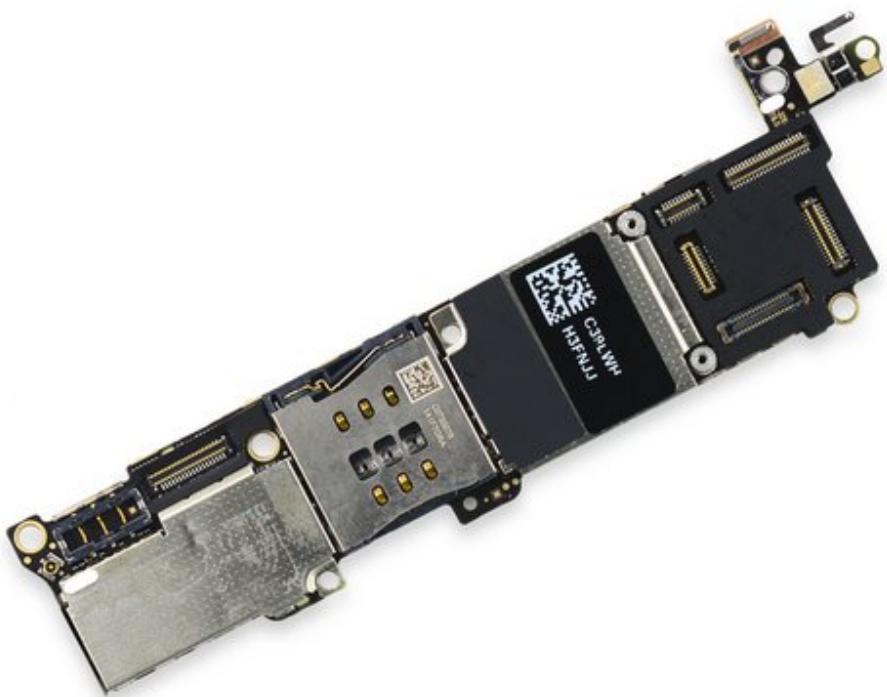


Figure 8.15: iPhone 5S Shielded Logic Board.



8.2.2 Settling Time Instrument Conceptual Overview

Conceptually, the goal of the Settling Time Instrument is to provide several stages of unit cells. Where each unit cell adjusts the DC offset, multiplies the input by a certain gain factor, and clips the output to limit the output range. This can be colloquially said as: zooming in on the top of the waveform, where the small settling time signal exists.

The block diagram of a unit cell is shown in figure 8.16.

Figure 8.16: Unit Cell block diagram.



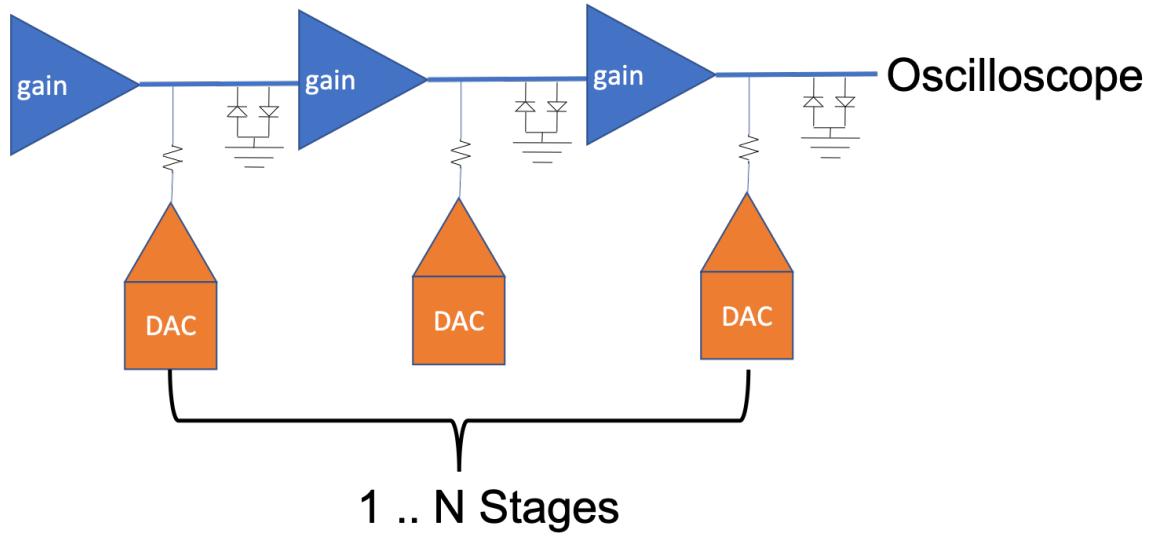
The unit cell has several functions it can perform. The first is the subtraction of an offset value. The subtraction function is for removing the DC portion of the AUT output. Instead of using a very precise source as Jim Williams did and subtracting once in the circuit. Here there are multiple less precise subtractions being conducted. The amount of subtraction per unit cell is controlled by a feedback algorithm that measures the output voltage to see if it is centered around zero. If the output voltage is not centered around zero the algorithm uses an optimizer routine to determine, which unit cell or cells should be used to correct for the offset. The algorithm will consider the location of the unit cell in the signal chain. A unit cell closer to the output will have a more fine-grained ability to shift the output signal than one placed near the beginning. This is because DC offsets in unit cells near the beginning will be multiplied in each consecutive stage by the gain factor. The algorithm must also have some hard limitations for the maximum voltages it can subtract from a stage. This is to ensure that it will not saturate a unit cell amplifier.

The second function that a unit cell can perform is a multiply function. The multiply function is used to increase the size of the waveform features. This enables the smaller settling time signal features to be viewed on an oscilloscope without having to use the gain in the oscilloscope. The third function is a clipping function that is used to limit the output range of each unit cell. This is important because we wish to remove all parts of the signal except the small settling time signal. The clipping function can be thought of as a cropping function in an image editing tool.

A slightly more detailed diagram is shown in figure 8.17. This diagram shows the functions for the unit cells being performed by generic electronic components. The amplifiers providing the gain in each unit cell are drawn as triangles with the word gain in them. The subtraction is performed by a DAC connected to the circuit by some resistance. The clipping function is performed by a pair of diodes. The output is sent to the oscilloscope.

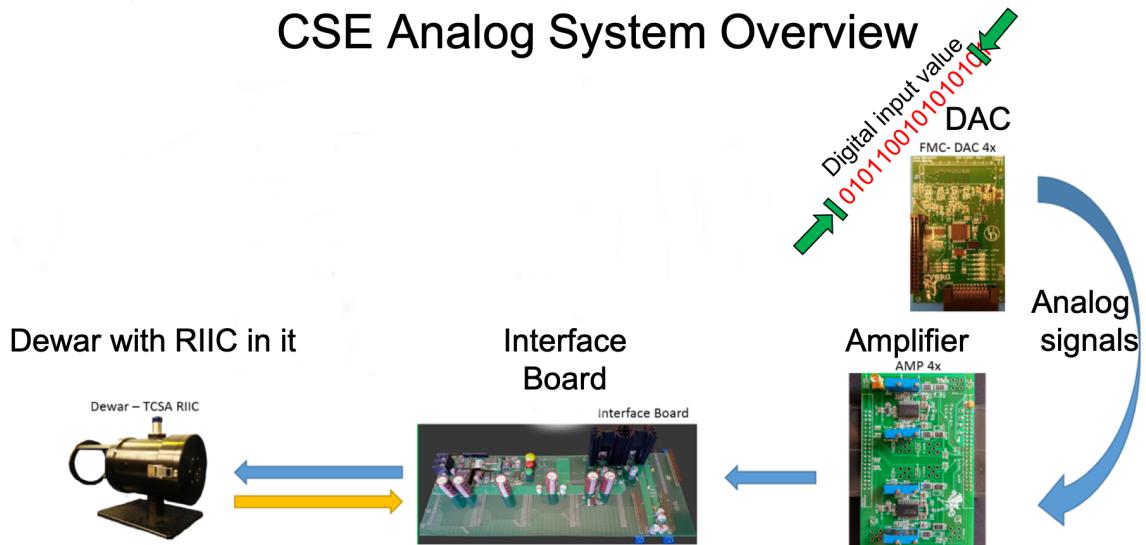
As a recap, conceptually with this circuit we would like to zoom in, and crop the signal in every unit cell until we have expanded the desired error band (14, 16, 18 bit LSB etc.) to be the same size as the voltage range allowed by the forward voltage drop of the diodes used. The next section shows how this circuit works in the most ideal scenario using a mathematical model written in Python.

Figure 8.17: Settling Time Instrument Conceptual Diagram.



8.3 CSE Analog System Overview

Figure 8.18: CSE Analog System Overview



The main function of the analog system is to set the brightness for each IRLED

pixel in a frame. The brightness of the IRLED pixel is set by increasing or decreasing the voltage sent from the DAC and Amplifier pair. This voltage can be thought of as a symbol in an information transmission system. The greater the resolution of the DAC and Amplifier combination the more symbols that can be transmitted and displayed by the IRSP.

The Analog System for the CSE is composed of four main components: the DAC, the Amplifier, the Dewar and RIIC, and the transmission lines that connect the other components together. I have combined the Dewar and the RIIC into one unit because they are physically inseparable and it is not possible to isolate the parasitic loads associated with each one.

The DAC is an AD9747. It is a 16 bit DAC current output DAC. There are two DACs per package. The DAC board has two AD9747 ICs on it. Yielding a total of four DACs per board. The AD9747 was chosen because of its 16-bit accuracy and 250 MSPS output rate. A complete review of the DAC PCB is given in appendix [A.3](#).

The Amplifier in the system is a THS6012. The THS6012 is a DSL line driver capable of driving 400 mA into a 25 ohm load, with a max slew rate of 1300V / μ s. The high current output is required for this application because of the inductive and capacitive parasitics inherent in the analog system. The inductance is largely due to poor grounding in the Dewar and the large loop area caused by the ribbon cables and the interface board. The capacitance is a result of the nature of the RIIC. The RIIC has pad capacitance, but also a large input capacitance per pin. Unfortunately, it has not been possible to measure and quantify this capacitance value. Combining the parasitic inductance and the parasitic capacitance results in a hard load to drive to full value within the time budget of a frame being displayed. To overcome the parasitics inherent in the system an amplifier with enough output current capacity to really push the RLC parasitics to the desired value.

The Dewar and the RIIC are custom devices. The RIIC is a large CMOS ASIC that was designed in CVORG and CDS. It was then fabricated at the ONSEMI facility with a 0.5 micron process. The RIICs function for the Analog System is to transmit

the incoming voltage from the DAC and Amplifier combination to the correct pixel. This voltage then sets the brightness of that particular IRLED. The Dewars function is to provide an environment that the IRLED hybrid can be cooled to cryogenic temperatures in. Going to cryogenic temperatures requires a vacuum chamber to increase the insulation between the outside Dewar wall and the cooled IRLED hybrid.

8.4 Settling Time Circuit Mathematical Model

To prove the validity of the conceptual idea of the Settling Time Instrument presented in this dissertation a mathematical model was first developed. It is convenient to start from a math model because it eliminates circuit parasitics and the non-idealities of circuit components.

8.4.1 Unit Cell Overview

In 8.19 a block diagram for the unit cell of the novel settling time architecture is shown.

The input signal enters into the unit cell and a constant value is subtracted from it. The subtraction step is used to center the input signal around zero. In 8.20 we see a signal that after an initial slew period is centered around 1 Volt. After the subtraction step it is now centered around 0 Volts. The slew portion of signal is also now negative.

In order to view the small settling time signal at the end of the time series we must multiply the input signal time series by a gain value to increase the magnitude

Figure 8.19: Block Diagram of Settling Time Mathematical Model Unit Cell



Figure 8.20: Block Diagram of Settling Time Mathematical Model Unit Cell

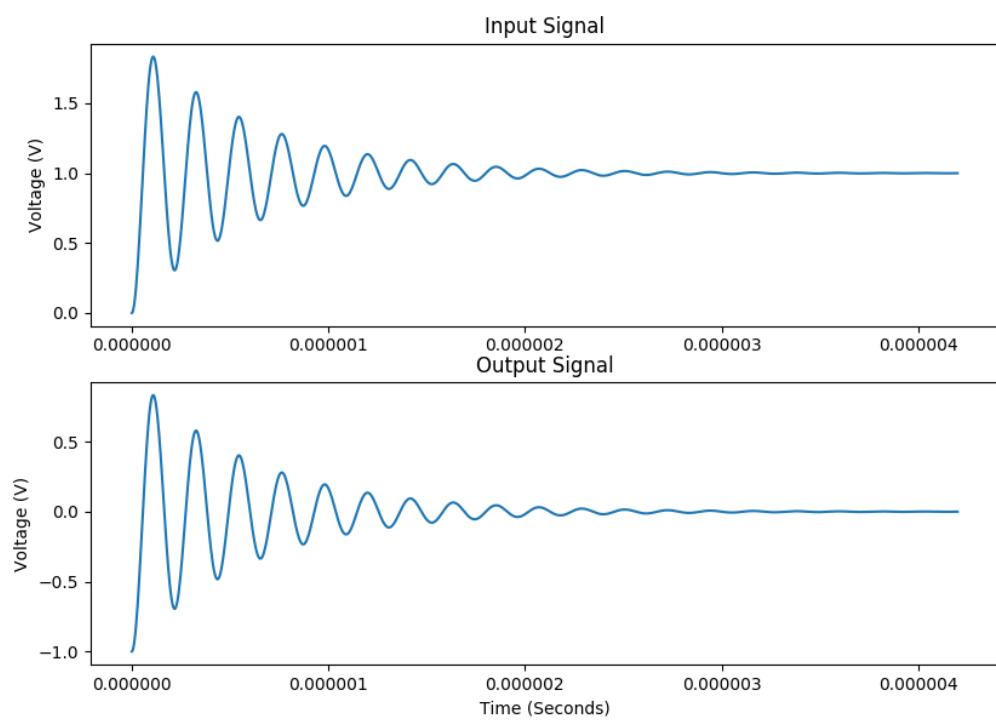
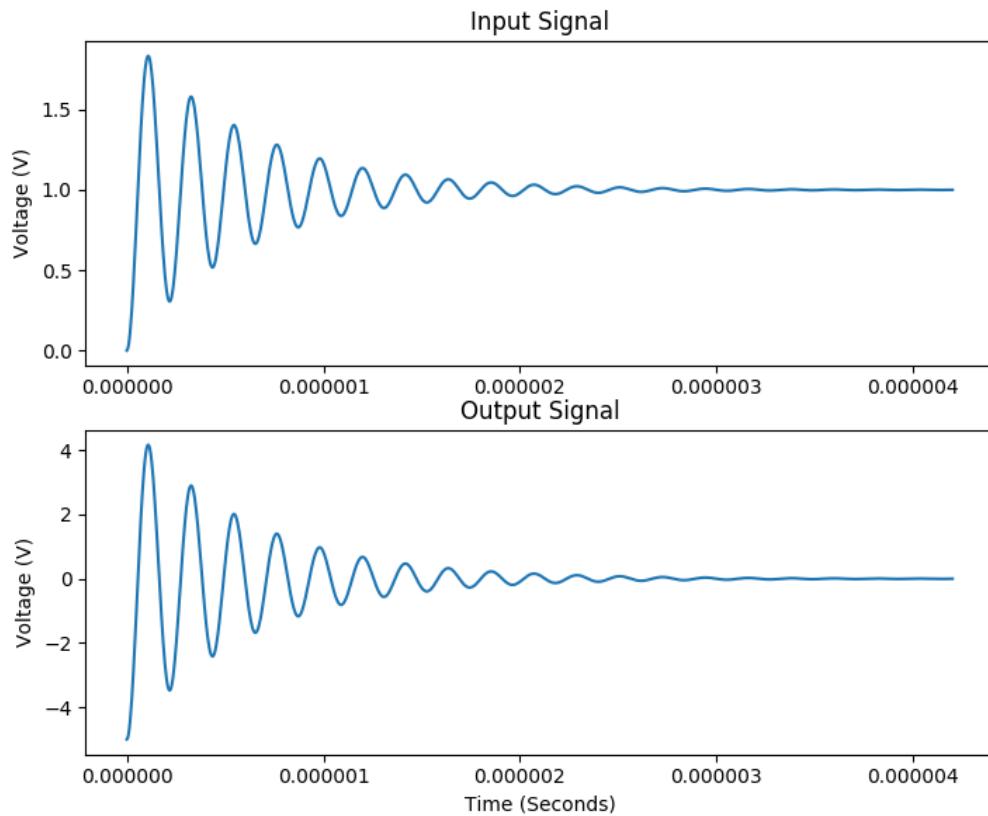


Figure 8.21: Input signal and output signal showing the effects of the subtraction and the multiplication steps together.



of the signal. This is done in the multiply step. The results of both the subtraction step and the multiplication step are shown in 8.21. Here we see that the signal is five times larger. A gain of five was arbitrarily chosen for demonstration purposes.

The third step in the unit cell is to clip the output of the unit cell to a small value. This is to limit the possible output range and avoid oscilloscope overdrive. Oscilloscope overdrive is explained in detail in Appendix A.2. The clipping is performed by the Numpy Clip function (`np.clip`). The entire output of a single unit cell is shown in 8.22. The output signal is clipped to $\pm 300\text{mV}$. This value was chosen because it corresponds to the forward breakdown voltage of the diodes chosen for the actual circuit design. In the beginning of the signal the input signal is too large and causes

Figure 8.22: Input signal and output signal showing the effects of the subtraction and the multiplication steps together.

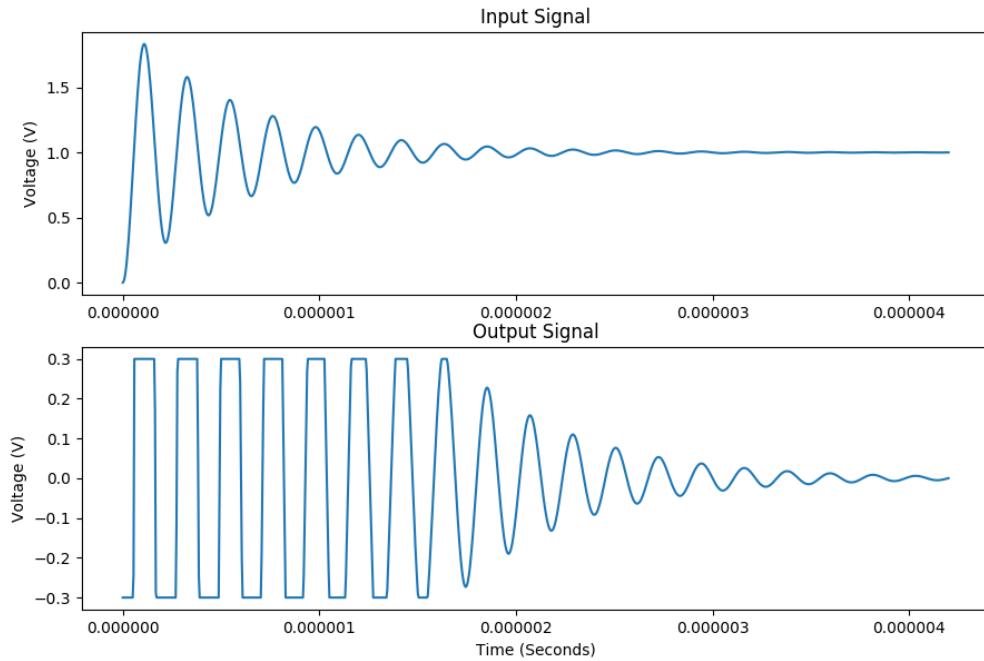


Figure 8.23: Unit Cell Python Code.

the clipping function to clip the value to ± 300 mV. At the end of the time series the signal has a small enough range to fit within the limits set in the clipping function. The signal towards the end in the output is also larger now due to the multiplication step.

The Unit Cell code is shown below. It includes all three steps in the block diagram. The subtraction value is called `subv`, the multiplication value is called `gain`, an optional offset parameter is included to model input voltage offset in the operational amplifier, but is not used in these simulations. The clamping values are manually set internal to the function.

If there are input offset voltages present in the operational amplifier used to

perform the multiplication step. They can be modeled by generating a random offset value and then adding that to the input signal. This is shown in the unit cell code by subtracting the randomly generated offset value from the desired subtraction value. This only works for positive offset values.

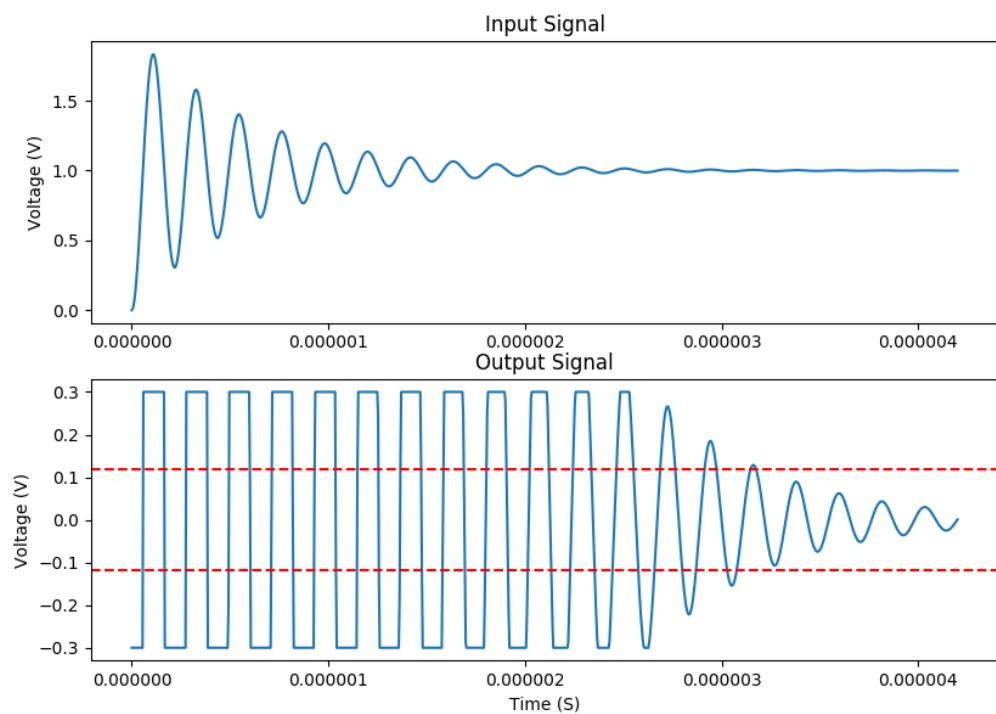
8.4.2 System Simulation

The whole system consists of several unit cells attached sequentially together. The output from one unit cell is attached to the input of the following unit cell. This occurs until the last unit cell is reached and the output of that unit cell is attached to an oscilloscope or in this case is plotted. The goal of the Settling Time Instrument is to amplify the small settling signal, while avoiding oscilloscope overdrive and signal distortion.

Oscilloscope Overdrive in general, is caused by drawing off screen on the oscilloscope. To avoid that the output range of the total system is clamped to $+/- 300\text{mV}$. Jim Williams notes that this can still cause overdrive depending on how much gain the oscilloscope is set to use. He uses time sampling to only look at the signal when it is beyond the slewing portion. This eliminates having a large feature and a small feature being displayed at the same time on the oscilloscope. In the instrument presented here the deleterious effects of having two differently sized features displayed at the same time is overcome by amplifying the desired error band to the same size as the range of the limiting diodes. In this case that range is $+/- 300\text{mV}$. No gain is used on the oscilloscope with this instrument. All gain is provided by the instrument. Figure 8.24 shows the output of the instrument after five stages with a gain of five.

The desired error band in this simulation was a 16 bit LSB on a 5 Volt system. The error band is approximately 76 microvolts for a 16 bit resolution. Using 5 stages where each stage has a gain of 5 magnifies the error band to approximately 230mV. This is very close to the forward voltage drop of the limiting diodes. The magnified error band is shown in figure 8.24 with red dashed lines. The rest of the signal is cut

Figure 8.24: The final system output is shown along with the corresponding upper and lower limits of the error band. The error band is shown by the dashed red lines.



off with the limiting diodes. The features have been made to be a similar size and can be viewed at the same scale on the oscilloscope.

8.4.3 System Bit Resolution

One of the unique attributes of this architecture is that instrument resolution can be added by adding more unit cells into the design. Each unit cell provides a gain of 5 in this simulation. A gain of 5 is equivalent to approximately 2 bits of resolution because $\log_2 5 \approx 2$. In this simulation, the instrument has a system resolution of approximately 18 bits – 10 bits from the unit cells and 8 bits from the oscilloscope.

8.5 SPICE Simulation

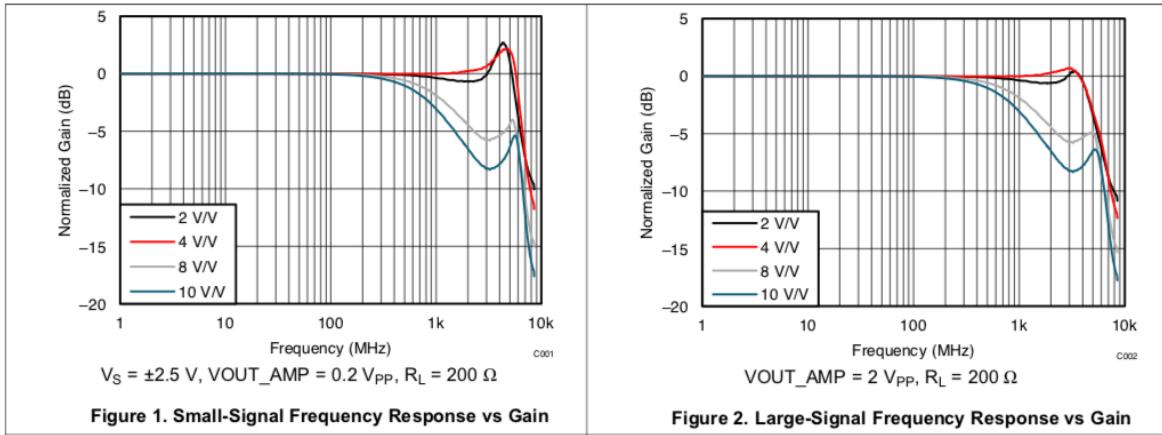
8.5.1 Electronic Component Choices

The electronic components used to design this circuit had to be chosen carefully to maximize bandwidth of the circuit. A higher bandwidth translates into a faster circuit rise time. The circuit rise time is required to be much less than the device under test (DUT) to ensure that the settling time circuit does not dominate the response seen when connecting the settling time circuit to the device under test. The following several sections describe the trade off space and the choices about why specific components were chosen.

8.5.1.1 Operational Amplifier

There were two major considerations for the choice of op-amp in this circuit: bandwidth, and differential. The operational amplifier for this circuit is required to have a bandwidth that is high enough to pass a 1 - 5 ns rise time pulse with little distortion. This could be calculated by assuming some idealities and considering what first order low pass system would be able to do this. However, when actually constructing the circuit other parasitics and non-idealities will play a major role. The best option is to find the op-amp with the highest bandwidth that can support the voltage input and output level requirements of the circuit. It was also convenient to use a voltage feedback style op-amp because they are more tolerant to different gain values due to their frequency response not being tied to the gain resistors.

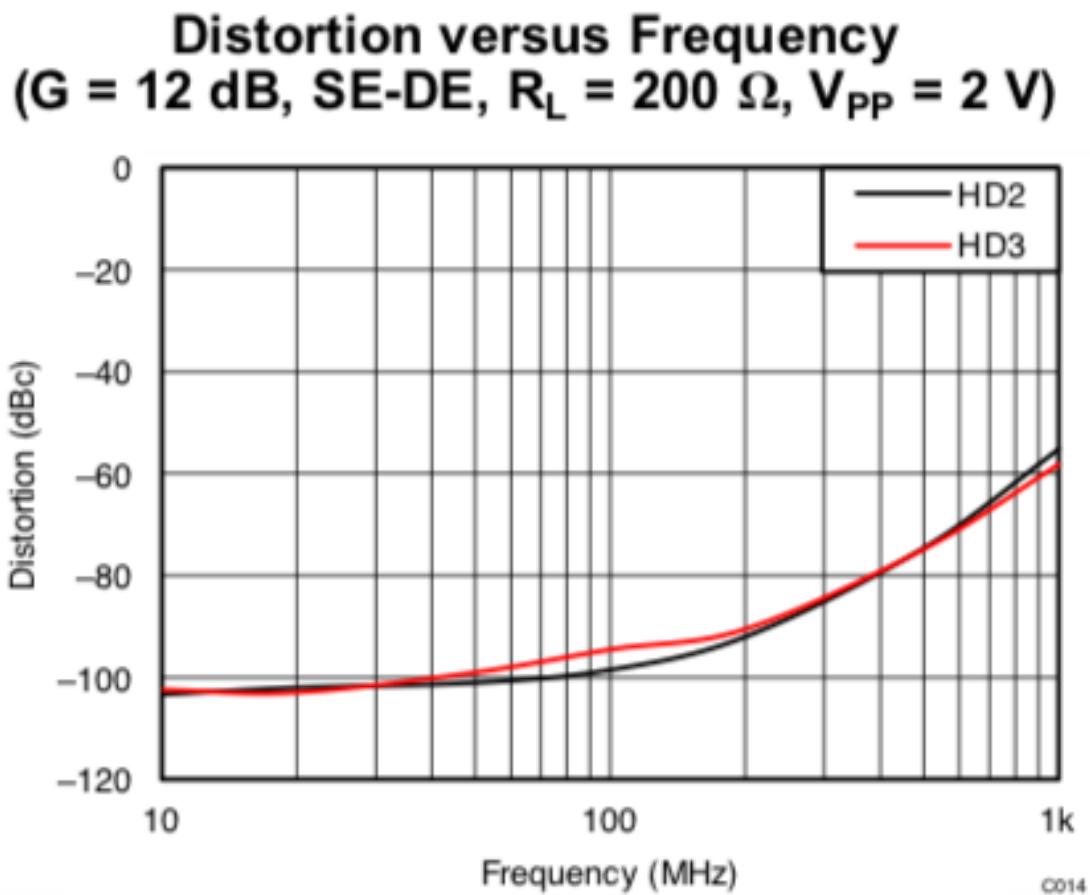
Figure 8.25: Frequency Response of the LMH5401.



The second major consideration was the differential or single ended. It was decided that differential was preferable because then the circuit would carry its ground with it. In a single ended configuration the return current must travel back to the source on a ground plane. The ground plane will create a loop area that will increase the inductance in the circuit. Due to the speed of this circuit any additional inductance was not preferable. A good choice for this application was the LMH5401. The LMH5401 was designed for use in a variety of applications involving driving or being driven by Giga-sample per second (GSPS) ADCs. The LMH5401 is a Fully Differential Op-amp that has a gain-bandwidth product of 8GHz. This is a very good gain-bandwidth product especially for a voltage feedback op-amp. The frequency response is shown in 8.25. It can be seen that the for a gain of 4 V/V (red line) that the frequency response extends well out to 8GHz.

The LMH5401 also has a very low distortion shown by the plot of HD2 and HD3 levels across frequency in 8.26. Low distortion in this application is good because the signal to be measured will be small. Any distortion incurred by the op-amp will mask some of the signal. Full information about the LMH5401 is available in the datasheet: <http://www.ti.com/lit/ds/symlink/lmh5401.pdf>

Figure 8.26: Frequency Response of the LMH5401.



c014

8.5.1.2 Clamping Diode

The choice of clamping diodes is important because they are directly connected to the fast settling node. Any parasitics the clamping diodes have will directly impact system performance. The selection process for the clamping diodes was to first find two diodes in an antiparallel configuration. This configuration has the minimum amount of pads and PCB traces because the diodes are already configured in a clamping orientation. When selecting for this configuration on Digikey only one product was listed, the SMS7621-092.

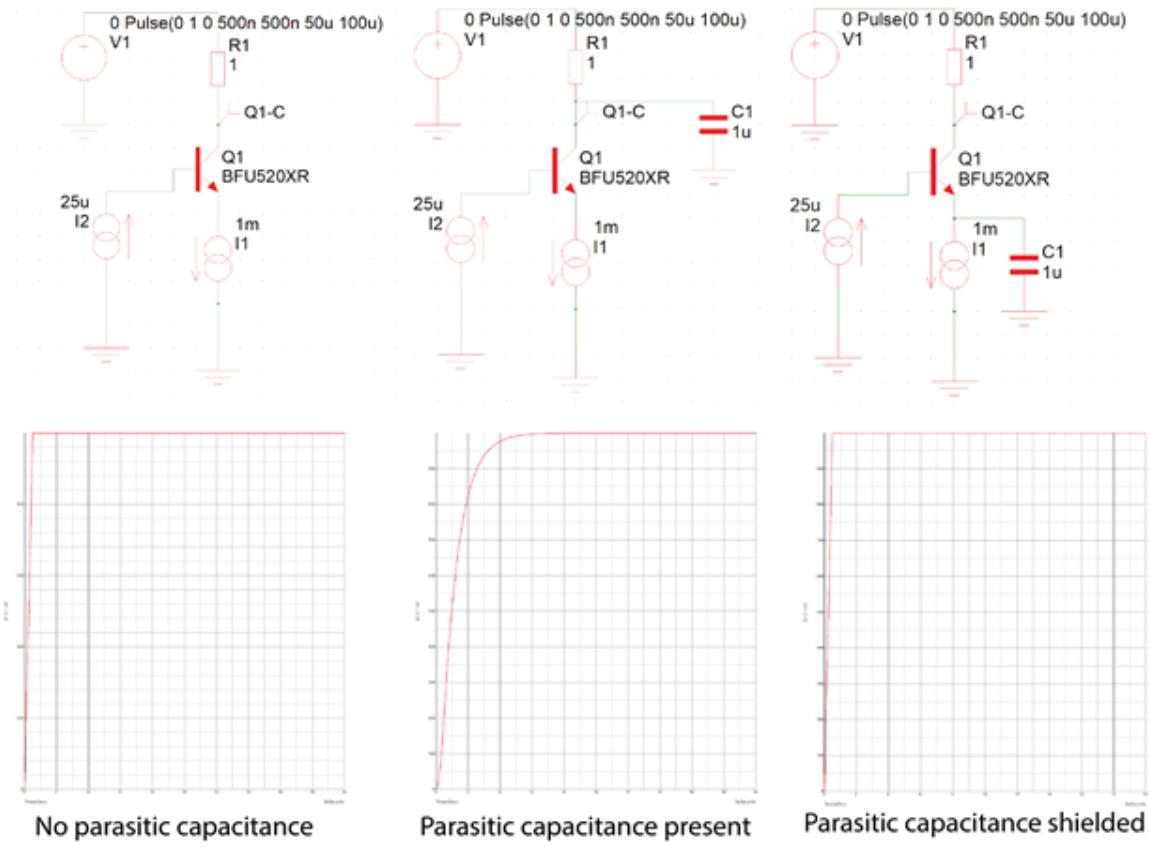
The SMS7621-092 has very good characteristics for the settling time circuit. It has very low parasitics: $C_p < 0.05 \text{ pF}$ and $L_s < 0.2 \text{ nH}$. The forward voltage of these diodes is also good for this application. This is because the goal of the circuit is to greatly amplify the very small settling signal near the end of the settling period. For this application we are not interested in any of the other parts of the settling signal because we want to determine at what time the signal settles to a given error band that corresponds to a certain bit resolution.

8.5.1.3 Common Base Transistors

In the Settling Time Circuit two transistors are used in a common base configuration to shield the fast settling node from the output capacitance of the DACs. The transistors chosen for this function should have low output capacitance and parasitics in order to maintain the integrity of the settling node. The transistors that were chosen for this function are the BFT92W and the BFU520XR. A simple simulation showing the effectiveness of the transistors at shielding the settling node from the output capacitance of the DACs is shown in [8.27](#).

In [8.27](#) the leftmost panel shows a single BFU520XR transistor with no added capacitance. The BFU520XR is biased on with the current sources and a fast pulse is injected at the collector. The transient response of the fast pulse is shown in the plot below the circuit schematic. The response for the leftmost panel is very sharp and accurately transmits the square wave across the fast node. The middle panel shows a

Figure 8.27: Frequency Response of the LMH5401.



large capacitance directly connected to the fast node. This large capacitance low pass filters the injected square wave. The rightmost panel shows the same capacitance now behind the BFU520XR. In the rightmost panel the output of the fast node is the same as the simulation with no parasitic capacitance. This is good because it shows that the common base made from the BFU520XR can properly shield the fast settling node from a parasitic capacitance that is much larger than what is expected.

8.5.1.4 Other Components

The other components chosen for the design were not critical for the circuit to work properly. The resistors were chosen to have a tolerance of 1% or better. They were also chosen to have a low change in value across temperature. Any 8-bit DAC

would work for this architecture. The connectors were chosen because they were edge launch and high bandwidth connectors.

8.5.2 SPICE Simulation

The SPICE simulation was performed in the Simetrix SPICE program. The full circuit simulated for this circuit is shown in the schematic in [8.28](#). This circuit includes a model for the LMH5401 provided by the manufacturer. A feedback network that creates a gain of 4 V/V has been created. A gain of 4 V/V gives the best bandwidth performance and also the best time domain performance. The parasitics of the clamping diodes are included in the simulation with C1 (50 fF) and L1 (200pH). The values are chosen by the maximum parasitic values reported in the data sheet for the SMS7621-092. The output of the LMH5401 is driving a 100 ohm differential load with an estimated 3pF of pad capacitance per output. The results of this simulation are shown in [8.29](#).

The plot shows three separate time series. The blue time series is the differential output (positive output minus negative output). The red and yellow time series are the positive and negative inputs into the LMH5401 to ensure that no reflections were occurring during the simulation. The results for the differential output show a 20 picosecond rise time of the whole system. This indicates that this circuit configuration will be able to properly transmit the output of the devices under test.

Figure 8.28: Frequency Response of the LMH5401.

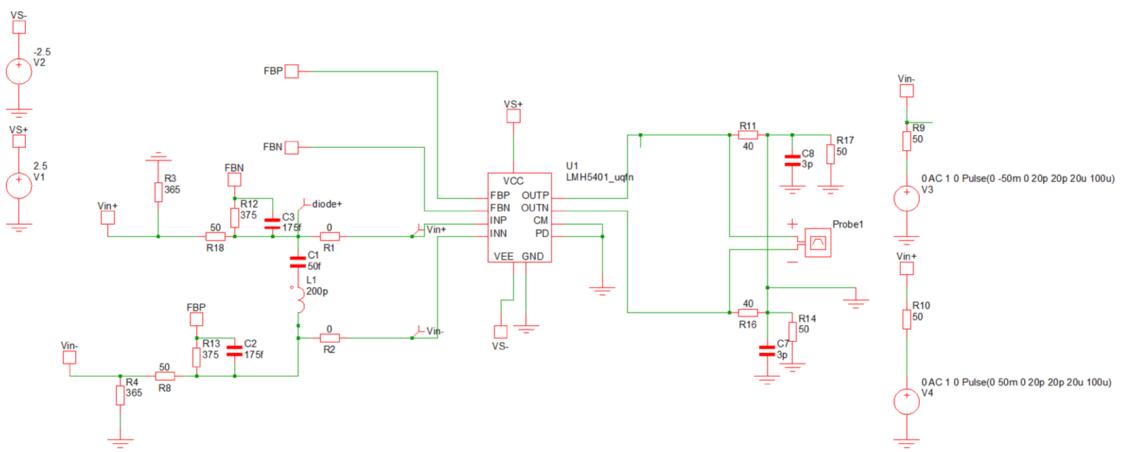
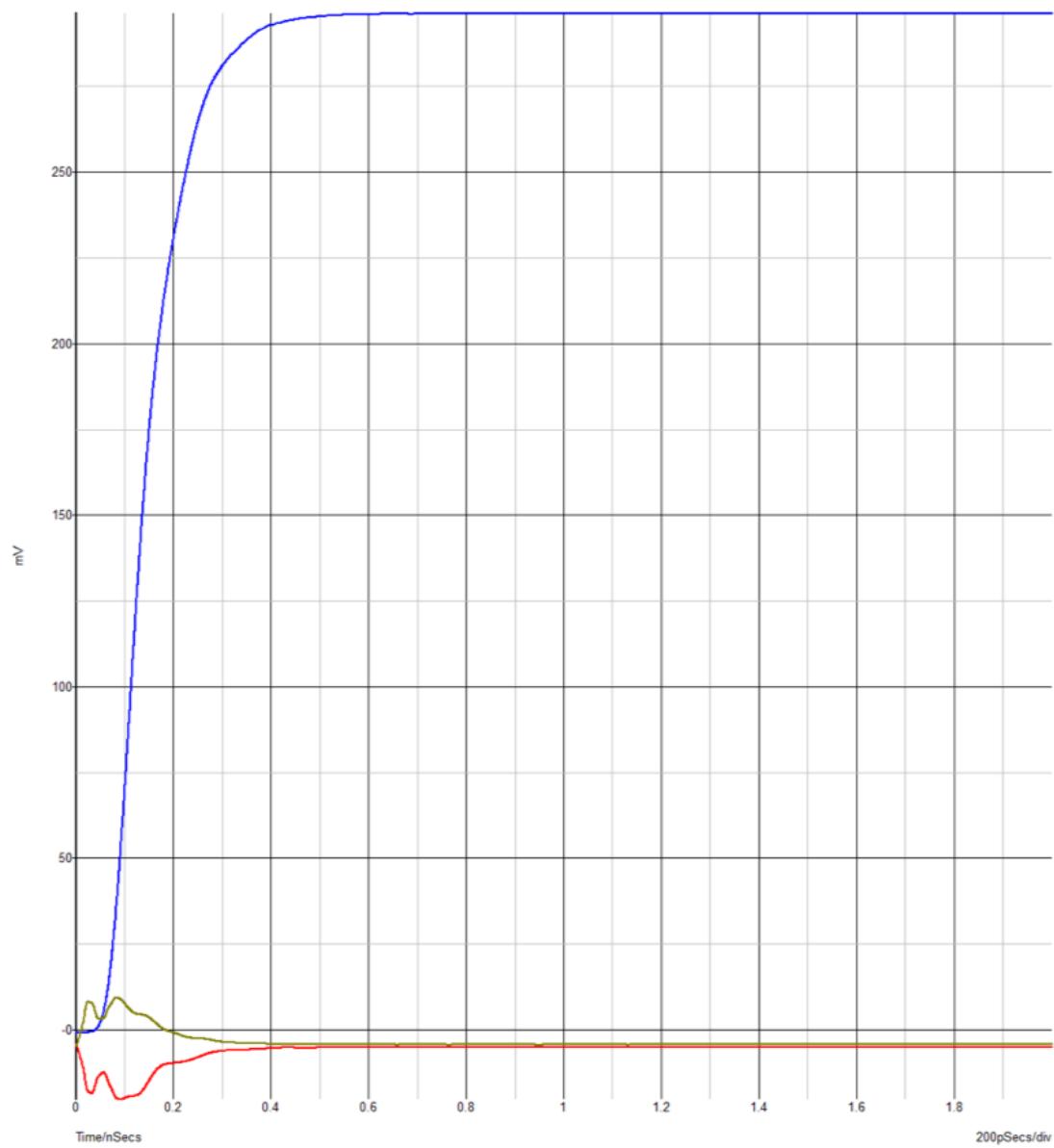


Figure 8.29: Frequency Response of the LMH5401.



Part II

ABUTTED IRLED HYBRID DEVELOPMENT

Chapter 9

AIREA OVERVIEW

9.1 Summary

Hardware-in-the-Loop (HITL) test and evaluation of advanced precision guided munitions requires the capability to stimulate sensors and seekers under test with synthetic IR imagery via real-time IR scene projection. An IRSP must be capable of displaying realistic scenes at required refresh rates with sufficient resolution, dynamic range, pixel response times, and accurate radiant intensity output to properly stimulate the unit under test (UUT). Advancements in IR seeker and sensor resolution, sensitivity, and field of view are exceeding IR scene projection capabilities. Analogous advancements in IRSP performance are needed for HITL testing of advanced IR sensors and seekers. The Advanced Infrared Emitter Array (AERIA) program has focused on creating and proving technology to make a viable path towards IRSPs with pixel resolutions larger than 2k x 2k.

Novel techniques are required to increase spatial resolution of advanced emitter arrays. Phase 1 focused on four main areas: fabrication of new SLEDs devices to accommodate the use of NMOS drive transistors in the RIIC, RIIC architecture development for an extensible RIIC design, post-processing of SLEDs Hybrids and accurate alignment of the hybrids, and thermal modeling of the new emitter array.

During phase 1 of this program, the University of Iowa successfully grew and demonstrated p side down contact SLEDs. These new devices allow the use of an NMOS drive transistor in the RIIC, which are physically smaller in size than PMOS drive transistors used in traditional SLEDs IRSPs. The smaller transistor size means pixels can be smaller and higher density yielding higher resolution emitter arrays. The

idea of abutting two or more SLEDs hybrids in very close proximity was also created during phase 1.

The abutment technique required the hybrids to be placed at a sub-pixel distance apart to keep the gap between the hybrids from being visible. This goal was non-trivial for several reasons. The first reason being the roughness of the edge of the hybrids had to be carefully controlled to ensure that the parts could be brought to a sub-pixel distance together. The abutment technique also required a method for the hybrids to be physically placed next to each other and for a new attachment method to the heat sink plate to be created.

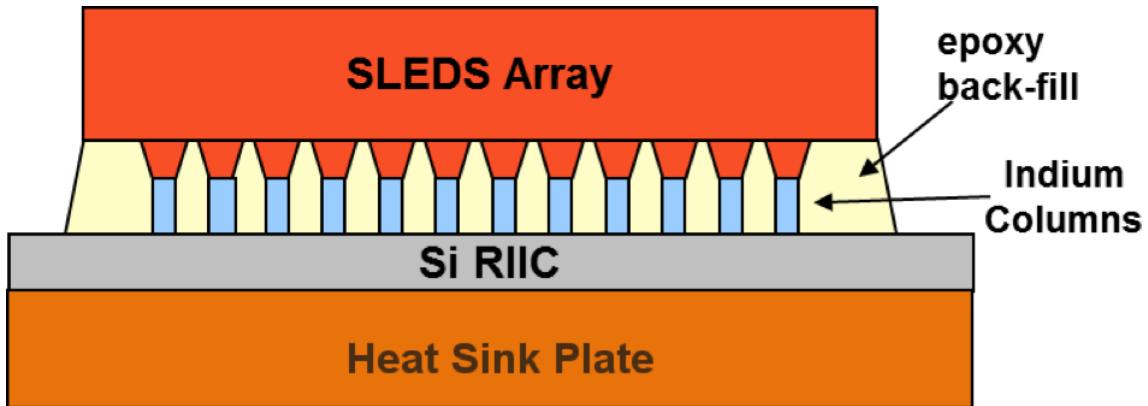
Beyond technical challenges phase 2 of AERIA required a high level of coordination between the University of Iowa, Teledyne Scientific Imaging, and Chip Design Systems to ensure that every piece would fit together and that the goals of the AERIA Phase 2 program would be accomplished.

During the course of phase 2 of the AERIA program these goals were accomplished. While, the original plan outlined in the phase 2 proposal was modified as new unseen challenges emerged during the course of the program the goal of creating technology and a process flow for making IRLED hybrids with a resolution greater than 2K x 2K was maintained.

9.2 Introduction

Hardware-in-the-Loop (HITL) test and evaluation of advanced precision guided munitions requires the capability to stimulate sensors and seekers under test with synthetic IR imagery via real-time IR scene projection. An IRSP must be capable of displaying realistic scenes at required refresh rates with sufficient resolution, dynamic range, pixel response times, and accurate radiant intensity output to properly stimulate the unit under test (UUT). Advancements in IR seeker and sensor resolution, sensitivity, and field of view are exceeding IR scene projection capabilities. Analogous advancements in IRSP performance are needed for HITL testing of advanced IR sensors and seekers. The Advanced Infrared Emitter Array (AERIA) program has focused

Figure 9.1: Cross Section View of an IRLED Hybrid.



on creating and proving technology to make a viable path towards IRSPs with pixel resolutions larger than 2k x 2k.

There are significant difficulties with fabricating an IRLED IRSP Hybrid with a resolution of 4 Megapixels or greater at a 24 micron pixel pitch because of the physical size of the components required. An introduction to the different components of an IRLED hybrid will be helpful to understand and appreciate the difficulties involved in the fabrication of large IRLED hybrids. Figure 9.1 below shows a cross-sectional view of an IRLED hybrid.

9.2.1 IRLED Hybrid Overview

From the top down in Figure 9.1 there is the SLEDs Array. The SLEDs are the IRLED emitters and are responsible for producing the infrared emission required for reproducing the imagery on the array. Below the SLEDs array are the indium columns or bumps. These are 8 - 10 micron tall deposits of indium that are deposited by Teledyne Scientific Imaging through a photolithography process. They are responsible for making electrical connection between the emitters (SLEDs array) and the CMOS circuitry that provides the logic and power required to light up the SLEDs in the appropriate manner. Below the indium bumps is the Silicon Read-In-Integrated-Circuit (RIIC). A RIIC is a CMOS circuit array that is organized as a two-dimensional

array of pixels. Each pixel integrates one or more current drive transistors that are responsible for providing the current the IRLED requires to generate photons, and the logic circuitry to facilitate addressing individual pixels. The final component is the heat sink plate. Currently, this heat sink plate is made out of copper tungsten (CuW). The heat sink plate prevents the hybrid from forming cracks when being cooled down to cryogenic temperatures by forcing the Silicon to contract at the same rate as the Gallium Antimonide. The heat sink plate also provides a physical platform for the hybrid, so that it can be mated to a cold finger in a dewar.

9.2.2 Problems Associated with IRLED Production Beyond 4 Megapixels

As stated previously there are significant difficulties with producing an IRLED hybrid with a resolution beyond 4 Megapixels at a 24 micron pixel pitch. Following the same order of components as in the IRLED Hybrid Overview section this section will elucidate the different difficulties.

The SLEDs component has a very fundamental limitation in that GaSb wafers with a diameter greater than four inches are not commercially available and have only recently been successfully produced [2]. This can be seen in the brochure from the company Wafer Technology[31], a commercial producer of GaSb wafers. Wafer Technology lists the largest size wafer available for sale as having a four inch diameter. The largest monolithic SLEDs hybrid produced to date is the HD-ILEDs hybrid[5]. This hybrid is a 4-Megapixel hybrid at a 24 inch pixel pitch. Due to the size of the HD-ILEDs hybrid only one SLEDs emitter array was able to be grown on a four-inch wafer. Four inch GaSb wafer technology only recently became available[2] and it is unlikely that larger wafers will be commercially available soon. Furthermore, the molecular-beam-epitaxy machines at the University of Iowa are designed to accept a four inch or smaller wafer. In order, to go beyond the four megapixel limitation on the SLEDs emitter array size a method for joining two or more SLEDs emitter arrays together must be developed.

The traditional RIIC design will not work indefinitely for larger sized RIICs because as IRSP Systems are scaled beyond 2 megapixels, the manufacturing of fully functional CMOS RIIC chips to drive such large IR emitter arrays becomes uneconomical. Table 1 below highlights the yield and production cost of all of the IRLED IRSPs that CDS has been involved with. A good example of the cost increase due to yield issues is exemplified by the difference in RIIC cost between the NSLEDs and the HD-ILEDs programs.

At a 2048 x 2048 array size and a 24-micron pixel pitch the HD-ILEDs RIIC is 5.69 cm x 5.69 cm. Four of these RIICs can be placed onto an eight-inch silicon wafer. The measured yield for the HD-ILEDs RIICs is 8%. This yields a cost of \$30,000 per RIIC. Comparatively, the NSLEDs program has a 1024 x 1024 array size with a 24-micron pixel pitch, and physical size of 3.32 cm x 3.32 cm. The NSLEDs yield of 55% is significantly better than the HD-ILEDs yield of 8%. The improved yield also has a significant impact on the cost per RIIC with a \$900 cost per RIIC for NSLEDs. It is useful to plot the yield percentage versus die area for the RIICs to see the exponential like relationship between these two parameters. In Figure 9.2 this plot is done. Looking at Figure 9.2 and the standard CMOS yield plot shown in Figure 9.3 the similarity between the two plots is very recognizable.

Figure 9.2: A plot of the RIIC yield percentage vs. the RIIC die area.

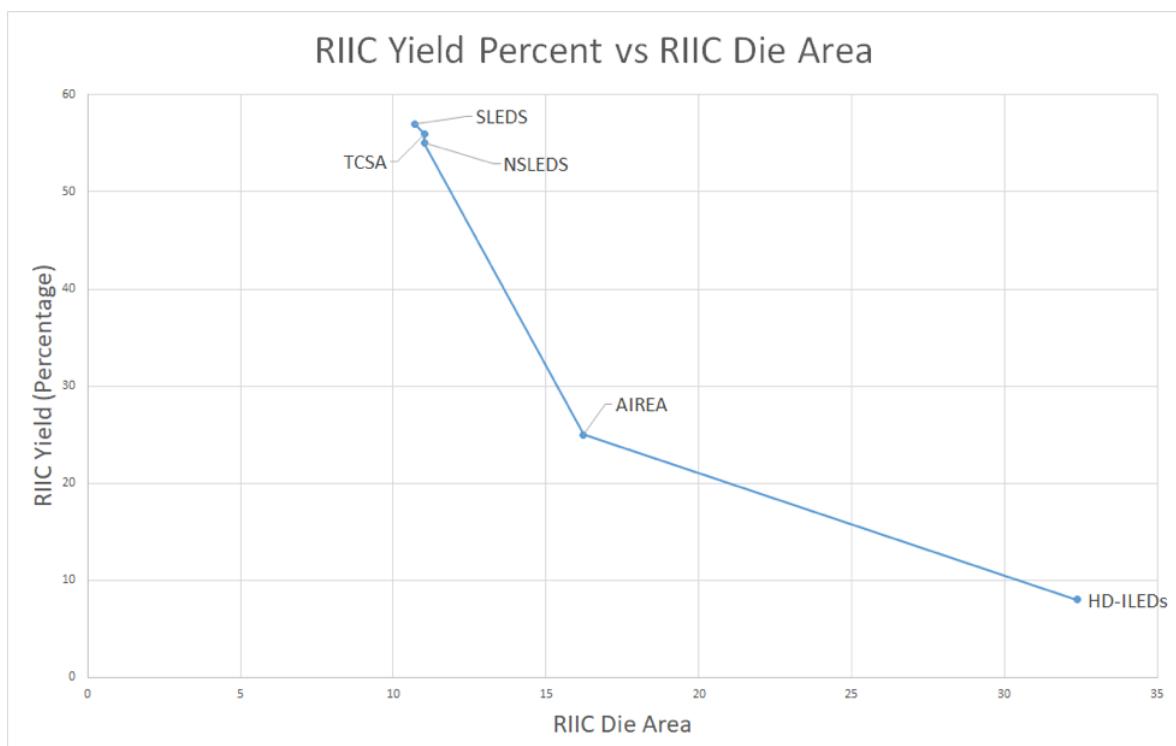


Figure 9.3: Wafer yield vs. die size for D=0.002..

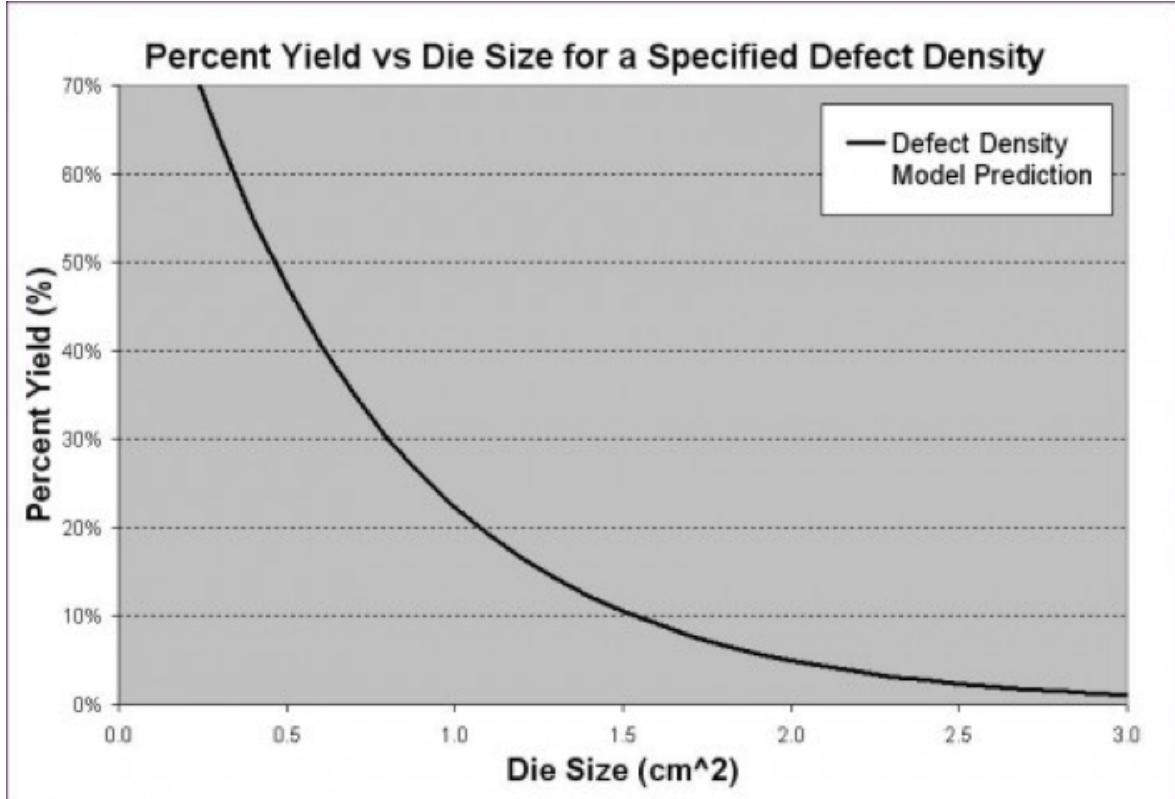


Table 9.1: Overview of the IRLED IRSPP program and the associated cost per wafer of the RIIC component (excludes fixed NRE cost of making masks etc inherent in CMOS production. This cost can be between \$10K and \$120K).

	SLEDS	TCSA	NSLEDS	AIREA	HDILED
Resolution	512 × 512	512 × 512	1024 × 1024	1024 × 2048	2048 × 2048
Emitters / Pixels	1	2 (two-color)	1	1	1
Pixel Pitch (Microns)	48	48	24	24	24
Die Size (cm)	0.27 × 3.27	3.32 × 3.32	3.32 × 3.32	2.85 × 5.69	5.69 × 5.69
Die / Wafers	19	19	19	8	4
Transistors / Super-Pixel	7	36	60	60	60
Transistors (M)	2	10	15	30	60
Measured Yield	57%	56%	55%	25%	8%
Cost / RIIC*	\$900	\$900	\$900	\$5K	\$30,000

Using several smaller hybrids and combining them together has the advantage of being able to choose the best parts and combine those together. Smaller RIICs and SLEDs arrays have been consistently shown to have better performance over the larger varieties. This is due to a smaller sized RIIC or SLEDs array accumulating less processing errors. Smaller RIICs and SLEDs arrays are also more economical.

The fabrication of IRSPPs beyond 2K x 2K resolution with 24-micron pixel pitch cannot be accomplished without a method for joining several SLED hybrids together

to form a larger hybrid. This is due to limitations in the growth and fabrication of the SLEDs, the CMOS RIIC fabrication, and the infeasibility of producing a hybrid of that physical size. This goal of joining SLED hybrids together is what the AIREA Phase 2 program has sought to solve.

9.2.3 AIREA Goals

The goals for phase 2 of the AERIA program were to:

1. Develop an abutment process for 24 and 48-micron pitch emitter arrays.
2. Develop technology for packaging abutted emitter arrays.
3. Maintain compatible interfaces to existing CSE hardware for low-cost and low-risk path to future system insertion.
4. Fabricate a 1Kx2K IRLED emitter array using two (2) abutted 1Kx1K Super-Lattice Light Emitting Diode (SLED) hybrids with 24-micron pixel pitch.

Note that these goals were amended during the course of the phase 2 program to increase the delivered resolution of the SLEDs hybrid to be a 2k x 2k hybrid. This was possible due to the ability to cost share the Read-In-Integrated-Circuit (RIIC) CMOS wafer fabrication with the HD-ILEDs program. It was decided to cost share with HD-ILEDs program because of the delayed start date of the AIREA program. Initially, it was planned that AIREA would cost share with the NSLEDs CMOS wafer fabrication, which is a 1K x 1K array. Abutting two NSLEDs would yield the 1K x 2K array referenced in the original goals of the phase 2 program. The delayed start date for the AERIA program was fortuitous because it was possible to deliver an array with twice the resolution for no additional cost to the government.

In Phase 2, the AERIA program focused on solving two main issues: the design and fabrication of an abutable edge, and the ability to place IRLED hybrids close together.

9.2.4 Methods, Assumptions, and Procedures

Fabrication of the IRLED devices in this project was performed in the state-of-the-art optoelectronic device fabrication and characterization laboratory at the University of Iowa, founded by Professor Thomas Boggess. In addition to MBE growth using either of two independent MBE systems (VEECO GEN20 and VEECO EPI 930), the University of Iowa has a complete microfabrication laboratory in which LEDs and LED arrays have been successfully processed with pixel size as small as 24um. The microfabrication laboratory is equipped to do a wide variety of processing, fabrication, and materials/device characterization. A class 100 clean room contains equipment for optical lithography with an OAI model 800 mask aligner, which has frontside and backside IR and optical capabilities. It also contains 2 spin coaters, programmable hot plates and a wet bench for processing. Other wet processing is performed in a dedicated acid bench with wash down capabilities under downdraft HEPA filtered Air. A separate plating and chemical area exists for other processes. Metallizations may be carried out using a 6-pocket electron beam evaporator and 2 thermal evaporators. Dielectrics can be deposited in the laboratory by our or thermal evaporation as well as E beam evaporation. An Intlvac reactive sputtering machine and an Oxford OPAL Plasma Atomic Layer Deposition (ALD) system are also available. Surface preparations and material removal are accomplished by using a Oxford NGP 80 Reactive Ion Etcher (RIE) as well as a Branson Plasma Cleaner. The laboratory is equipped with a rapid thermal annealer, high temperature and vacuum ovens, as well as a multi zone tube furnace for a wide variety of processing steps. A chlorine-based, inductively-coupled plasma (ICP) etcher will soon be available in the laboratories for deep etching of the antimonide materials. While we routinely wet chemical etch LEDs, the ICP will offer much greater versatility, accuracy, and reproducibility of etch.

Characterization of the IRLED devices in this project was carried out at the UIowa laboratory using Zeiss Nomarski and Leitz bright field dark field semiconductor microscopes. A Wollam spectroscopic ellipsometer was used for film characterizations as well as a Dektak 3030 stylus profilometer and a Wyko NT1100 white light optical

profiler. A complete set of electrical characterizations can be performed in the laboratory. Two probe stations with long working distance objectives can be interfaced to semiconductor parameter analyzers, RF and microwave characterization equipment (up to 18GHZ), and curve tracers. We also have a pace hybrid rework station for small scale chip placement. Additional equipment for wire bonding, UV processing, and film thickness characterization, lapping, diamond sawing, and semiconductor dicing are available in laboratory and were used in the performance of this project.

Testing of the RIIC design was conducted at the University of Delaware in the Testing and Evaluation laboratory founded by Professor Kiamilev. This laboratory has state of the art test and measurement capabilities for measuring circuit operation. Characterization of the RIICs operation was carried out with Keithley 2400s that were used for precise power sourcing and measurement of current draw to different part of the circuits. Timing characteristics and correct output verifications were done with an MSO 4034B mixed signal oscilloscope. All measurements were made with substantial static electricity protections to ensure accurate measurements.

Chapter 10

AIREA RESULTS AND DISCUSSIONS

10.1 IRLED Work

10.1.1 AIREA SLED Pixel Design

Initially, the SLEDs pixel design depicted in the left panel of Figure 10.1 below was going to be the design used for AIREA. This design had a number of unique features. The first being a new novel super-pixel design in which four LEDs shared a common anode. These LEDs were square, with gold straps running from the tops of the LEDs to a shared center. The design allowed for a greater fill factor than the octagonal mesas (56% vs 46%), which increases the light output. However, this design incorporates two additional steps: a deposition of the dielectric, and the etching windows into that dielectric. Increasing the number of process steps can reduce the yield. Another concern was over the size of the bond pads: this design incorporated bond pads that were 8m and 4m on a side, which are much smaller than the 10m indium bumps TSI has used in the past. Teledyne expressed concerns over the size of the indium bumps becoming so small, as well as the spacing between the bumps decreasing to roughly 8m instead of the 17m used in previous 24m-pitch arrays (NSLEDs). John Lawler also expressed concerns that the heat transfer would be reduced because of the presence of the dielectric, and would be restricted by the small bond pads. Because of these concerns, we elected to redesign the pixel (Fig. 10.1 right). This new pixel design addressed the concerns with the new novel pixel design and had the added benefit of closer to the successfully tested NSLEDs pixel.

The new design features a central pillar (formed by reactive ion etching, rather than metal build up) for the common anode contact, surrounded by four emitters, each

Figure 10.1: Left side shows current AIREA/HDILED superpixel design. Right side shows proposed AIREA/HDILED superpixel design. A superpixel is a 48-micron square and integrated four 24-micron square pixels. The current design has 8 indium bumps and the proposed design.

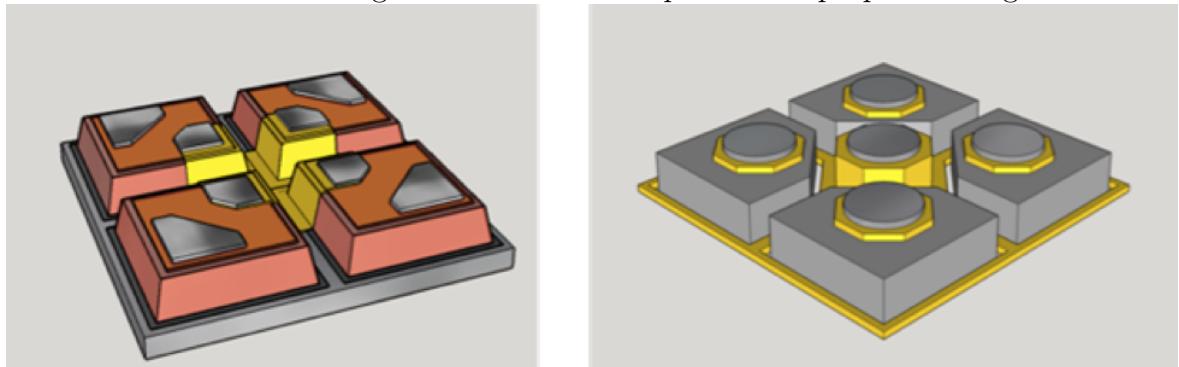


Figure 10.2: Identification of common single anode contact and four cathode contacts for each super-pixel.

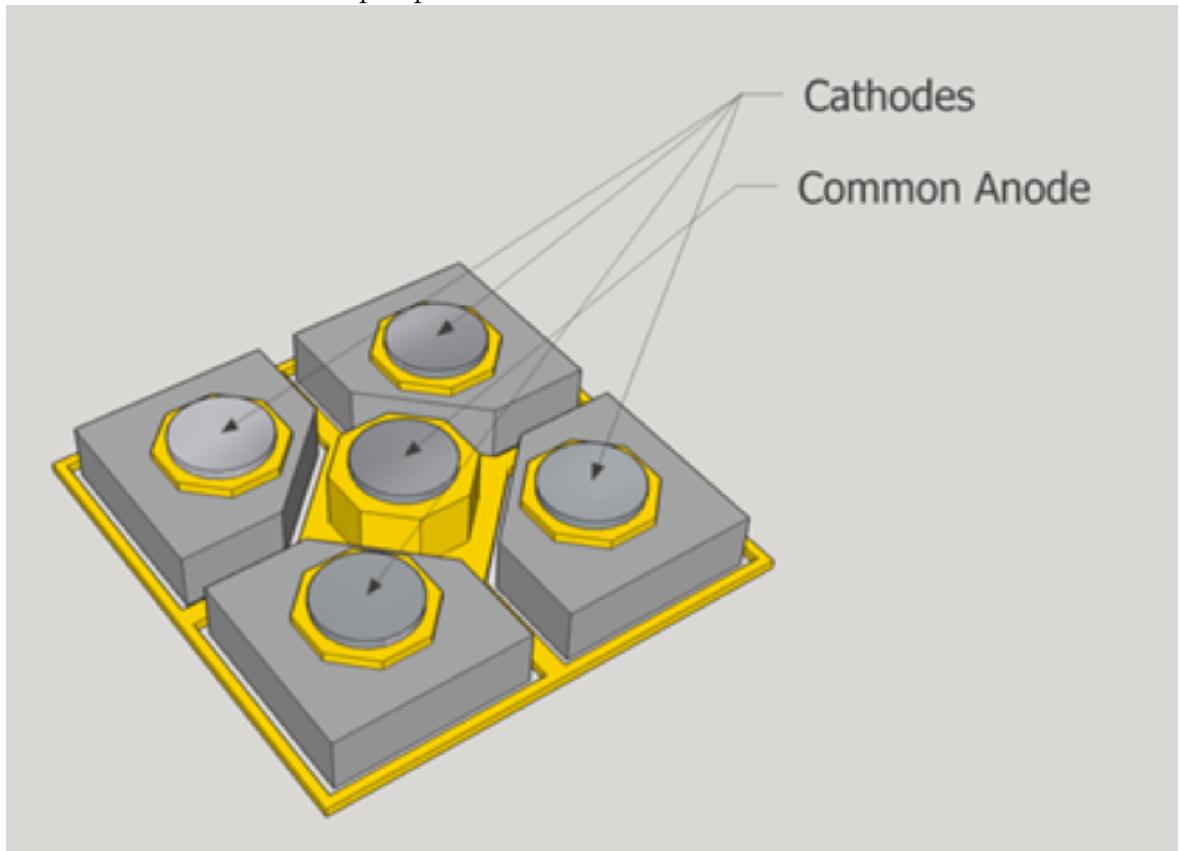
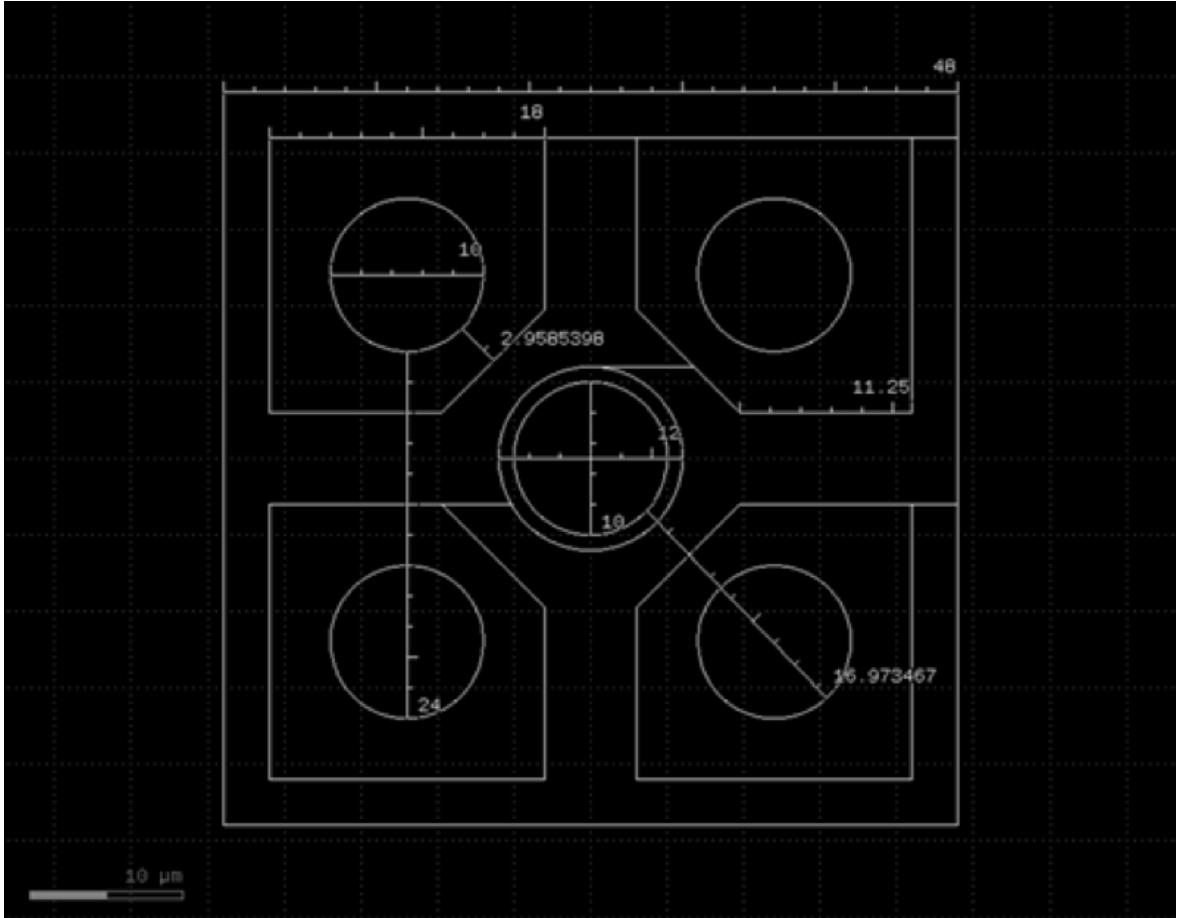


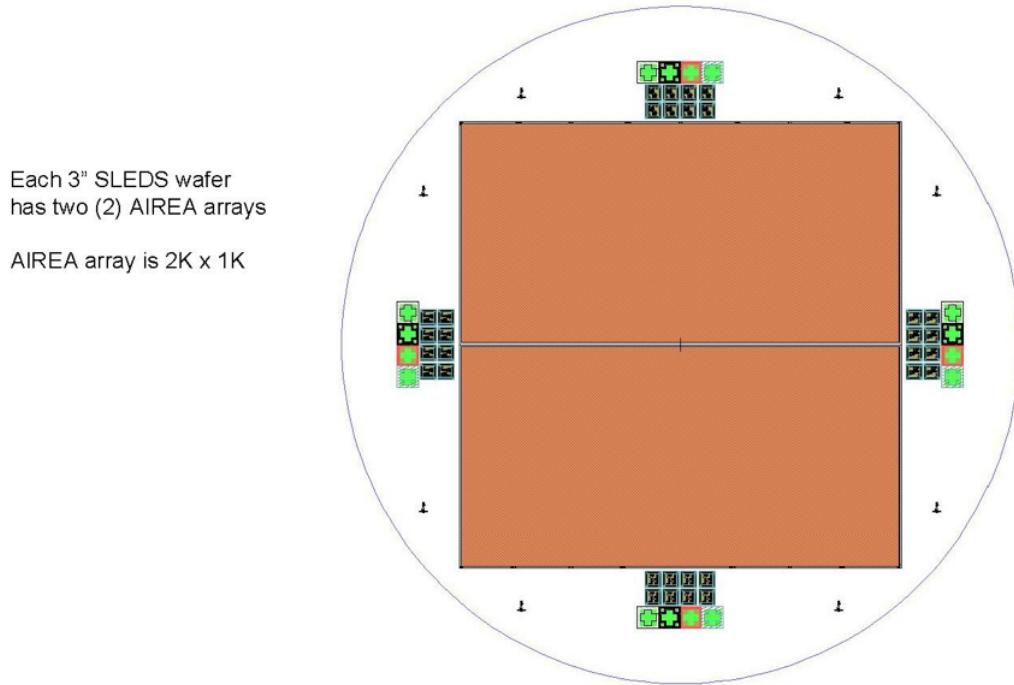
Figure 10.3: Plan view of the super-pixel with critical dimensions indicated.



with a cathode contact (see Fig. 10.2). This is similar to the old NSLEDs and SLEDs designs, but it now incorporates the super-pixel. The bond pads are again 10μm wide and 17μm apart, but now have a truncated square shape rather than an octagonal shape. The large bond pads help with thermal transfer, and increases indium bump process yield from TSI. This design also requires fewer processing steps due to it lacking a dielectric layer. The truncated square's fill factor is reduced to 52% from the square's 56%, but is still larger than the octagonal's fill factor of 46%. The width of the long edge was increased by 1μm on either side because there was no longer a need to etch a trench in the dielectric. This increased the fill factor to 59%. A plan-view of the super-pixel, with critical dimensions indicated, is shown in Fig. 10.3.

Figure 10.4: AIREA SLEDS Wafer Map.

SLEDS Wafer Map

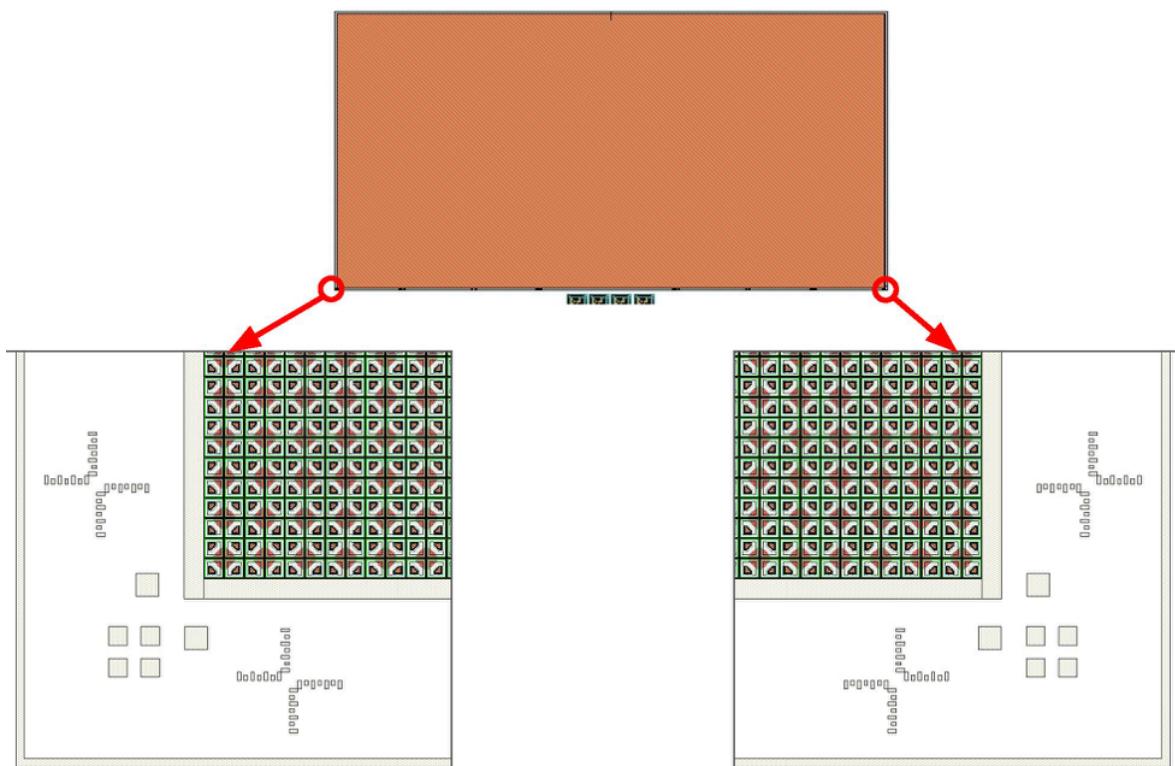


10.1.2 AIREA SLEDS Wafer Overview

In Figure 10.4, the AIREA SLEDS wafer mask is depicted. There are two $2k \times 1k$ arrays on the 3 GaSb wafer. Around the outside of the square formed by the SLEDs arrays there are some test devices for evaluating the quality of the SLEDs growth and alignment marks required for the hybridization process. In the center of the wafer there is 428 um gap between the two SLEDs arrays. This gap was made to accommodate the trench etch used to create a vertical sidewall appropriate for the abutment procedure. This trench etch is discussed in more detail later on.

Figure 10.5: Hybridization Alignment Marks.

Indium alignment marks on SLEDS Array



10.1.3 AIREA SLEDs Wafer Growth

The growth recipe for AIREA was directly based on a sample grown in April of 2016 that was calibrated for 3.8um emission, exhibited little to no strain, and yielded high-performance working devices. The process of growing sample devices until the recipe is optimized ensures that the deliverable wafer will have little to no defects. High-resolution X-ray diffraction measurements were used to evaluate the quality of the growth. The X-ray diffraction measurements indicated that the superlattice emitter region and the quaternary layers that are a part of the tunnel junctions, are both highly lattice matched to the GaSb substrate (see Fig. 10.6). This is an indication of a high-quality MBE-grown device and that the device level process was optimized properly. On the wafer level, it was noticed early on that the AIREA wafers had some blemishes near the edge of the wafer that appears to have been group-V flux deficient during Reflection High-Energy Electron Diffraction (RHEED) intensity oscillations (see Fig. 10.7). RHEED intensity oscillations are our primary tool to calibrate material growth rates, which is necessary to meet wavelength and strain requirements. While the blemish was less than ideal, it was localized to one small area on the wafers edge. The localization occurs because the substrate is continually rotating throughout the growth, except for during RHEED intensity oscillations.

The defects were determined to be an arsenic deficiency during the InAs RHEED check. Since the molecular beams do not hit the substrate at normal incidence, there was a flux gradient over the wafer. Normally, III-V semiconductors are grown III flux limited, meaning there is an excess of V flux on the surface at all times. However due to this flux gradient, the defect region became slightly V flux deficient, which caused these defects to form. To correct for this, the arsenic flux was increased 25%. While the gradient still exists, this keeps the entire wafer III flux limited, thus the defects did not form. These gradients are not an issue outside of RHEED checks, since the rotation of the substrate causes the flux gradient to average out. The AIREA wafers were then regrown and the deliverable wafers did not exhibit any blemishes once this part of the process was optimized.

Figure 10.6: A high resolution X-ray diffraction scan off the deliverable structure, showing good alignment of the zeroth order super-lattice peak and quaternary layers to the substrate peak.

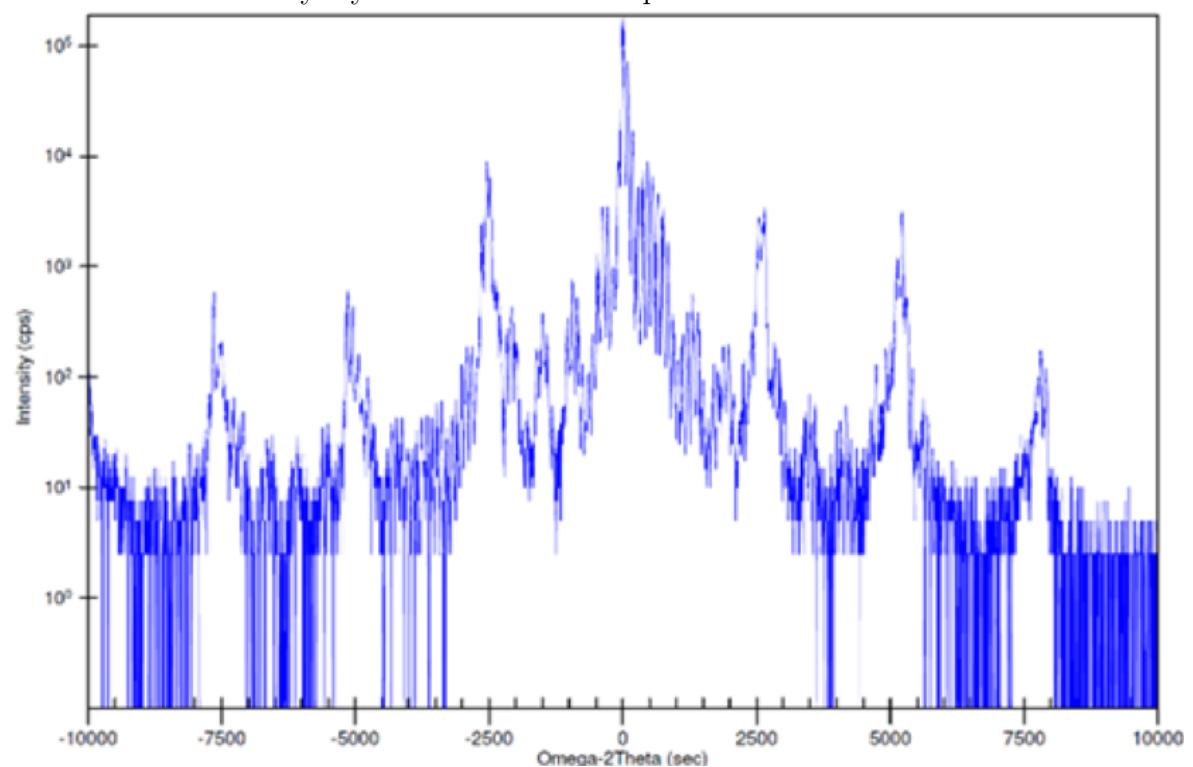
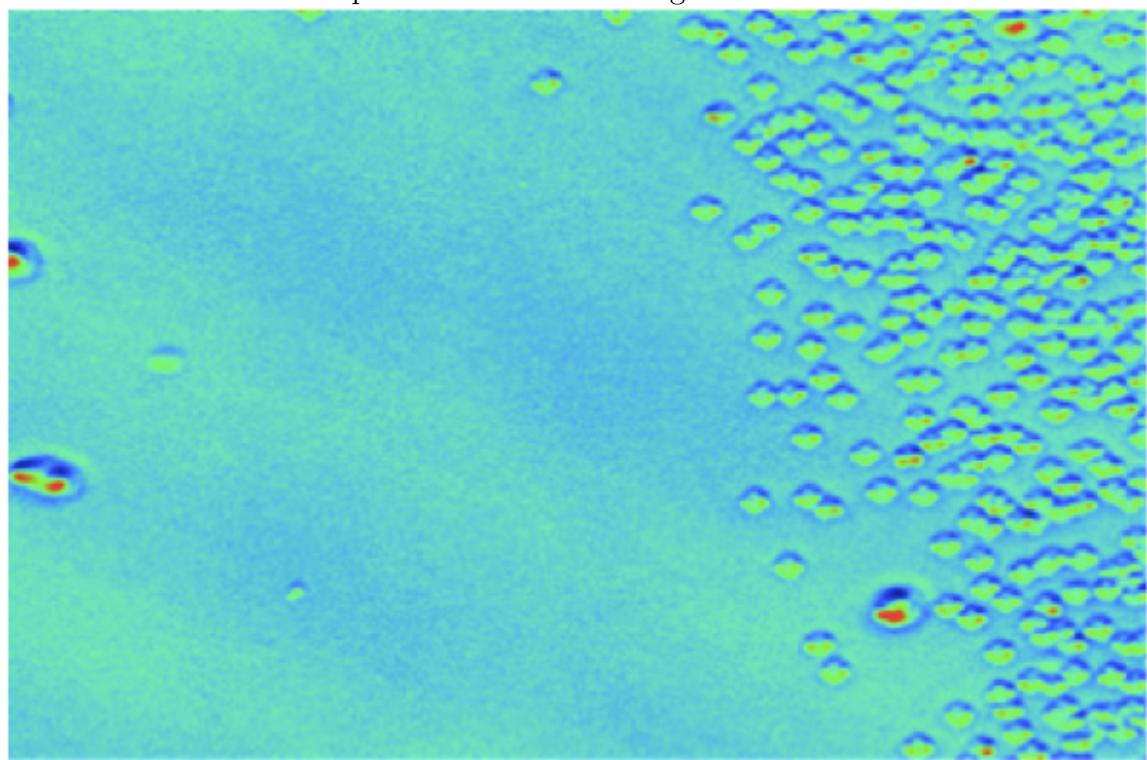


Figure 10.7: A 20x optical profilometry image of the boundary between a V-flux deficient (right side) and V-flux supported (left side) region. The sharpness of the boundary and its localization to a corner of the wafer lends itself to the interpretation of V-flux design.



10.1.4 AIREA SLEDs Wafer Fabrication

At the end of the growth phase of the SLEDs emitter array production process there is one large SLED grown on the wafer. The fabrication phase of the SLEDs wafer production involves using a photolithography mask to pattern the SLED material into small pixels. It also involves depositing metal connections to route electrical power to the SLED pixels. Figure 10.8 shows an exploded view of the gold deposition processing that occurs for each pixel. In Figure 10.8 it is possible to see that the AIREA super-pixel consists of four active LEDs and a central pillar. The central pillar and active LEDs are all etched from the super-lattice growth. The central pillar is then coated with gold to create a short to the bottom (common anode) of the four active LEDs. Gold octagons are placed on top of the LEDs for cathode contacts. The five indium bumps are deposited on top of the gold octagons and the central pillar.

To prepare for the fabrication of the AIREA SLEDs wafers test arrays were fabricated first. The test arrays helped to optimize and ensure the fabrication of the deliverable AIREA SLEDs wafers would not encounter any issues during fabrication. During the testing phase it was discovered that it was more advantageous to use a pulsed method for the etch recipe. This conclusion was arrived at by first noticing the test pieces demonstrated an extreme roughening in the inductively-coupled plasma etch (see Figure 10.9). After investigating the mask material, wafer crystal quality, and sample size in the ICP chamber, it was determined that the wafer was overheating during the ICP etch. The wafer mask material was also investigated because it was obvious that the etch mask was becoming rougher along with the wafer, as can be seen on top of the mesas on IAG577 (Fig. 10.9). Because methane is used as an etchant, polymer layers could have been forming on the surface. However, when a chemically similar, but with a higher temperature stability, mask material was used, no signs of degradation appeared. Furthermore, it appeared that the longer a single etch run required, the worse the problem became.

The roughness was also much more pronounced on larger test pieces ($\approx 1"$ on each side). This may have been caused by reactant depletion in the chamber, but again the

Figure 10.8: Exploded view of gold electrical connections.

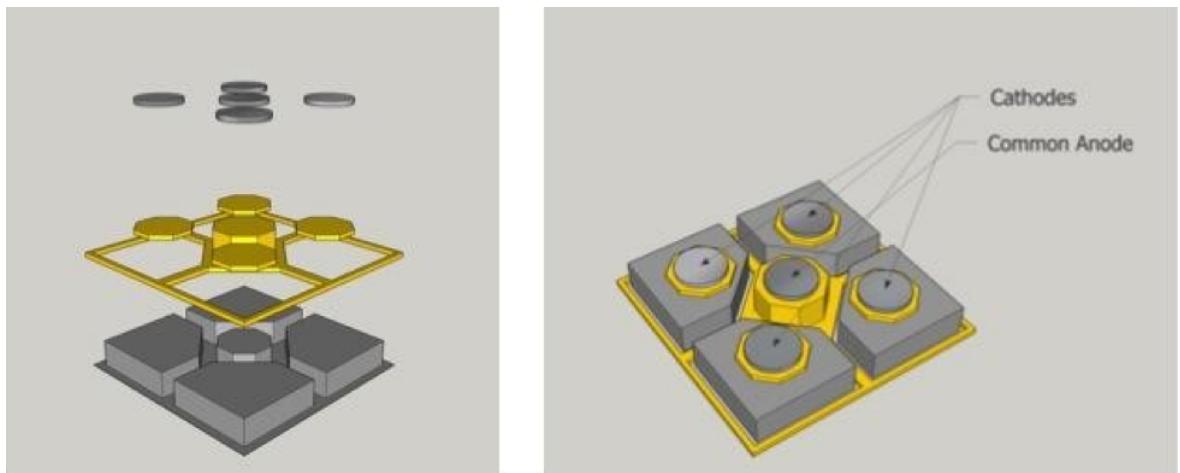


Figure 10.9: IAG577 etch mask after etching. Etching caused roughening of the mask.

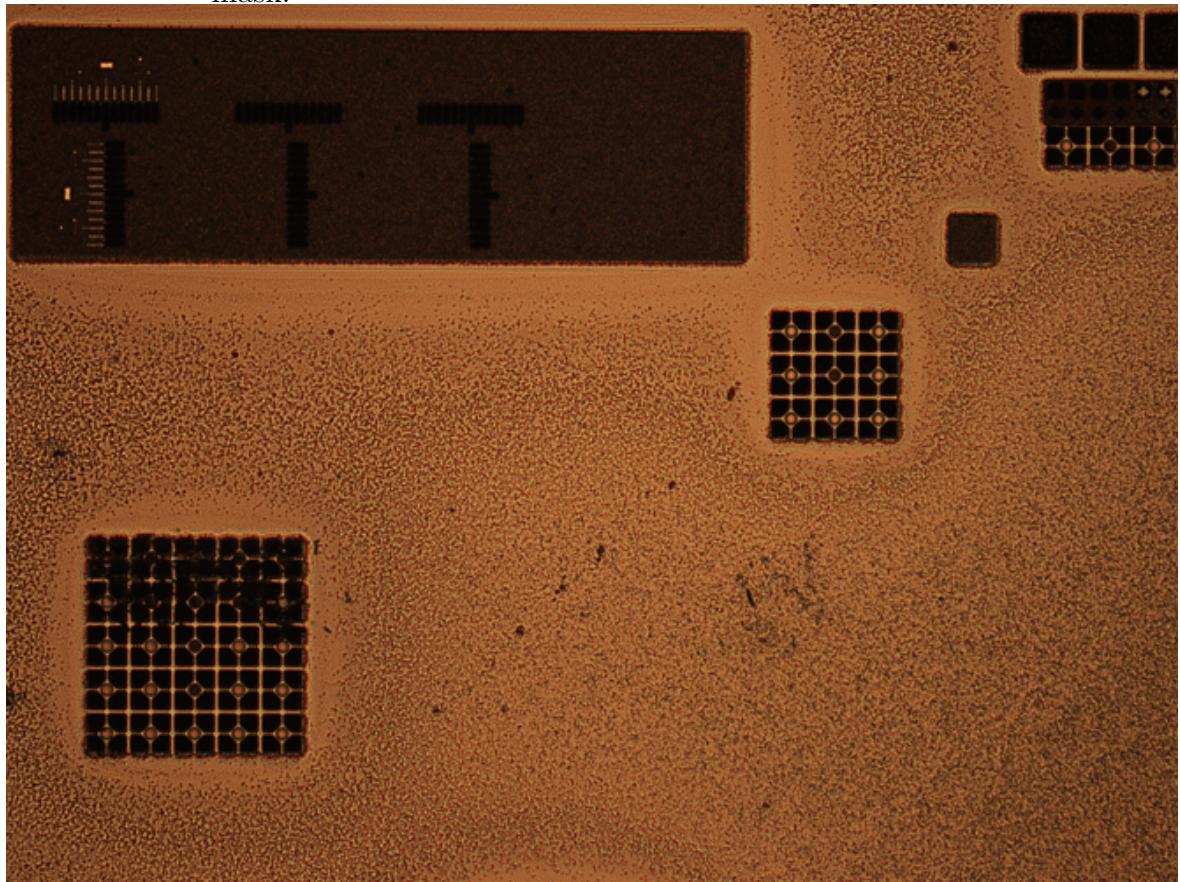
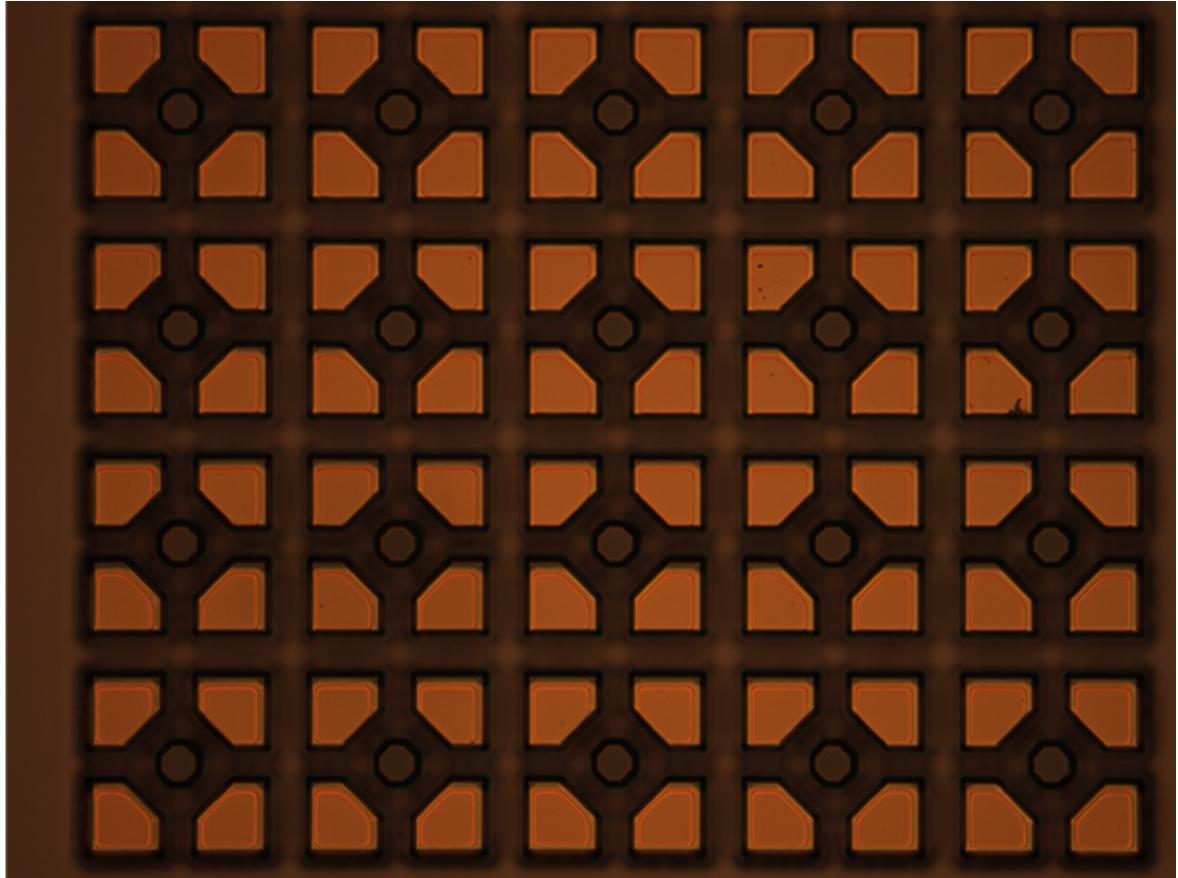


Figure 10.10: Etch mask on TSI1648 after etching no roughening occurred when the etched was pulsed at a low duty cycle to prevent heating.



roughness only appeared after 10 minutes of continuous etching on the large pieces. Thus, it was determined that the wafer heating was causing this issue. The rise in temperature caused chemical desorption that ruined the super-lattices, and degraded the mask. A simple fix was implemented that pulses the etch recipe, allowing the wafer to cool and maintain a stable temperature during the etch. Etch tests done on a large piece (2" x 1") were shown to be clear of the roughening (see Figure 10.10).

Once this issue was resolved the fabrication of the first deliverable wafer, IAG581, went smoothly and the fabrication of the second wafer, IAG616, began. The fabrication on IAG581 went quite well overall. The first metallization, which puts down metal on the tops of the mesas went excellently as seen in the photographs below (Fig. 10.11).

The ICP RIE process was also sound with an etch recipe of CH₄/Cl₂/Ar, RIE power at 100W, and ICP at 1200W. The etch depth was measured at 36 equally spaced points across the array and also at the four test arrays around the edge of the wafer. The etch depths ranged from 3.61um – 3.87um, with a depth of 3.74um being the most commonplace indicating that the etch reached between 100-300nm into the buffer and made it through the superlattice across the entire wafer (Fig. ??). Finally, the last metallization, which placed gold in the channels between the mesas, was satisfactory. A majority of the wafer had a great development while the development in the center of the array was acceptable (Fig. ?? and Fig 10.13.). There are some corners in the center, which didnt develop as fully, so the metal there didnt completely attach to the wafer. This was deemed not to be an issue based on past experience processing other SLEDs wafers. Figure 10.14 is a picture of an alignment mark near the edge of the wafer, fully processed.

The fabrication of the AIREA SLEDs wafer devices presented several issues, including wafer heating during ICP etching and surface degradation during resist removal. These fabrication issues were solved as described previously and a deliverable array was fabricated (Fig. 10.15). The array holds two 1kx2k patterns with alignment marks and test devices around the edges of the arrays. An edge was diced off of the array for quality assurance testing. The 16-stage device was the brightest that has ever been fabricated. It achieved apparent temperatures of 1700K over the 3-5m band with a 50% fill factor (Fig. 10.16). This was operated at 77K with 1kHz quasi-DC pulses, which are the same conditions under which the arrays will be operated. This was the first 16-stage device tested for the common anode series, and is a sample from a deliverable wafer. The devices, in comparison to a 4-stage sample, are three times as bright, but require voltages about four times greater.

In addition, to the main deliverable wafer, IAG581, a backup SLEDs wafer for AERIA was also fabricated in case something should happen to IAG581. IAG616 is the back-up to IAG581. Pictures of the resulting etch as well as pictures of the top metal contacts deposited in July 2016 for IAG616 are shown below (Fig. 10.17 Sub

Figure 10.11: Deliverable IAG581, after the RIE ICP etch. This creates the topography of the wafer, forming the four mesas surrounding the common cathode in between.

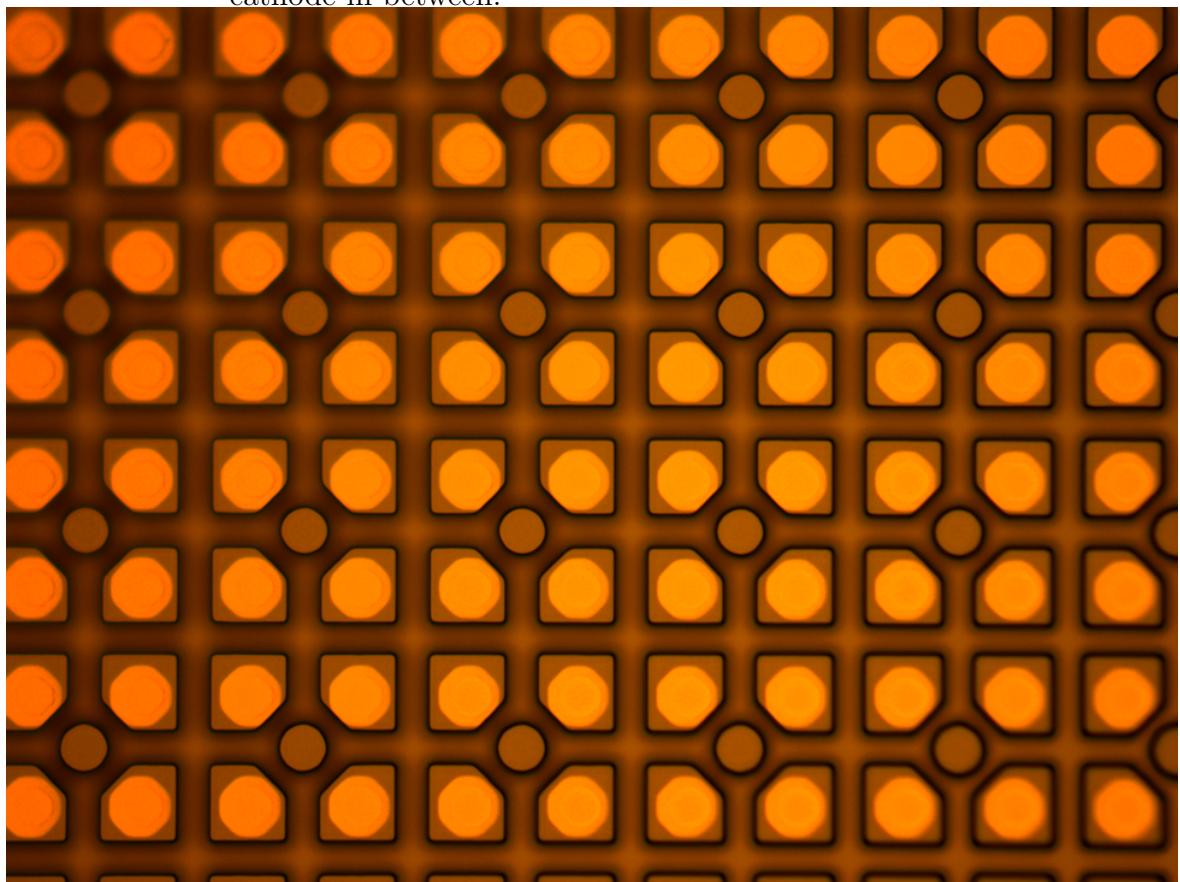


Figure 10.12: Deliverable IAG581, bottom metal near the edge of the array where the development was better, resulting in a more uniform coverage of gold in the channels between the mesas.

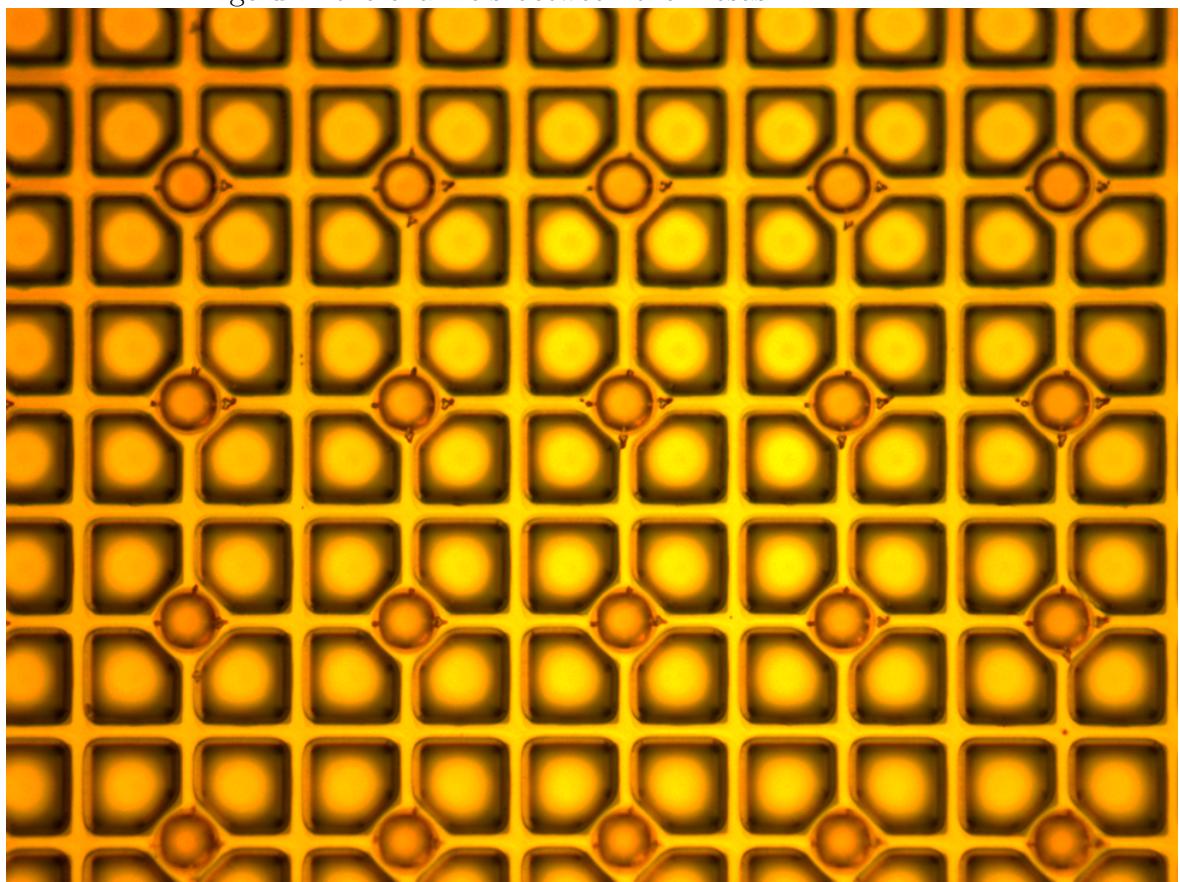


Figure 10.13: Deliverable IAG581, bottom metal deposition near the center of the array. The development did not progress as much here as it did near the edge of the wafer so it is visible that the metal didn't cling as well in the channels, especially near corners.

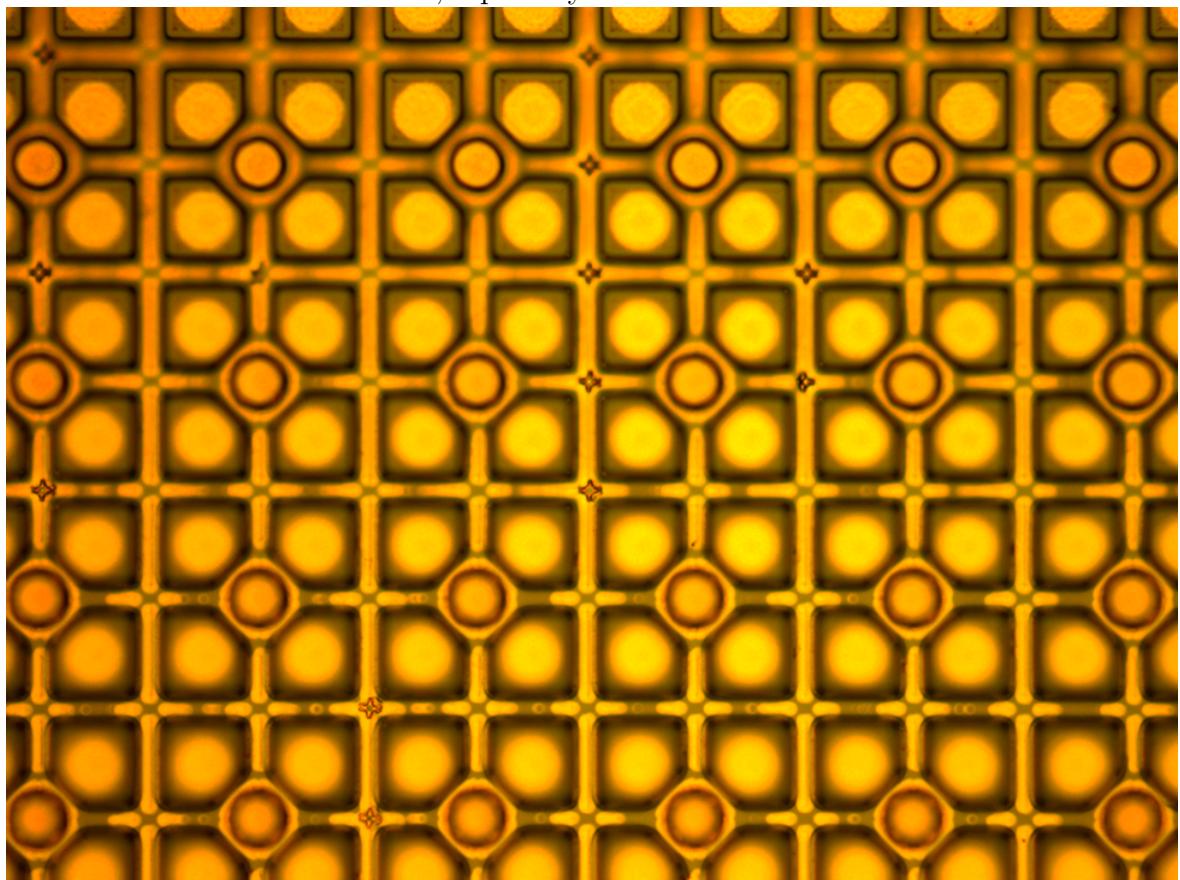


Figure 10.14: Deliverable IAG581, the alignment markings near the edge of the wafer. There is the gold markings from the first metallization being matched to markings from the bottom metallization which are more difficult to see. The alignment is excellent.

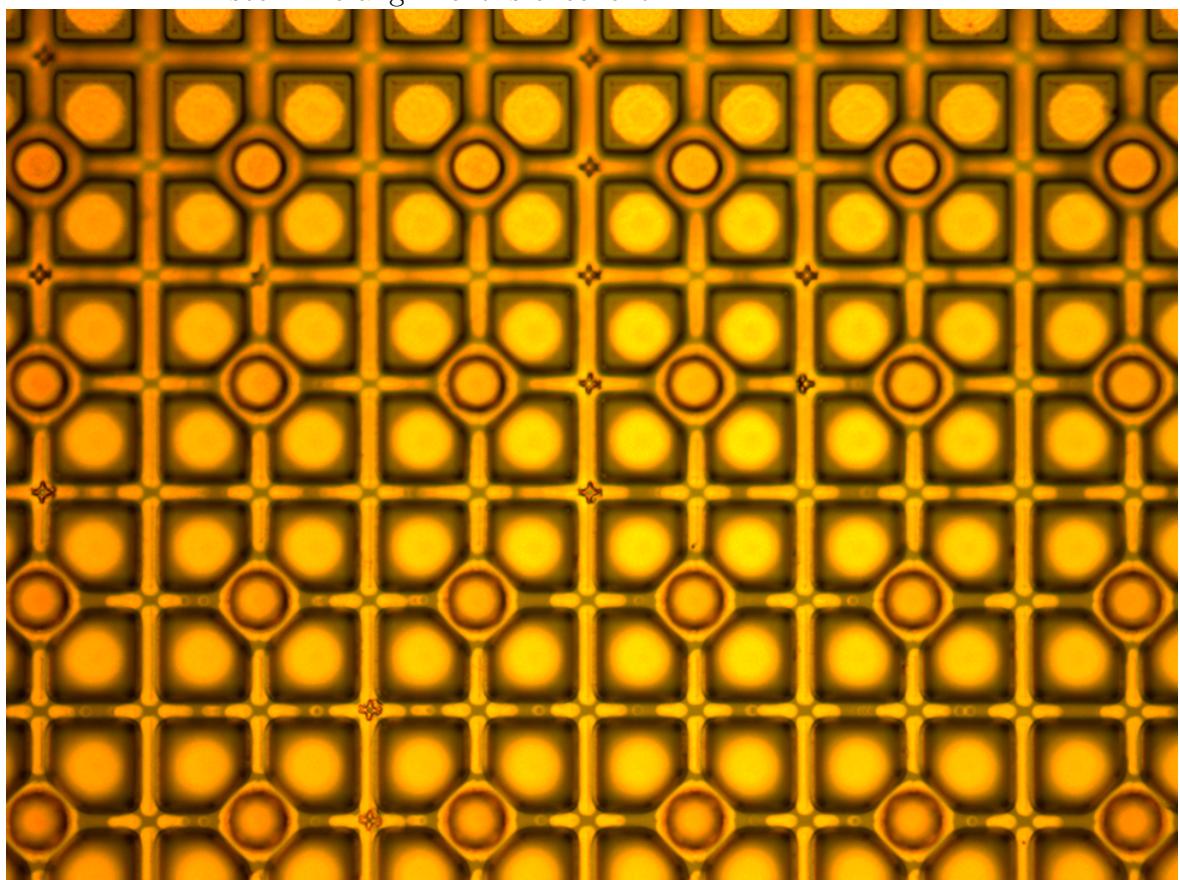


Figure 10.15: Image of a completed AIREA wafer. This wafer is ready for indium bumping and dicing.

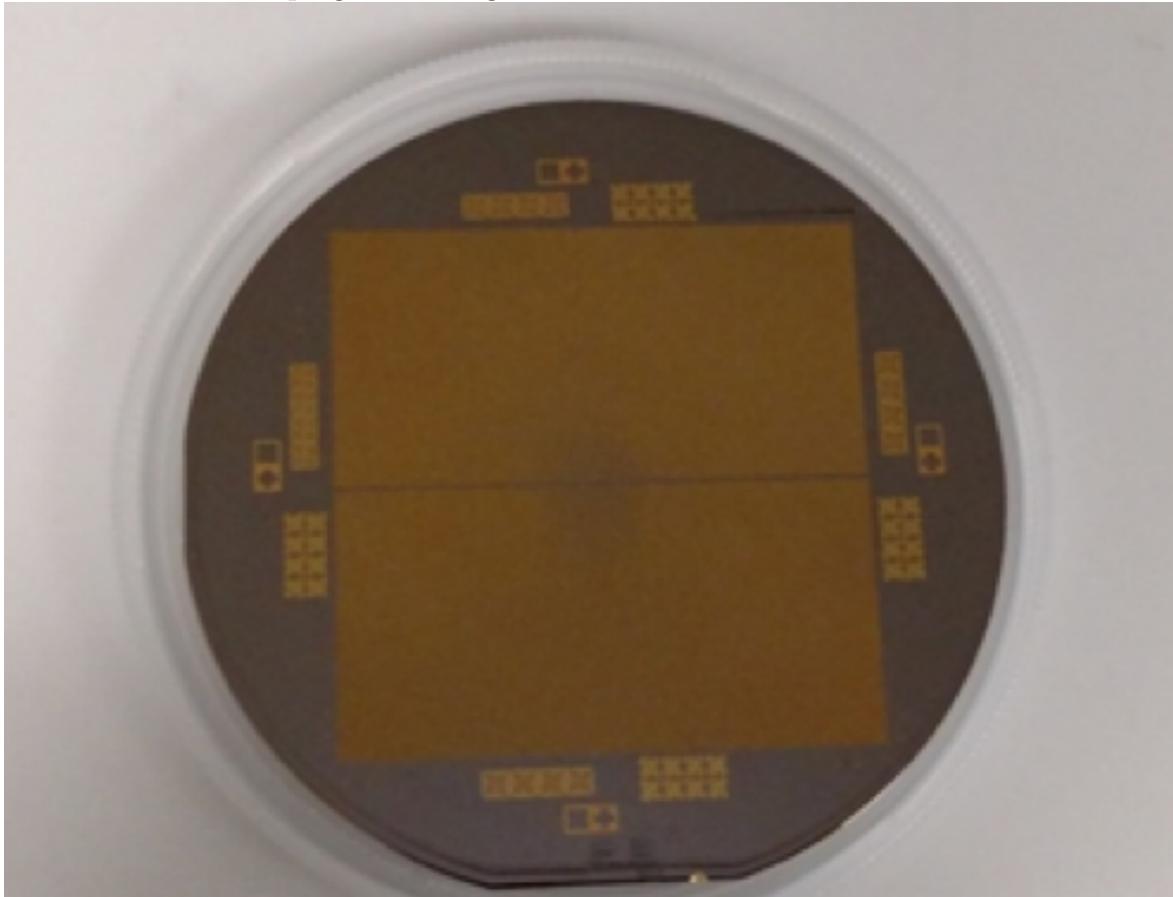
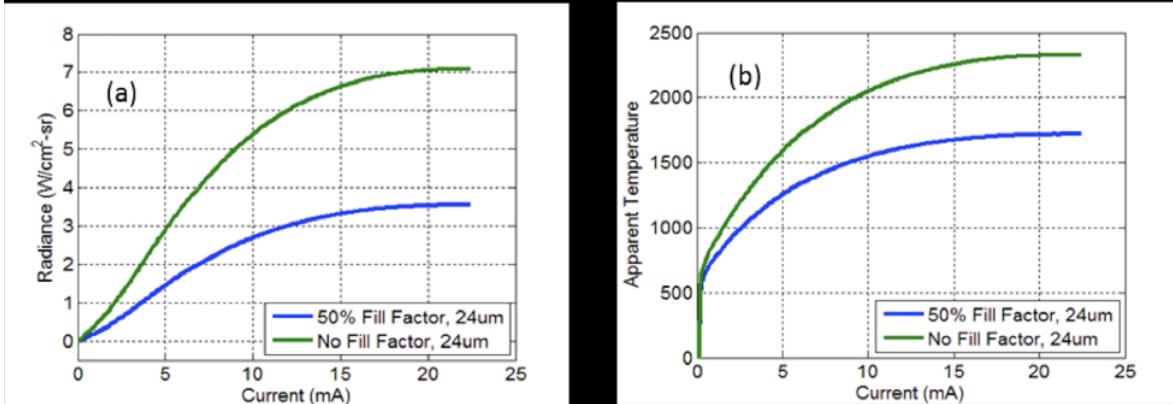
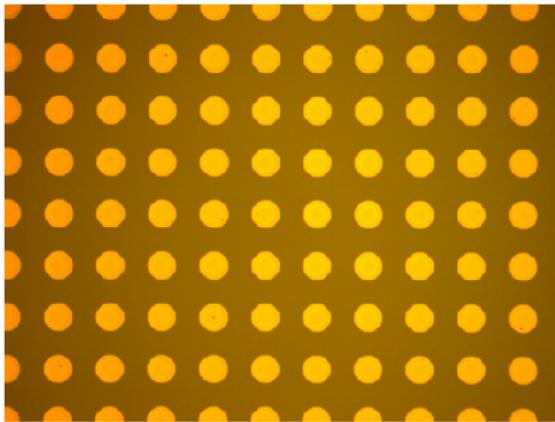
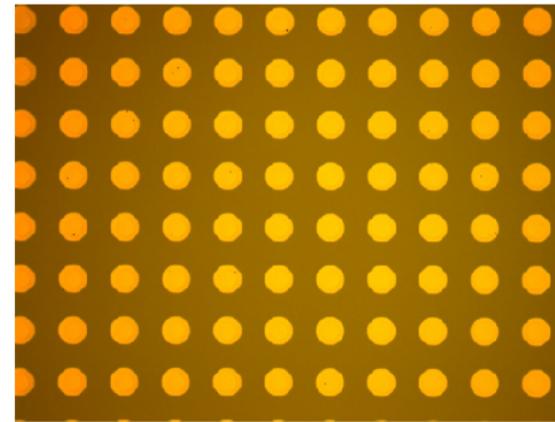
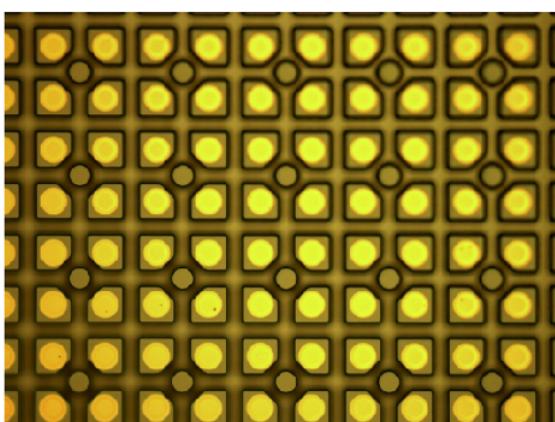
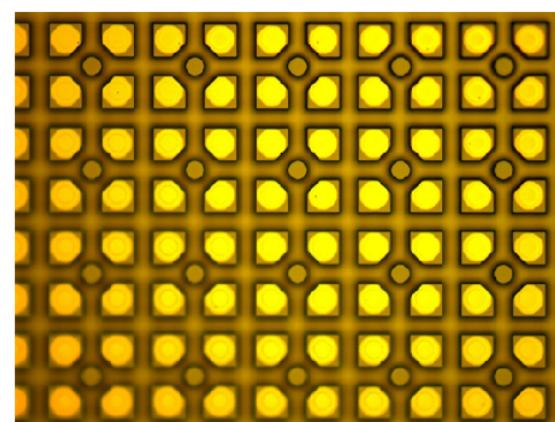


Figure 10.16: (a) Light-Current and (b) Apparent Temperature curves for a 24x24 μm^2 device across the 3-5 μm band.



figures 1-4). This wafer completed fabrication in September 2016.

Figure 10.17: Pictures of the etch and top metal contacts on IAG616.

	
Figure 1: Top metal contacts deposited in July near the center of the wafer.	Figure 2: Top metal contacts deposited in July near the edge of the wafer.
	
Figure 3: Etch of the mesas and common anode pillar near the center of the wafer.	Figure 4: Etch of the mesas and the common anode pillar near the edge of the wafer.

10.1.5 AIREA SLEDs Wafer Indium Bump Fabrication

The hybridization process requires that both the SLEDs die and the RIIC die have indium bumps deposited onto them prior to pressing both die together and fusing the indium bumps. The indium bumps are deposited onto the dice using a photolithography process. If good alignment is achieved between the RIIC die and the SLEDs die then the indium bumps should be right over each other. Figure 10.18 shows the general shape of an indium bump on the left and the location of the indium bumps for both the SLEDs die and the RIIC die on the right. Notice that the blue and purple markings overlap with each other in the diagram showing the ideal good alignment between the two dice.

Prior to performing any processing TSI performs a visual inspection of the parts to help troubleshoot future problems should they arise. Figures 10.19 and 10.20 below shows microscope inspection photos of the AIREA SLEDs array. They were taken when the array arrived at Teledyne with a microscope and show some small blemishes on the SLEDs array. The dark edges are from the microscope objective. Each gold spot represents a pixel in the array to give an idea of how many pixels are affected by these defects. These blemishes are a normal occurrence because no processing is perfect and not too many pixels appear to be affected by these blemishes.

There were some issues with putting the photoresist onto the SLEDs wafer because of the cleaved edge on the top of the wafer. In Figure 10.21 the round SLEDs

Figure 10.18: General shape of an indium bump on the left and the location of the indium bumps for both the SLEDs die and the RIIC die on the right.

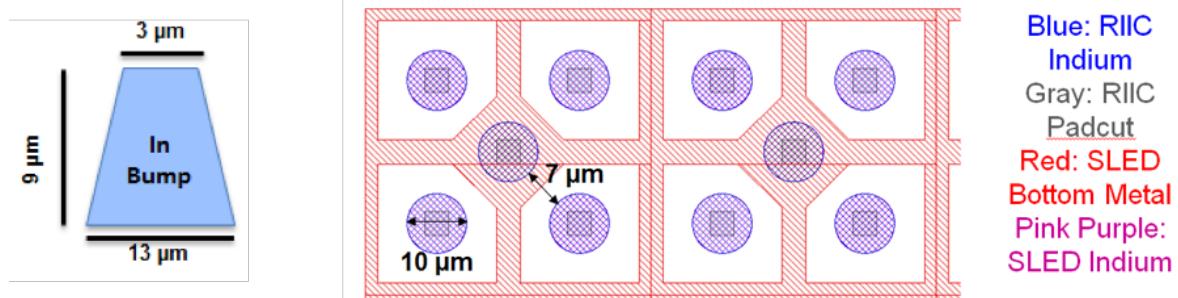


Figure 10.19: Microscope Inspection Image of AIREA SLEDS Wafer.

AIREA Inspection Photos

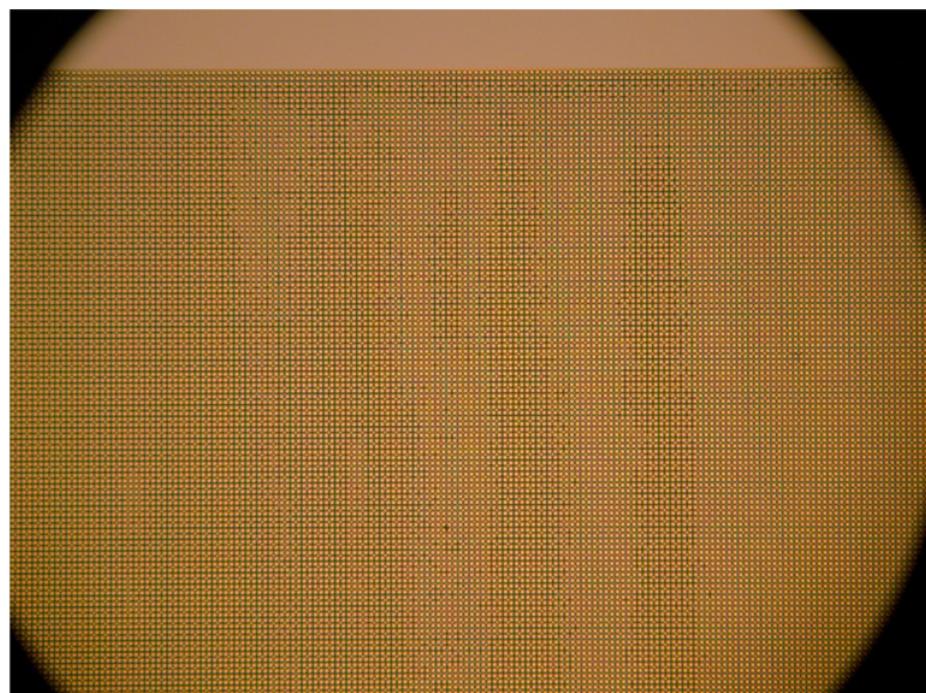


Figure 10.20: Microscope Inspection Image of AIREA SLEDS Wafer.

AIREA Inspection Photos

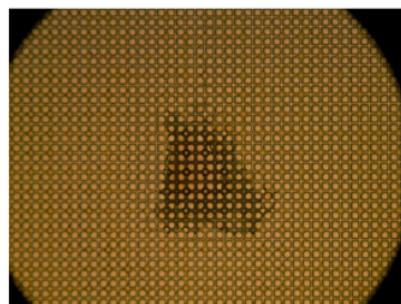
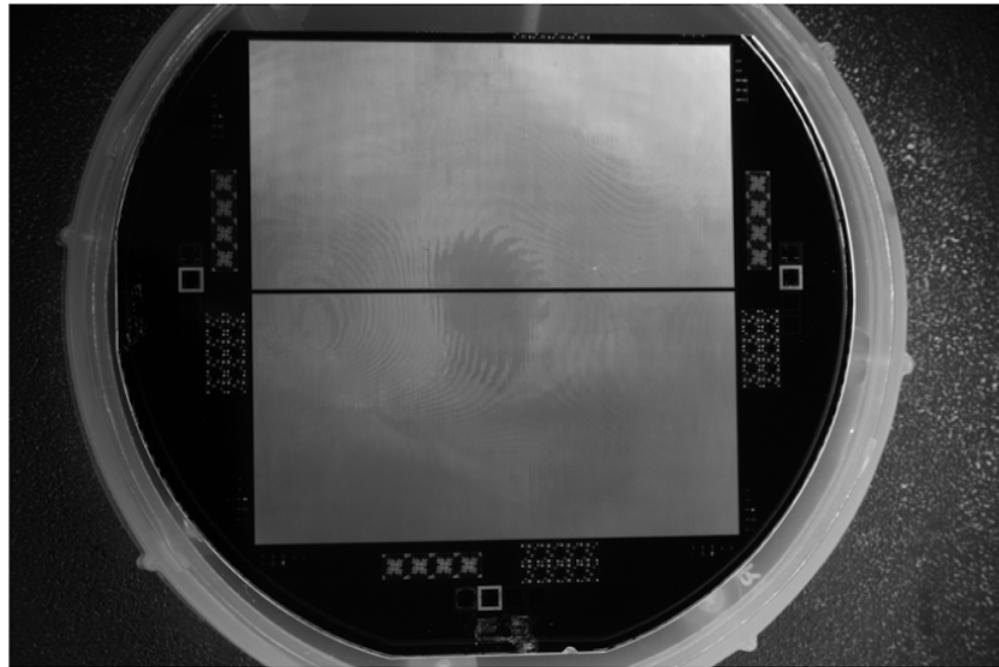


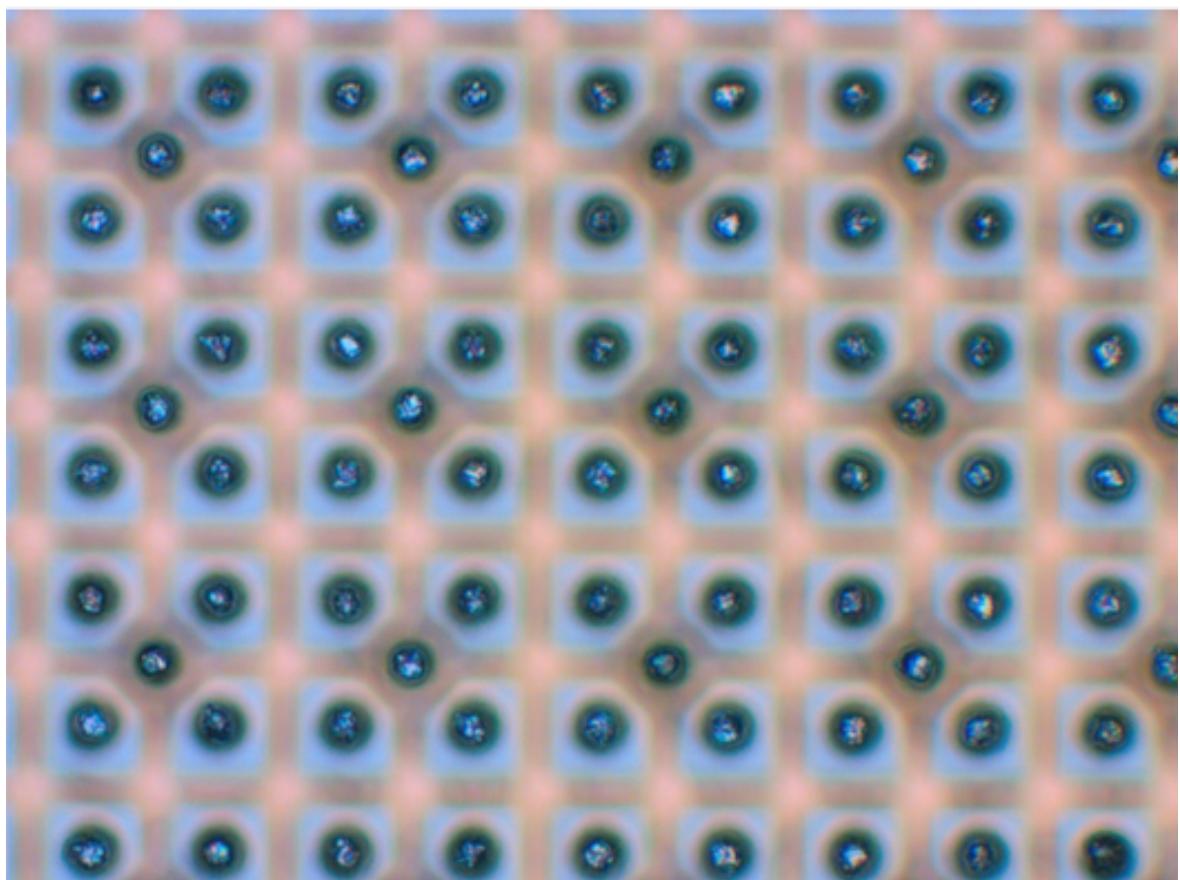
Figure 10.21: Edge bead bubbles and cracks during lithography bake on the cleaved edge.

AIREA Lithography Issues



wafer looks like a flat tire now. The flat tire causes a thicker layer of resist and bubbles to accumulate along the edge of the cleave. This cleave was done to remove the PECs test devices for UIOWA to study and improve their growths. The buildup of the resist caused bubbles and cracks to form once the photoresist for the indium bump deposition is baked to harden the photoresist. The photoresist buildup prior to baking is shown in Figure 10.21 and the resultant bubbles and cracks post-baking process are shown in Figure ???. The bubbles and cracks formed near the cleaved edge cause indium bumps to not to be deposited. This renders the pixels in that region non-functional because no electrical connection can be formed between them and the RIIC pixels. In the future, the cleave will be farther away from the SLEDs hybrid to avoid these edge issues. It was decided that the loss of the pixels was acceptable because the affected edge was not the edge that would be abutted. Thus, AIREA would still be able to demonstrate the operation of two arrays abutted next to each other and accomplish the goals of the AIREA program. A close-up picture of the finished indium bumps on the SLEDs wafer can be seen in Figure 10.22.

Figure 10.22: Finished Indium bumps on the SLEDs die.



10.1.6 SLEDs Wafer Trench Etch Overview.

One of the challenging aspects of abutting two hybrids together is the need for a smooth vertical sidewall on the hybrids. Figure 10.23 below shows two hybrids with very rough sidewalls. The dashed red lines mark the most prominent feature of each hybrid. It can be seen that when these two hybrids are brought close together the minimum spacing will be limited by how much the prominent features protrude from the hybrids. To minimize the roughness of the sidewalls of the SLEDs die it was decided to use an Inductively Coupled Plasma (ICP) etch. In the literature this etch has been shown to create an exceptionally vertical sidewall for InAs / GaSb focal plane array applications [11].

The steps for creating a smooth vertical sidewall on the SLED die are as follows:

1. ICP etch a 50 micron deep trench at the edge of each SLEDs die.
2. Use a dicing saw to separate the SLEDs dice from the wafer.
3. Perform a facing cut with a fly cutting machine to expose the etched edge and separate the two SLEDs dice.

Figure 10.24 below shows the location of the 50 um deep trench with a wafer level perspective. Figure 10.25 shows a zoomed in view of the trench etch. In the zoomed in view it is possible to see that the trench is 50 um deep and 430 um wide. Once a trench is etched into the wafer in the appropriate place a dicing saw is used to cut along the rectangular outer perimeter of the SLEDs wafer. The resultant piece is then flycut to release the individual SLEDs die. The location of the fly-cut is shown in Figure ?? below.

Figure 10.23: Rough abutted vertical sidewalls.

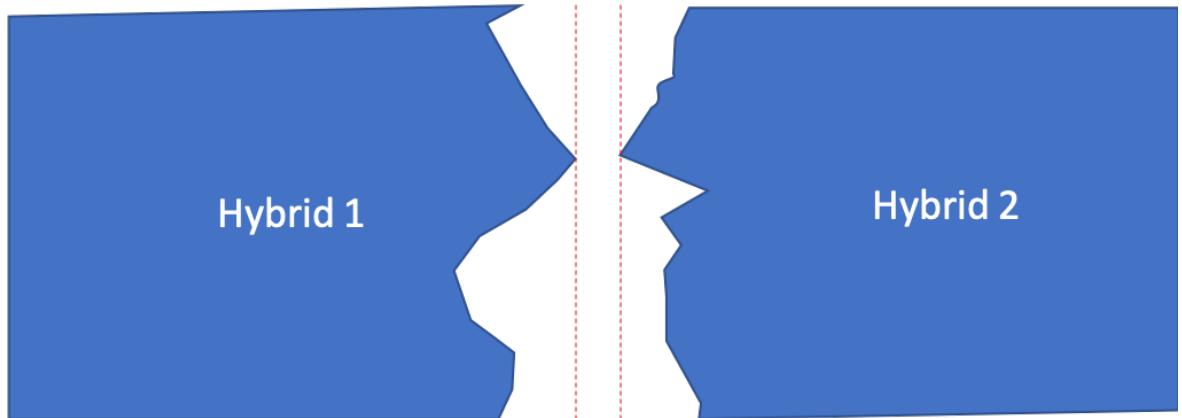


Figure 10.24: SLEDs Wafer Trench Etch.

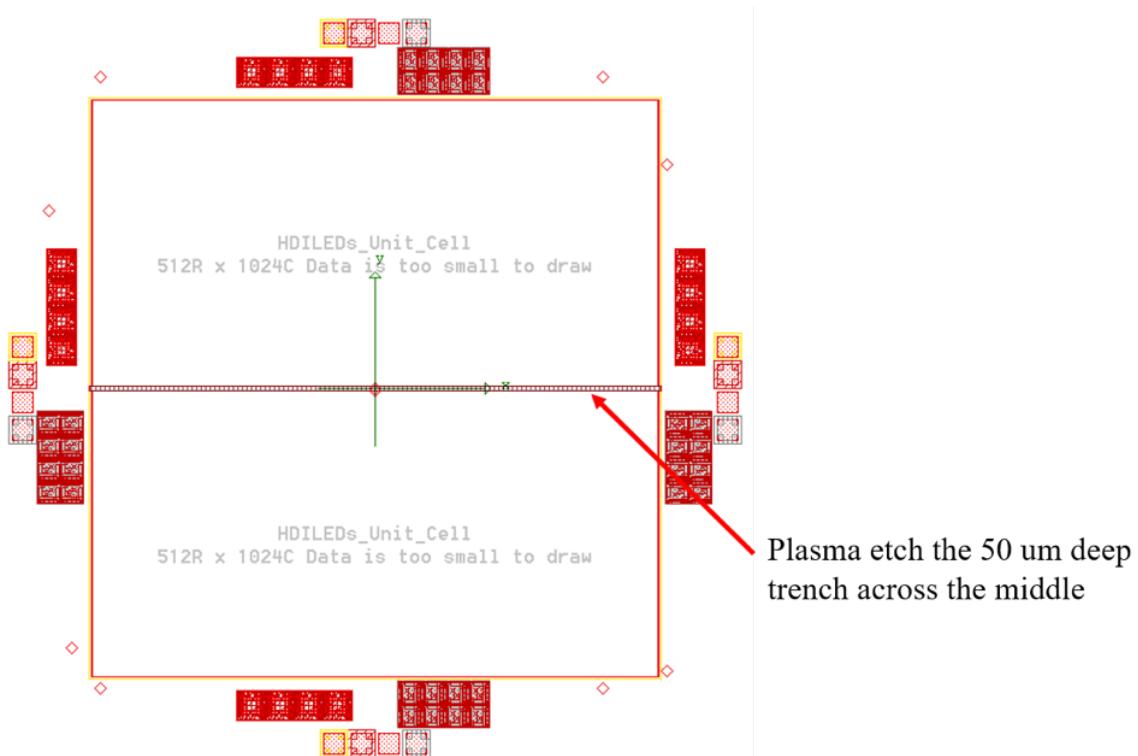


Figure 10.25: SLEDs Wafer Trench Etch.

Location of the Plasma Etched Trench on the GaSb wafer

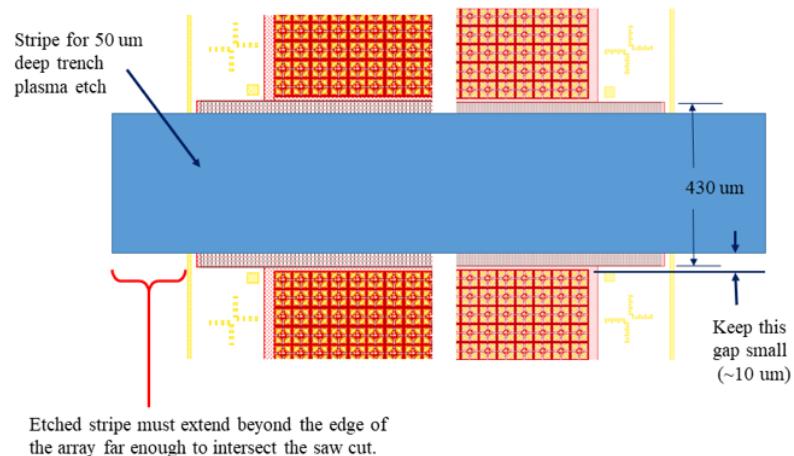
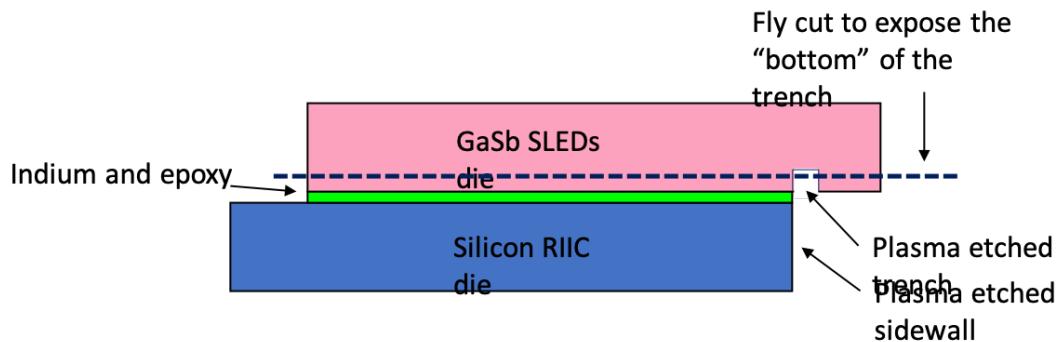


Figure 10.26: Zoomed in view of the 50 micron deep trench and overview of the fly cut procedure.



10.1.7 SLEDs Wafer Trench Results

A 50 um deep trench was etched into the SLEDs wafer in the appropriate place by the University of Iowa. The trench etch was performed after the indium bumps were deposited onto the SLEDs die. This order was chosen because there was a concern that the doing the trench etch prior to the indium bumps would cause issues with the photoresist as seen with the cleaved edge of the SLEDs wafer, and introduce optical edge effects that would reduce the quality of the indium bumps. The issue with doing the trench etch second is that the indium bumps may melt during the ICP etch. This is because the wafer must be heated to facilitate the ICP etch. Unfortunately, some of the indium bumps did melt during the ICP etch. These can be seen in Figure 10.27.

Figure 10.27: Melted Indium bumps from the ICP trench etch.

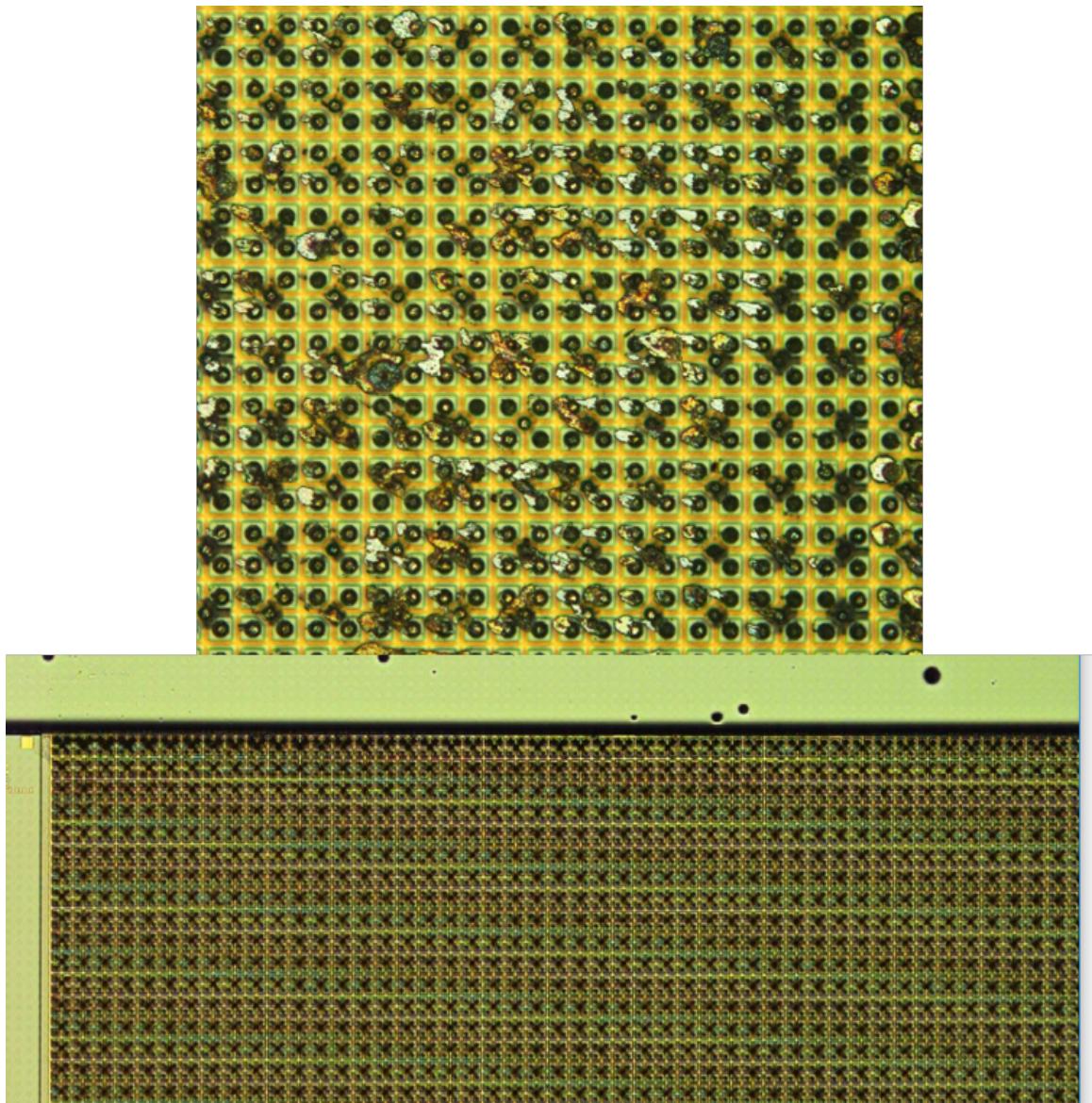
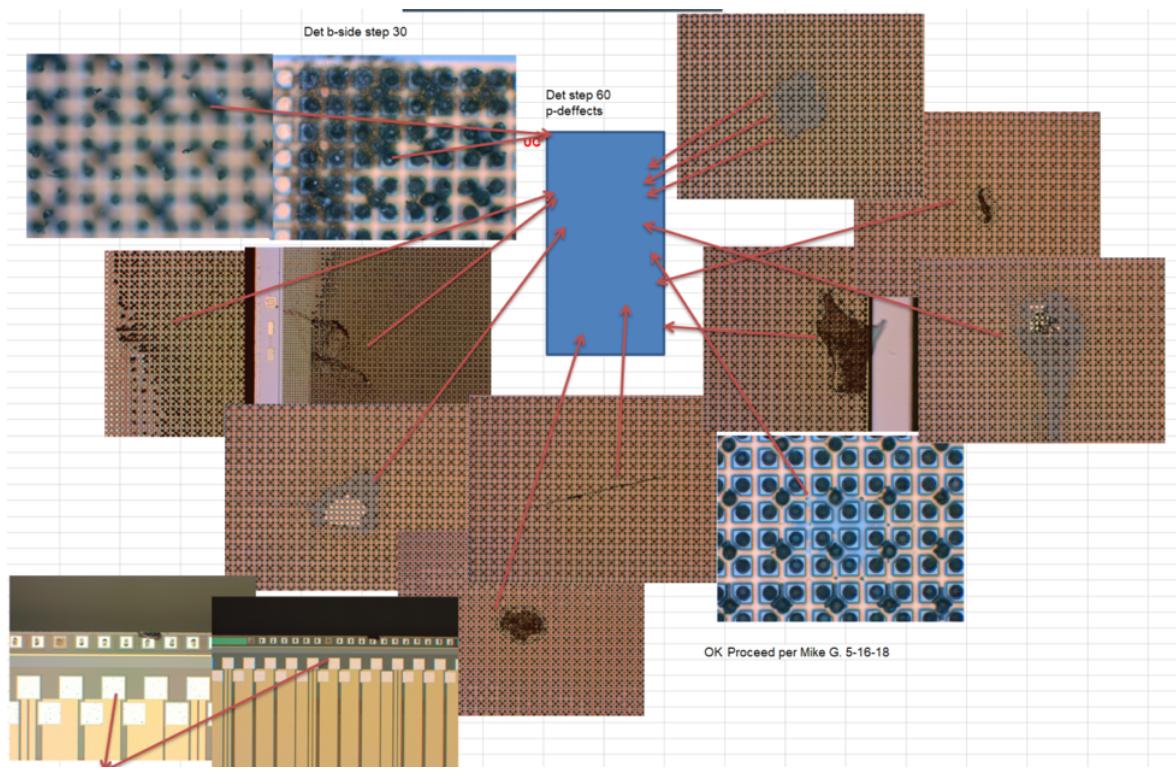


Figure 10.28: Overview of all defects observed on the AIREA SLEDs die.



10.2 RIIC Work

10.2.1 AIREA RIIC Overview

It was initially proposed to abut two 1K x 1K hybrids to obtain a 1024 x 2048 pixel resolution hybrid in the AIREA Phase 2 Proposal. However, it was later possible to increase the final resolution to a 2048 x 2048 array by abutting two 1024 x 2048 hybrids together. This boon was possible because of the ability to share masks and costs with HDILEDs program. The rectangular hybrids are each 1024 x 2048 pixels and only require one butt joint for the hybrid. This reduced cost and risk for the program, while also developing the abutment process. The final version of the Cadence Virtuoso layout of the AIREA RIIC is shown in Figure 10.29 below. A cartoon version of the AIREA RIIC is shown in Figure 34 highlighting the different major architectural pieces of the RIIC.

The AIREA RIIC is two inches long along the long side and one-inch long along the shorter side. The abutment edge is the long edge without the yellow bond pads. Figure 10.31 shows how the two RIICs are abutted together. The AIREA RIIC design is fairly similar to the original 100 Hz system [12] except that it has 24-micron pitch pixels. It uses the same architecture as the NSLEDs and HDILEDs projects[5], [4]. The RIIC does not include any TSVs and has an X-Y addressing method rather than the theorized shift register architecture for larger sized arrays of hybrids. These design choices reduced risk and placed the only risk in the development of the abutment process. An area devoid of metal fill layers had to be added along the side of the AIREA RIIC to facilitate etching through the silicon substrate. The trench area is 100 microns wide and filled with the DIF layer in the On-Semi C5N process. This layer is used to dope the silicon p substrate for transistor placement. By including this layer the metal fill layers that would normally be deposited during the wafer processing are removed. The area in the trench is composed of Boron doped Silicon and TEOS oxide. A diagram showing a cross-section view of the region to be etched is shown in Figure 10.32.

Figure 10.29: AIREA CMOS RIIC.

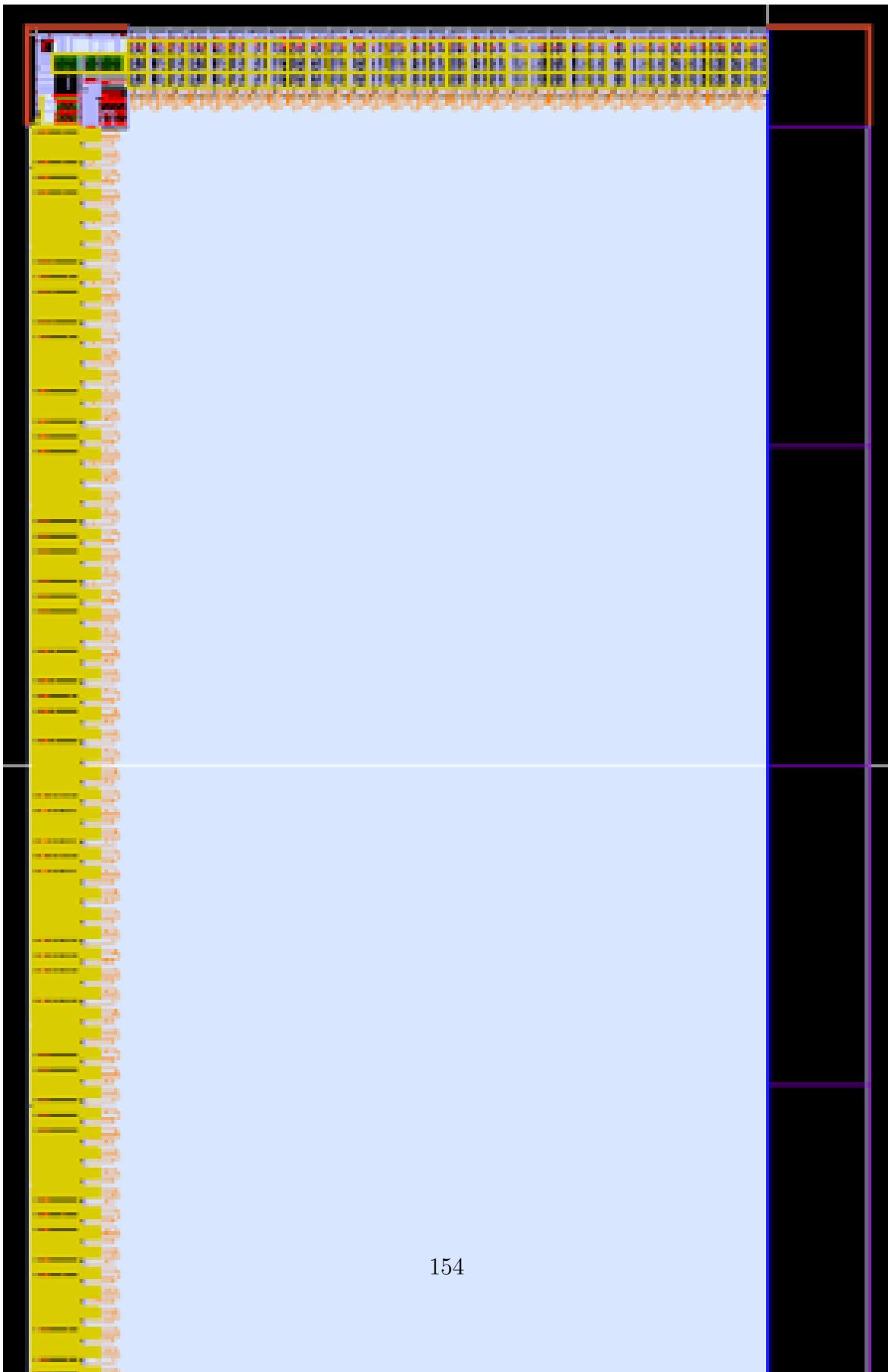


Figure 10.30: Architectural overview of the AERIA RIIC.

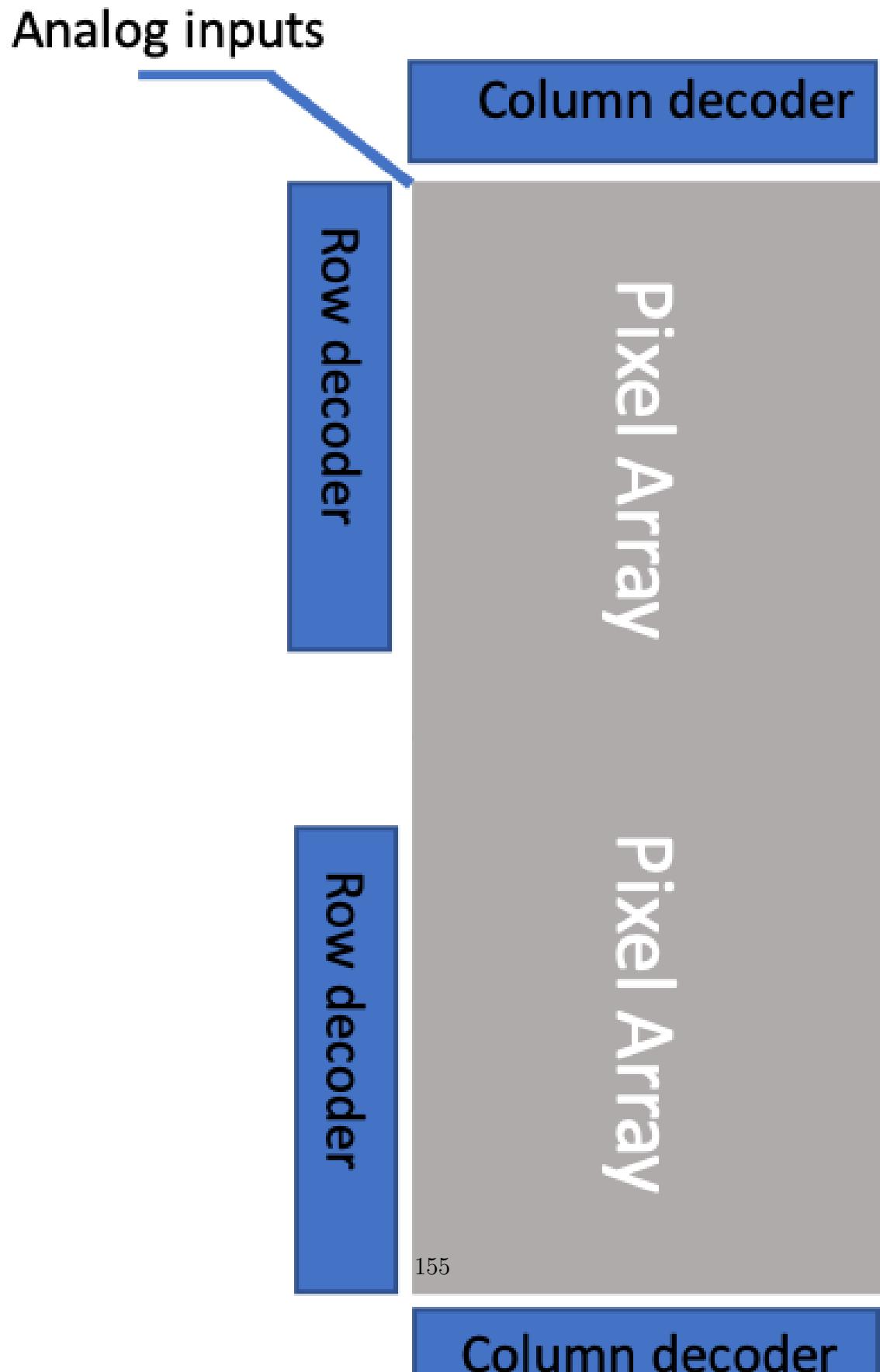


Figure 10.31: Architectural overview of the AERIA RIIC.

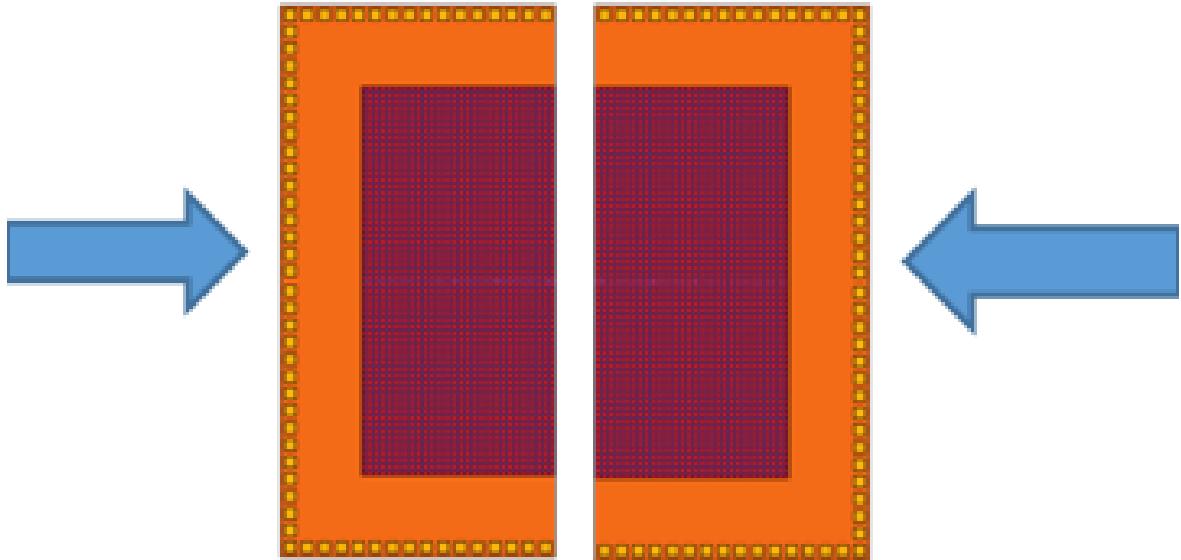
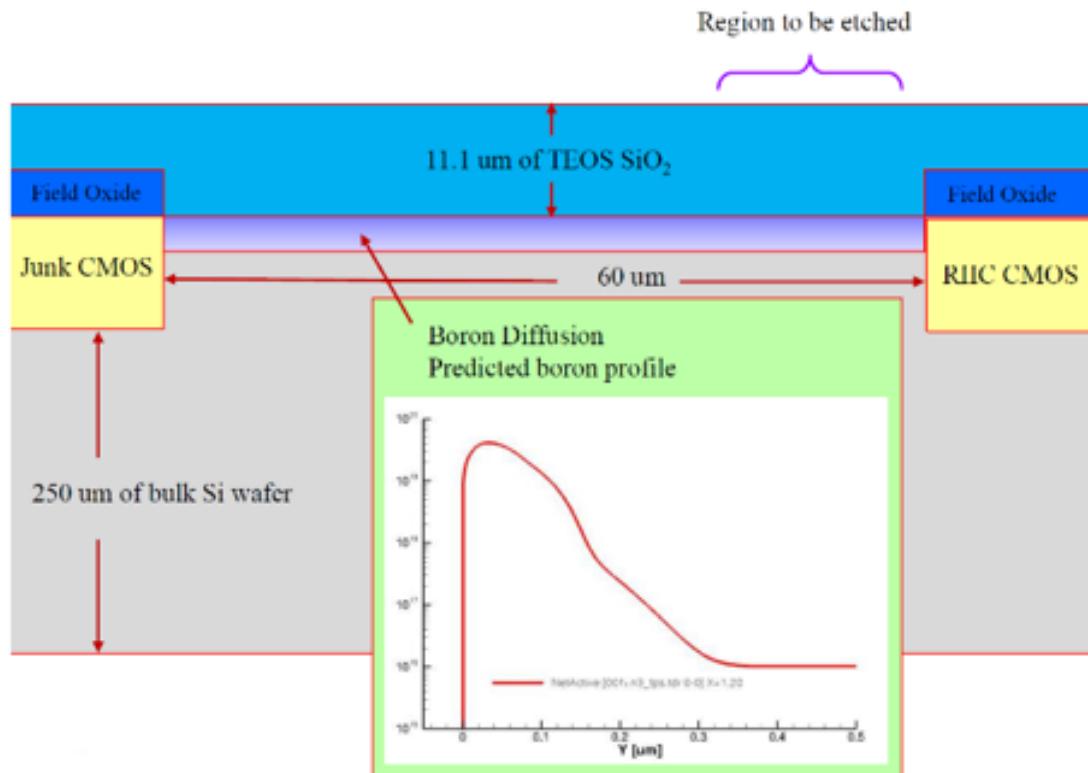


Figure 10.32: Architectural overview of the AERIA RIIC.



10.2.2 RIIC Pixel Testing

32x32 pixel arrays of the pixel circuit that the AIREA RIIC uses were fabricated and tested in the beginning of the AIREA program. The test chips from MOSIS were packaged in a PGA257 package and as bare die. The purpose of these test chips was to test the pixel design of the RIIC and ensure that it worked properly.

The testing of the 32x32 AIREA RIIC test chips was successful. Figures [10.33](#) and [10.34](#) below shows strong drive transistor sweep (left side) and weak drive transistor sweep (right side) for 100 pixels measured on the AIREA test RIIC. The measured sweeps of the strong drive and the weak drive were within the desired specification.

Figure 10.33: Strong drive transistor I-V sweep.

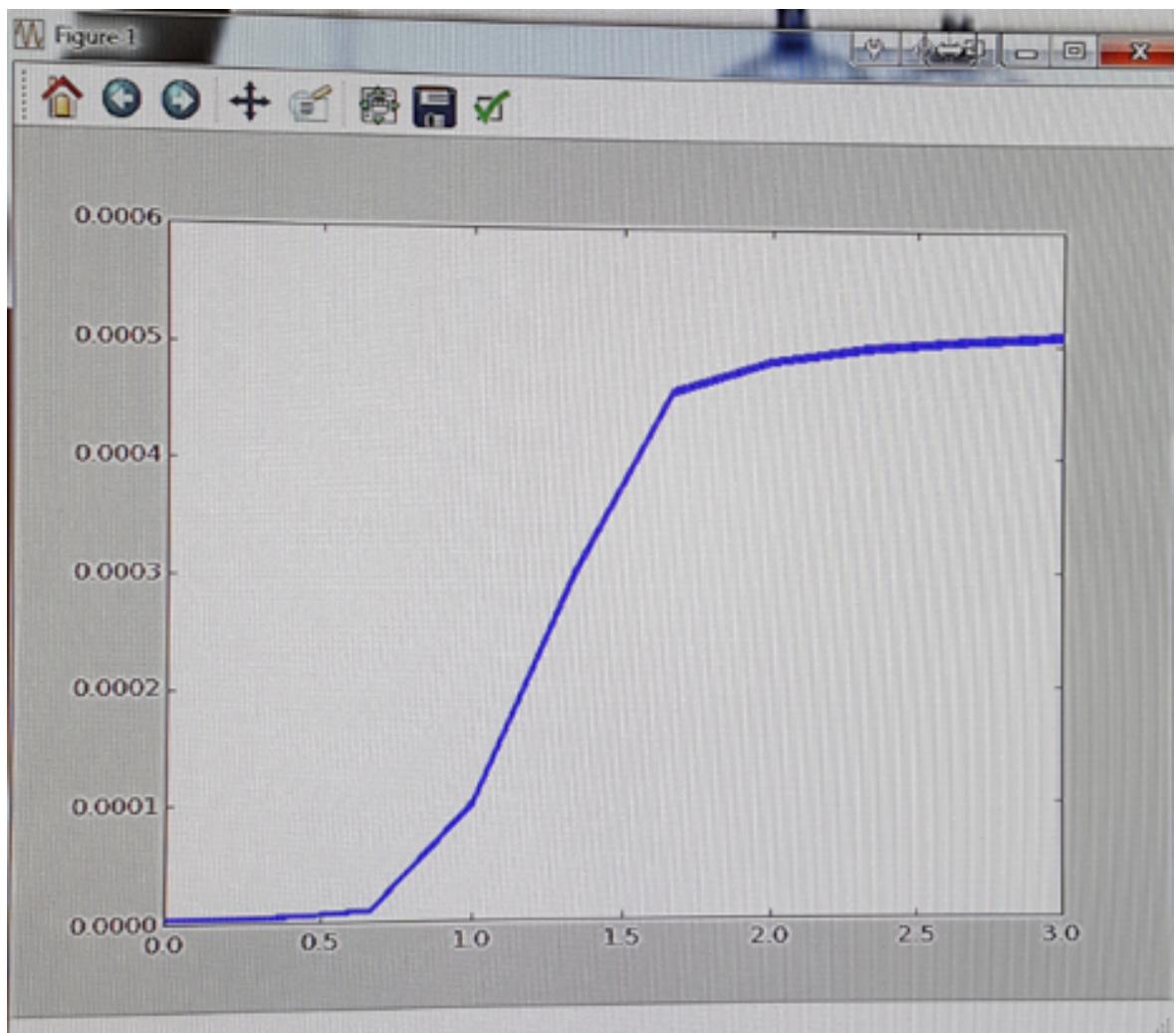
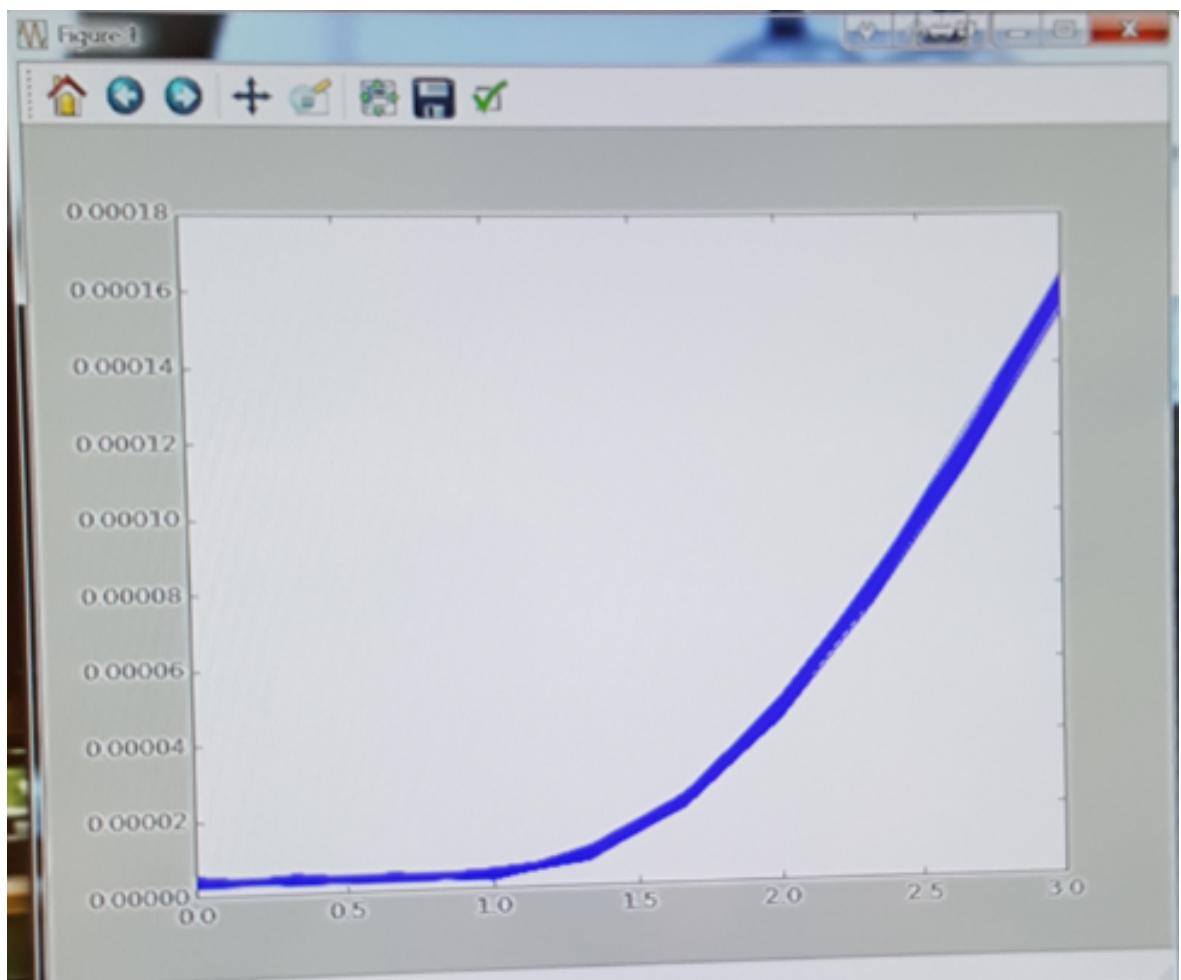


Figure 10.34: Weak drive transistor I-V sweep.



10.2.3 Oslo RIIC Design Update

The AERIA program was fortunate to be able to use the CDS Oslo RIIC design instead of designing a new RIIC. This choice reduced risk in the parts of the project already addressed by other programs and let AIREA focus on developing abutment technology. However, there were some RIIC design changes for AIREA as new information was available from testing the NSLEDS RIIC. Design changes were implemented to the AIREA RIIC to eliminate issues with the quiescent power drain that we found in NSLEDS RIIC. NSLEDS and AIREA share the same pixel circuit so issues affecting the NSLEDS RIIC would also likely appear in the AIREA RIIC. In summary, the quiescent power will be completely non-existent during normal AIREA projector operation. The discussion below provides the technical information about the source of this issue and its mitigation.

The figure below depicts the circuit responsible for the NLSEDS pixel quiescent current. The circuit is a dynamic digital latch that stores the strong/weak value for the pixel. Dynamic latches forget the stored value after a certain time. The forgetting is caused by charge leakage through the PMOS and NMOS pass transistors (e.g. reverse biased diodes at the drain of those transistors). The NMOS pass transistor leaks to ground and the PMOS pass transistor pulls to VDD. Since these transistors are equally sized, the un-driven latch will eventually settle to $\frac{1}{2}$ VDD voltage at its input. When a CMOS inverter has its input sitting at $\frac{1}{2}$ VDD, it will conduct current because both NMOS and PMOS will be in saturation region. This was the source of the quiescent current draw in the NSLEDS RIIC.

To verify this hypothesis, a simulation where the CMOS inverter leakage current for supply voltages ranging from 0V to 5V was measured. The results from this simulation were compared to leakage current that was measured on the NSLEDS RIIC. The measured and simulated curves are shown below and have a very good correlation. The simulations show that at 3.3V the leakage current in inverter is 10 micro-amperes. This would result in a 10 Ampere quiescent current draw for a 1Kx1K NSLEDS RIIC. However, the final settled voltage at the input of the CMOS inverter maybe slightly

Figure 10.35: Selstrong circuitry.

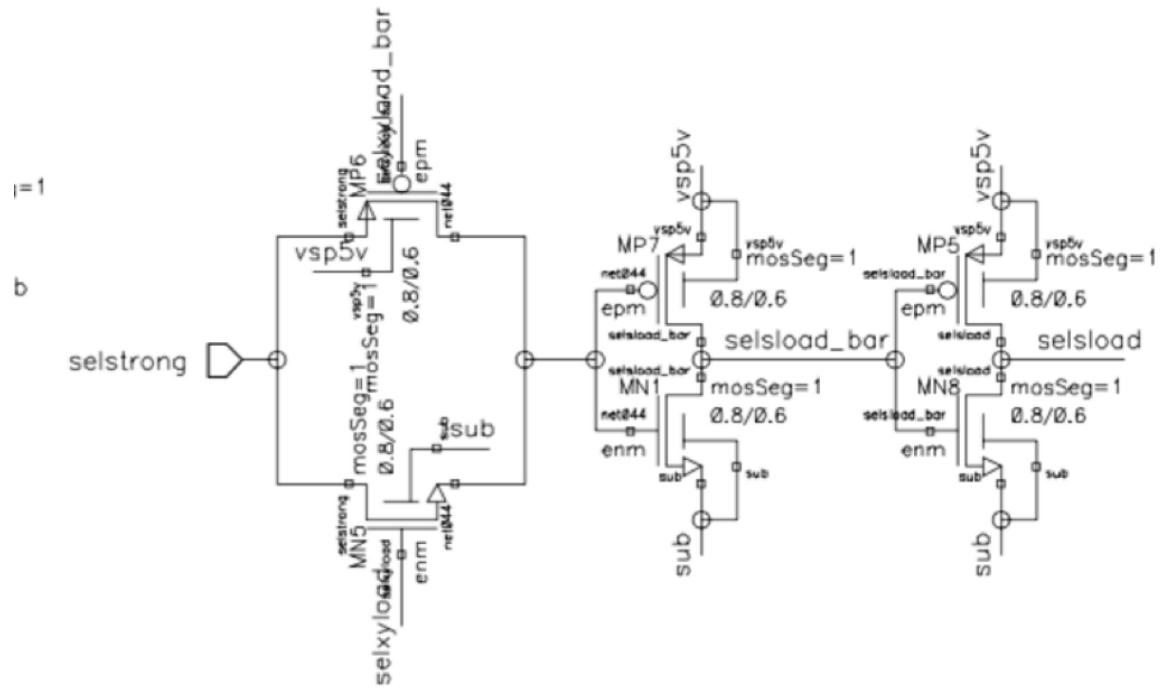
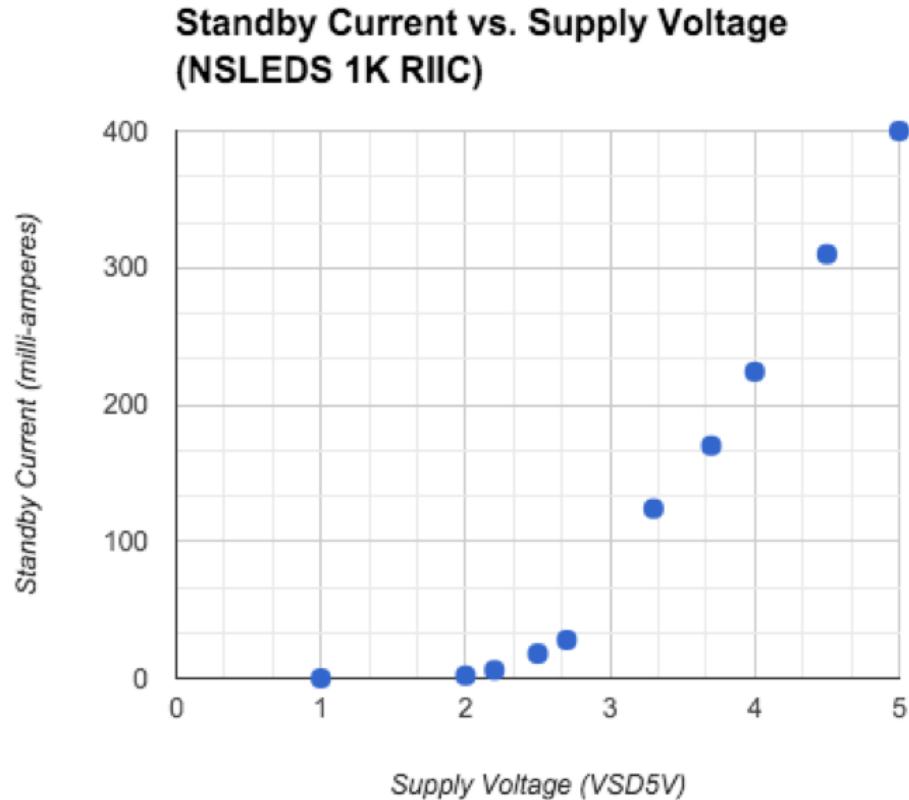


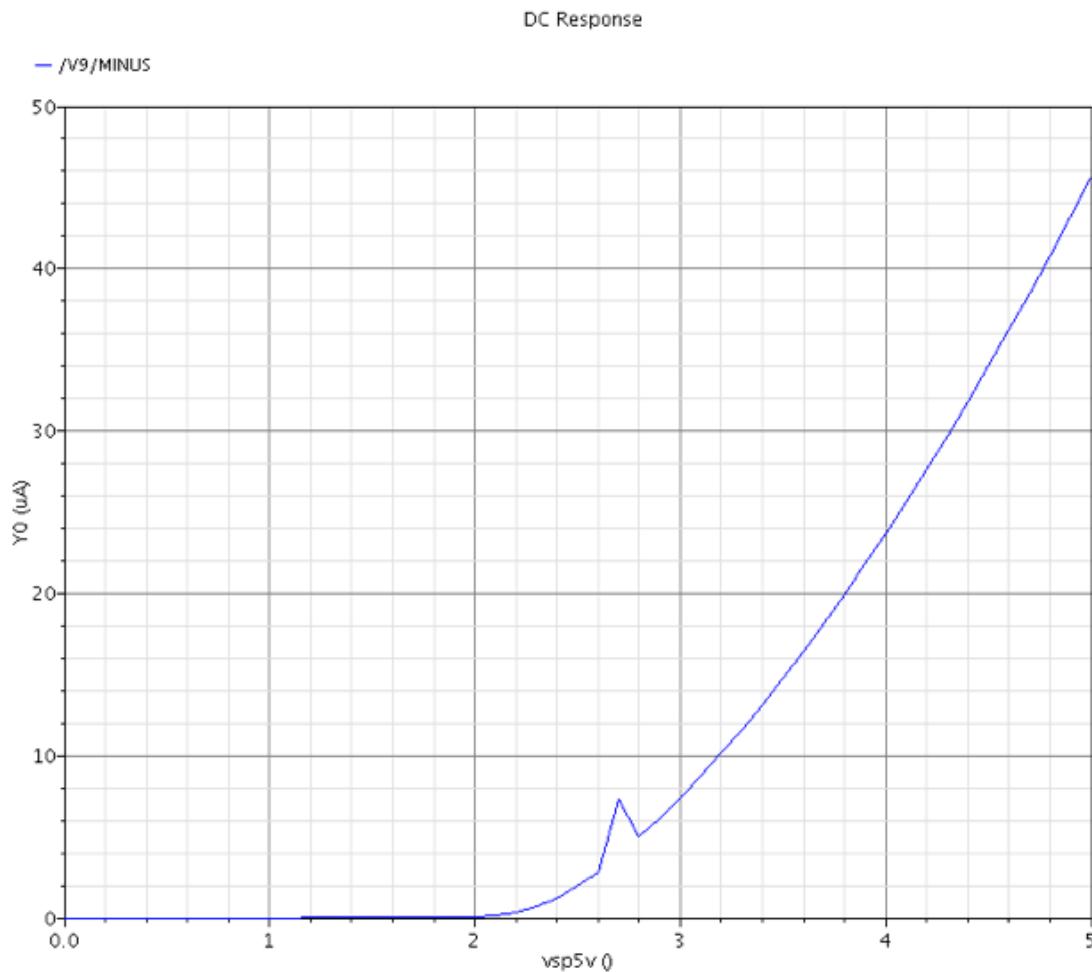
Figure 10.36: Standby current vs supply voltage.



lower or higher than $\frac{1}{2}$ VDD because it depends on strength of PMOS and NMOS leakages. This explains why the NSLEDS RIIC had a quiescent current smaller than 10 Amperes. This was not an issue on the TCSA RIIC even though the same memory circuit is used because there was room to add a large capacitor in the pixel design at the CMOS inverter node. In the case of TCSA if the node is initialized, it is likely to stay there for a long time due to the capacitors ability to hold charge.

The reason quiescent power draw will disappear during normal AIREA projector operation is because in projector operation, every pixel in the projector will get updated at the frame rate of the projector. The tests indicated that the dynamic memory time constant at room temperature is around 20 seconds. Since the refresh rate is much smaller than 20 seconds, the pixels will not have time to lose their dynamic memory.

Figure 10.37: Simulated standby current vs supply voltage.



This in turn means that quiescent power draw will remain at a negligible amount during normal projector operation. And if the projector is not being operated in DVI mode, then a reset signal can be applied at time intervals less than 20 seconds to ensure that pixels do not lose their dynamic memory.

The issue of quiescent current draw during wafer testing of AIREA RIICs was still an issue. In wafer testing, it is not possible to periodically refresh or reset all of the pixels, so the approach described in previous paragraph will not work. To resolve the quiescent current issue during wafer testing of AIREA RIICs, two things were changed in the RIIC design:

1. All digital RIIC inputs were pulled down to low input when pins are not connected.
2. During the Reset State during power on all digital and analog memory in every pixel must be set to 0 volts.

Change 1 was accomplished by putting a 100KOhm resistor to ground on-chip at each of these inputs. The reason this change was required was that during probe testing, it is only possible to control inputs for one of the four RIIC quadrants. However, all four quadrants were powered during testing, so the three quadrants that were not controlled must enter a sleep mode. Sleep mode was enabled by pulling the digital inputs (SPIRSTB) low. Change 2 was accomplished by including additional logic on the RIIC that implemented a reset for the entire array.

These changes resulted in the AIREA 1Kx2K RIIC having a standby current of around 50 milliamperes instead of 1 Ampere. The figure below shows the section of the AERIA RIIC before and after pull-down resistors were added. The figure that follows shows additional logic that was added to implement reset for the entire array.

The updated AIREA design is otherwise functionally equivalent to the previous AIREA design and to the NSLEDS design. The two exceptions to this are that the polarity of the LOAD bit in the SPI register was inverted and the LOAD input must be held low when RESET is asserted to clear out the entire pixel array (if LOAD input

Figure 10.38: Top image shows the old layout of the digital IO section before adding pull-down resistors. Bottom image shows updated digital IO section with pull-down resistors.

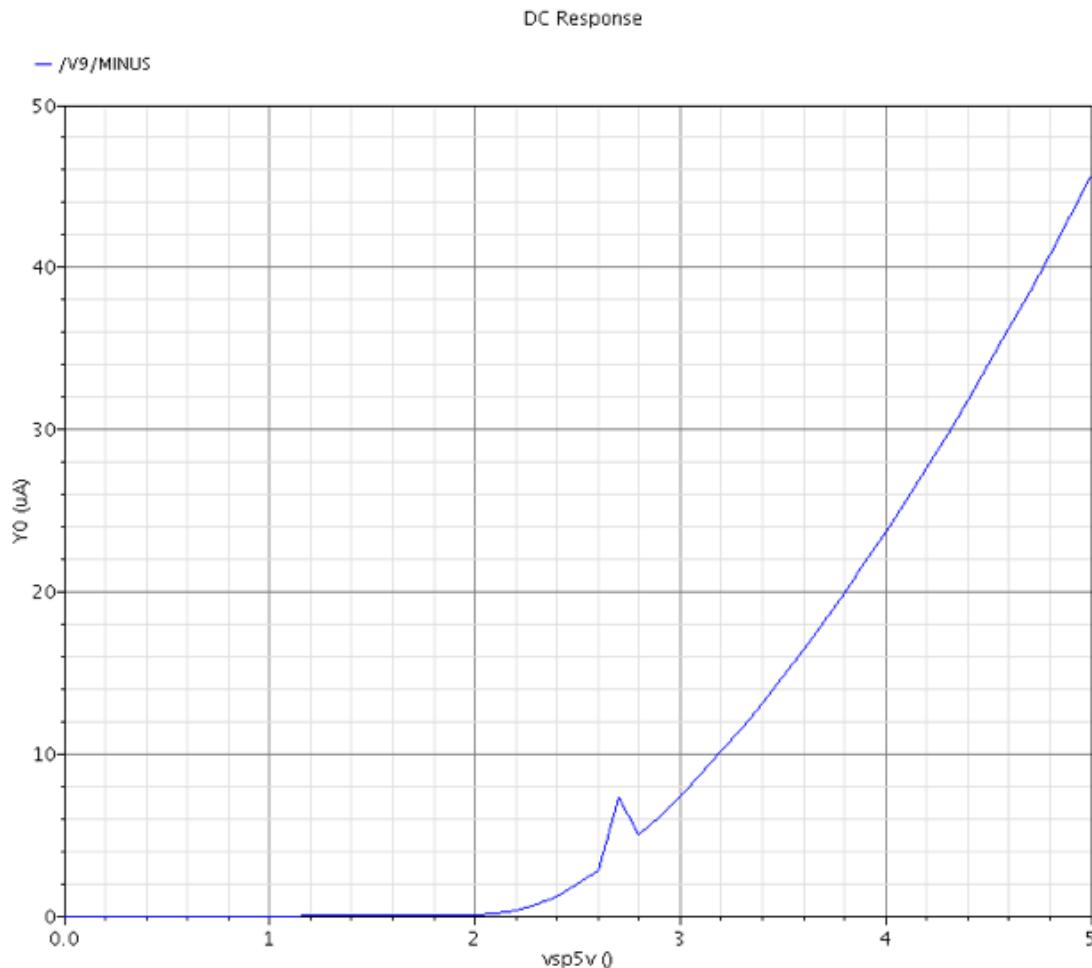
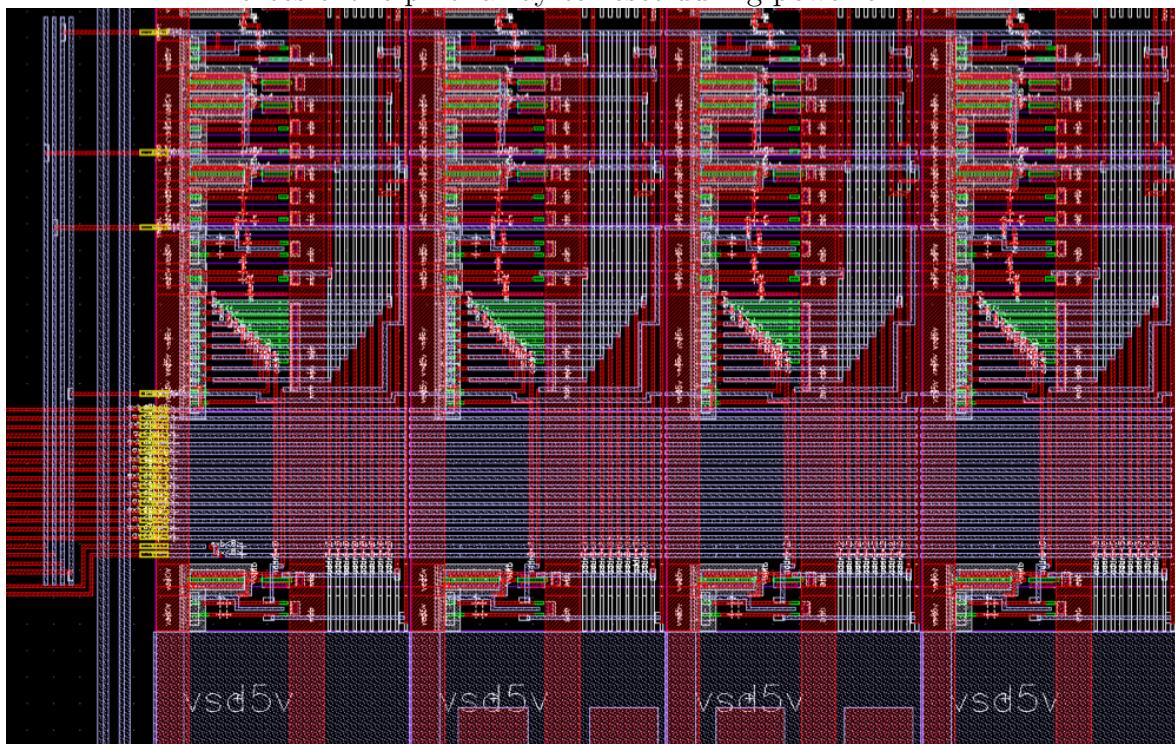


Figure 10.39: Top image shows the old layout of the address decoder section. Bottom image shows updated address decoder section. The added logic is an OR gate that computes $\text{load} = (\text{load or reset})$ - this additional logic forces entire pixel array to reset during power on.



is held high, then only half of the array will be reset). In other words, the SPI register stores LOADB instead of LOAD.

10.2.4 AIREA Wafer Layout.

Initially, it was thought that AIREA could share wafer space with the HDILEDs program. This resulted in a wafer design as shown in Figure 10.40 below. The red outlines represent the outlines of RIICs on the green wafer background. From the image it can be seen that there are six 1K x 2K AIREA RIICs, 2 HDILED RIICs, and six 1K x 1K AIREA RIICs. These values are tabulated in table 2. This wafer design went through several iterations while working with ONSEMI. This version was the most optimal as it abided by all of the rules for reticle stitching and produced the most RIICs.

It was decided due to the complexity involved to not share wafer space with HDILEDs and for AIREA to have its own wafers. The final wafer design had the benefit of sharing everything but the metal 1 - 5, via 1 - 4, and pad masks with the HD-ILEDs project. This approach required ONSEMI to make 10 new GDS masks instead of the full set of 22 masks normally required for a separate wafer run. This was still cheaper than not cost sharing with the HDILEDs program. This method also yielded two more AIREA RIICs than the previous design. Figure 42 shows the final AIREA wafer layout.

Four wafers were ordered from ONSEMI giving a total of 32 AIREA RIICs. This wafer mask design was also ideal because it places the most AIREA RIICs into the highest yielding part of the wafer. This wafer mask design also allows the AIREA RIICs to be die singulated using an etch process and a traditional wafer sawing approach. This gave some flexibility if the die singulation process needed to be changed later on.

Table 10.1: RIIC die count for shared HDILED/AIREA RIIC wafer.

RIIC Design	Aug. Stitch Wafer # Die	Sep. Stitch Wafer	Oct. Stitch Wafer
HDILED 2K x 2K RIICs	2	2	2
AIREA 1K x 2K RIICs	2	4	6
AIREA 1K x 1K	2	4	6

Figure 10.40: Plot of the shared HDILED/AIREA wafer stitch. The two AIREA 1Kx1K RIICs on the left edge of the wafer are not usable because their corners extend past wafer edge.

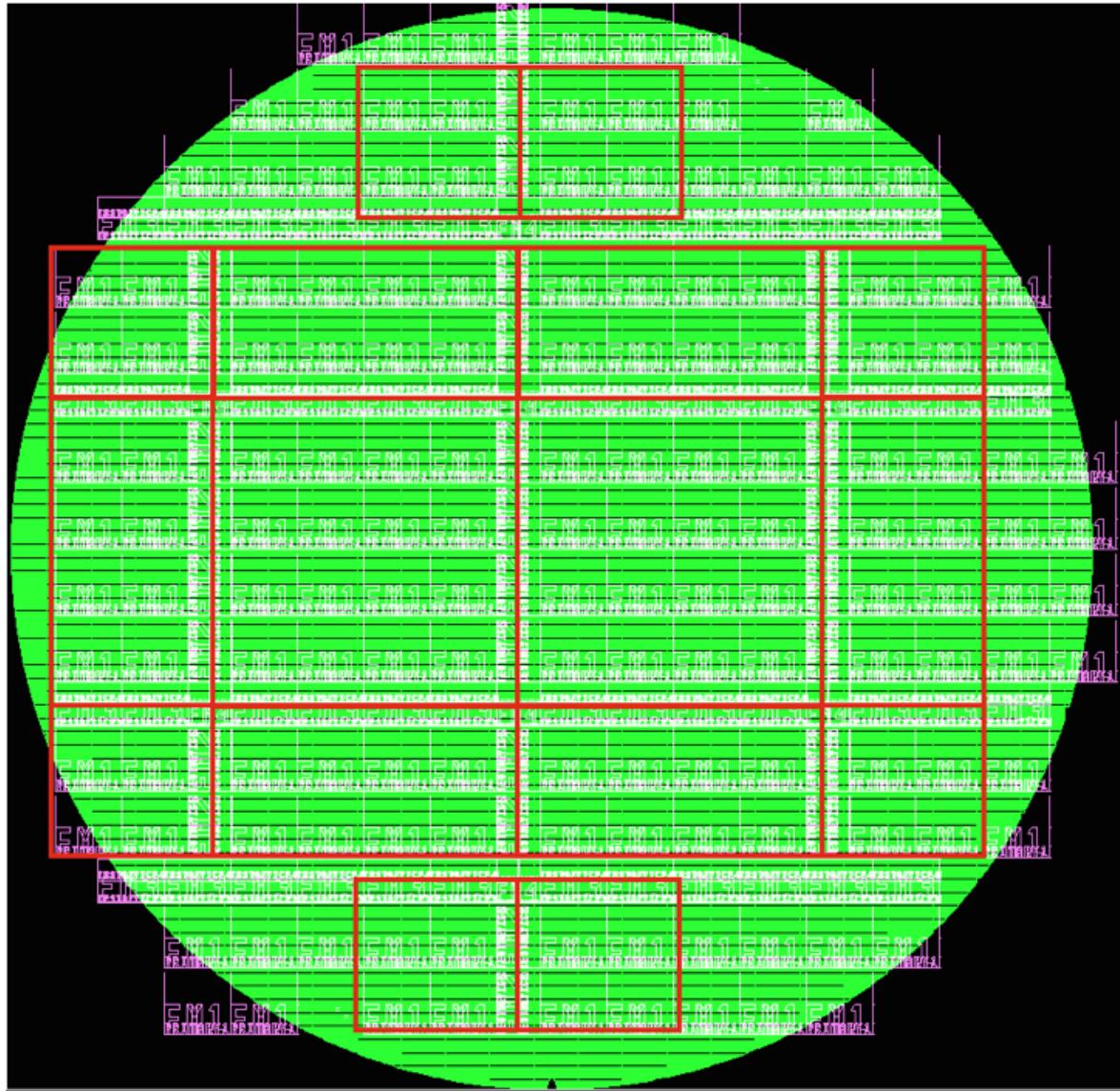
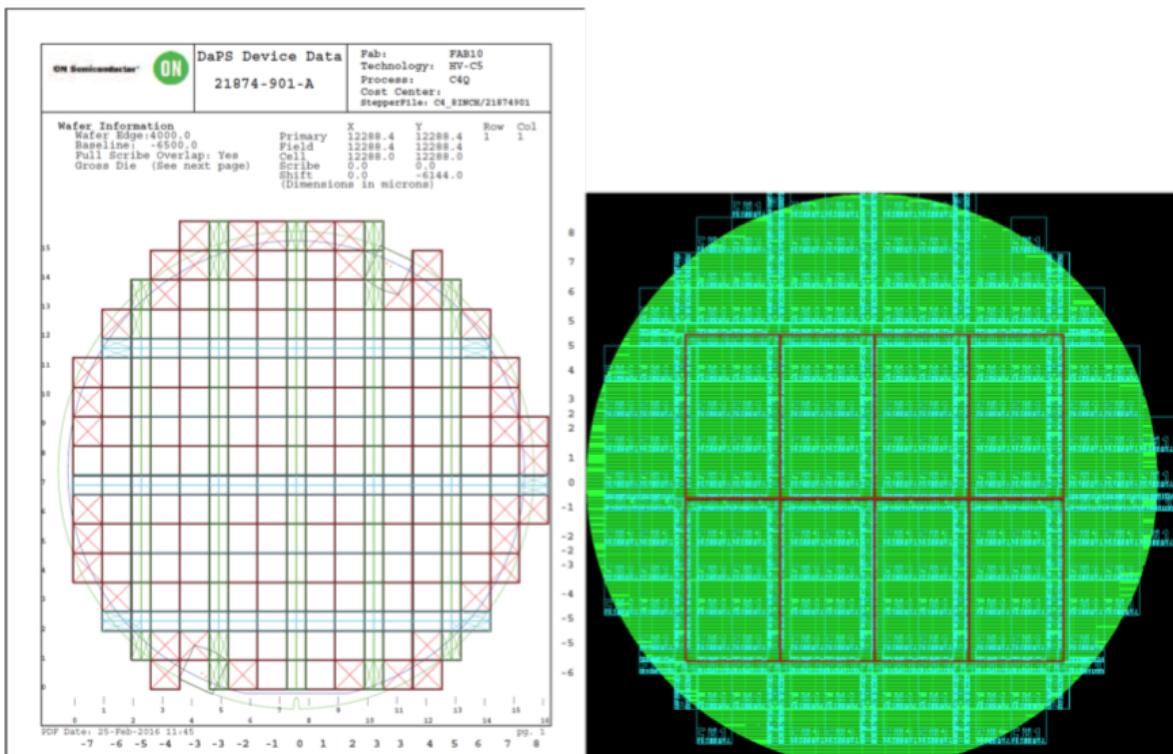


Figure 10.41: AIREA Final CMOS wafer design.



10.2.5 Die Stitch Design.

Die stitch design is the method used to make a die that is larger than the maximum size of the reticles that are used in the lithography process at the CMOS foundry. Die stitching is complicated because it is mostly a manual process. A diagram of a reticle mask and how it is used to create a larger die is shown in Figure 10.42. The reticle has all of the pieces necessary to make a complete die, but they are not in an arrangement that will yield a useable RIIC. The different pieces of the reticle are masked out and selectively exposed by the lithographic stepper. This can create a design as large as is desired on the eight-inch CMOS wafer as long as the different Primary 1 pieces are designed appropriately to be tiled.

Appropriate design of the Primary 1 pieces is tricky because the edges of the pieces will touch and short together. A scheme that allows the signals meant for the correct Primary 1 piece to be routed only to that Primary 1 piece (we refer to the Primary 1 piece as cores in other documents) must be employed. For a 2x2 array of Primary 1 pieces this involves changing to metal 2 from metal 1 at one of the edges so that signals can be routed on metal 2 and not short to the metal 1 signals of the next Primary 1 piece. For AIREA and HD-ILEDs cut pieces have to be used to isolate the signals from each of the tiled Primary 1 pieces. These are special pieces created by the foundry that do not let metal to be filled in an area. They are outside of the normal design flow and must be checked manually for design rule violations. An example of an error found is shown in Figure 10.43. The yellowed vias were half inside of the cut piece space and had to be moved down to avoid being ruined during the fabrication process. The completed design showing the cores and cut pieces is shown in Figure 10.43. This design also avoided the claw marks

Also there were some hard limitations due to the claws that hold the wafer during the processing at ON-SEMI. The indent from the claws can be seen in Figure 10.44 below.

Figure 10.42: Die Stitch Process.

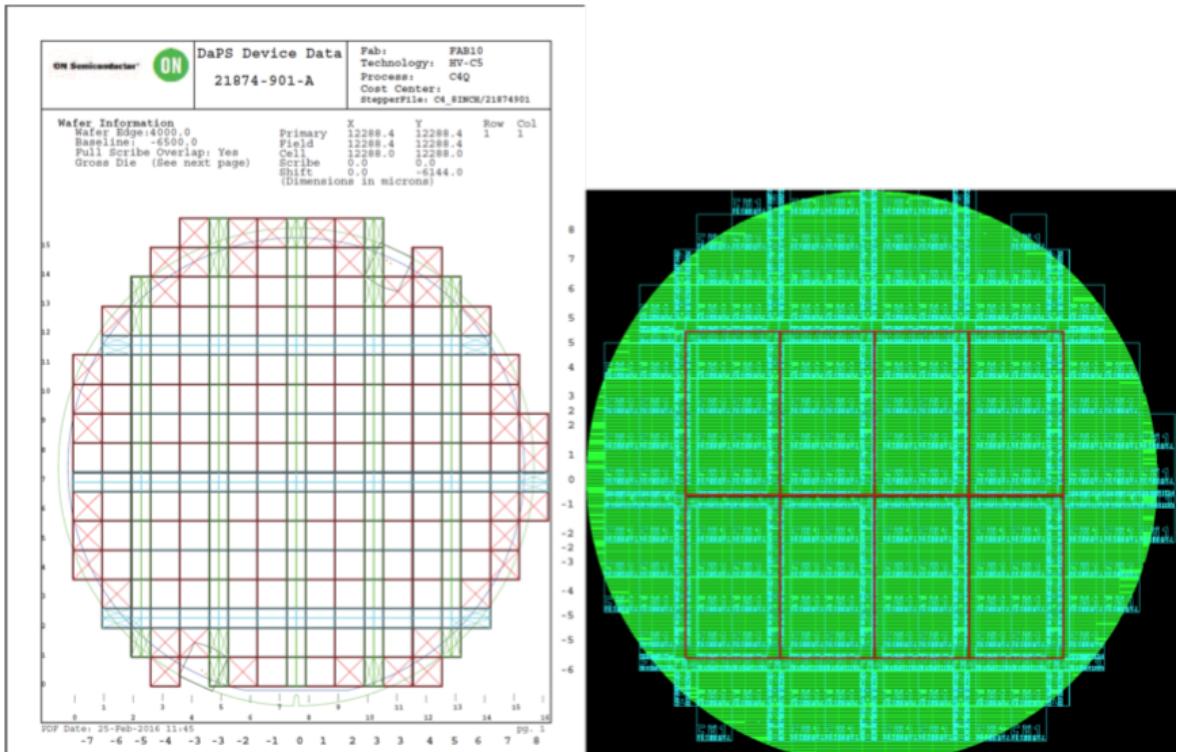


Figure 10.43: Cut Piece Error Example.

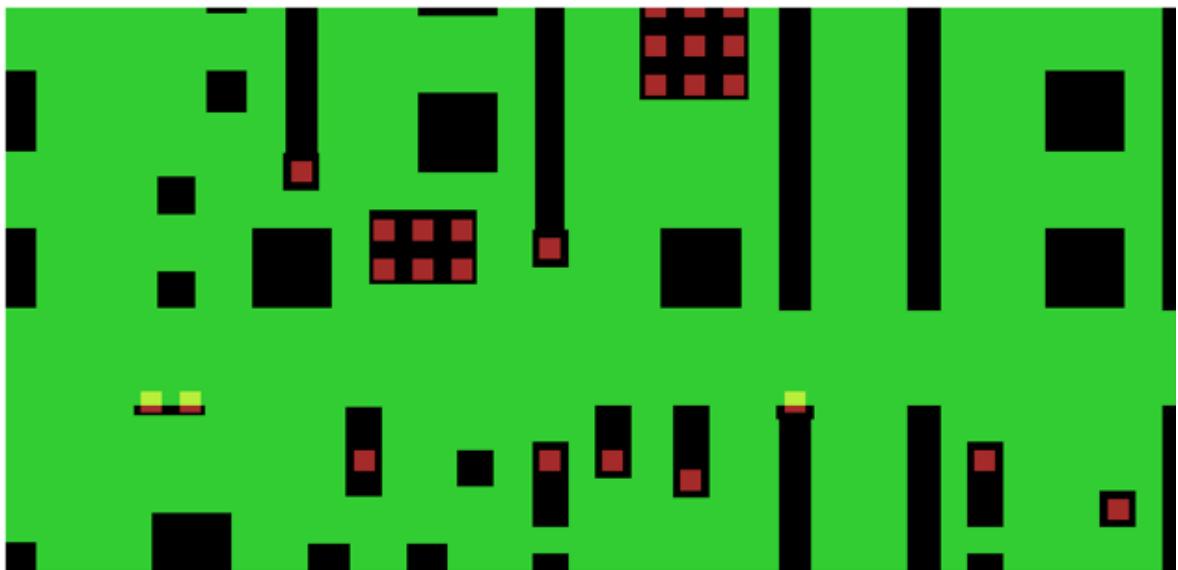
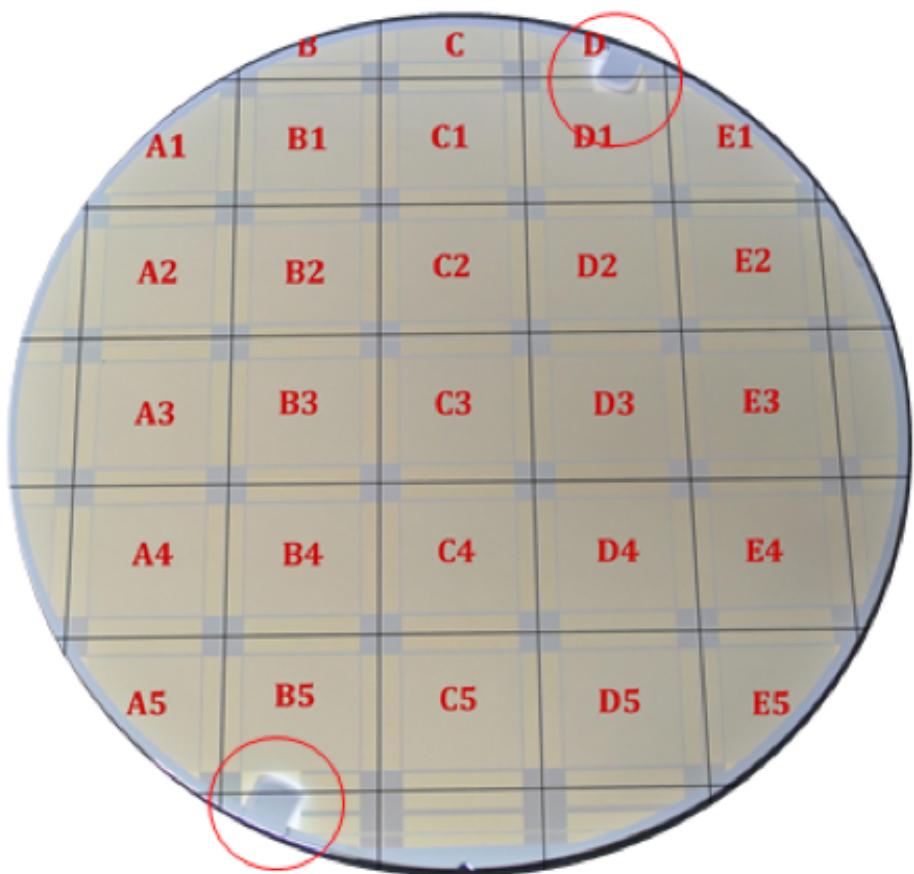


Figure 10.44: The wafer holder "claw" marks are circled in red.



10.2.6 Wafer Testing

All four AIREA wafers were tested. The tests involved choosing a random sampling of 10% of the pixels in the array and measuring the current vs voltage curves of these pixels. The wafers were graded based on the number of dead pixels (those that had no response to an applied voltage), the variance of pixel values, and power rail shorting. To visualize what a bad pixel curve is several plots were generated. The first plot shown in Figure 10.45 has a green area, a grey area, and a number of black lines. The grey area represents the area where 80% of the pixel curves lie. The green area is the outer bounds of pixel curves that have the correct shape. These two plots together give a good visualization of the variance in the pixel curves. If the pixel curve points are very far away from the median curve then they are labelled as bad curves. These are shown as black lines in the plot. The next plot in Figure 48 shows the physical location of the bad pixels. It also shows the random sample of pixels chosen for testing. The yellow pixels are the bad pixels and the green are the good pixels. Blue pixels are untested.

From the four wafers the two best dice were D2 on wafer 3, and A1 on wafer 1. Wafer 1 proved to be the best wafer of the bunch and had decent yield and good looking curves without a lot of variance. The individual yield maps are included in the Appendix later on. It should be noted that the wafer map for wafer number 4 is not included because all RIICs had shorted power rails on it.

Figure 10.45: Bad pixel curves and good pixel curves overlaid on a plot.

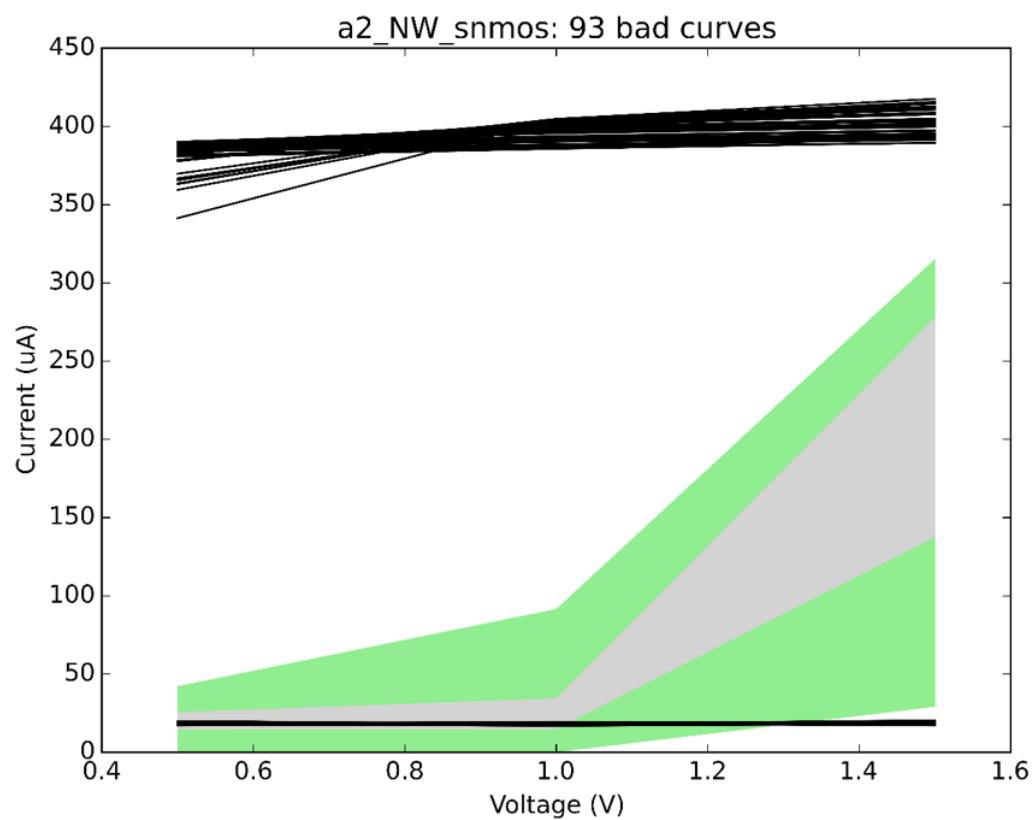
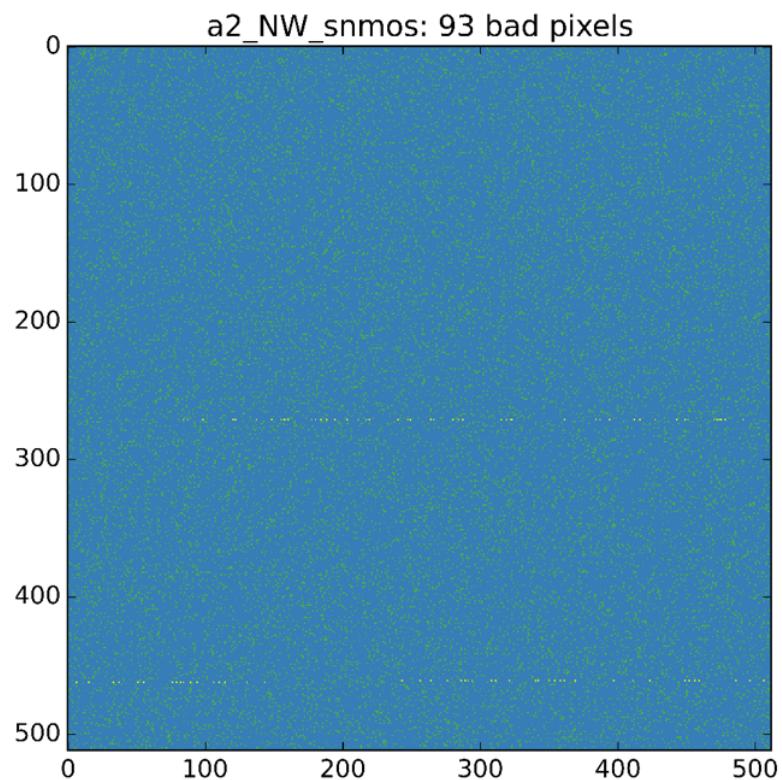


Figure 10.46: Physical location of bad pixels shown in yellow. Tested pixels shown in green. Untested pixels shown in blue.



10.2.7 Silicon RIIC Wafer Etch Die Singulation Overview

Initially, there was some trouble designing the etch die singulation for the RIIC wafers because the RIIC wafers are 8 inch diameter wafers and would not fit in Teledynes machines. It was determined that this situation could be remedied by cutting the RIIC wafer into pieces. This was an exciting new development because processing non-standard sized wafers is a challenging process.

The first part of the RIIC process was to process the Silicon wafer for hybridization. This involved thinning the 8 inch Silicon wafer to 250 microns at Corwil. Then Molybdenum-Nitride was applied to the back of the Silicon wafer for increased indium adhesion. Next, the indium bumps were fabricated on the front of the Silicon wafer. These indium bumps were used to hybridize the SLEDs and the RIIC together. The process then became non-standard.

In Figure 10.47 below there is a diagram showing the Silicon wafer with the RIIC dice on it and six red lines that indicate where a dicing saw was used to cut the wafer. Along the edges that have been labelled etch edge a 60 um wide stripe was opened in the wafer for plasma etching. A cross-sectional view of the area to be etched is shown in Figure 10.48 below. The etch has to be done in two steps to go through the entire wafer. The first step is to etch through the 11.1 um of TEOS oxide. This will be done by using a photoresist pattern. The second step is to plasma etch through the bulk silicon of the wafer. This will use the edges of the TEOS oxide as the mask instead of a photoresist mask. Figure 10.49 shows two different etch steps.

There was some complications aligning the photolithography machine to the RIIC wafer because the alignment marks had to be removed for the AIREA wafer in order to have an etch lane that did not have any metal in it. The alignment was done manually. This method however does typically yield a less precise etch than the automatic machine. In this application this isn't as important because we're not interested in nanometers of precision.

Figure 10.47: AIREA Silicon wafer dicing cuts and etch window.

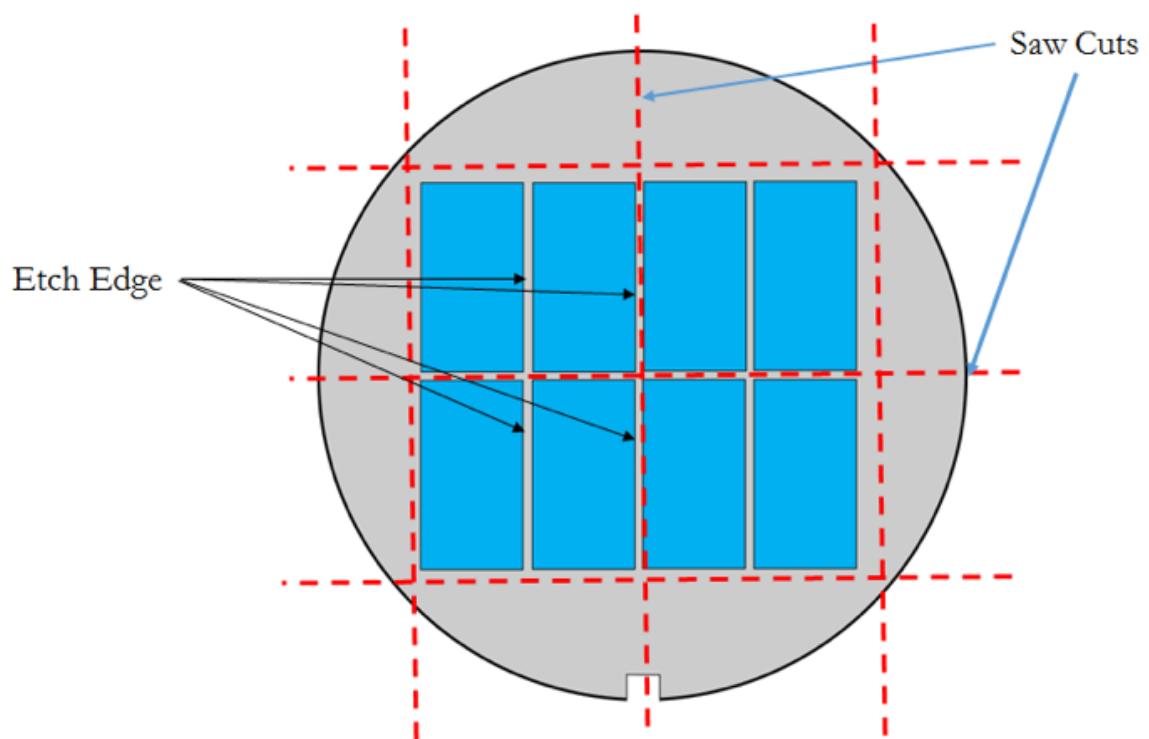


Figure 10.48: Cross-section view of Silicon wafer and the region to be etched.

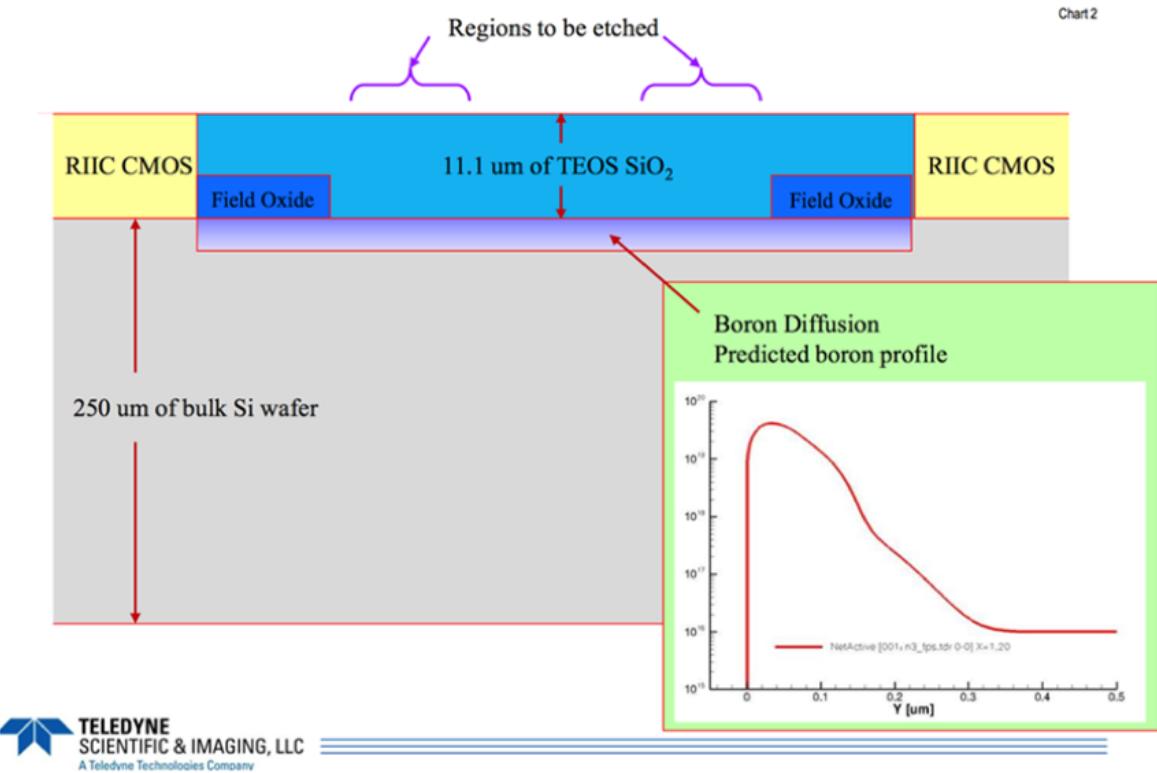
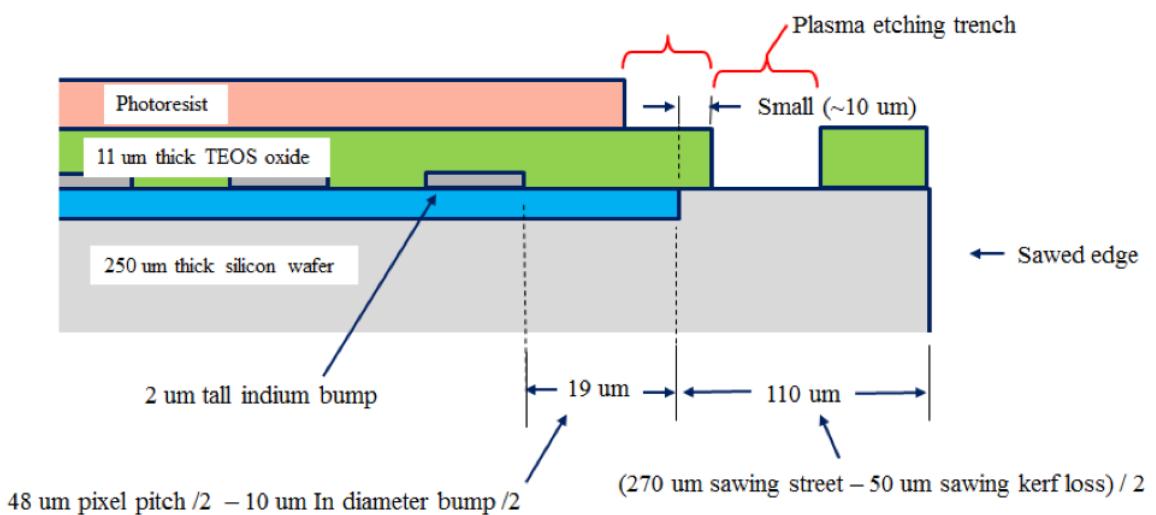


Figure 10.49: Cross-section view of Silicon wafer and the region to be etched.



10.2.8 SLED Wafer and Abutted Hybridization Overview

The SLEDs wafer had 10 um tall indium bumps fabricated on the anode and cathode pads of the SLEDs. The wafer was then shipped back to the University of Iowa. At Iowa a 50 um deep trench was etched into the center of the SLEDs wafer. This step is shown in Figure 10.24 below. The wafer was then shipped back to Teledyne. The RIIC die and the SLEDs die will then be hybridized yielding a hybrid that will look like the drawing in Figure 10.51. In Figure 10.51 a dashed line indicates where a facing cut with a fly cutter will be done. The facing cut will expose the etched trench in the SLEDs wafer and the smooth vertical etched sidewall. It should be noted that the SLEDs die are still connected until the facing cut is performed. It was thought it would be easier to hybridize both RIICs to the SLED wafer prior to separating the SLED dice.

Figure 10.50: 50 um etched trench in the center of the SLEDs array.

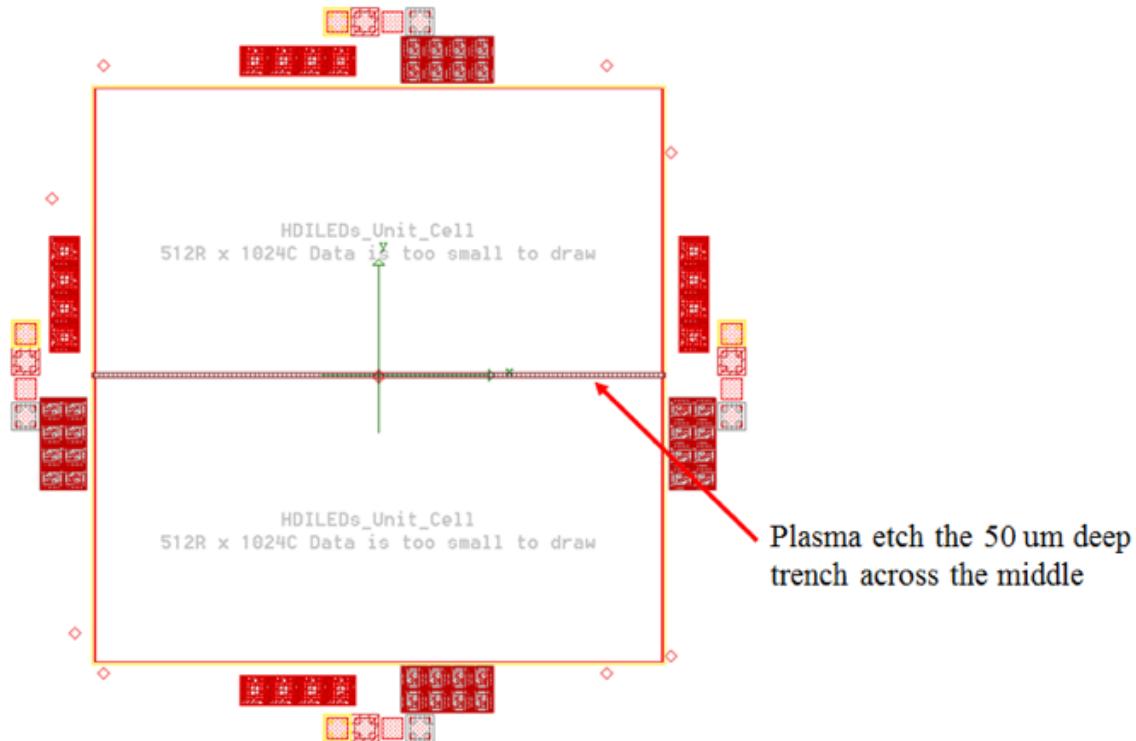
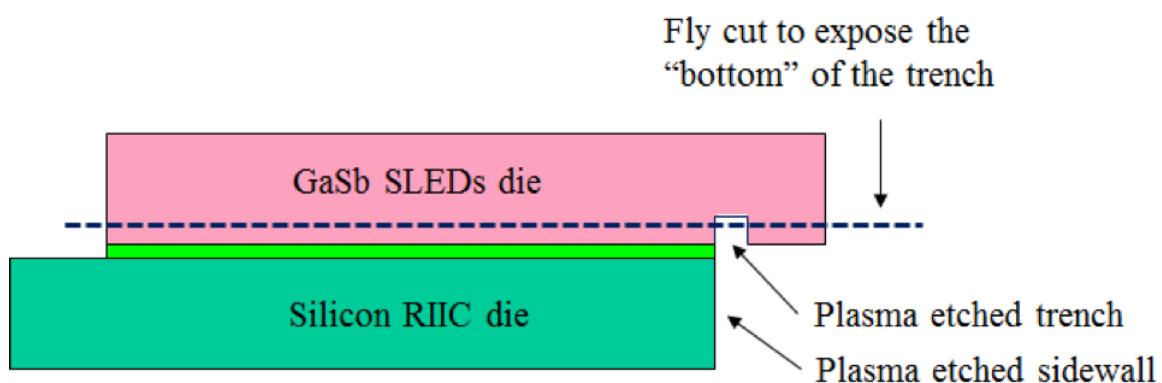


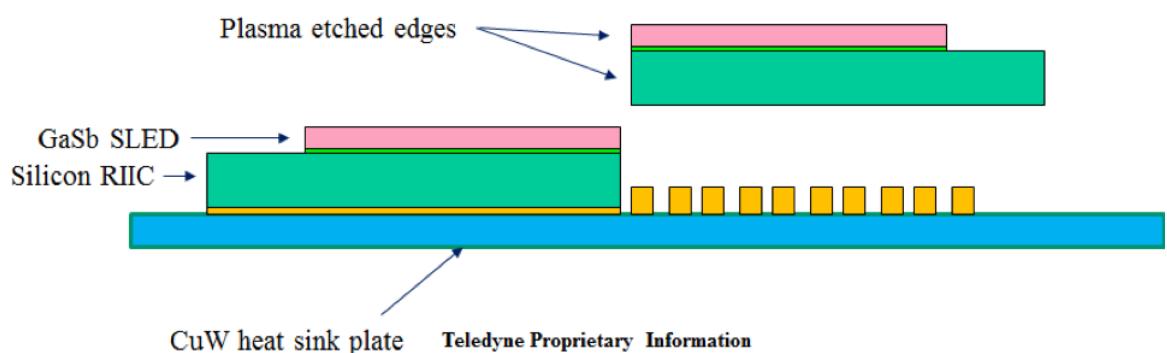
Figure 10.51: Hybrid without vertical sidewall exposed.



10.2.9 Final Assembly

The final assembly of the hybrids will be done with the hybridization machine onto a copper-tungsten heat sink plate. This step is shown in Figure 10.52 below.

Figure 10.52: Assembled AIREA hybrids.



10.2.10 AIREA Etch Die Singulation Design

The RIIC design had to be setup properly to facilitate an etch die singulation. To do this an area devoid of metal fill layers had to be added along the side of the AIREA RIIC to facilitate etching through the silicon substrate. The trench area is 100 microns wide and filled with the DIF layer in the On-Semi C5N process. This layer is used to dope the silicon p substrate for transistor placement. By including this layer the metal fill layers that would normally be deposited during the wafer processing are removed. The area in the trench is composed of Boron doped Silicon and TEOS oxide. A diagram showing a cross-section view of the region to be etched is shown in Figure 10.53.

The etch die singulation process developed during the AERIA program involved TSI plasma etching the TEOS oxide on the 8 CMOS wafer to form a 20 micron wide stripe around the RIIC die. The 20 micron stripe was to be inside of the 60 micron red stripe shown in Figure 10.53. In Figure 10.53 a side view of the area to be etched is shown. The TSI plasma etch was to expose the boron doped top surface of the silicon substrate. This step is shown in Figure 10.53. The photoresist was then to be stripped, and new photoresist was to be applied and patterned, such that the photoresist stops on top of the TEOS oxide, near the edge of the stripe. The TEOS oxide would have defined the edge of the silicon plasma etch. This second photoresist layer was used to cover the indium bumps on the top surface of the CMOS, to protect the indium bumps during the silicon substrate etch.

Figure 10.53: The side view of the region to be plasma etched by TSI.

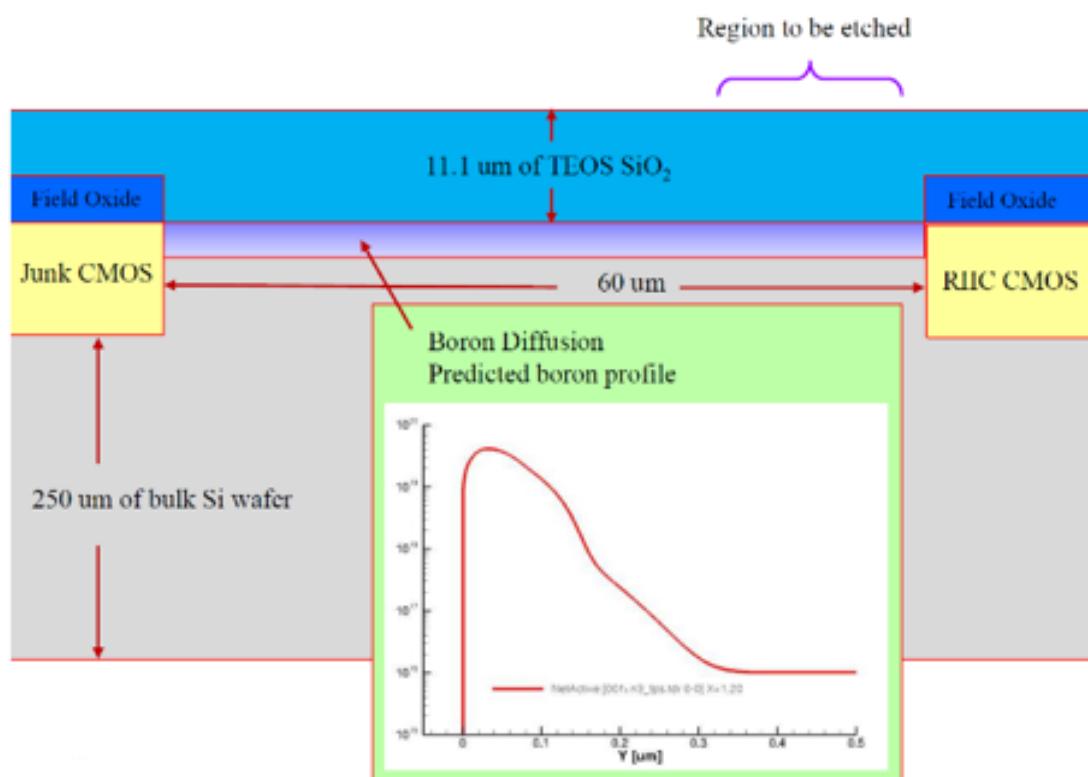


Figure 10.54: The AIREA RIIC wafer after TSI has plasma etched through the TEOS layer and deposited the positive photoresist. Teledyne patterns the photoresist, and plasma etches the TEOS oxide.

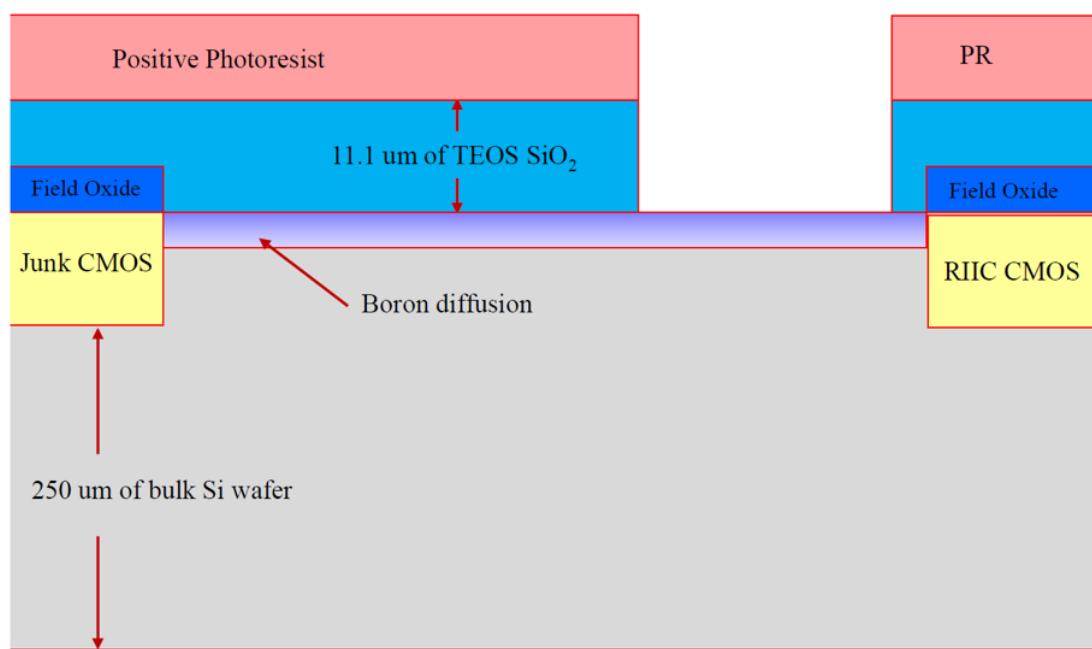
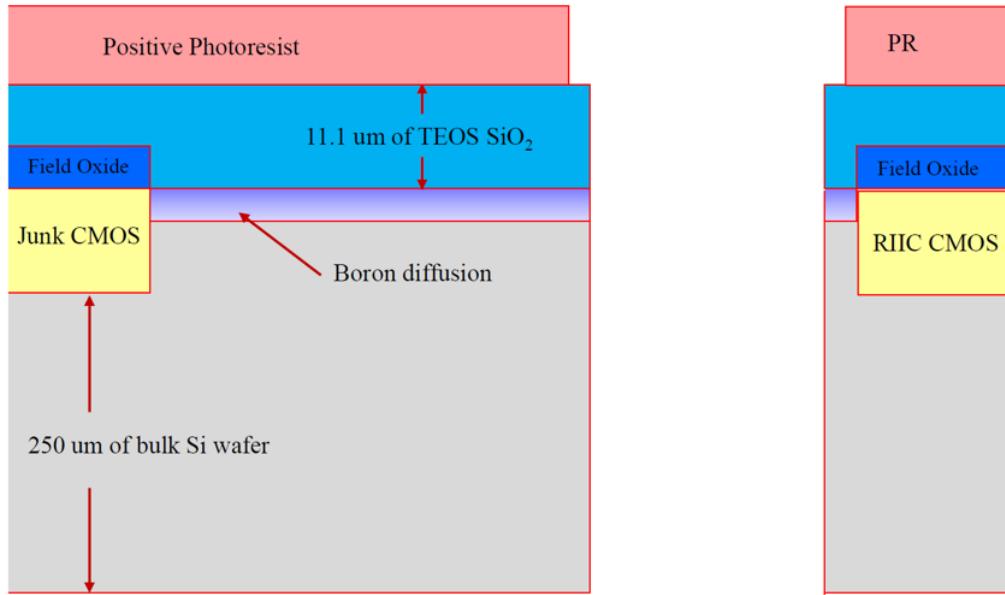


Figure 10.55: The AIREA RIIC wafer after die singulation.

Teledyne patterns the new photoresist (Covers all the CMOS), and puts the edge of the PR on top of the TEOS oxide. The edge of the TEOS oxide is used to mask the Bosch etch (Better selectivity).



10.2.11 TEOS Oxide Etch Experimental Results

Experiments were conducted at Teledyne to develop the silicon etching process to etch through the RIIC substrate. The first part of the etch process that needed to be tested was the TEOS oxide etch. This is because the TEOS oxide is on top and must be removed before the bare Silicon underneath can be exposed.

The test was conducted by first depositing 11.1 um of PECVD Silicon Oxynitride on to a Silicon test wafer. The AIREA RIIC wafers will have 11.1um of TEOS oxide instead of the PECVD oxide used in this experiment. However, both oxides are comparable and use the same etch chemistry. It was easier to deposit PECVD oxide for a test. Figures 10.56, 10.57, and 10.58 show the results of the etch. A good etch selectivity and isotropy were achieved in this test. Further tests were conducted to improve the process.

Figure 10.56: First etched sidewalls.

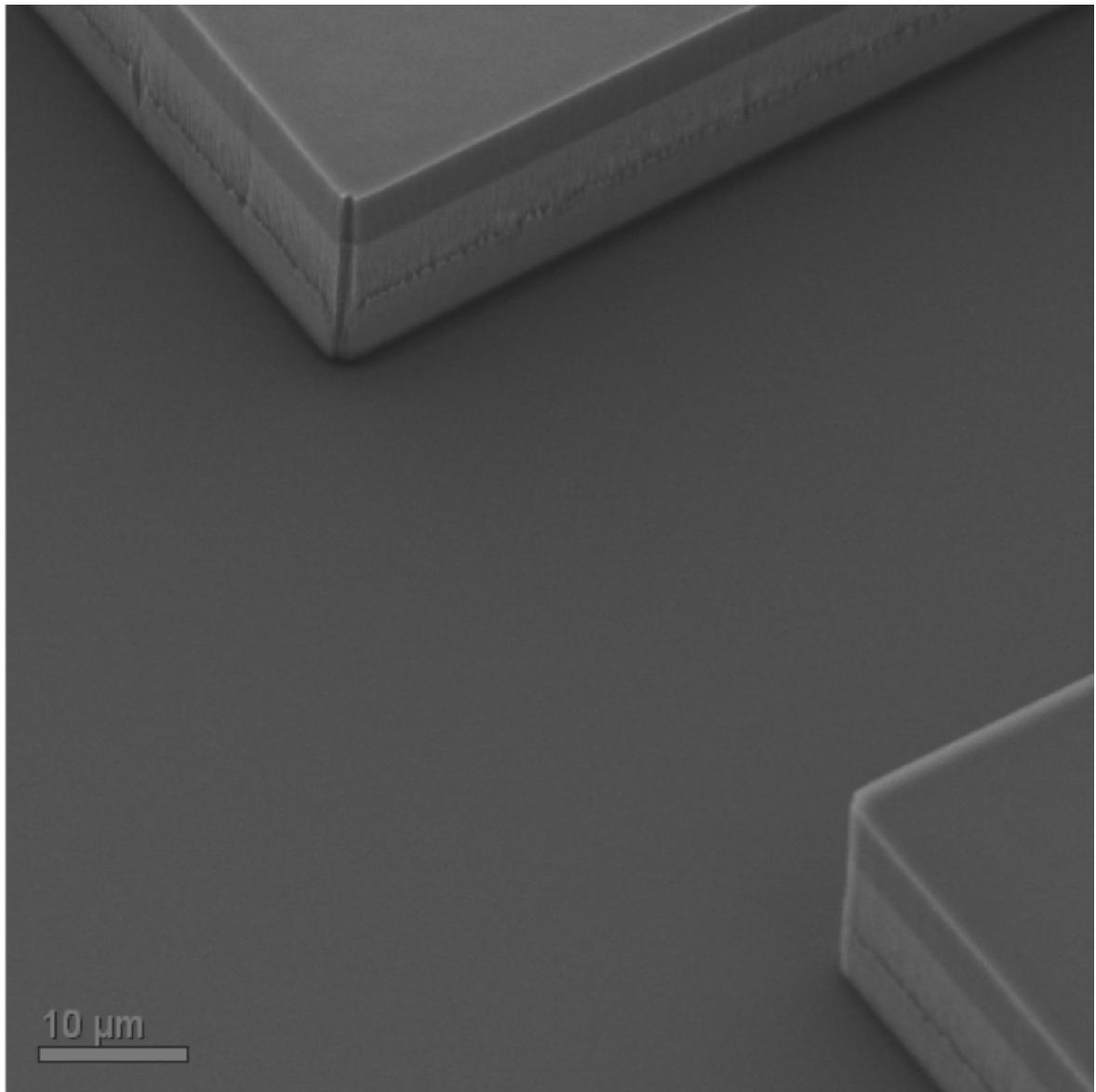


Figure 10.57: A second attempt with improved results.

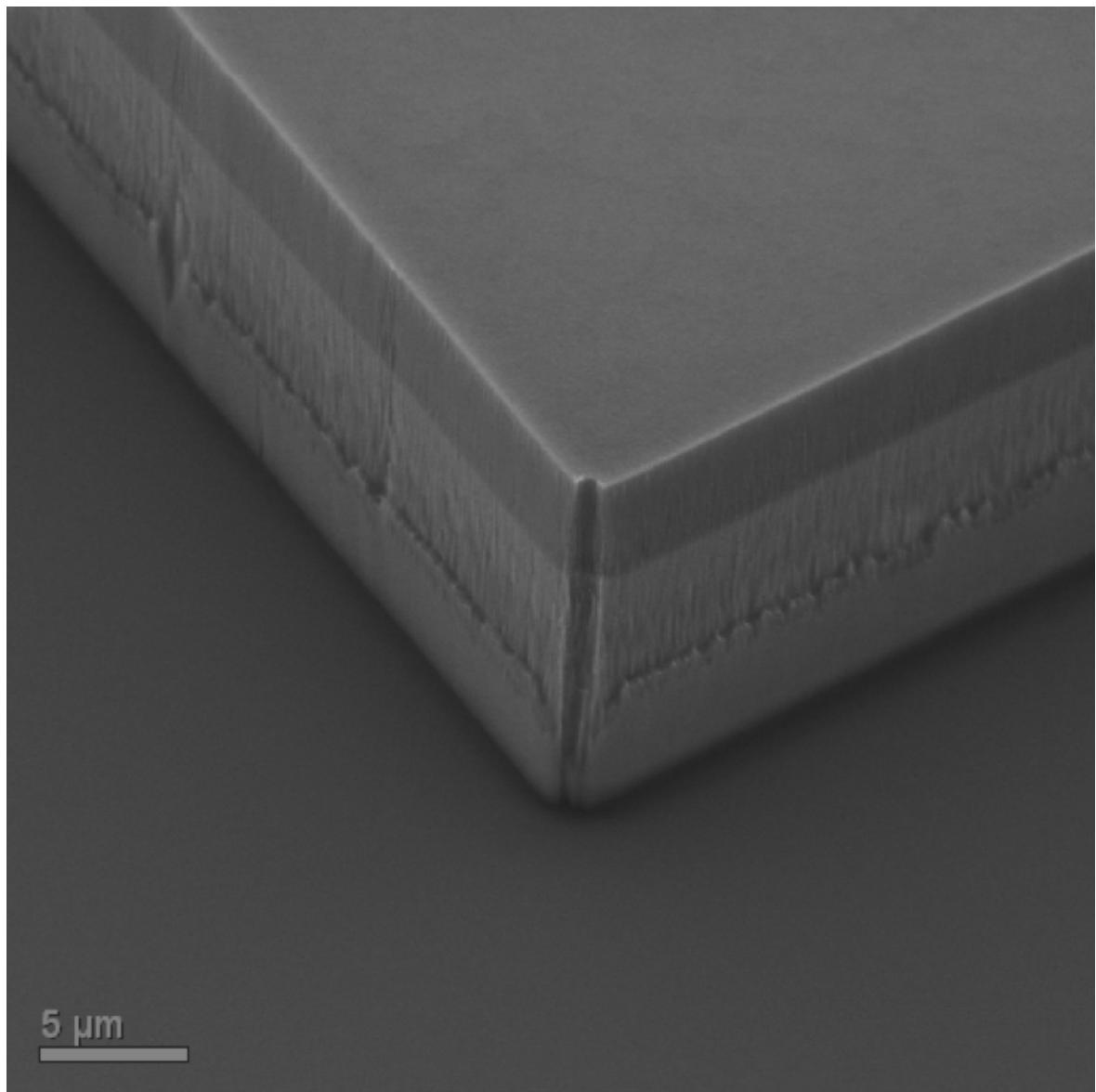
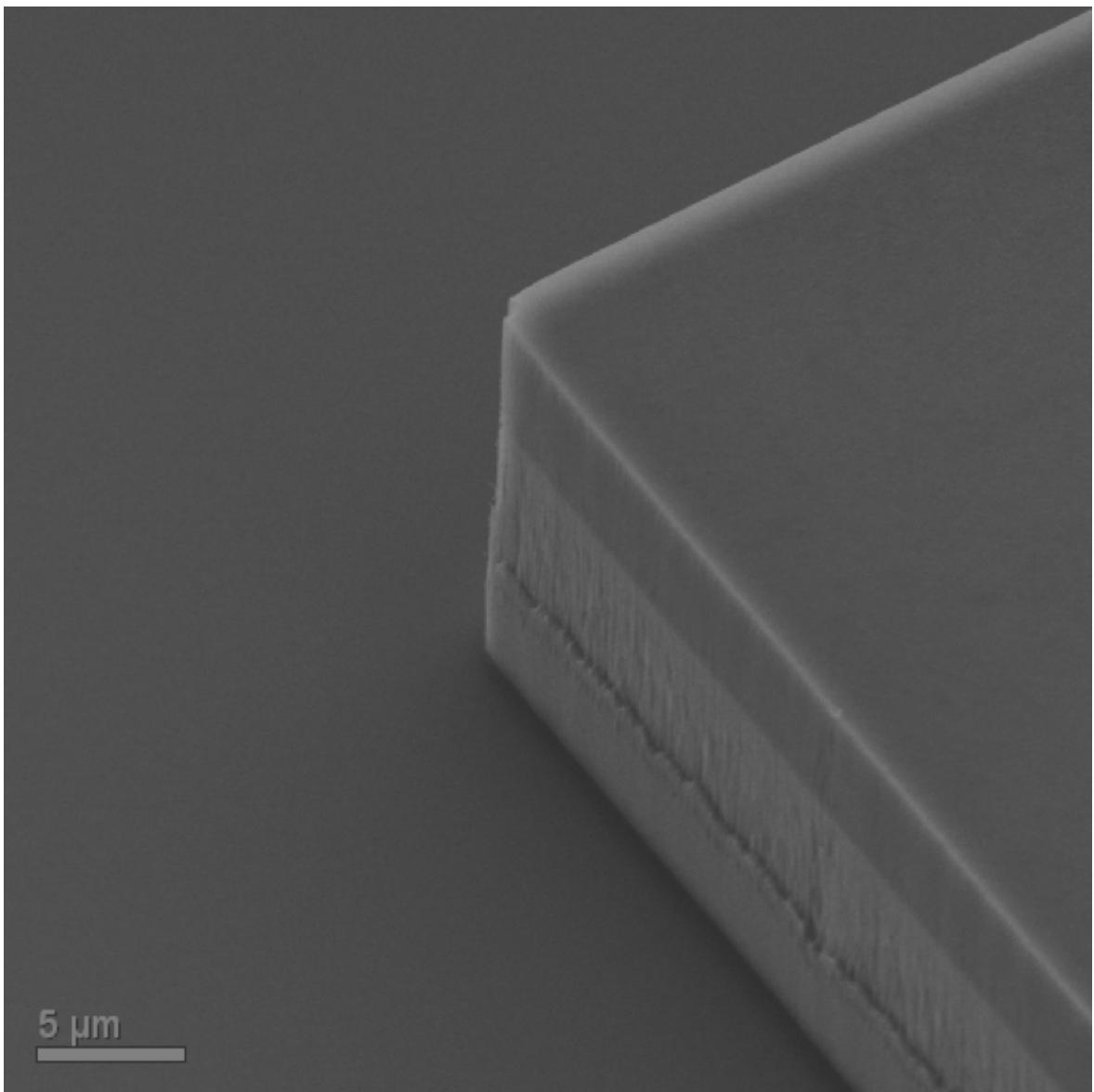


Figure 10.58: A view of the other edge in the second attempt.

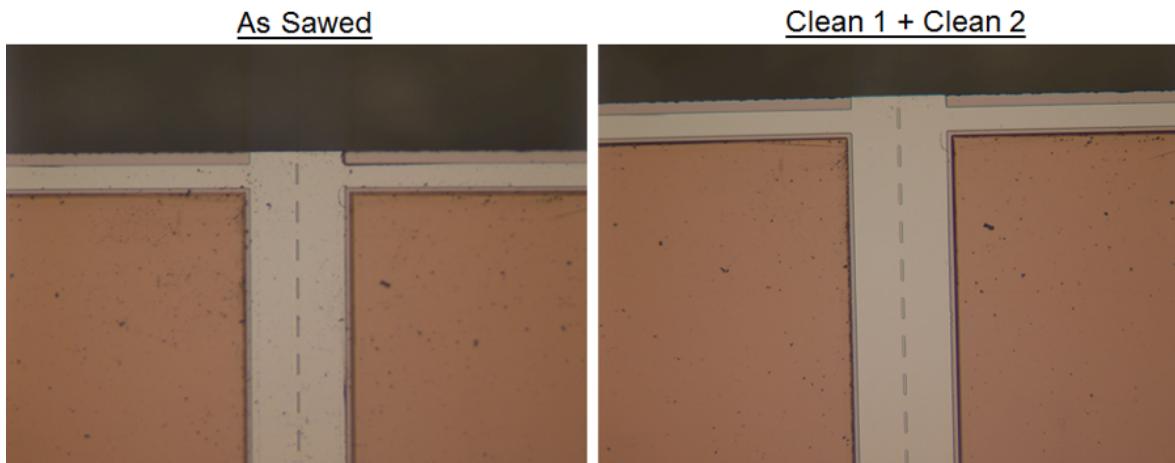


10.2.12 TEOS Oxide Etch and Through Substrate Etch Test Wafer Results

Test wafers with the PECVD oxide were used to test the through substrate etch in addition to the TEOS oxide etch. The results of this test were very promising. The Figure below shows the difference between an edge that has been diced with a dicing saw and the same edge after the through substrate etch was performed to create an even more vertical and smooth edge.

Figure 10.59: Comparison between sawn edge and etched edge.

Post Saw Cleaning, Detail Interior Street (Wafer Spin L2)



10.2.13 RIIC Wafer Die Singulation Etch Complications

The RIIC wafer etch is shown in Figure XXX below. The dashed red line is the area where the through substrate etch is being performed. The purpose of this etch is to create a sidewall that is smooth and vertical enough for a successful abutment of the two hybrids. There are two etches in this process a shallow etch through the oxide layer and deep etch through the silicon substrate of the wafer. The oxide etch was completed and there were no major issues. The through substrate etch had complications arise.

There were two main complications when performing the through Silicon etch on the actual RIIC wafer. The first was the dicing saw alignment marks in the dicing lane. In Figure 10.61 the dicing saw alignment mark is shown in the middle and looks like two white triangles abutting each other or a bow-tie. In Figure 10.62 an optical and a height map of the aluminum structure after the oxide had been etched is shown. In Figure 10.63 a side-view of the etch channel is shown along with an SEM image of an oxide test piece etch. The RIICs are the white castellated structures above and below the aluminum structure. It was not anticipated to have to etch through these

dicing saw alignment marks when originally designing the RIIC wafer because it was believed to be outside of the etch area. The etch area is visible in Figure 10.61. It is the area between the edge of the RIIC (castellated white squares) and the start of the metal fill squares. This was believed to be the area to be etched. However, it was required to extend the etch into the dicing lane to meetup with the dicing saw cut and free the RIIC. This was not originally believed to be a problem because structures in the dicing lane are infrequent and it is mostly empty. In this case it was an unlucky alignment of the bow-tie structure and the desired RIICs. One long etch continuous etch along both of the RIICs also had the advantage of providing better alignment because manual alignment of the masks would not have to be repeated.

The second issue encountered are the small squares of metal. These structures are used to improve yield by increasing the metal density in the CMOS process. Figure 10.61 uses green areas to highlight these metal squares. The TEOS oxide was removed from the top of these metal fill structures and thus they would be exposed to the inside of etching machine. While the etch could have been performed it may have caused the aluminum from the squares to sputter into the etching machine and damage the machine and also possibly sputter onto the RIIC. It was suggested that these structures could be covered with photoresist which would protect the etching machine and the RIIC from the sputtered aluminum. In the future, these would not be uncovered prior to the through silicon etch and the etching lane next to the RIIC would be widened to make the through silicon etch easier. Given the expense of processing a different wafer it was not possible to use one of the other wafers that had not had the TEOS oxide.

Several methods were tried to remove the bow-tie structures.

Figure 10.60: RIIC wafer etch for AIREA hybrids.

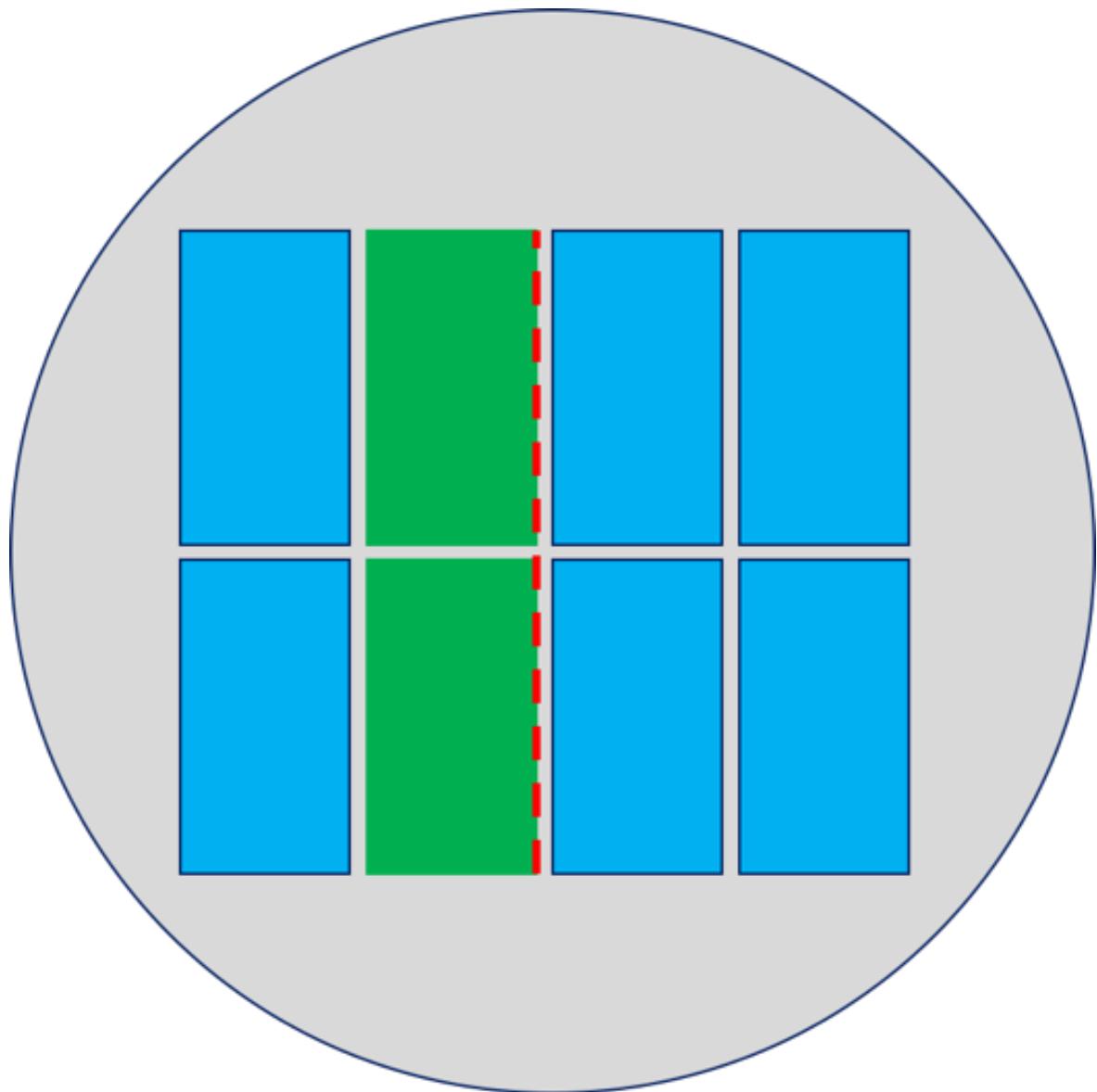


Figure 10.61: Aluminum stress relief structure.

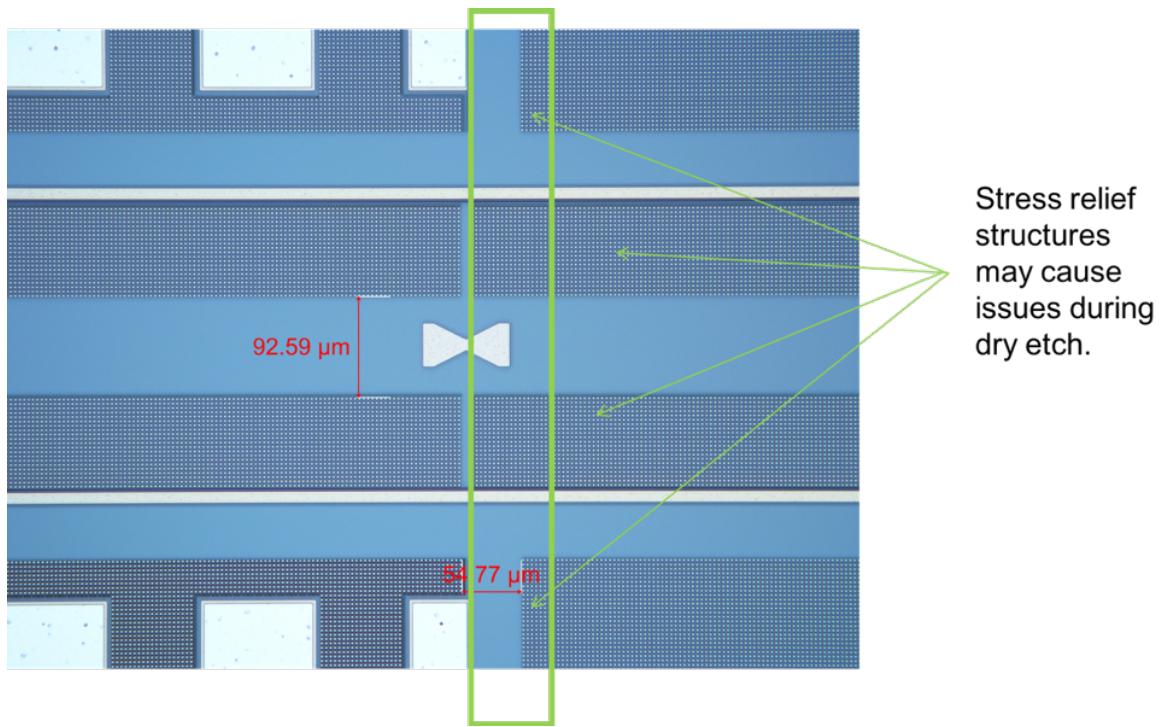


Figure 10.62: Overhead view of the aluminum test structure and height profile.

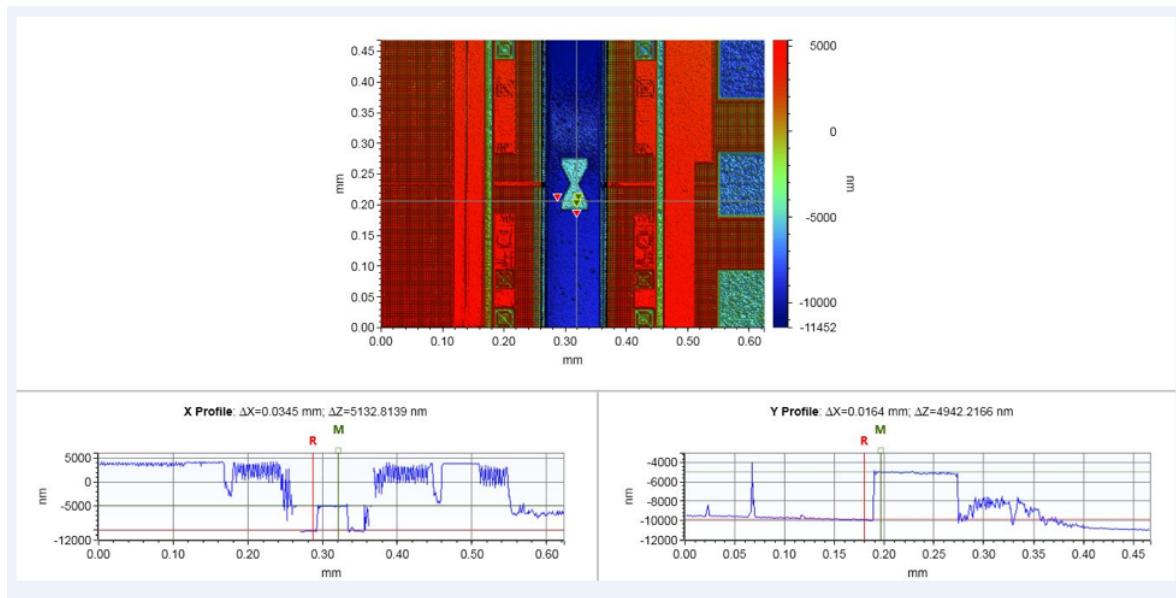
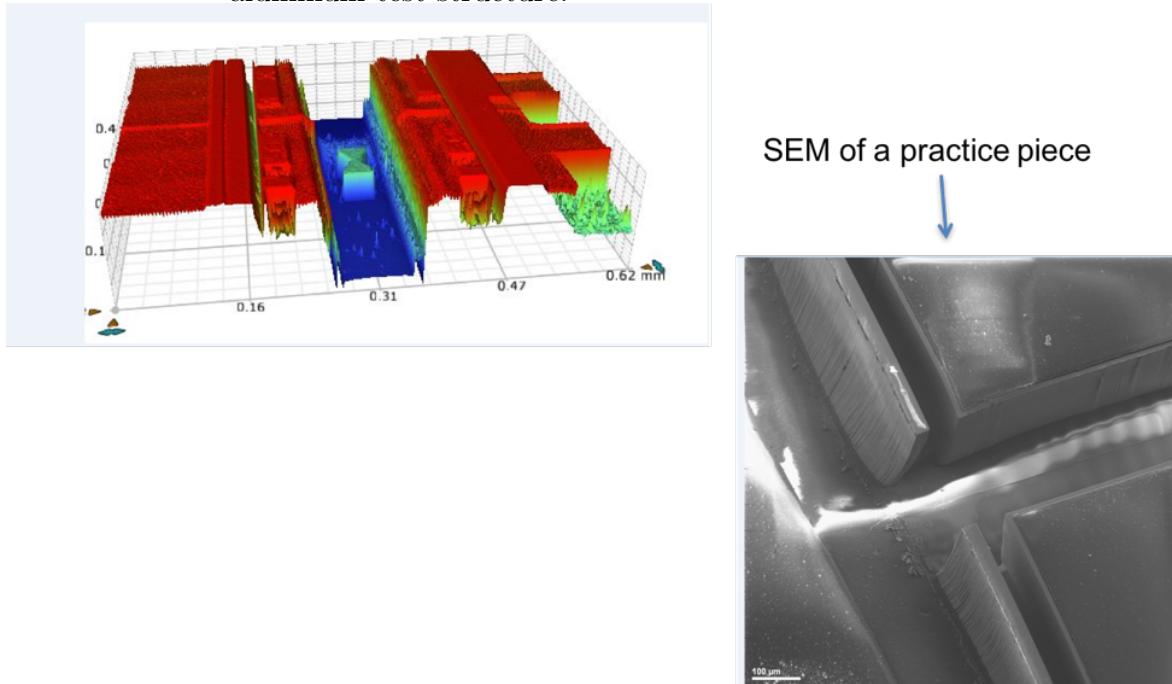


Figure 10.63: SEM image of a test piece and a side view of the height profile for the aluminum test structure.



10.2.14 RIIC Wafer Die Singulation Etch Attempted Solutions

It was attempted to remove both the bow-tie dicing saw alignment marks and the small metal fill squares with several types of etches. First a Reactive Ion Etch with Chlorine / Argon and SF₆ / Argon was attempted with the following settings:

- Power: 160 W
- CHF₃: 30sccm
- O₂: 3sccm
- Pressure: 30mTorr

This method proved to be unsuccessful at removing the structures. Next, a series of wet etches were attempted. These etches are well known in the literature to work on Aluminum and Copper. The etches tried were:

- HCl Acid
- HCl / H₂O₂

Table 10.2: Etch Recipe

Step	1	2	3	4	5	6
MainCham_Abort_Option	2	2	2	2	2	2
Pressure	750	750	750	750	350	350
RF Upper	0	0	600	1400	0	1400
RF_Upper_RefL_Max	30	30	30	30	30	30
GAP	1.05	1.05	1.05	1.05	1.05	1.05
Ar 1000	300	300	300	300	500	500
CF4 200	150	150	150	150	120	120
CHF3 50	35	35	35	35	0	0
SF6 100	0	0	0	0	0	0
N2 100	0	0	0	0	0	0
O2 500	0	0	0	0	0	0
Gas-07	0	0	0	0	0	0
Gas-08	0	0	0	0	0	0
Gas-09	0	0	0	0	0	0
Gas-10	0	0	0	0	0	0
He-Clamp	0	12	12	12	12	12
Completion	Time	Stab	Time	Time	Stab	Time
Time	4	30	2	140	45	100

- $H_3PO_4/HNO_3/CH_3COOH$

These also proved to be unsuccessful. It was believed to be the Titanium Nitride film on the metal causing the etches to not work properly. Advice was sought from C5 etch experts at ONSEMI.

Deborah Florence suggested the following etch recipe:

This recipe included an oxide etch step (step 4) and then a TiN etch step (step 6). This is a typical recipe used to etch oxide from the top of a pad, then to remove the TiN ARC top metal from the pad to expose the aluminum. The Oxide etch is a combination argon, CF4, and CHF3. TiN etch is a combination argon and CF4. This etch is done on a plasma etcher with top split RF power.

Sheila Burtosky another C5 expert suggested the following for wet metal etching off the marks after the top oxide is removed:

Table 10.3: Etch Recipe

Step	1	2	3
Pressure	10	10	90
RF_Upper	0	510	0
RF Lower	0	265	0
GAP	5.3	5.3	5.3
Cl2-200	80	80	0
BCl3-100	40	40	0
SF6-100	0	0	0
O2-500	0	0	0
He-Clamp	10	10	0
Completion	Stab	Time	Time
Time	30	75	10

H₂O₂ mixed in with a little nitric, and phosphoric acetic acid mixture for the TiN layer. Then use a Nitric, Phosphoric, Acetic acid mixture for the bulk Aluminum. This etch works for the bulk Al because the Al is converted to Al-O and it is the Aluminum oxide that is etched away.

Sheila also recommended a standard dry etch option to try for a CMOS clad metal stack (TiN ARC 1000 Ang/AlCu 6K Ang/TiN 250 Ang/Ti 150 Ang for example). This etch is listed here:

During the process of consulting with the experts at ONSEMI it was discovered that ONSEMI has a fairly unknown process for removing the metal objects and TEOS oxide from the scribe lane for etched die singulation customers with a 5 layer metal process with planarized passivation. All masks would require rebuild to remove scribe structures, or to widen scribes to add a double saw lane (if removing scribe structures is not desired), and an additional scribe mask for final oxide removal would need to be added.

Ultimately these etches were not possible given the amount of time and expense it would have taken Teledyne to setup their etching machines properly to try these etches. It also was not clear if these etches would be successful. A less expensive and

easier solution was to dice the RIICs out with a dicing saw and hopefully remove the bow ties with the saw blade.

Fortunately, the dicing method removed all but a very small piece of a bow tie the following figures show the results of dicing around two RIICs. This produced a rectangle the had two RIICs stuck together inside of it. The two RIICs then needed to be separated.

The plan then was to cover that part of the bow-tie up with photoresist and then etch the silicon in the etching machine. The metal fill squares could also be covered with photoresist before the dice go in the Silicon etching machine. Due to the limited budget and the expensive nature of conducting experiments at Teledyne, it was decided to attempt to singulate the RIICs with a dicing method. This decision was made in consultation with our program sponsors at the Guided Weapons Evaluation Facility. It was decided that the most important goal of AIREA was to produce an abutted hybrid.

C1 Top Right and D1 Top Left

Figure 10.64: D1 Top Right Corner.

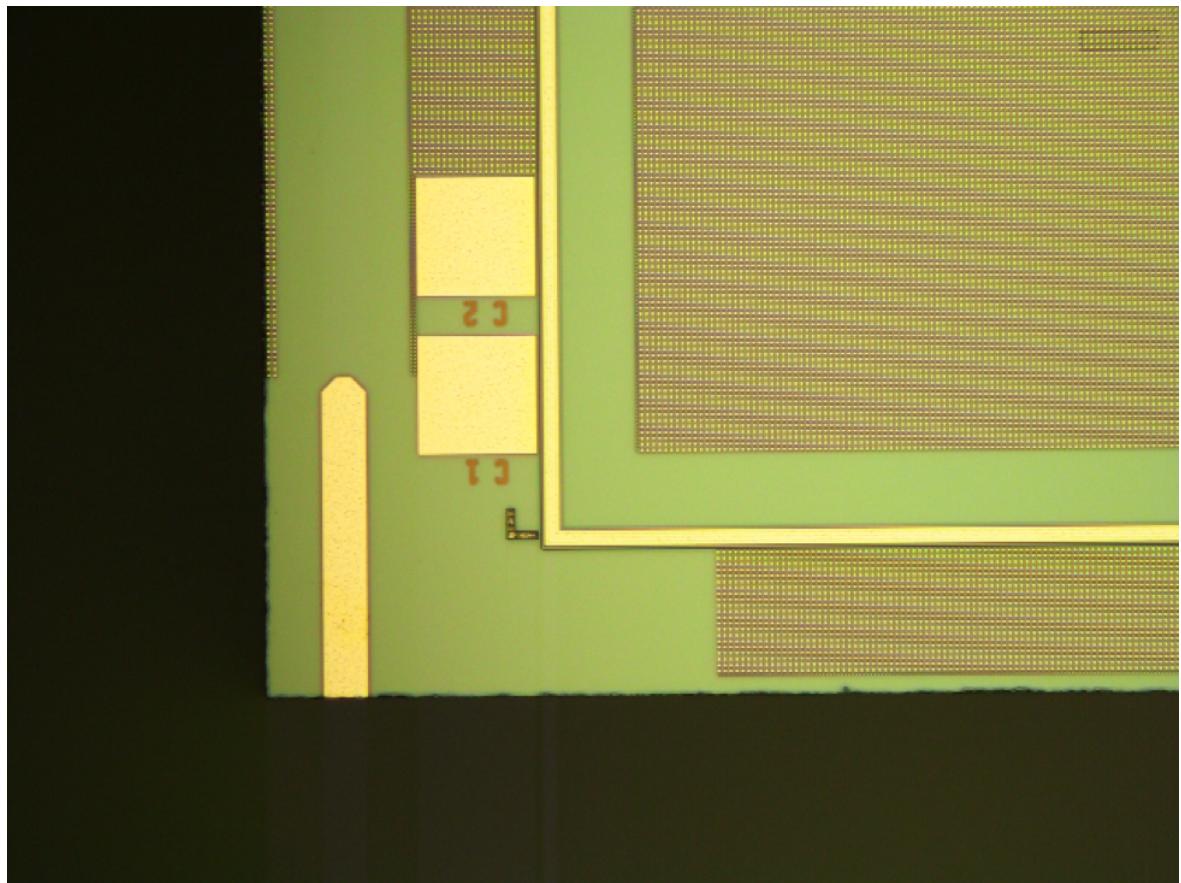


Figure 10.65: C1 Bottom Right and D1 Bottom Left.

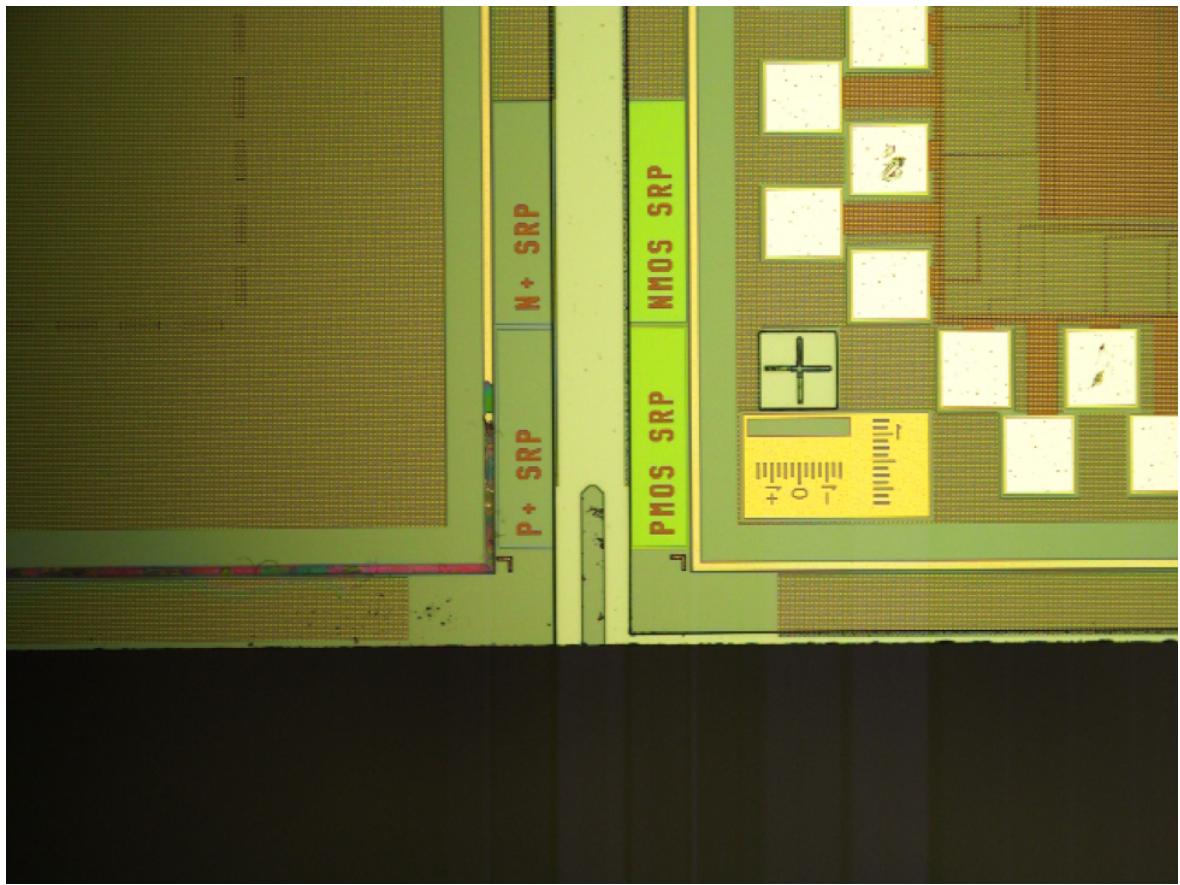
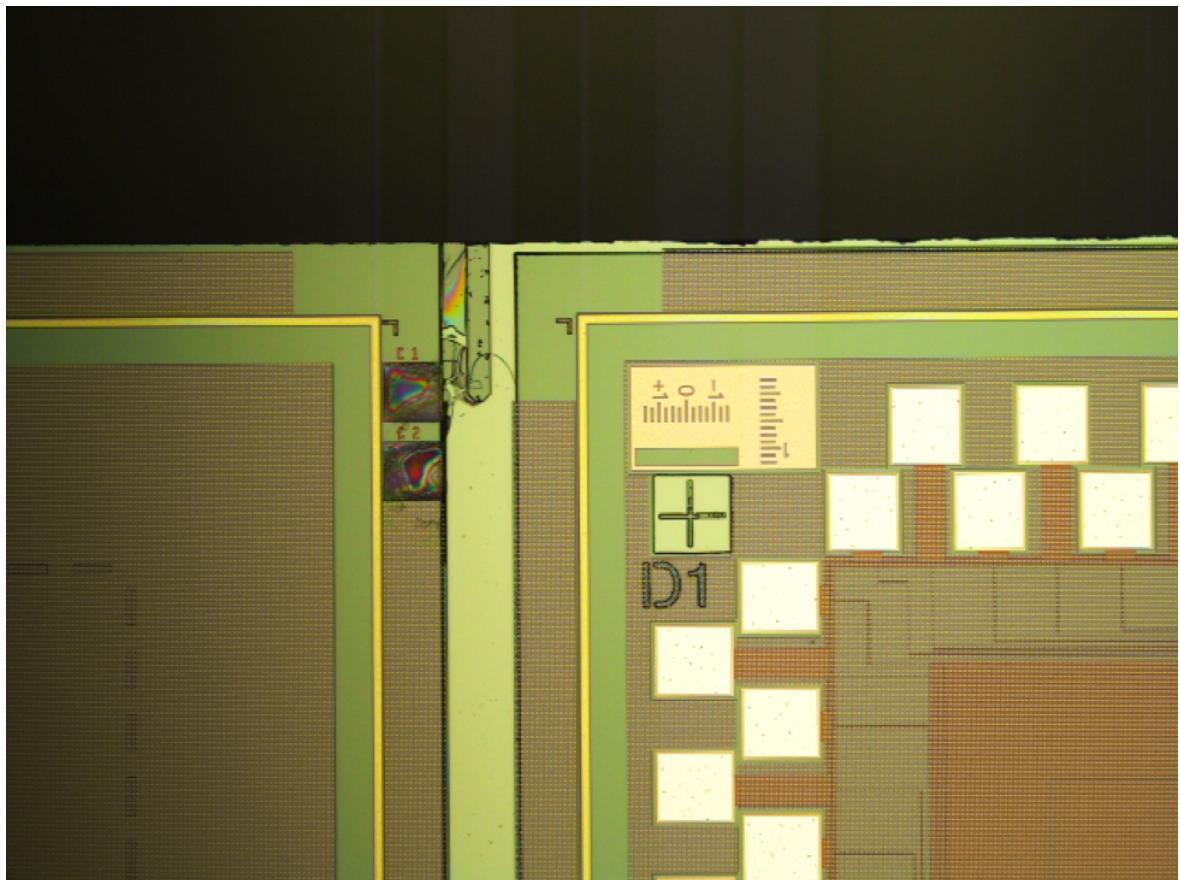


Figure 10.66: C1 Top Right and D1 Top Left.



10.2.15 RIIC Singulation: Dicing Method

Due to the expensive nature of experimenting with etching through the silicon substrate in terms of both time and money it was decided to attempt a dicing method. The dicing method appears to have created adequately smooth sidewalls. Albeit not as good as the ones the test results from the practice pieces indicated that could be expected. In the Figures below there are microscope photographs of the edges produced by dicing with the largest chip-outs measured.

Figure 10.67: Close up view of chip out produced by dicing method.

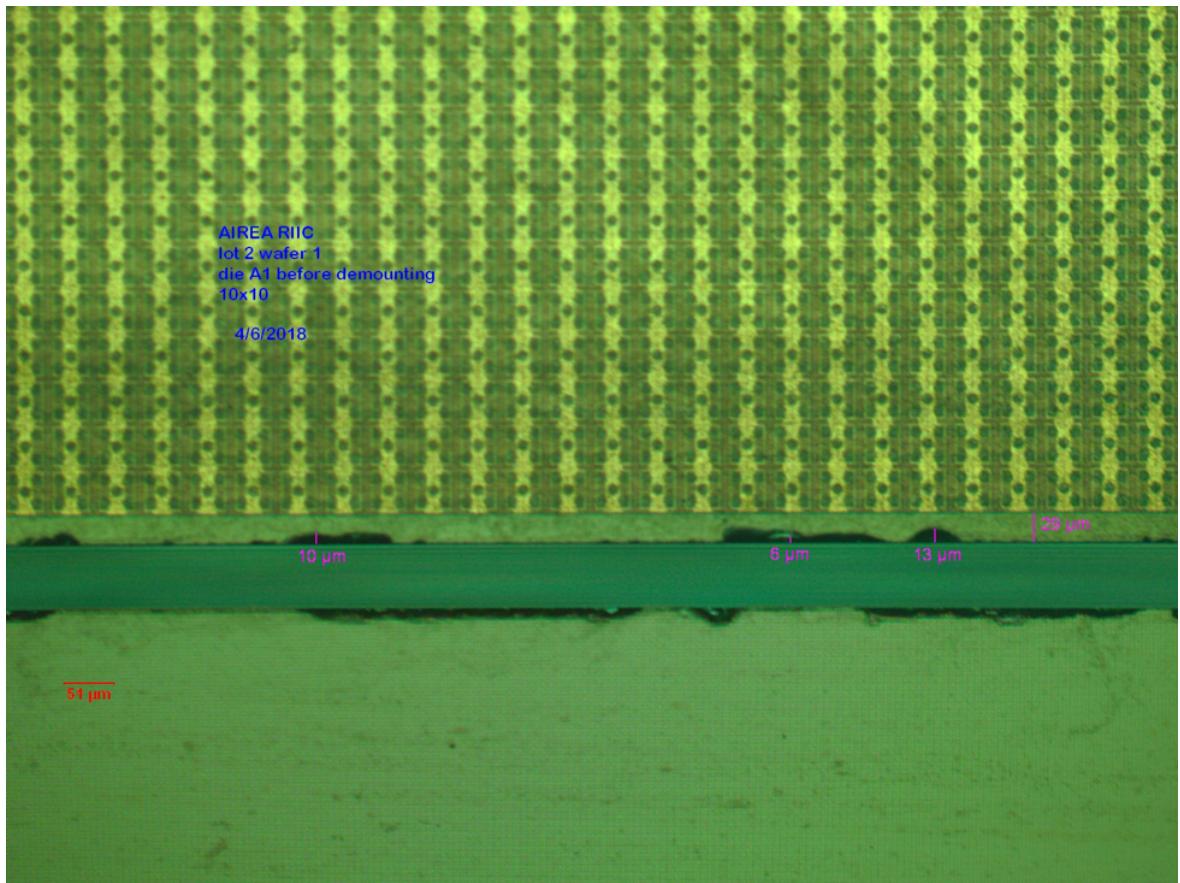
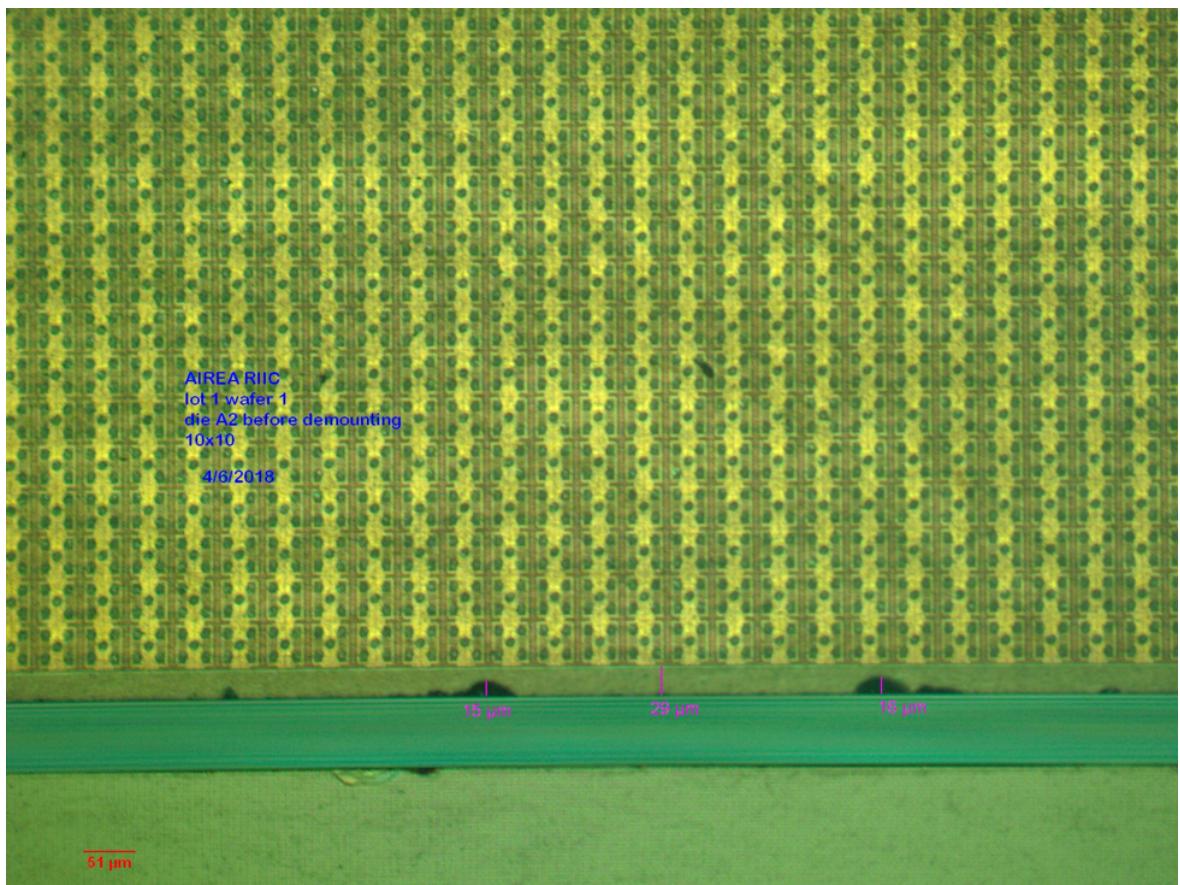


Figure 10.68: Close up view of dicing method.

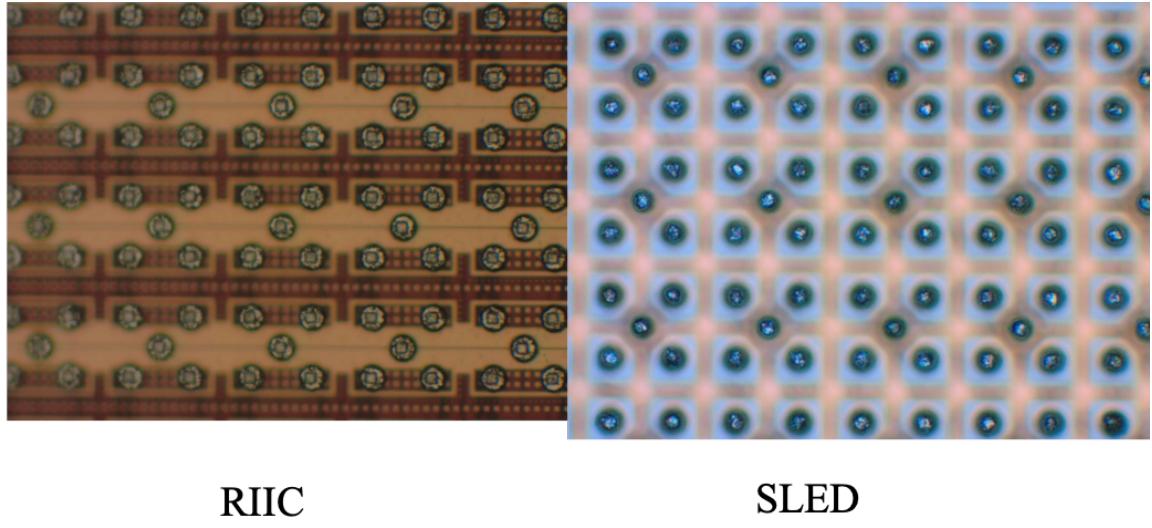


10.3 Hybridization Process

10.3.1 Indium Bump Deposition

Indium bumps were successfully deposited onto both the SLEDs dice and the RIIC dice. Figure 10.69 below show images of a few indium bumps on both dice.

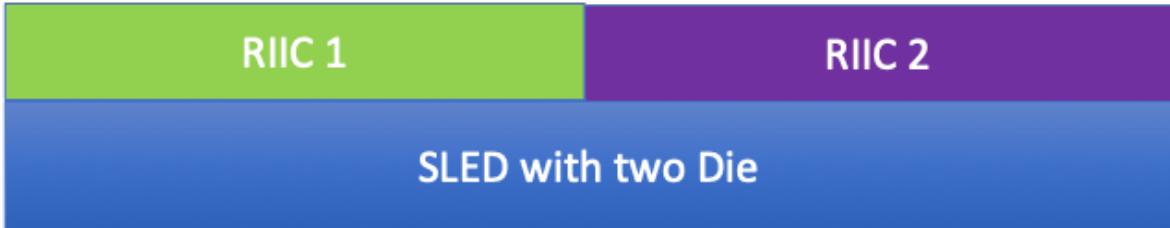
Figure 10.69: Indium bumps deposited on both the SLEDs and the RIICs.



10.3.2 Hybridization and Fly-Cutting

The RIIC dice and the SLEDs dice were successfully hybridized together. This process involved aligning the wafers over each other, so that the indium bumps on each die are aligned. The dice are then pressed together in a hybridizer machine and the indium bumps are fused together creating an electrical connection between the RIIC and the SLED. It is important to note that the SLED wafer is still two SLED dice held together by the material left in the trench etch. A diagram showing this is shown below. The SLED piece would then be fly cut and the SLED dice would be released. This would reveal the abutment edge and allow for the placement of the hybrids close to each other on the Copper Tungsten Plate. This process had two issues. The first issue was that RIIC 2 was not completely parallel with the SLED wafer piece due to the natural bow of the RIIC. This is visualized in Figure 10.71 below. This was caused by the natural bow of the RIIC die. This did not cause a failure, but it will affect the planarity of the projected image and possibly the quality of the electrical connections between the indium bumps. It is not known whether this will significantly affect the quality of the projected image as the degree of tilt of RIIC 2 is not that much. Testing

Figure 10.70: Ideal hybridization.



will have to be done to see the affect. In the future this situation would be remedied by hybridizing the least bowed piece first to ensure that when the second RIIC is placed on the SLED that the second RIIC will be pressed rather than the bowed RIIC absorbing all of the force. The SLED die could also be separated prior to hybridizing to avoid this situation. This method may be better overall, but may also present its own unique challenges.

Once the RIICs were hybridized onto the SLEDs wafer piece the SLEDs wafer piece was fly cut to thin the SLED and expose the trench edge. This was successfully done except for two small rabbit ears that remained after the fly cut procedure. It should be possible to simply break these rabbit ears off completely with no damage to the hybrid if done carefully. The rabbit ears are visible in Figure 10.72. The last issue that occurred is that the epoxy underfill seeped out into the trench area upon hybridization of the SLED and the RIIC. This is also visible in Figure 10.72 and is marked with a ruler to show the size. The epoxy under-fill would make placing the hybrids at a sub-pixel distance impossible because the epoxy is physically in the way. This issue could be resolved by performing an etch to remove the excess epoxy. This kind of etch is familiar for Teledyne and should not be an issue in the future.

Figure 10.71: Actual hybridization system caused by natural bow of the RIIC pieces.

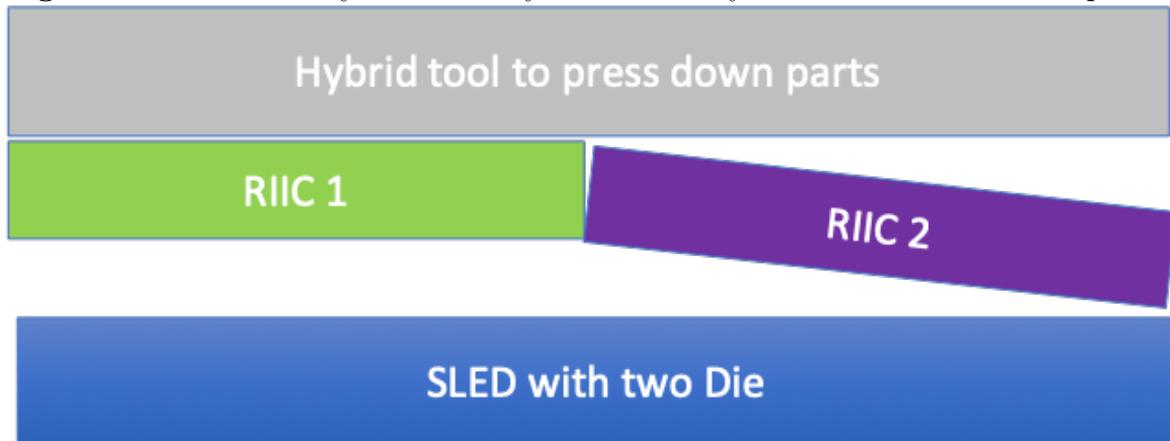
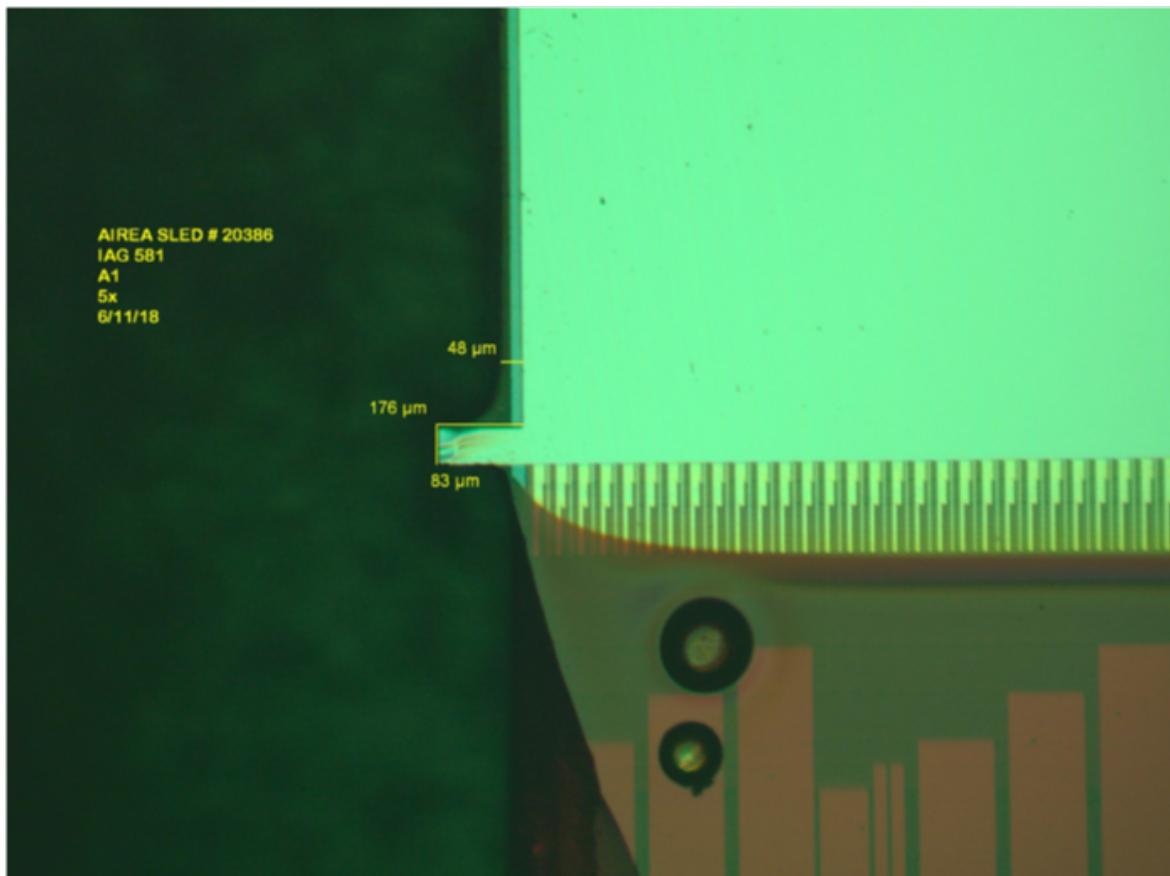


Figure 10.72: Rabbit ears after fly-cutting.



Chapter 11

CONCLUSION

During the course of the AIREA program many challenges, unforeseen and planned for, were overcome and solved. The program has moved abutment technology forward a great deal and has brought IRLED IRSPs with a resolution greater than 4 Megapixels within grasp. Many of the mistakes made that caused unforeseen challenges have been learned from and will continue to yield value well into the future.

The goals for phase 2 of the AERIA program were to:

1. Develop an abutment process for 24 and 48 micron pitch emitter arrays.
2. Develop technology for packaging abutted emitter arrays.
3. Maintain compatible interfaces to existing CSE hardware for low-cost and low-risk path to future system insertion.
4. Fabricate a 2Kx2K IRLED emitter array using two (2) abutted 1Kx2K Super-Lattice Light Emitting Diode (SLED) hybrids with 24-micron pixel pitch.

In the course of this Phase 2 program two abutment processes for 24 and 48 micron pitch emitter arrays were developed. The first process utilized etching technology to create smooth and vertical sidewalls that would be excellent for abutting together two hybrids. This method was conducted on the SLEDs devices. While some damage occurred to the indium bumps along the etched edge it is believed that with a more careful thermal management strategy this issue could be mitigated.

An etching method was also developed for the RIICs and tested on blank test wafers. The test wafer results were extremely promising and had the RIIC wafers been devoid of anomalous metal structures the etch method should have not been a problem. Unfortunately, due to the cost of unforeseen challenges this process was not conducted

on the RIICs. A less expensive and timelier dicing method was instead utilized for the RIICs. This dicing method produced what are believed to be adequate results. The dicing method could not be tested due to funding running out at Teledyne. Its estimated that \$15,000 would be needed to place the pieces on the copper tungsten heat sink plate to test the abutment process with the hybridizer machine.

Packaging technology was developed for abutted emitter arrays. This packaging had the form of a Copper Tungsten heat sink and the novel idea to use indium bumps and epoxy backfill to attach the hybrids to the Copper Tungsten. The indium bump method was necessary to use instead of the traditional epoxy bond to the heat sink plate to avoid epoxy forcing its way between the hybrids and separating them. This would make placing the hybrids at a sub-pixel distance apart impossible.

The Copper Tungsten heat sink had to be properly processed to have the proper finish on it to support indium bump photolithography and have precisely placed alignment holes to align the indium bump mask to the Copper Tungsten heat sink plate. The indium bump technique was novel enough to be patentable.

The RIIC interface was maintained to enable existing CSE hardware to interface with the AIREA hybrid.

Unfortunately, due to development costs a 2K x 2K IRLED emitter array using two abutted 1K x 2K SLED hybrids with 24-micron pixel pitch was not able to be fabricated. The program would have required an additional \$15,000 to finish hybridizing the two arrays onto the Copper Tungsten heat sink plate and an estimated \$30,000 to \$40,000 to finish the hybridizing process.

REFERENCES

Lastname, Firstname “Title.” *Journal*, Year.

Lastname, Firstname, and Firstname Lastname. *Title of Book*. Publisher, Year.

REFERENCES

- [1] Effect of Light on Selenium During the Passage of An Electric Current*. *Nature*, 7:303, feb 1873.
- [2] Sasson Amirhaggi, Brian Smith, Rebecca Martinez, Mark J. Furlong, and Andrew Mowbray. Multiwafer production of epitaxy ready 4" GaSb substrates: requirements for epitaxially growth infrared detectors. *Quantum Sensing and Nanophotonic Devices IX*, 8268(January 2012):826818, 2011.
- [3] E.Scott Barr. The infrared pioneers -ii. macedonio melloni. *Infrared Physics*, 1(1):1 – IN6, 1961.
- [4] J Benedict, R T McGee, J Marks, K Nabha, A Waite, G Ejzak, J Dickason, H Ahmed, M Hernandez, P Barakhshan, T Browning, J Volz, R J Ricker, F Kiamilev, J P Prineas, and T F Boggess. 1Kx1K Resolution Infrared Scene Projector at 24um Pixel Pitch. *GOMACTech Conference*, page On CD, 2017.
- [5] Jacob Benedict, Rodney Mcgee, Hamzah Ahmed, Miguel Hernandez, Nicholas A Waite, Jonathan Dickason, Tyler Browning, and Christopher Jackson. 4-Megapixel Infrared Scene Projector Based on Superlattice Light Emitting Diodes. pages 2–5.
- [6] H.P. Bonzel and Ch. Kleint. On the history of photoemission. *Progress in Surface Science*, 49(2):107 – 153, 1995.
- [7] T. W. Case. Notes on the change of resistance of certain substances in light. *Phys. Rev.*, 9:305–310, Apr 1917.
- [8] Carlo Corsi. History highlights and future trends of infrared sensors. *Journal of Modern Optics*, 57(18):1663–1686, 2010.
- [9] N C Das, M Tayssing-Lara, K A Olver, F Kiamilev, J P Prineas, J T Olesberg, E J Koerperick, L M Murray, and T F Boggess. Flip Chip Bonding of 68 \times 68 MWIR LED Arrays. *IEEE Transactions on Electronics Packaging Manufacturing*, 32(1):9–13, jan 2009.
- [10] Naresh C Das, Kim Olver, F Towner, G Simonis, and H Shen. Infrared (3.8μm) interband cascade light-emitting diode array with record high efficiency. *Applied Physics Letters*, 87(4), 2005.

- [11] P.-Y. Delaunay, M. Razeghi, E. K. Huang, B.-M. Nguyen, and D. Hoffman. Inductively coupled plasma etching and processing techniques for type-II InAs/GaSb superlattices infrared detectors toward high fill factor focal plane arrays. *Quantum Sensing and Nanophotonic Devices VI*, 7222:72220Z, 2008.
- [12] G. A. Ejzak, J. Dickason, J. A. Marks, K. Nabha, R. T. McGee, N. A. Waite, J. T. Benedict, M. A. Hernandez, S. R. Provence, D. T. Norton, J. P. Prineas, K. W. Goossen, F. E. Kiamilev, and T. F. Boggess. 512×512, 100 hz mid-wave infrared led microdisplay system. *Journal of Display Technology*, 12(10):1139–1144, Oct 2016.
- [13] Greg Franks, Joe Laveigne, Tom Danielson, Steve McHugh, John Lannon, and Scott Goodwin. Development of an ultra-high temperature infrared scene projector at Santa Barbara Infrared Inc. 9452:94520W–94520W–9, 2015.
- [14] H. Julian Goldsmid. *Introduction to Thermoelectricity*. Springer, 2010.
- [15] W. Herschel. Experiments on the refrangibility of the invisible rays of the sun. *Phil. Trans. Roy. Soc. London*, 1800.
- [16] A.W. Van Herwaarden and P.M. Sarro. Thermal sensors based on the seebeck effect. *Sensors and Actuators*, 10(3):321 – 346, 1986.
- [17] Philip C. D. Hobbs. *Building Electro-Optical Systems: Making It All Work*. Wiley Publishing, 2nd edition, 2009.
- [18] S.F. Johnson. *A History of Light and Colour Measurement. Science in the Shadows*. IOP Publishing Ltd, Bristol, 2001.
- [19] S Jung, S Suchalkin, D Westerfeld, G Kipshidze, E Golden, D Snyder, and G Belelky. High dimensional addressable LED arrays based on type I GaInAsSb quantum wells with quaternary AlGaInAsSb barriers. *Semiconductor Science and Technology*, 26(8):85022, 2011.
- [20] E J Koerperick, D T Norton, J T Olesberg, B V Olson, J P Prineas, and T F Boggess. Cascaded Superlattice InAs/GaSb Light-Emitting Diodes for Operation in the Long-Wave Infrared. *IEEE Journal of Quantum Electronics*, 47(1):50–54, jan 2011.
- [21] E J Koerperick, J T Olesberg, J L Hicks, J P Prineas, and T F Boggess. Active Region Cascading for Improved Performance in InAs #x2013;GaSb Superlattice LEDs. *IEEE Journal of Quantum Electronics*, 44(12):1242–1247, dec 2008.
- [22] Corey Lange, Rodney McGee, Nick Waite, Robert Haislip, and Fouad Kiamilev. System for driving 2-D infrared emitter arrays at cryogenic temperatures. *2011 IEEE Winter Topicals, WTM 2011*, 801507(May 2011):143–144, 2011.

- [23] John Lannon, Tom Danielson, Scott Goodwin, Dennis Norton, Greg Franks, Steve McHugh, Greg Matis, Nicholas Holmes, Joe LaVeigne, and Tony Vengel. Achieving ultra-high temperatures with a resistive emitter array. *Infrared Imaging Systems: Design, Analysis, Modeling, and Testing XXVII*, 9820:98200Z, 2016.
- [24] John Lannon, Kevin Sparkman, Scott Goodwin, Steve McHugh, and Joe LaVeigne. Ultrahigh-temperature emitter pixel development for scene projectors. *Infrared Imaging Systems: Design, Analysis, Modeling, and Testing XXV*, 9071(June 2014):90711H, 2014.
- [25] Joe LaVeigne, Greg Franks, and Marcus Prewarski. A two-color 1024x1024 dynamic infrared scene projection system. 8707:870703–870709, 2013.
- [26] Benjamin Lee. Chapter 1 Introduction to 12 Degree Orthogonal Digital Micromirror Devices (DMDs) Introduction to 12 Degree Orthogonal Digital Micromirror Devices (DMDs). (July 2008):1–13, 2008.
- [27] Jack R. Lippert and Kipp Bauchert. Testing a new generation 512 x 512, >200 Hz capable, liquid crystal on silicon (LCoS) with ferro-electric liquid crystal, IR scene projector. *Technologies for Synthetic Environments: Hardware-in-the-Loop Testing XI*, 6208(May 2006):62080L, 2006.
- [28] V K Malyutenko, K V Michailovskaya, O Y Malyutenko, V V Bogatyrenko, and D R Snyder. Infrared dynamic scene simulating device based on light down-conversion. *IEE Proceedings - Optoelectronics*, 150(4):391–394, aug 2003.
- [29] B.A. Matveev. Flip-chip bonded inassbp and ingaas leds and detectors for the 3-m spectral region. *IEE Proceedings - Optoelectronics*, 150:356–359(3), August 2003.
- [30] FLIR Media. Uncooled detectors for thermal imaging cameras: Making the right detector choice. *Infrared Imaging News*, 14, April 2008.
- [31] M. Neuberger. Gallium Antimonide. *IIIV Semiconducting Compounds*, pages 35–44, 2013.
- [32] Scott P. Newbry, Julia R. Dupuis, Ryan Benedict-Gill, Robert Vaillancourt, and David J. Mansur. High-dynamic range DMD-based IR scene projector. *Emerging Digital Micromirror Device Based Systems and Applications V*, 8618(March 2013):86180R, 2013.
- [33] D T Norton, J T Olesberg, R T McGee, N A Waite, J Dickason, K W Goossen, J Lawler, G Sullivan, A Ikhlassi, F Kiamilev, E J Koerperick, L M Murray, J P Prineas, and T F Boggess. 512 ,\times, 512 Individually Addressable MWIR LED Arrays Based on Type-II InAs/GaSb Superlattices. *IEEE Journal of Quantum Electronics*, 49(9):753–759, sep 2013.

- [34] D T Norton, J T Olesberg, R T McGee, N A Waite, J Dickason, K W Goossen, J Lawler, G Sullivan, A Ikhlassi, F Kiamilev, E J Koerperick, L M Murray, J P Prineas, and T F Boggess. 512 ,\times, 512 Individually Addressable MWIR LED Arrays Based on Type-II InAs/GaSb Superlattices. *IEEE Journal of Quantum Electronics*, 49(9):753–759, sep 2013.
- [35] R.S. Ohl. Light-sensitive electric device. *United States Patent Office* 2402662, 1946.
- [36] Jean Peltier. Nouvelles expriences sur la caloricit des courants lectrique [new experiments on the heat effects of electric currents]. *Annales de Chimie et de Physique (in French)*, 56:371–386.
- [37] P. L. Richards. Bolometers for infrared and millimeter waves. *Journal of Applied Physics*, 76(1):1–24, 1994.
- [38] A. Rogalski. History of infrared detectors. *Opto-Electronics Review*, 20(3):279–308, Sep 2012.
- [39] Jeffrey B. Sampsell. Digital micromirror device and its application to projection displays. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 12(6):3242, 2002.
- [40] Dr. Rudy Schlaf. Tutorial on work function. 2005.
- [41] Kevin Sparkman, Joe LaVeigne, Steve McHugh, Jason Kulick, John Lannon, and Scott Goodwin. Scalable emitter array development for infrared scene projector systems. 9071:90711I–90711I–7, 2014.
- [42] William Thomson. On a mechanical theory of thermo-electric currents. *Proceedings of the Royal Society of Edinburgh*, 42(3):91–98, 1851.
- [43] Wikipedia contributors. Infrared — Wikipedia, the free encyclopedia, 2019. [Online; accessed 1-February-2019].
- [44] Jim Williams. Application Note 120 March 2010 1ppm Settling Time Measurement for a Monolithic 18-Bit DAC When Does the Last Angel Stop Dancing on a Speeding Pinhead ? AN120-1 Application Note 120 AN120-2. *Analog Devices*, (March):1–36, 2010.
- [45] Jim Williams. 30 nanosecond settling time measurement for a precision wide-band amplifier: Quantifying prompt certainty. *Analog Circuit Design Volume 2*, (September):577–606, 2013.
- [46] Owen M. Williams. Dynamic infrared scene projection: A review. *Infrared Physics and Technology*, 39(7):473–486, 1998.

- [47] Owen M. Williams, George C. Goldsmith II, and Robert G. Stockbridge. History of resistor array infrared projectors: hindsight is always 100% operability. *Technologies for Synthetic Environments: Hardware-in-the-Loop Testing X*, 5785(May 2005):208, 2005.
- [48] C Wood. Materials for thermoelectric energy conversion. *Reports on Progress in Physics*, 51(4):459–539, apr 1988.
- [49] Y.H. Zhang, R. H. Miles, L. West, D. H. Chow, T. C. Hasenberg, H. L. Dunlap, and A. R. Kost. Midwave infrared diode lasers based on GaInSb/InAs and InAs/AlSb superlattices. *Applied Physics Letters*, 67(25):3700–3702, 2002.

Appendix A
TITLE OF APPENDIX

- A.1 Current Gating vs Voltage Gating**
- A.2 Oscilloscope Overdrive**
- A.3 DAC Board**
- A.4 AIREA Wafer Analysis**
- A.5 Dewar Impedance Measurement**
- A.6 RIIC Analog Signal Architecture**

Appendix B

LABORATORY REPORTS

Big takeaway from today: Current feedback op-amps are very particular about external component values. You must choose from the list of approved values in the datasheet or spend a lot of time hunting for an optimum value that gives you the gain and also provides stability.

Summary: Today I replaced the feedback resistor elements with 510 ohm resistors for R_f and R_g . This gives a gain of two and the widest bandwidth, 1.4GHz, from the OPA695. Op-amps behave much better. No more 416MHz ringing. I also removed the feedback capacitor because I read that this causes instability in the op amp.

B.1 21:1 Board Testing:

B.1.1 Initial results:

The 21:1 divider is constructed with R_{31} and R_{32} . The resistor divider formed by these two resistors minimizes the effect the cable and oscilloscope parasitics on the amplifier circuit. This gives a more realistic view of the behavior of the circuit. The following two figures show the value of the 21:1 divider.

With the 21:1 divider it can be seen that the behavior of the two circuits is the same. The difference seen before was due to the effect of the cable and oscilloscope loading the circuit. **What this meant was the circuit design was very sensitive to parasitic loading.**

Figure B.1: Post-amp circuit with 21:1 divider circuit. Resistors R32 and R31 form the 21:1 divider.

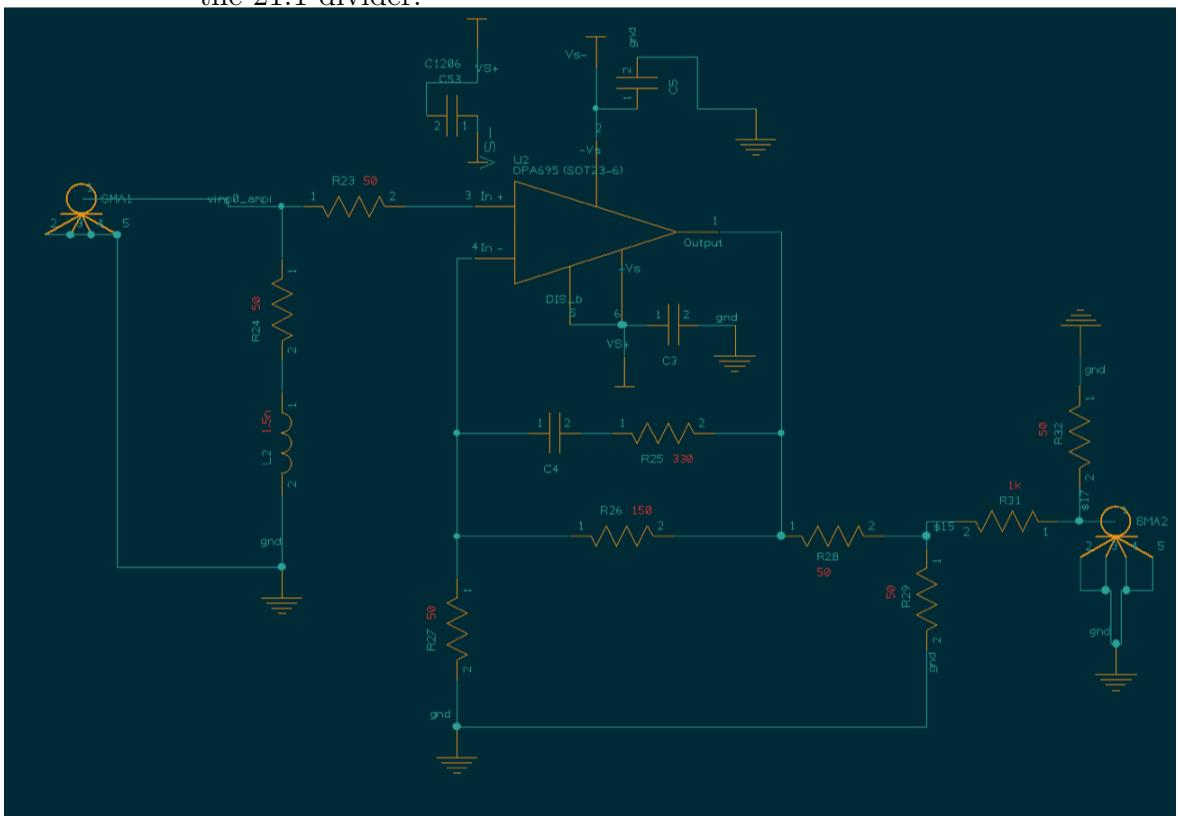


Figure B.2:

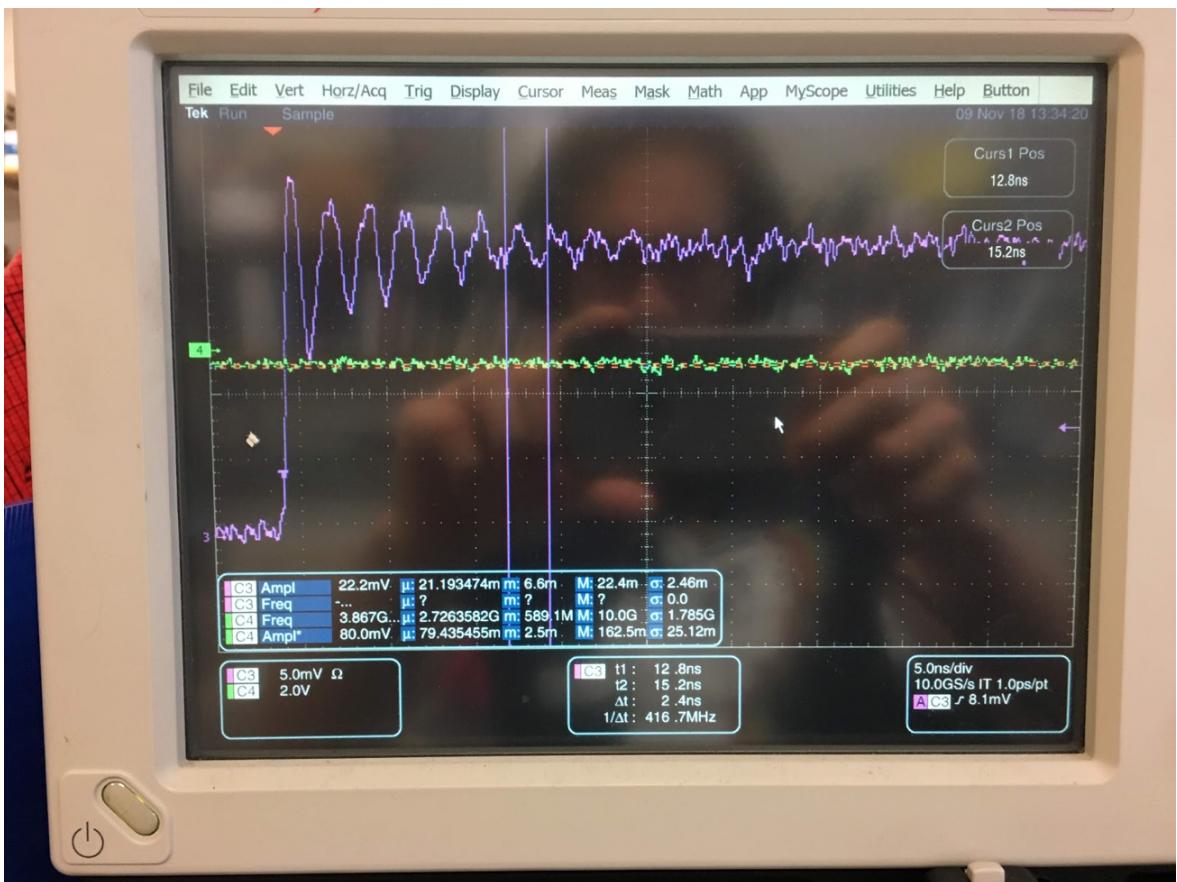
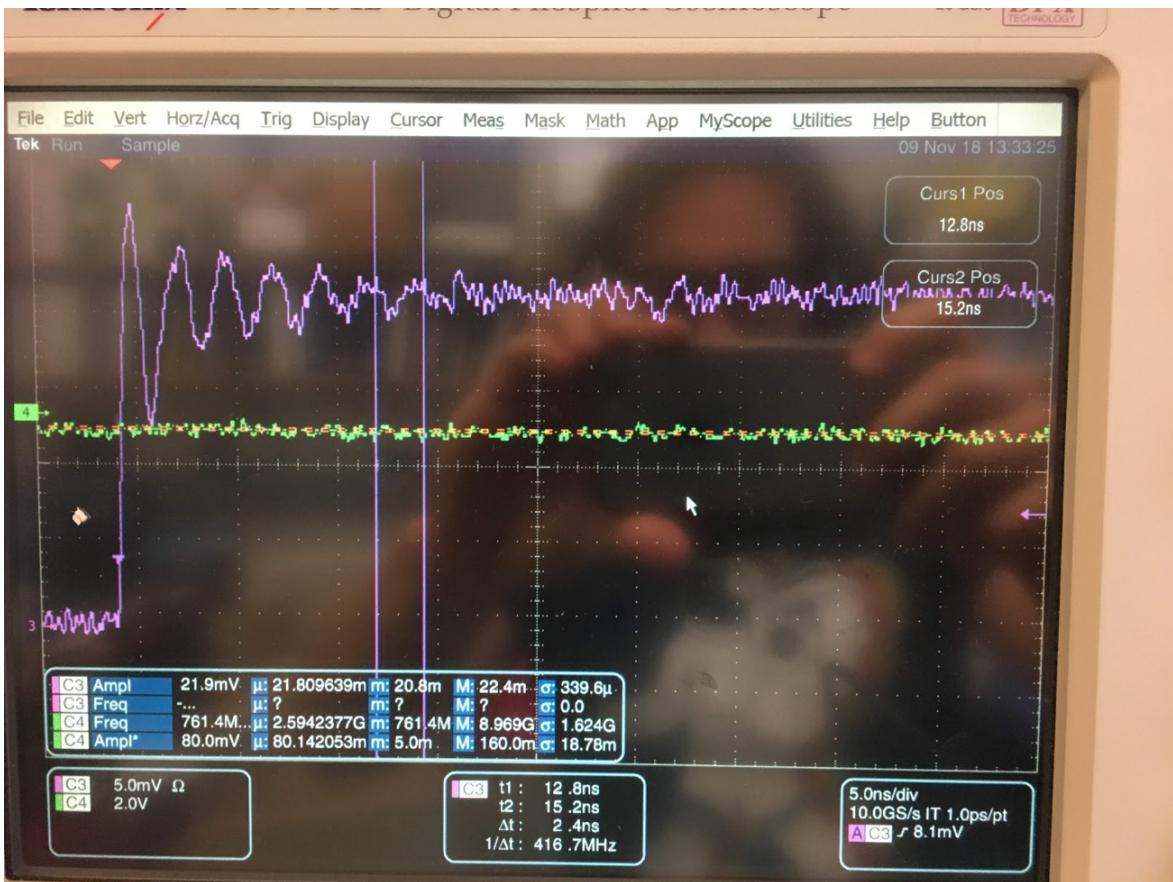


Figure B.3:



B.1.2 Circuit Update

I learned from this document, <http://www.ti.com/lit/an/sloa021a/sloa021a.pdf>, that current feedback op amps (CFAs) are very particular about the values of the external components. The IC designers spend a lot of time looking for good values of external resistors. It is not as easy as a voltage feedback op amp. The recommended values are shown below in the table. I ended up choosing a gain of two because the OPA695 will have the widest bandwidth at this gain value, 1.4GHz. To get a gain of 2 511 ohm resistors are used for the two feedback resistors. I put 510 ohm resistors on the test board because that was the closest part available in the lab. I also read that having a capacitor in the feedback loop of a CFA is very bad for stability so I removed the capacitor.

Both of these changes drastically improved the response of the amplifier.

The resistors R_f and R_g are the 511 ohm resistors in this schematic.

Figure B.4:

Gain 2V/V Video Line Driver

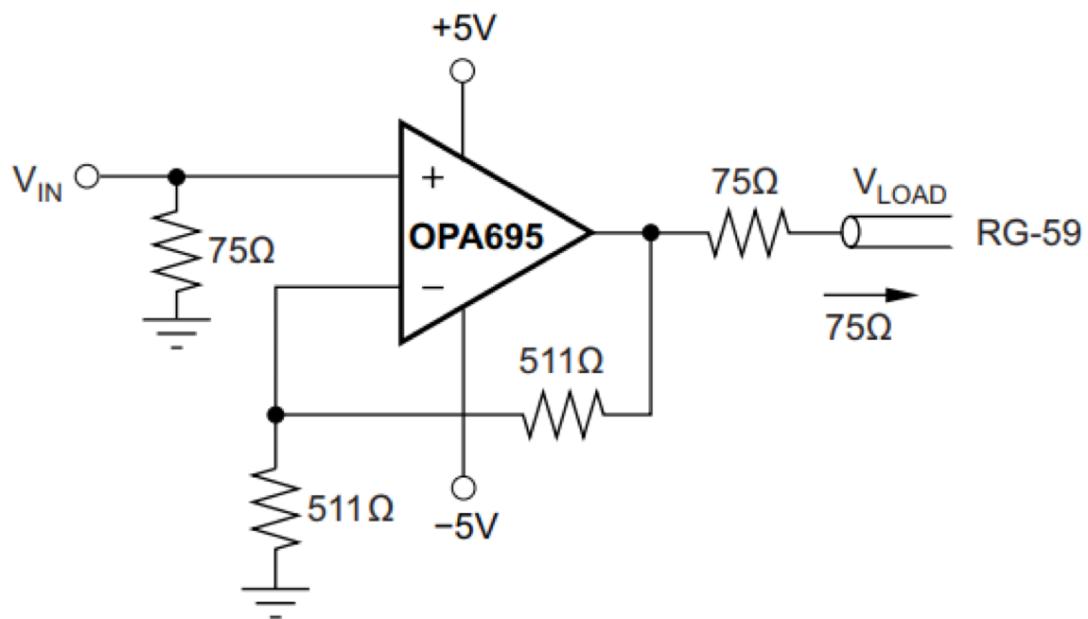


Figure B.5:

Table 1. Noninverting Wideband Operational Amplifier

GAIN TO LOAD (dB)	R _F (Ω)	R _G (Ω)	NOISE FIGURE
6	478	159	17.20
7	468	134	16.55
8	458	113	15.95
9	446	96	15.40
10	433	81	14.91
11	419	68	14.47
12	402	57	14.09
13	384	48	13.76
14	363	40	13.23
15	340	33	13.23
16	314	27	13.03
17	284	21	12.86
18	252	16	12.72

Copyright © 2003–2015, Texas Instruments Incorporated

[Submit Documentation Feedback](#) 27

Product Folder Links: [OPA695](#)



OPA695

SBOS293H –DECEMBER 2003–REVISED DECEMBER 2015

www.ti.com

Feature Description (continued)

Table 1. Noninverting Wideband Operational Amplifier (continued)

GAIN TO LOAD (dB)	R _F (Ω)	R _G (Ω)	NOISE FIGURE
19	215	12	12.60
20	174	9	12.51

Figure B.6:

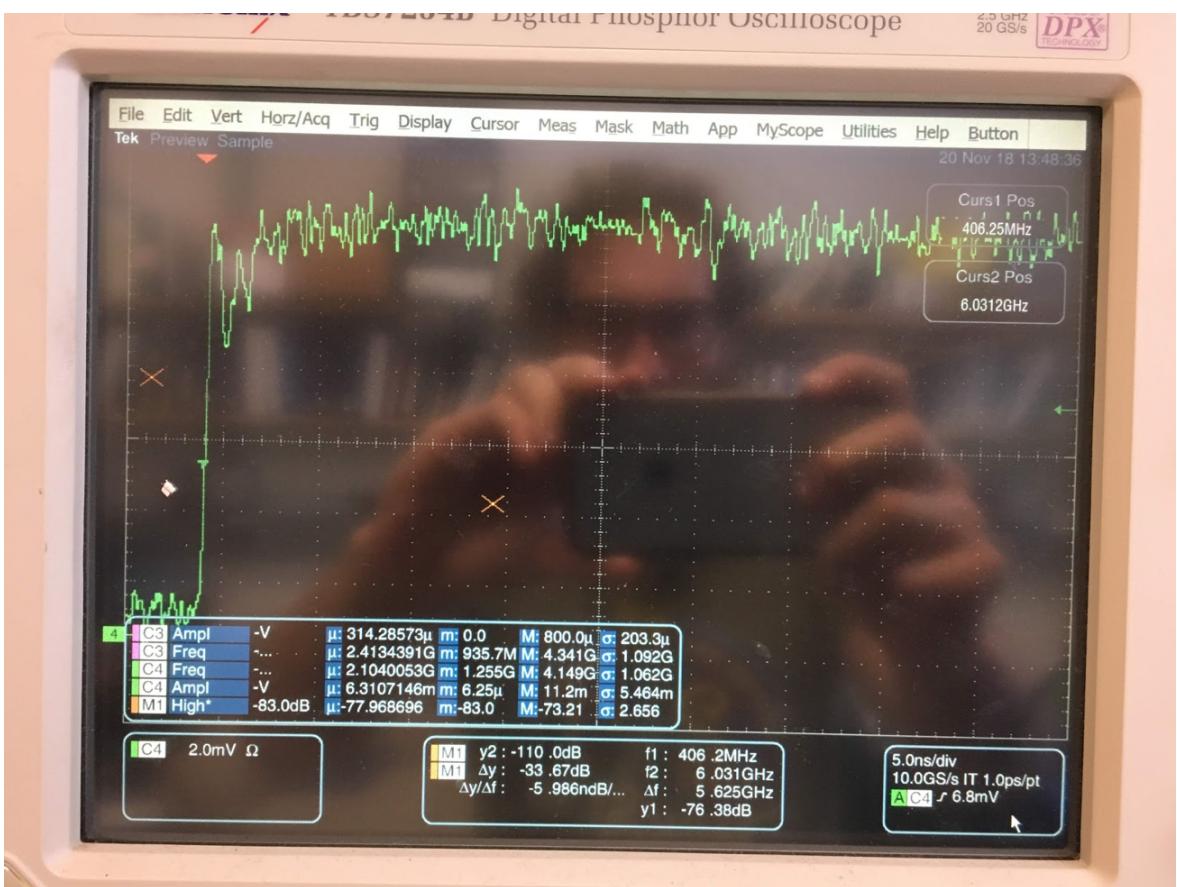


Figure B.7:

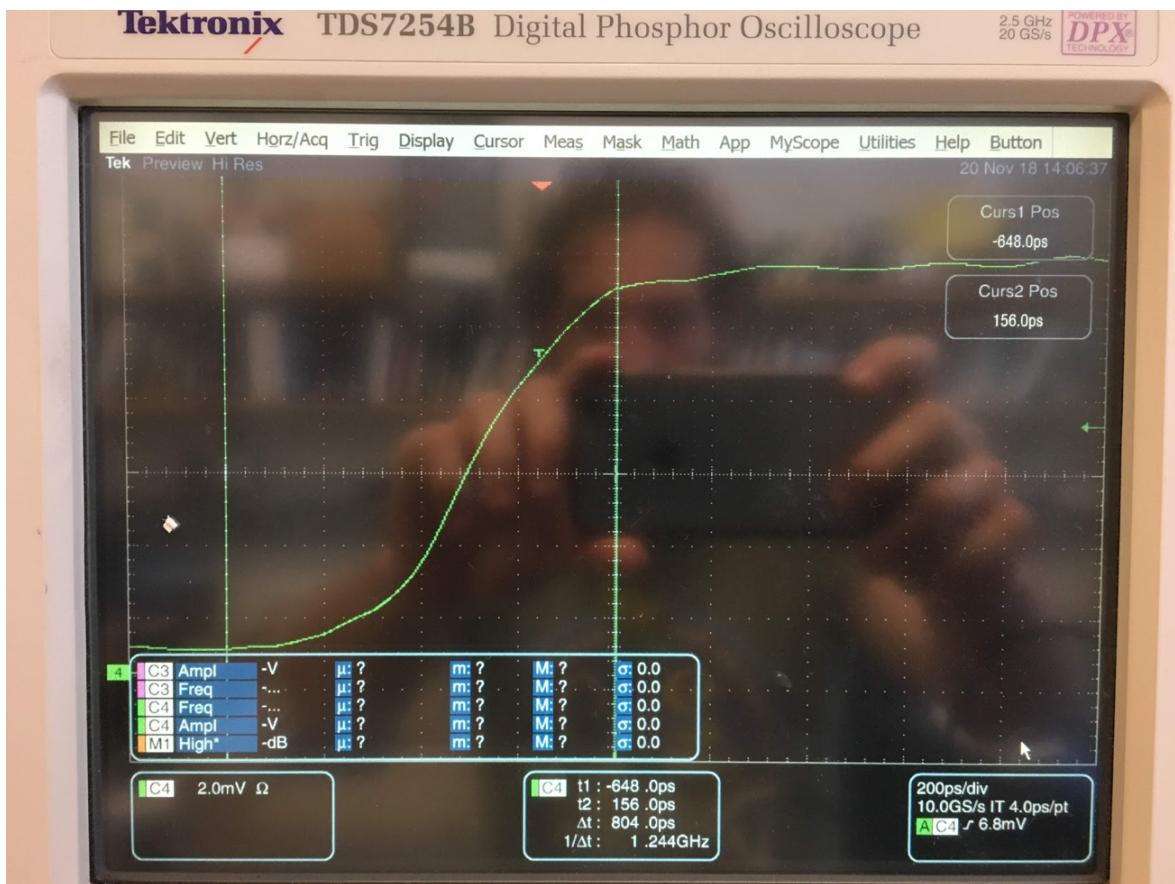


Figure B.8:

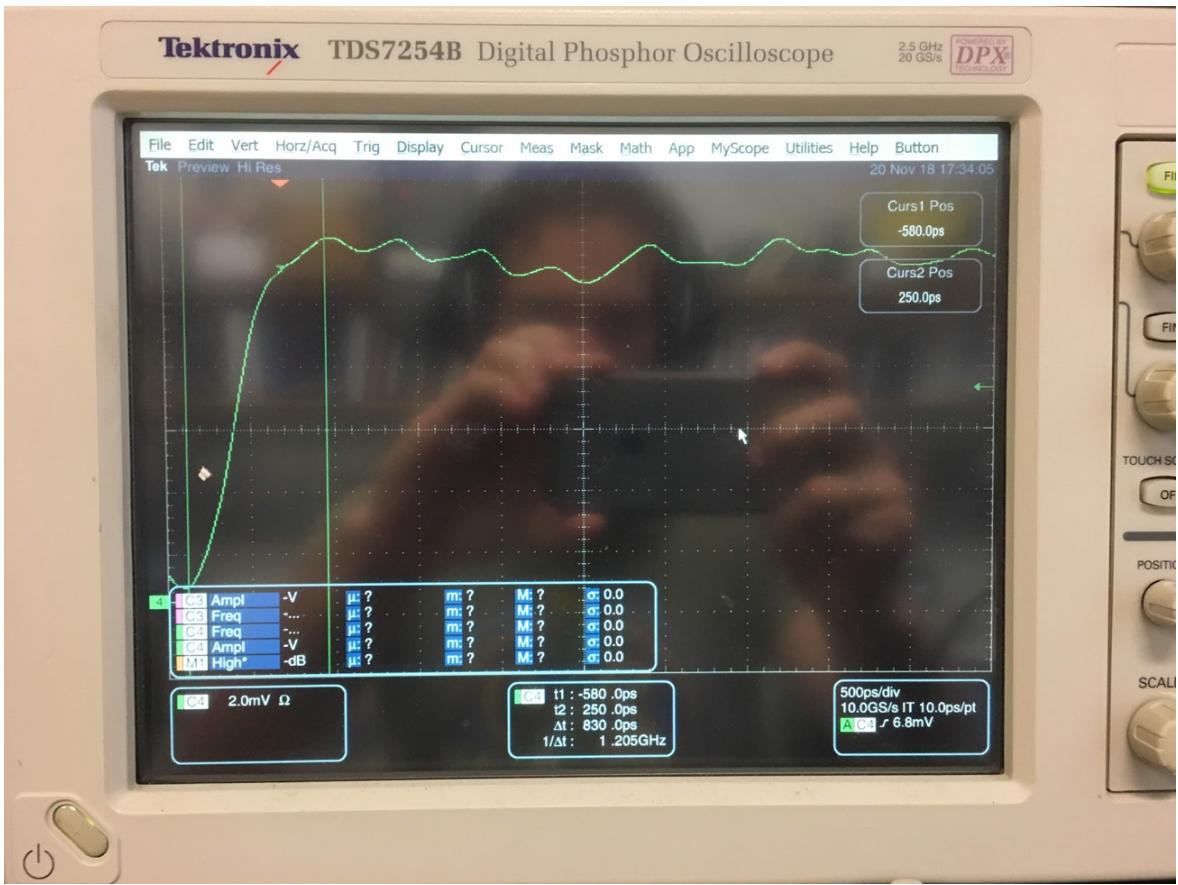
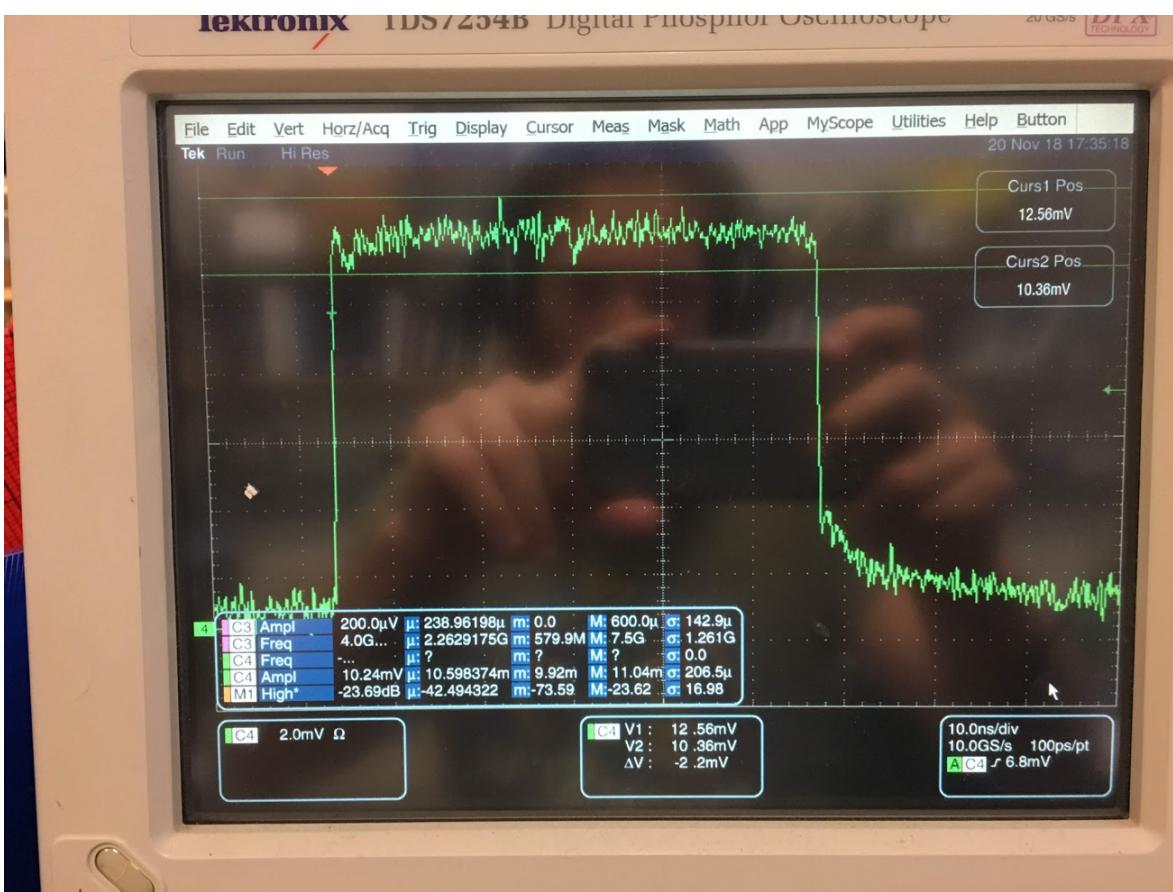


Figure B.9:



B.1.3 Straight Post-amp Testing:

After seeing an improvement in the response of the 21:1 divider board I wanted to see what the improvement was for the straight post-amp test board.

After modifying the circuit to also have a gain of 2 like I did for the 21:1 divider the response is greatly improved.

Figure B.10: Post-amp circuit without 21:1 divider circuit.

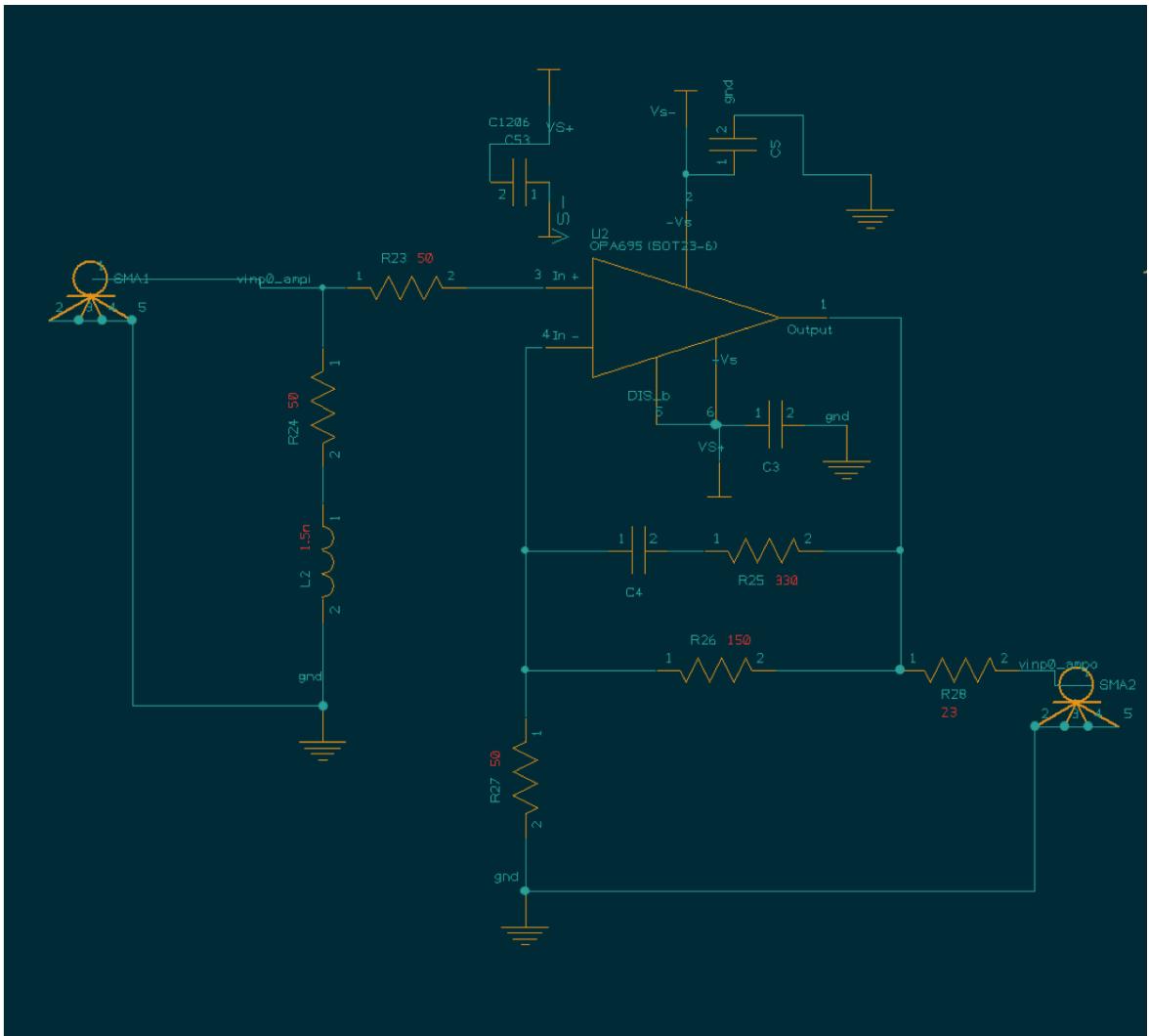


Figure B.11:

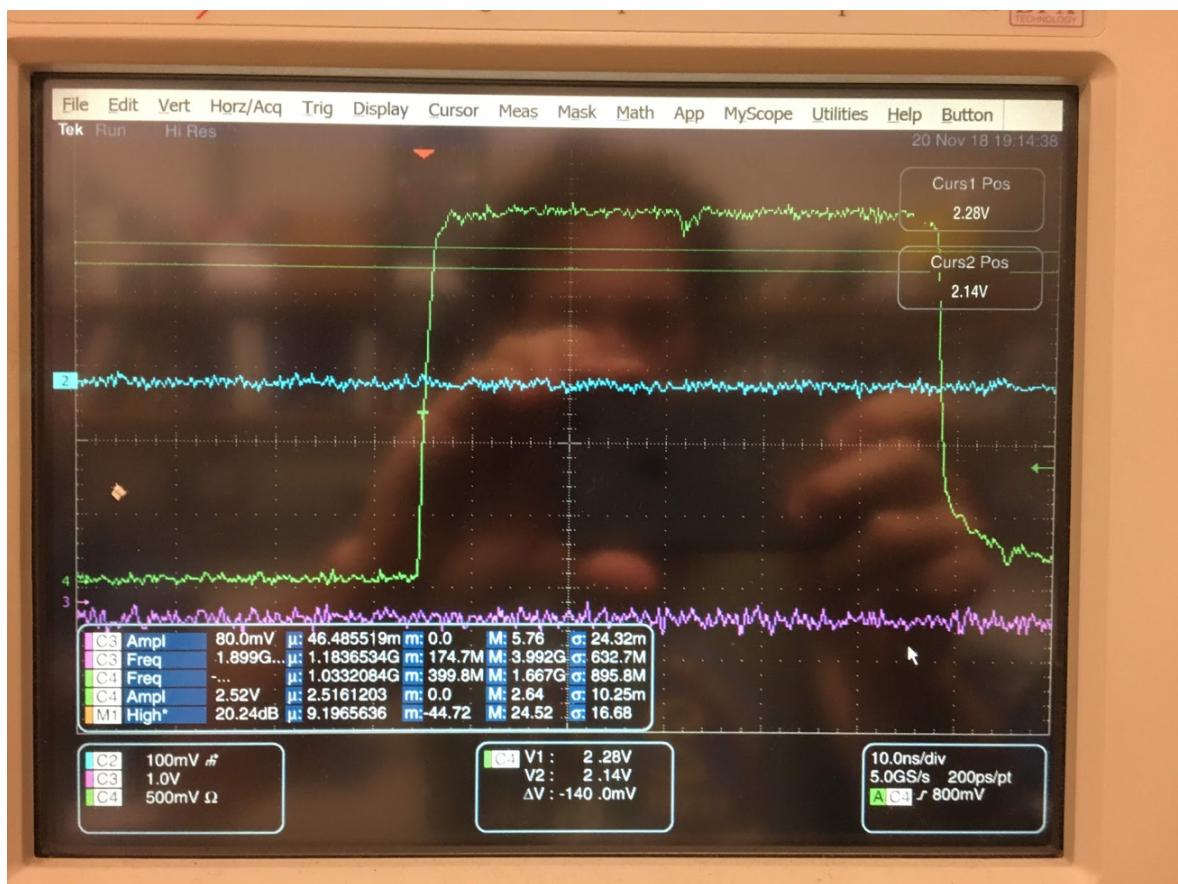
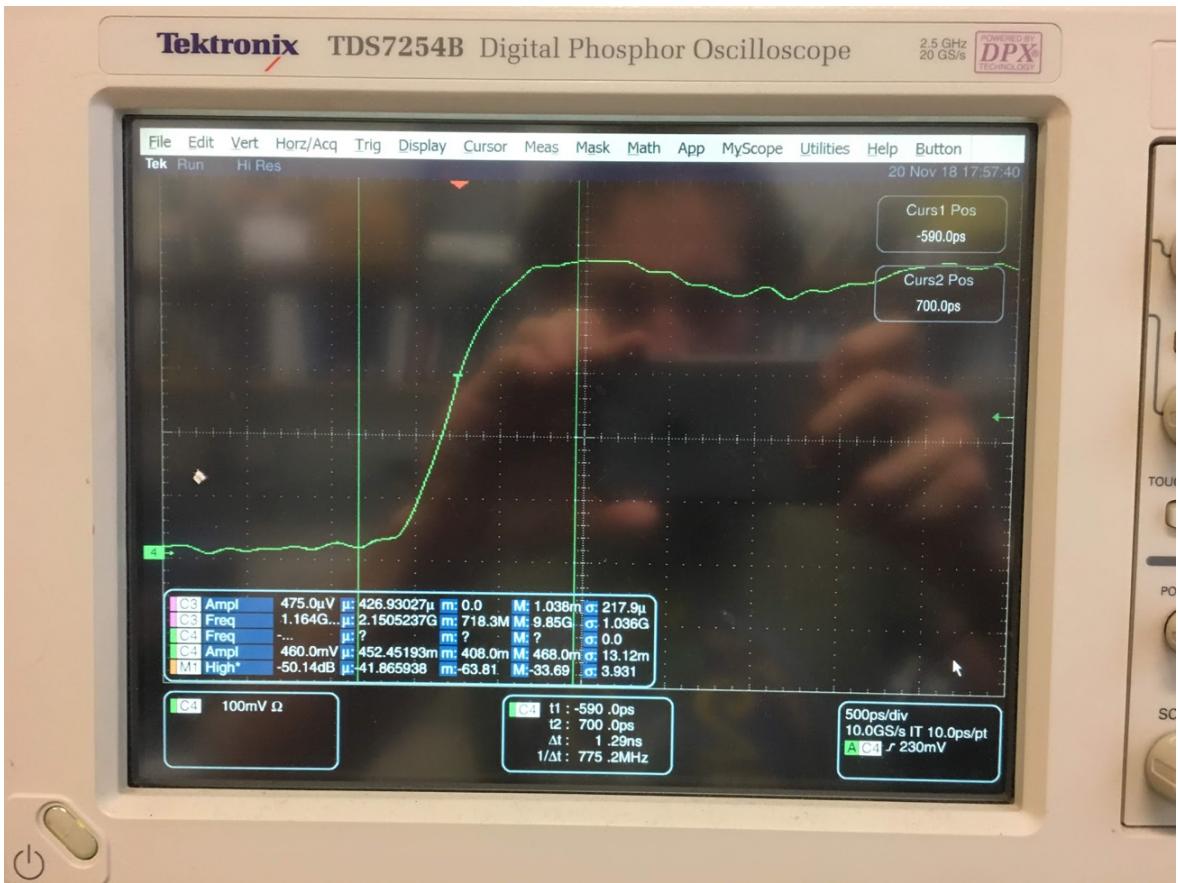


Figure B.12:



Figure B.13:



B.1.4 Bit Resolution:

A crude measurement of bit resolution can be done by measuring the rough noise level. This measurement is shown in the following image and is 30mV.

To get the amount of bits lost first the LSB must be calculated:

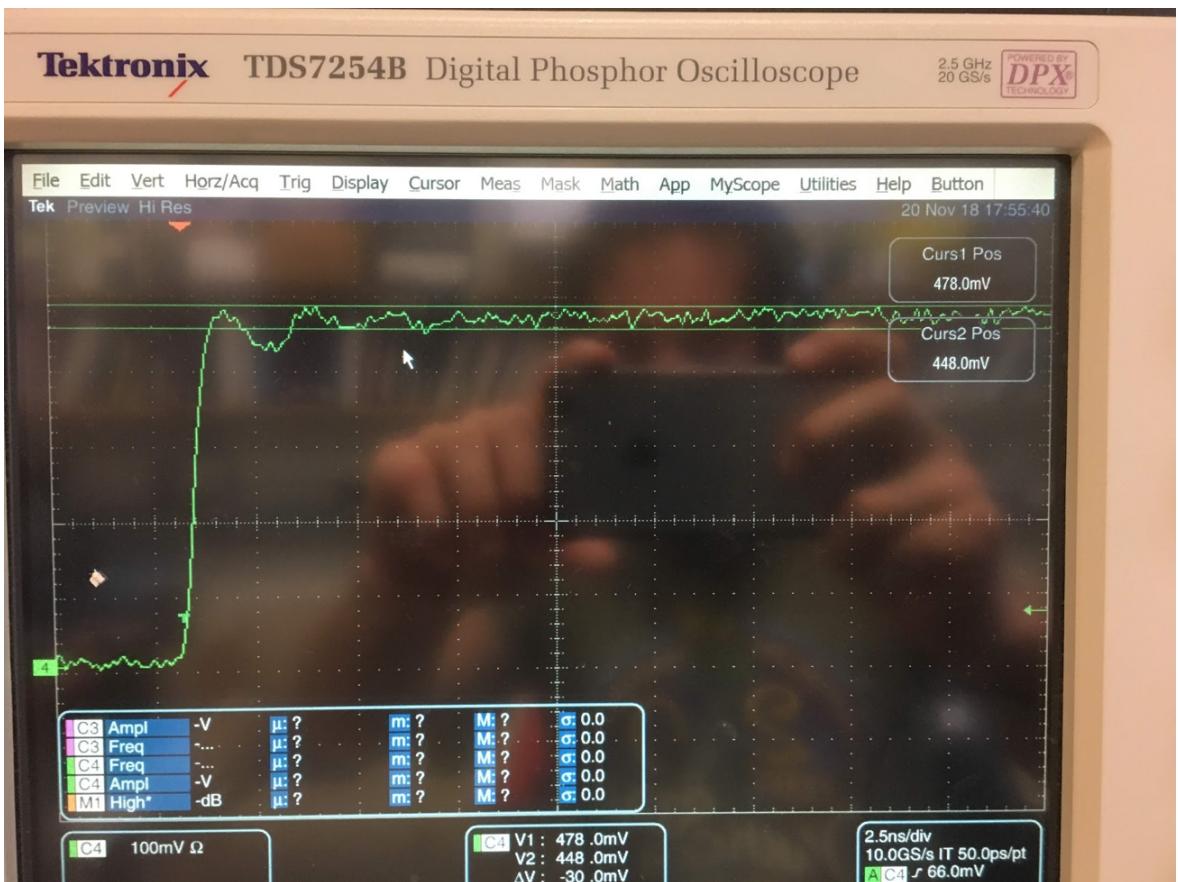
$$\text{Maxvoltage}/2^n \text{um}_b\text{its} = \text{voltage}/\text{bit}$$

For 16 bits this works out to 7.62939E-05 volts / LSB.

Using our measured noise margin of 42mV the number of lost numbers can be calculated. $0.042/7.62939 * 10^{-5} = 550$. Taking the log base 2 of 550 gives us the number of bits lost: 9.104605043. And subtracting this value from 16 bits gives us the remaining bits we have: 6.895394957. So 6 or 7 bits.

I also measured the signal generator directly and it had the same amount of noise. So, the noise level seems to be inherent in the scope or signal generator.

Figure B.14:



B.1.5 5V operation

5V operation was accomplished with the power supplies set to ± 6.5 . The scope shows 2.5 volts because of the resistor divider on the output of the post amp.

Figure B.15:

