THERMAL PERFORMANCE CHARACTERIZATION OF A 512x512 MID-WAVE INFRARED SUPER LATTICE LIGHT EMITTING DIODE PROJECTOR

by

Peyman Barakhshan

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

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ABSTRACT

In 2014, our team built the world's first infrared LED scene projector. This system is called the SLEDS projector. It displays 512x512 MWIR images from a DVI computer interface at 100HZ. The projector has been successfully evaluated at multiple user facilities and has logged several hundred hours of operation. Thermal modelling was done to simulate the dissipation of heat in the infrared scene projector (IRSP). Current work is being done at the University of Delaware's Scene Projection Evaluation and Research (SPEAR) laboratory to evaluate and update the thermal models.

Due to the importance of the infrared detectors in today's world, it is necessary to accurately test and characterize these detectors with a frame of reference related to the application. IR projection systems are a great way to characterize the detectors because they can be used as a high accuracy reference.

Described in this work, is a 512x512 super-latticed light emitting diode system (SLEDS) operating at a frame rate of 100Hz. This system has been fully developed, tested, and corrected for non-uniformity (NUC). Stress testing and heat response characteristics are the main goals of this paper.

Chapter 1

INTRODUCTION

1.1 SLEDS Background

Infrared (IR) detectors have applications across various fields such as scientific, industrial and medical. IR is able to detect information that is otherwise undetectable by a human eye which demonstrates the high technological advancement IR can achieve. Some examples IR applications consist of its usage in discovering stars that are millions of light-years away, locating shorts in electric circuits, gas leaks, and thermal night vision. It is essential to obtain testing equipment that is able to project realistic IR images at a large range intensity in order to test IR detectors. Blackbody radiation and resistive arrays are the existing technologies used to test IR detectors. However, the super-latticed emitting diode system (SLEDS) is the newest IR projector technology that can project highly precise images at a much higher intensity than currently existing projectors on the market. This is attained by utilizing a 512x512 SLEDS array that is driven and controlled by various electrical components. Having a 512x512 resolution makes the images projected by SLEDS exceptionally accurate depictions of the input images. The SLEDS have the ability to function at remarkably higher intensity than the resistor arrays without damaging the system by supplying a relatively low current to the SLEDS. The system is able to take

in any DVI input image and output that image on the SLEDS array. This enables the user to use a software interface to program the projector and display required images.

The main issue with the IR LEDs (light emitting diode) used in the SLEDS array is the power dissipation which is 90 percent. This figure is similar to the power dissipation seen in the first generation LEDs of the 19xx . This dissipation rate can lead to the system getting overheated and functioning abnormally.

This work consists of a detailed description of the heat effecting the SLEDS projector and how the system copes with the excessive heat. Several tests have been developed and run on the system to understand its strengths and weaknesses. The LED pixels have been corrected for non-uniformity after fully developing and testing the system. The impact of these tests on the system will be discussed and explained. Current goals for our SLEDS technology is to reach frame rates of up to 1 kHz and two frequencies of emission (colors), without overly heating the system and saturating the pixels.

1.2 Motivation

Today's IR Scene projection landscape is dominated by a technology based on Thermal Pixel Arrays (TPA) and supply temperatures in the mid-wave infrared up to only ~ 400□C at maximum frame rates of 200Hz. Goals of this project are to move past the limitations of TPAs using IR light-emitting diode technology. LEDs are inherently capable of very fast frame rates, relying on electronic transitions between energy bands in a semiconductor, rather than thermally generated quasi-blackbody

radiation from TPAs. Frame rates of the SLED arrays are effectively restricted only by the read-in integrated circuit (RIIC) and drive electronics. The electronic feature of IR LED emission allows the IR LED to be outstandingly more efficient than emission from TPAs [3]. Preliminary results show IR LEDs can reach higher temperatures than TPAs. LEDs also exhibit a narrower bandwidth emission compared to blackbody radiation. However, by fabricating an emitter array from two or more distinct LEDs in each pixel, an LED array can emulate subtleties of a broader band or multi-band source [5].

The current fully functioning system is the result of many years of SLEDS development. Previous work includes the development of a 64x64-pixel array which is described in Rodney McGee master's thesis [1]. The current system is constructed on lessons learned from previous systems and the requirement for newer features. Fully redesigned drive electronics have been developed and several versions of code and hardware have been implemented to reach an entirely operating system. In the past years, the SLED system has experienced several new developments and tests which has led to its transformation. These tests will be further discussed in this paper.

Chapter 2

SYSTEM OVERVIEW

2.1 3x3 System Example

This section will explain how the smaller components of the SLEDS system work together to make the system. An overview of the system will be given, starting with the read-in integrated circuit (RIIC) and SLEDS, as well as the main LED driver.

The SLEDs array is made out of 512x512 pixels, and each individual pixel is an infrared light emitting diode. IR LEDs work just like the regular LEDs in that they get brighter as their input voltage is increased. In this section we will be discussing a 3x3 pixel RIIC. The same concept is used in the entire array and is valid for any size array.

In order to turn on a single pixel, the address of the pixel along with the appropriate voltage should be given to the driver. The voltage will control the brightness of the pixel. Figure 2.1 illustrates this idea.

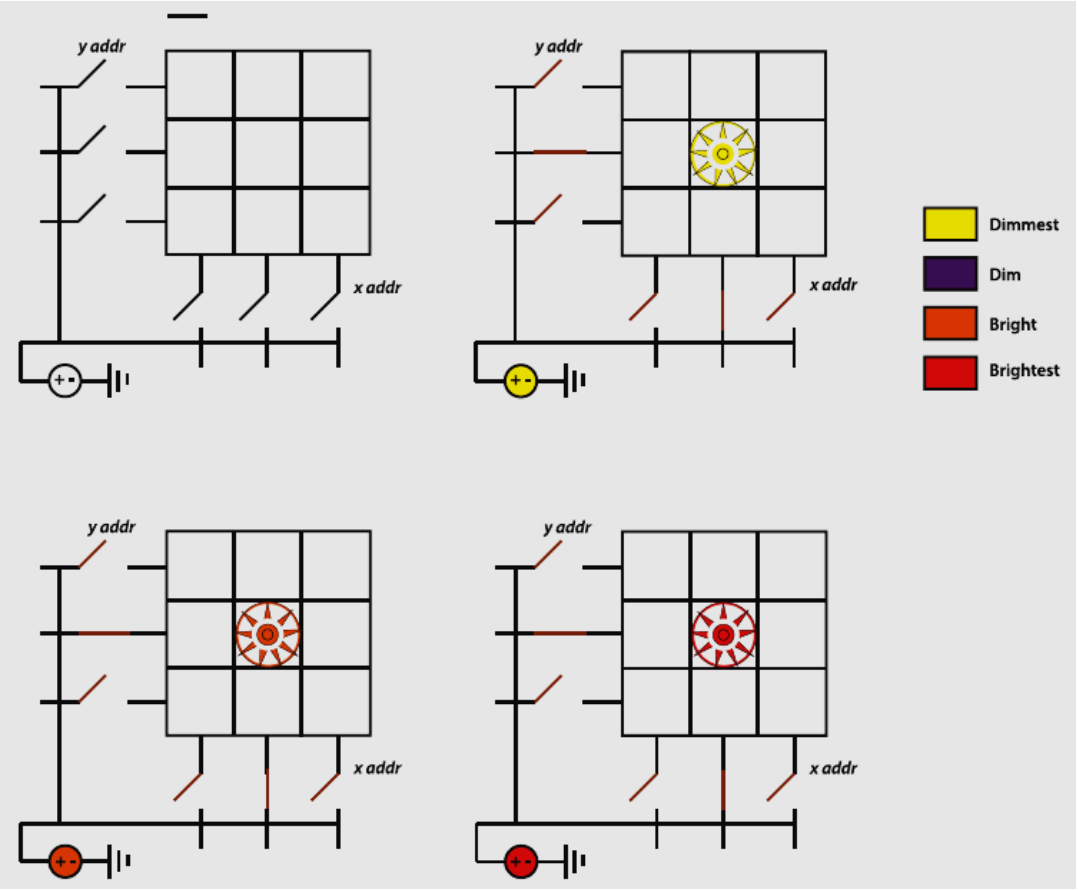

Figure 2.1: 3x3 pixel RIIC

Figure 2.1 illustrates how to operate a single pixel at different brightness levels. As shown in the Figure 2.1, each pixel gets a y address and a x address that corresponds to its location in the array. Once the appropriate switches for the x and the y locations are closed, then the appropriate voltage will be supplied to the pixel which then will cause the pixel to light up.

The brightness of the system can be changed through the amplifier and the digital to analog converter (DAC) that are in the system. The amplifier converts an

analog current signal to a voltage signal at a desired range. The analog current signal is supplied by the DAC, which converts a 16-bit digital input into a corresponding output current. Using this technique, the emission brightness of the SLEDS is controlled by digital values and not analog inputs. Figure 2.2 shows how a digital input signal can be used to control the brightness of each individual pixel. For example, it can be seen that sending zeros to the DAC will cause the pixel to turn off.

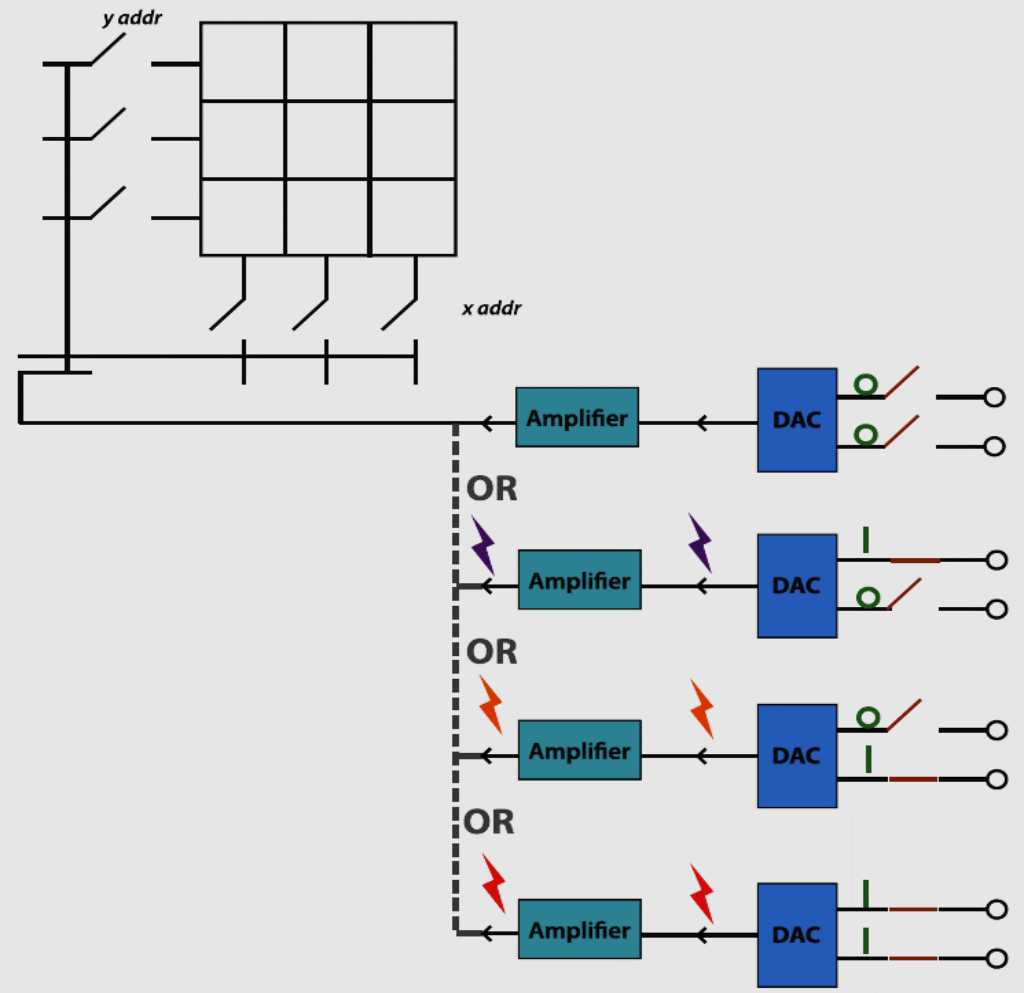

Figure 2.2: DAC, amplifier, and the RIIC with a changing digital input

The question now is where does this binary signal and the address of the pixel come from? Xilinx ML605 FPGA board uses the hardware description language or HDL to control signal and the address of the signals. The DAC and the amplifier board could not connect to the output of the ML605 board directly, so in order to solve that issue an interface board was used to connect these interfaces together. The ML605 board uses Microblaze to allow users to program the board using C programming language. Figure 2.3 graphically shows the connection between the FPGA board, the DAC, the amplifier, and the RIIC.

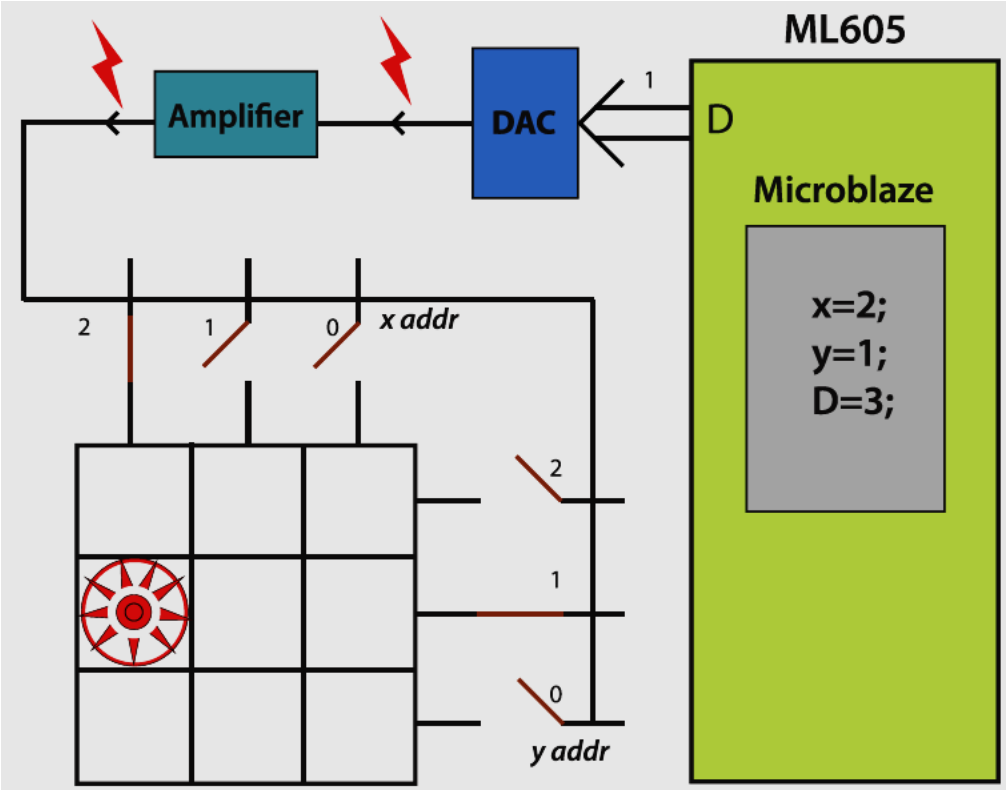

Figure 2.3: ML605 driving the system

Since the SLEDs system is a projector, it needs to be able to project from another device other than the Microblaze. In order to make this system into a complete projector a DVI interface allows the user to send any inputs from their system through DVI to the ML605 board and the projector will show the input. A simple example of the DVI mode setup is shown in Figure 2.4 below.

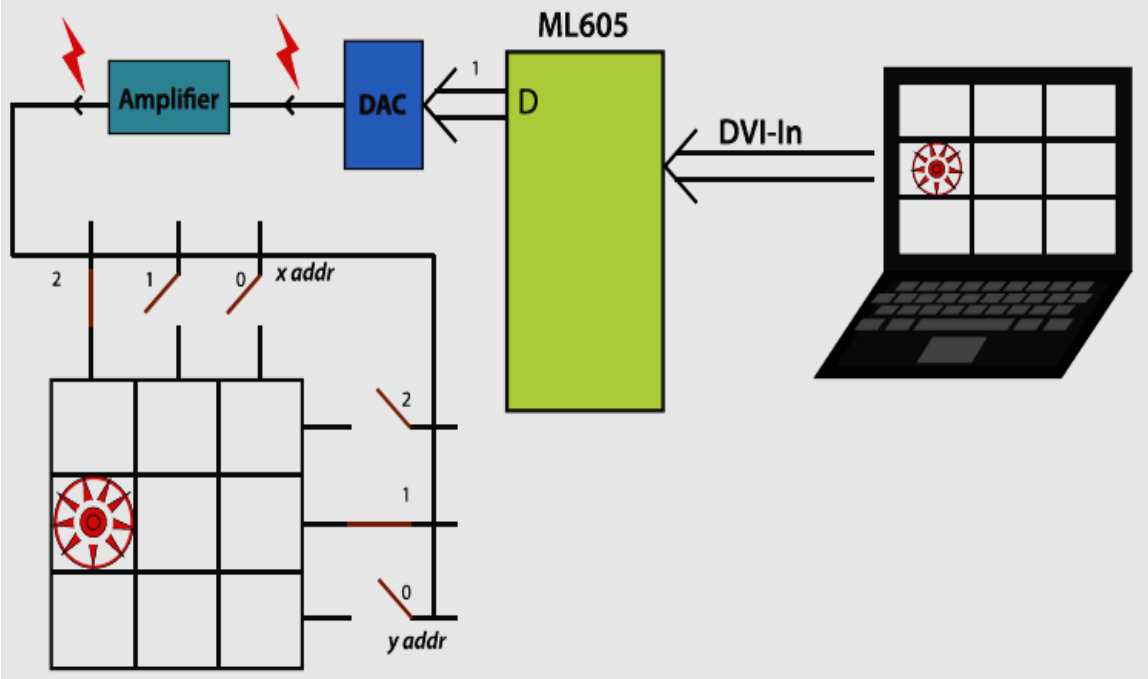

Figure 2.4: DVI input to ML605

Chapter 3

SYSTEM COMPONENTS

3.1 Pixel

Each LED consists of 10V CMOS pass transistor pairs, which are used to pass the analog input to the drive transistor as shown in Figure 3.1 below.

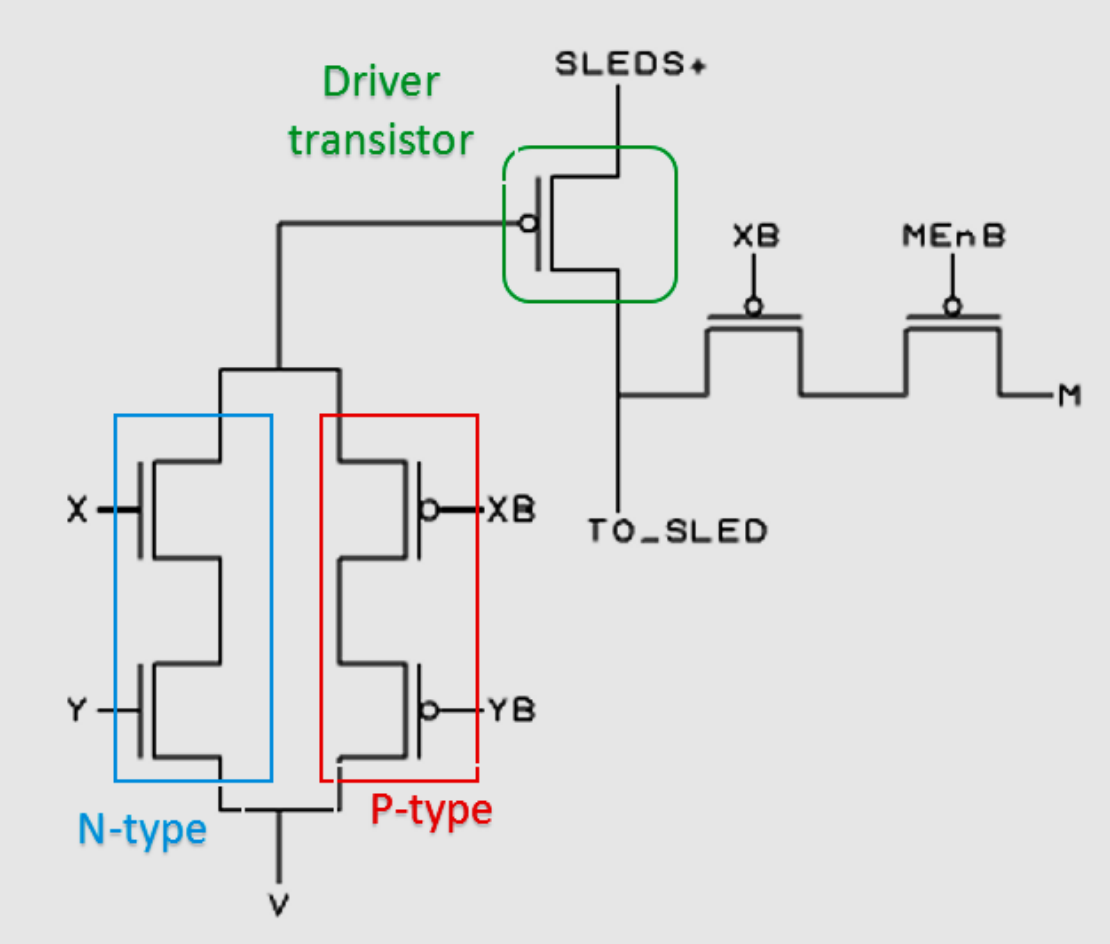

Figure 3.1: Single pixel schematic

Pass transistors shown in Figure 3.1 consist of both N type and P type MOSFETs in parallel, and can be used to pass Low and High voltages without any issues. For example, by looking at Figure 3.1 we can see that in order to turn on a pixel at high intensity the XB and YB values need to be used. In order to test the LEDs, the two transistors XB and MEnB were implemented in the pixels.

3.2 RIIC

The LED driver of the system is called a Read In Integrated Circuit (RIIC). The RIIC controls each LED with a controllable current signal which is provided externally. This driver was fabricated using On Semiconductor's C5N process [3]; a three metal, 0.5μm CMOS process with thick oxide, and lateral high-voltage transistors. Each individual LED driver circuit occupies an area of 48 x 48 μm^2, matching the SLEDS array, and connects to the LED anode and cathode terminals using 15μm high contact pads to minimize thermal and electrical impedance between the SLEDS and RIIC [4]. The RIIC is shown in Figure 3.2.

The RIIC driver chip is split into 4 different quadrants and is stitched up to make the bigger chip. Each quadrant consists of 256x256 pixels and all four quadrants together can make the 512x512 SLEDs array. The RIIC was processed on an 8-inch silicon wafer, and a total of 19 good RIICs were obtained from this wafer.

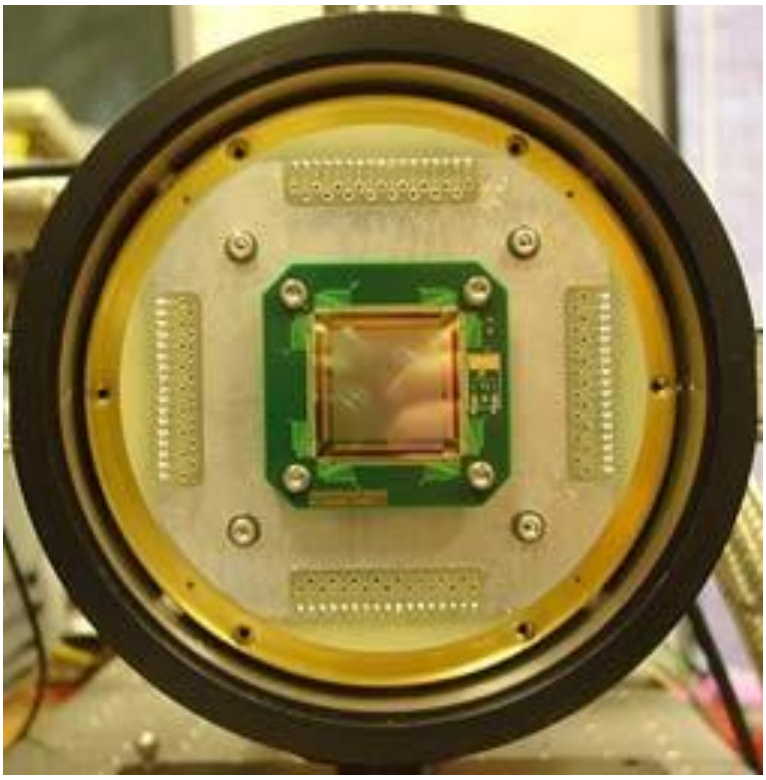

Figure 3.2: RIIC mounted in a Dewar

The operating temperature of the RIIC needs to be 77 degrees Kelvin. In order to reach that temperature, the RIIC needs to be placed in a Dewar filled with liquid nitrogen. In order to connect the pins of the RIIC to the output pins of the Dewar, a PCB board was made to handle this task. The board has 20 digital lines, 4 analog lines as well as the power lines [6]. Figure 3.3 shows the PCB board and Figure 3.4 shows the pin layout and the picture of the Dewar. In order to reach each pixel in the 512x512 RIIC, 32-bit address lines were needed. However, to decrease that number we introduced 4 pre-charge lines that control each quadrant individually and then the address lines were reduced to 16 bits. Since all quadrants share the same address lines, we can turn up to 4 pixels on at the same time.

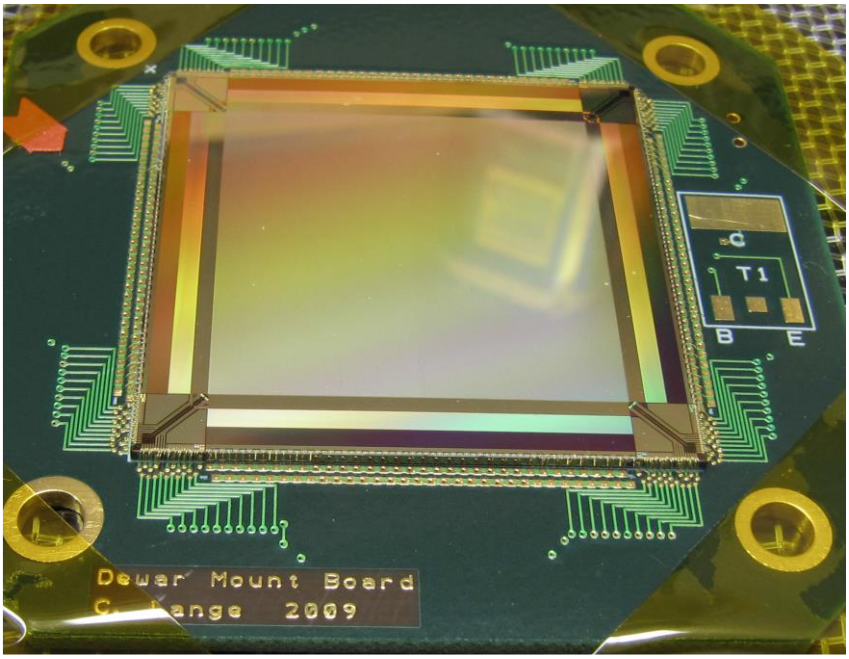

Figure 3.3: RIIC on PCB

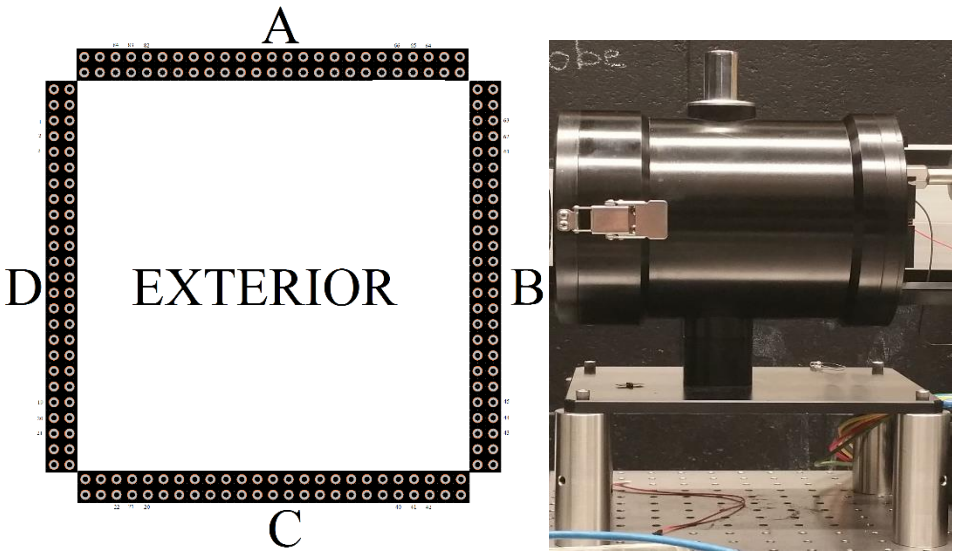

Figure 3.4: Dewar and its pin layout

3.3 Interface Board

The SLEDs Interface board plays a huge role in the system. It acts as the glue between each component in the system. The interface board needs 10V to 12V of power which is then used to power up the RIIC, DAC Evaluation board and the DAC amplifier board. As shown in Figure 3.5 there are connection pins to the ML605 connector, which can be used to level shift the digital lines from the ML605 from 2.5V to 5V. The connector is also used so that the ML605 can control the software breaker implemented in the system to keep the system from over drawing current and keeping it safe. Four SMA cables bring in the analog lines from the DAC Amps. All the signals are routed to the Dewar with ribbon connectors using the connection pins that go in to the Dewar.

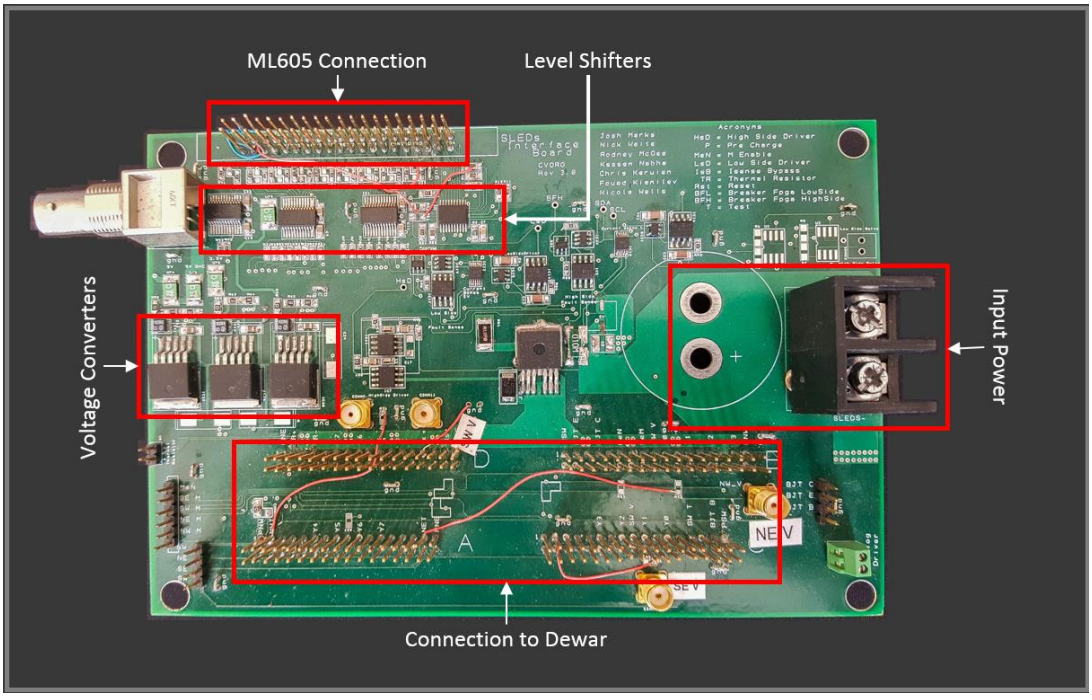

Figure 3.5: Interface board

3.4 AD9747 Evaluation Board

The AD9747 Evaluation board contains an AD9747 dual DAC chip manufactured by Analog Devices. In order to program the DAC chip, the program from the Analog Devices alongside with a computer and a USB cable is needed. Figure 3.6 shows this DAC evaluation board.

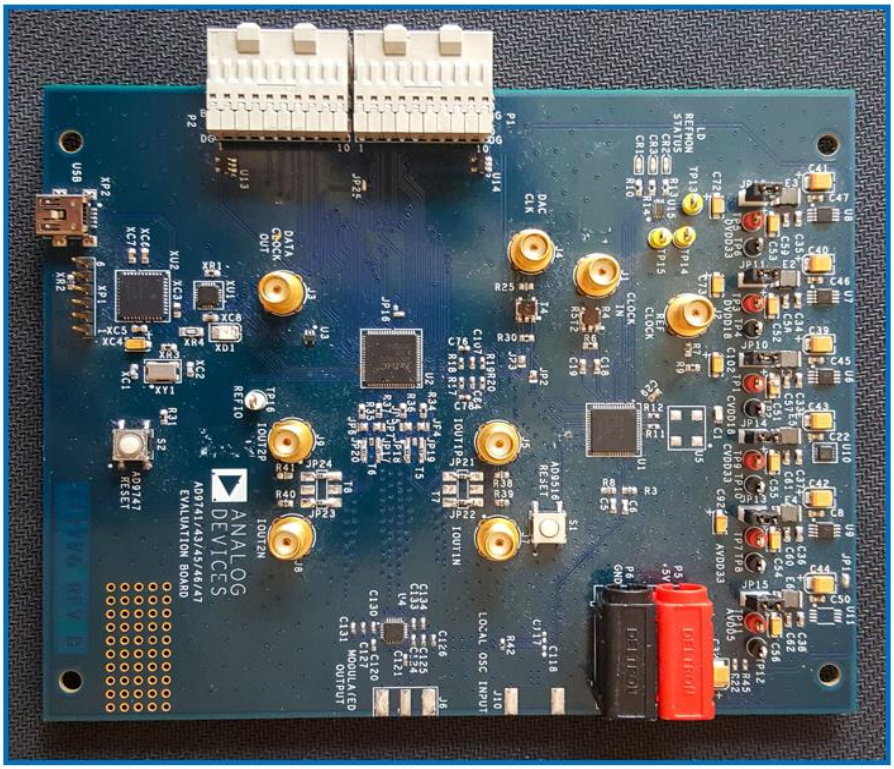

Figure 3.6 : DAC evaluation board

This Particular DAC has programmable current outputs as well as a high dynamic range. The DACs output current which is very useful for controlling the LEDs digitally. More details about the DAC Evaluation board can be found in Kerwien's thesis [2].

3.5 Analog Amplifier

As mentioned in the last section, the DAC Evaluation Board outputs current, however the LEDs require a voltage as an input. In order to run the system an amplifier is required. Figure 3.7 shows the analog amplifier designed by our team to satisfy the low noise, high speed requirements to run this system. The amplifier includes a TH6012 op-amp from Texas Instruments. The main job of the amp board is to amplify each output current line form the evaluation board to its corresponding voltage value. The SMA connector on the board are used to transmit the output of each channel to the interface board [7]. To account for the highly capacitive load of the SLEDs hybrid the design has a tunable RC snubber for output edge damping [8].

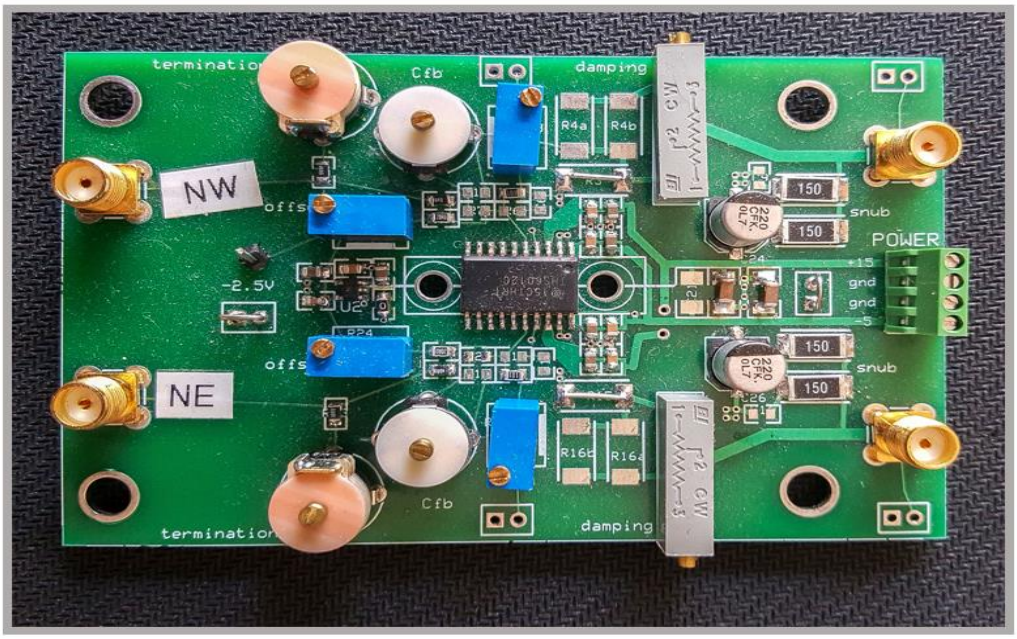

Figure 3.7: Amplifier board

3.6 ML605 FPGA

A Field Programmable Gate Array or FPGA, is the most important single element in this projector unit. The FPGA unit allows us to connect the hardware to the software interface. It also allows us to programmatically drive signals depending on the desired outputs. Xilinx provides their software in order to allow users to program their FPGA boards. The two main component in their software are the EDK (Embedded Development Kit) and SDK (Software Development Kit). The EDK unit allows us to design the VHDL peripherals, and the SDK unit allows us to use the VHDL language to develop the desired firmware. Figure 3.8 is an image of the FPGA board used in the SLEDs system. The two FMC slots are used to debug and then run the system through the DVI cable. An in depth description of the functions provided by the ML605 FPGA board can be found in Kassem Nabha's Master's thesis [9].

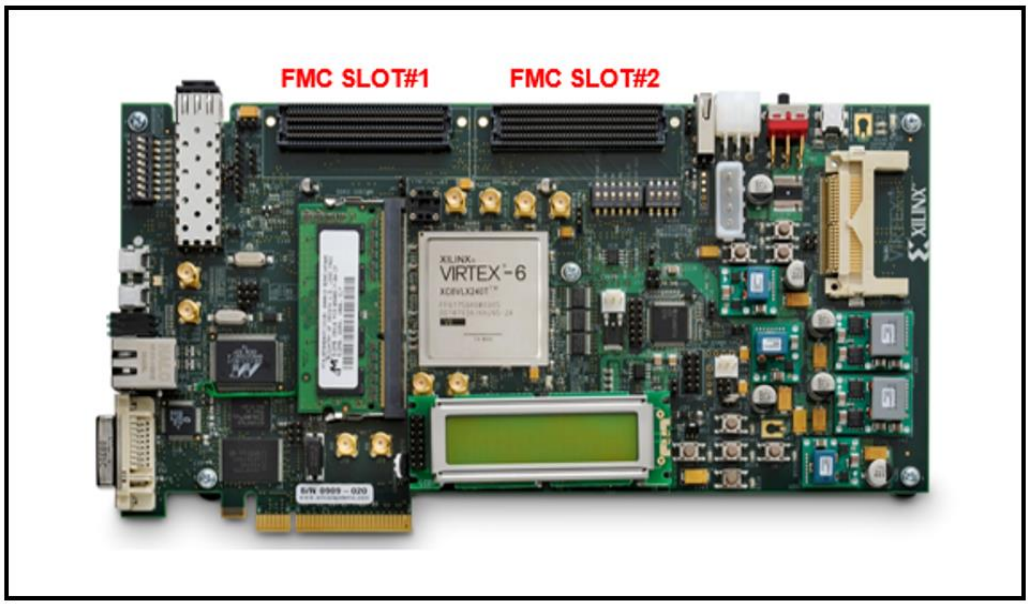

Figure 3.8: ML605 FPGA

3.7 Complete System

Figure 3.9 shows all components of the system connected together and operating as a system. The projector has 512x512 pixels running at 100HZ. The power supply supplies power to the interface board, which then is used to light up every single pixel in the Dewar. The Dewar helps to cool down the chip, since 99.7 percent of the power put through a pixel is converted to heat due to the current technology of the LEDs.

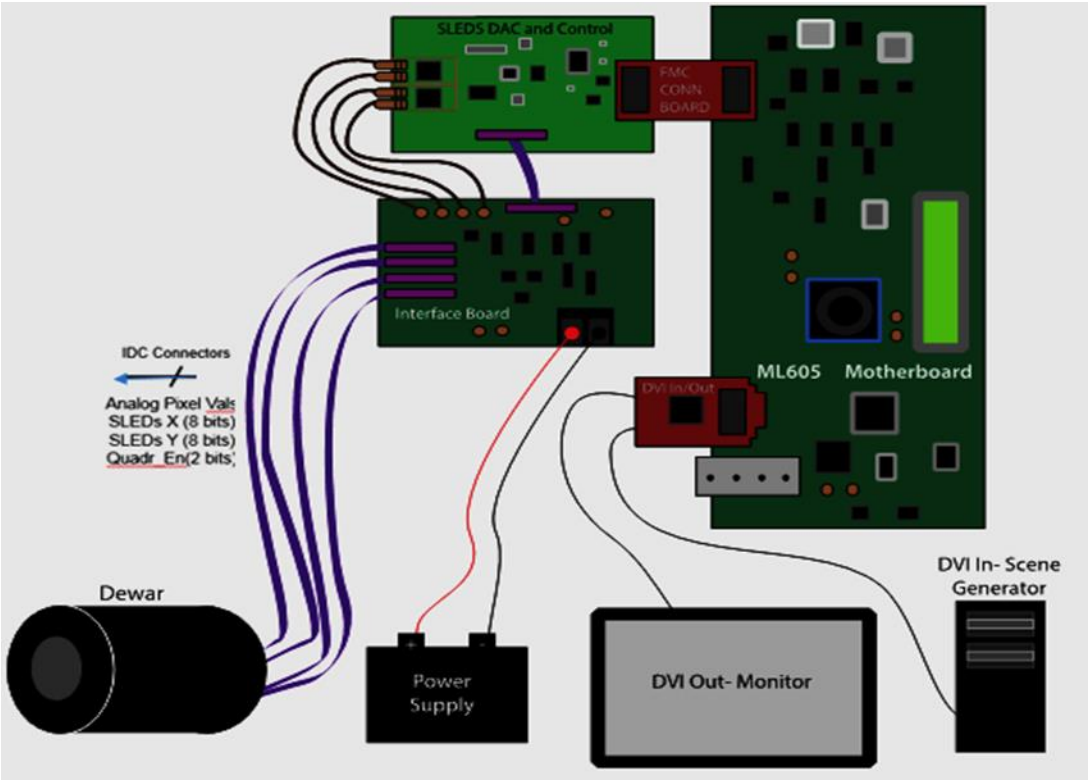

Figure 3.9: Complete system

3.8 Camera

One of the main components for testing of the system is the camera. Due to the characteristics and wave lengths of IR LEDs, the light they produce is not visible to the naked eye Therefore, an IR camera is required in order to observe how the LEDs light up on the array.

A FLIR SC8200 camera was purchased in order to test the 100HZ SLEDs array. This particular model works in the 3.0-5.0 μm spectral range. The resolution of the camera is 1024x1024 and it has a detector pitch of 18 μm. The camera can be controlled through RS-232, camera link, usb and Ethernet. Currently we operate the camera through Ethernet and camera link. The frame rate at full window is 133 Hz, but that can be increased if the user chooses a smaller window size. Figure 3.10 shows a picture of the FLIR camera looking at the Dewar. [10]

Figure 3.10: FLIR Camera

The FLIR camera software can be used to take single frames but in order to take multiple single frames sequentially, the software cannot be used and a capture card is needed. The camera link card is used to gather many sequential images to gather information. Vision Link F4 is a 4-lane PCIe frame grabber with two camera link connectors. It has an internal memory of 256 MB that can be used to store the image files in it for fast camera capturing [11]. The EDT software that comes with the capture card can be used to setup and configure the camera link frame grabber. In order to capture frames quickly, a batch file was written that automatically configures and runs the EDT software through the command prompt window.

Chapter 4

SLEDS TESTING

4.1 LED Current Testing

Light emitting diode brightness and output current have a direct relationship. To increase light output, higher current is needed in each LED pixel, leading to the generation of more waste heat. Since the SLEDS package was not designed with heat removal in mind, the array heats up quickly, adversely affecting the emission. To better understand and negate this effect, further work is needed in evaluating and improving our models.

For testing, breakout pads were added to corner pixels allowing for monitoring of voltage and current. In the SLEDS system, the pixel current is driven by the voltage level on a drive transistor, controlled by a digital to analog converter (DAC). In order to get an accurate reading for the voltage and the currents at each DAC count (DAC output level), the voltages and the currents were measured 10 times and the mean value was used. A Keithley was programmed and used and to measure the voltage, and python code was developed that could accurately read the current. Figures 4.1 and 4.2 illustrate the results of this test. The block of 9 pixels shows a more averaged and expected result [12]. Table A.1 in Appendix A can be used for further information about the relationship between current, voltage and dac-count.

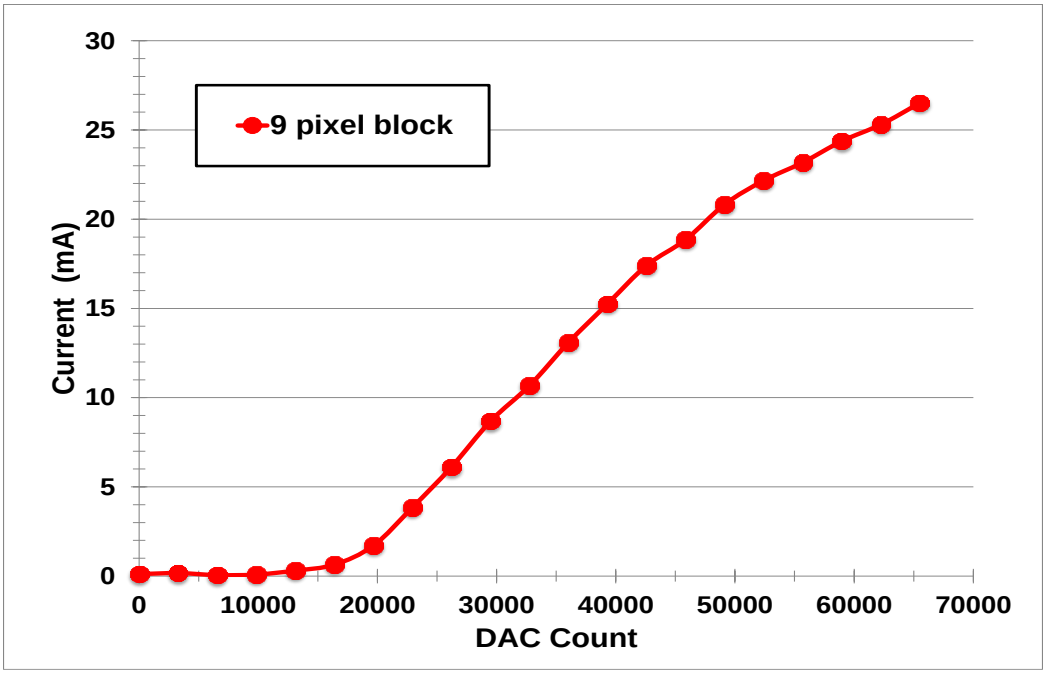

Figure 4.1: Current per pixel as a function of DAC Count.

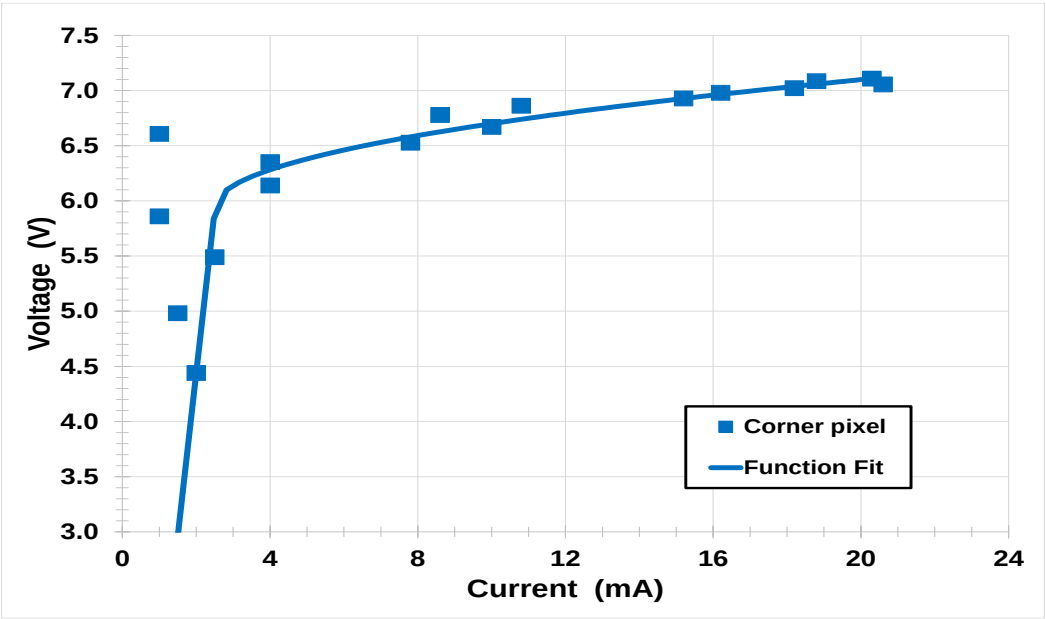

Figure 4.2: Voltage as a function of current for a small block of pixels.

4.2 Luminance Testing

The intention of the Luminance Testing is to measure the effect of heat over time on a single pixel. Four different duty cycles and nine different brightness levels were used. For each test, 9000 frames were collected and every 1000 frames the DAC count is increased.

A FLIR IR camera was used to capture the raw images, and Python code was used to sum the background in each of the images and graph the data. Figures 4.3 through 4.7 show the result for each duty cycle. All the zeros and off frames have been removed for clarity. Each graph shows a different duty cycle, at the same DAC counts. The last graph includes all duty cycles in 1 with background subtraction.

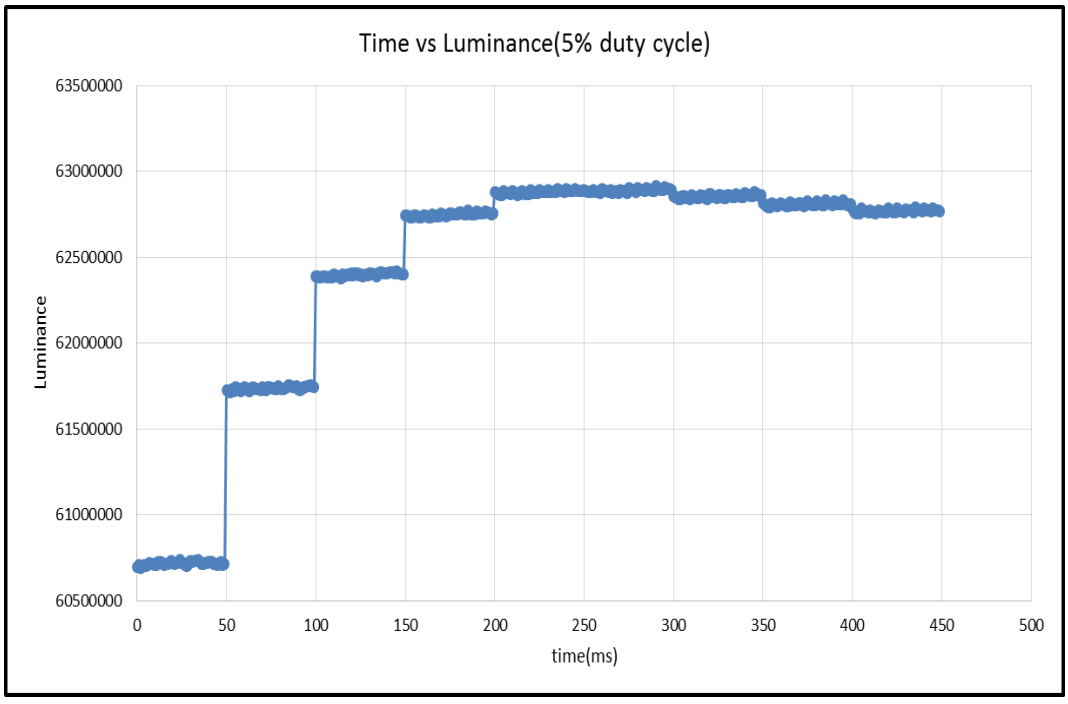

Figure 4.3: Time versus normalized luminance at 5% duty cycle

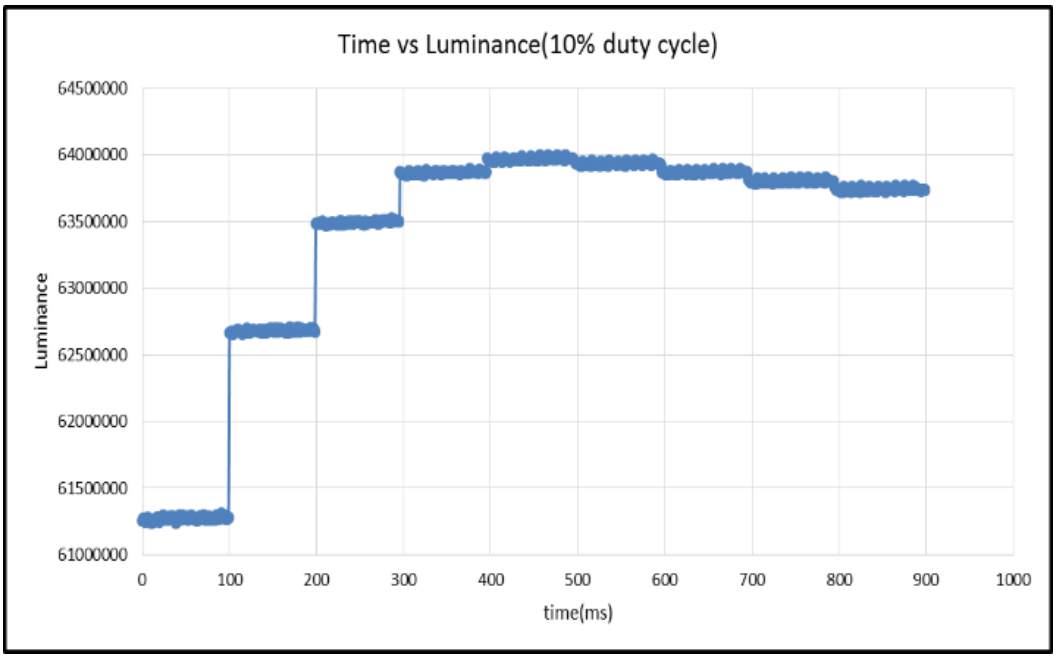

Figure 4.4: Time versus normalized luminance at 10% duty cycle

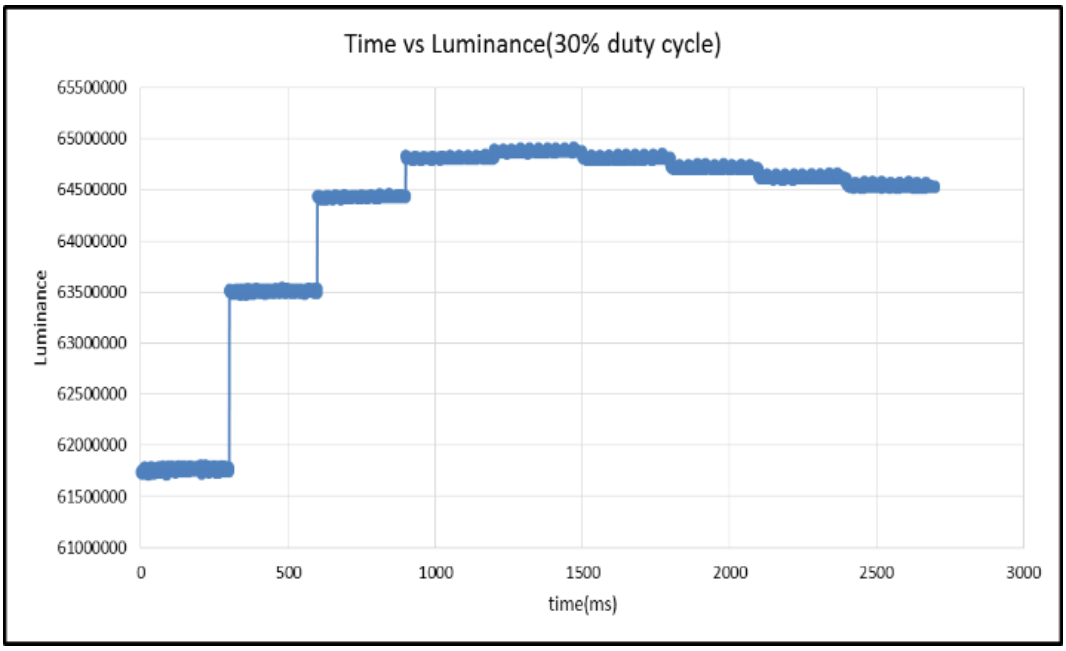

Figure 4.5: Time versus normalized luminance at 30% duty cycle.

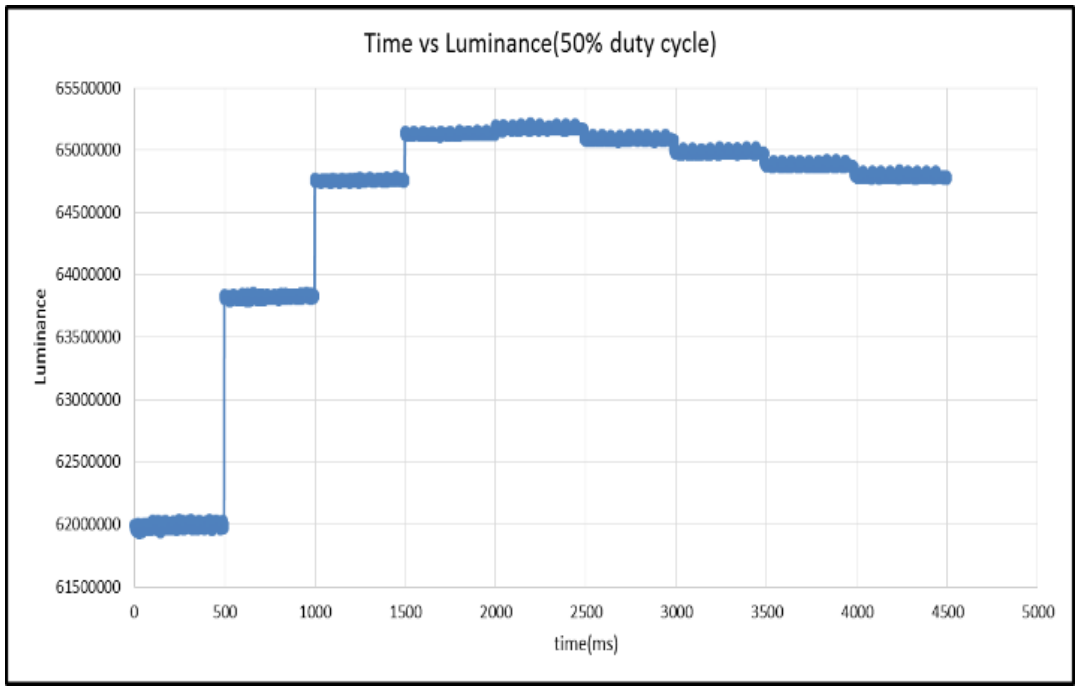

Figure 4.6: Time versus normalized luminance at 50% duty cycle.

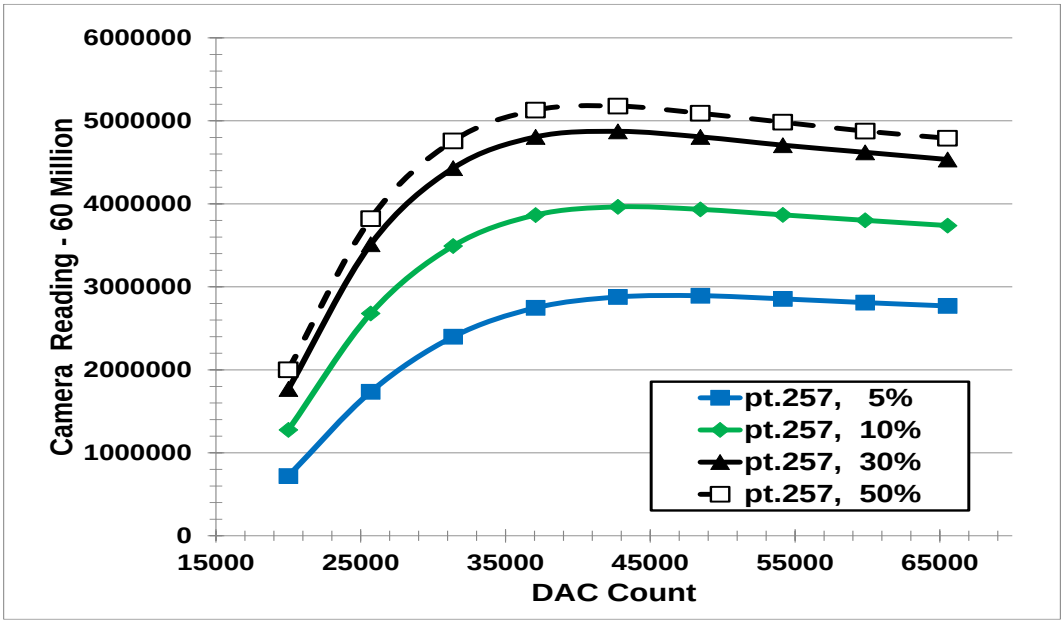

Figure 4.7: Time versus normalized luminance comparison.

4.3 Luminance Reduction

Previously it had been observed that pixels decrease in brightness with time. To confirm this and determine its extent, the system was operated for 120 seconds continuously.

For this test a group of about 75 pixels were lit up and kept on for 120 seconds. The starting intensity was at 6666_{16} and after each test it was increased by 3333_{16} until the full brightness of $FFFF_{16}$ was reached.

The luminance versus time data were captured using the FLIR camera and the raw images were processed using python code and the results are shown in Figures 4.8 through 4.10. After each test, to ensure removal of heat generated from the previous test, the system was allowed to cool down for 5 minutes before running the next one.

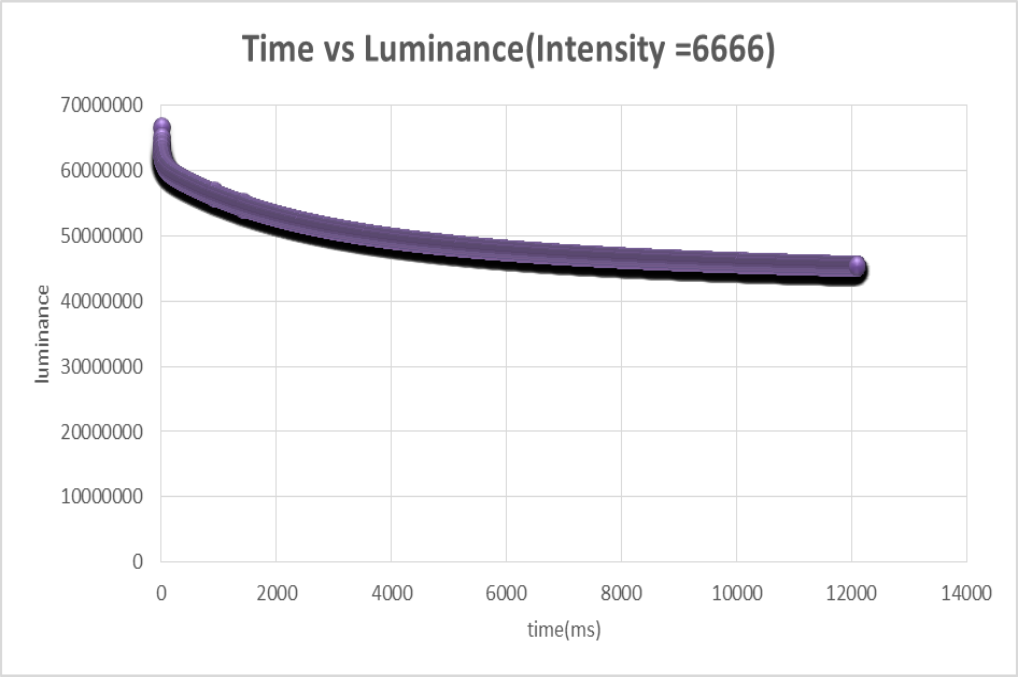

Figure 4.8: Time versus normalized luminance at Intensity 6666.

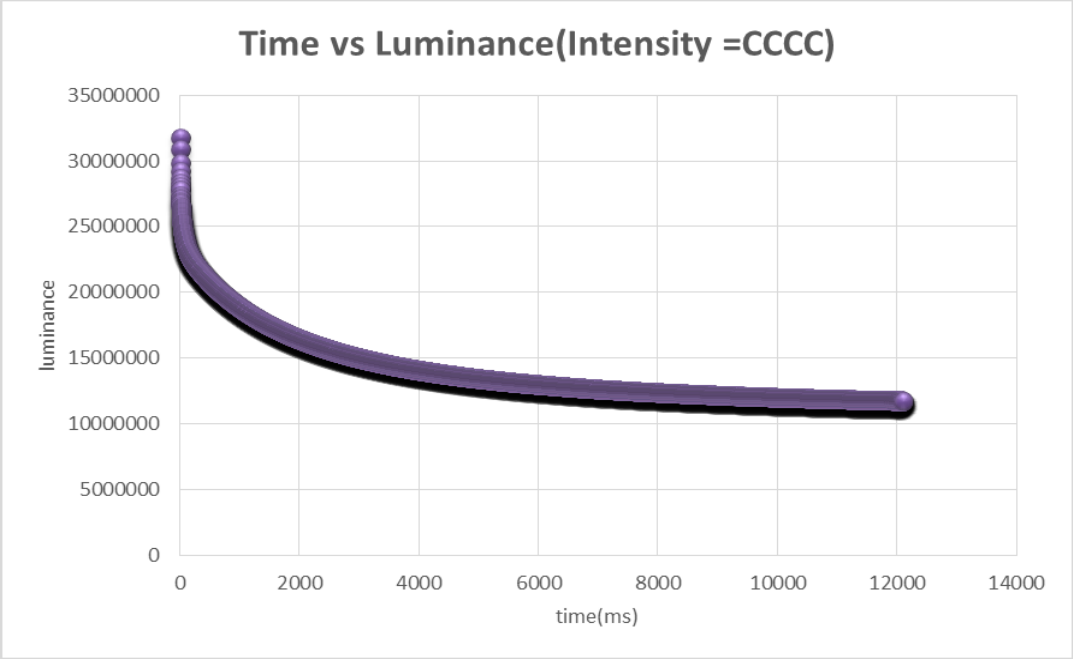

Figure 4.9: Time versus normalized luminance at Intensity CCCC.

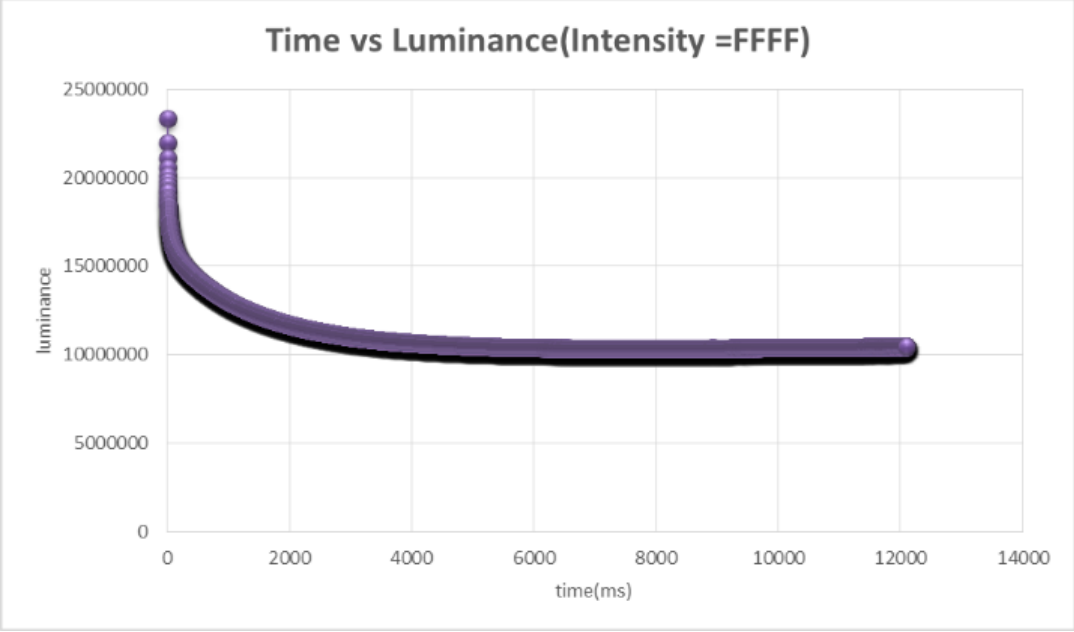

Figure 4.10: Time versus normalized luminance at full brightness

The diameter is in pixels and represents the size of the area lit up. The intensity in DAC counts increases with each test. The results indicate that as the DAC count increases the change happens quicker and pixels lose luminance faster. The suspected reason for this behavior is the poor performance of the current cryostat in cooling the SLEDS array. Also, the thermal impedance between the array and the cold finger was too high. These issues are being corrected in future SLEDS systems [13, 14].

4.4 Stair Step Test

In order to better understand the previous tests, stair step tests were conducted and compared for similarity to the duty cycle tests. Each DAC count was recorded one frame at a time to presumably remove all thermal effects.

The stair step test includes the DAC count of each pixel, the data that was processed from each individual raw image, and the measured current for each frame. Originally it was decided to use one of the corner pixels to measure the voltage of the pixel while being tested. However, due to the wire bonding around the pixel, there was no clear image due to reflections. As a result, one of the pixels in the middle was used to complete this test. Figures 4.11 and 4.12 illustrate the results. The DAC count is changed and reset to record luminance without thermal effects.

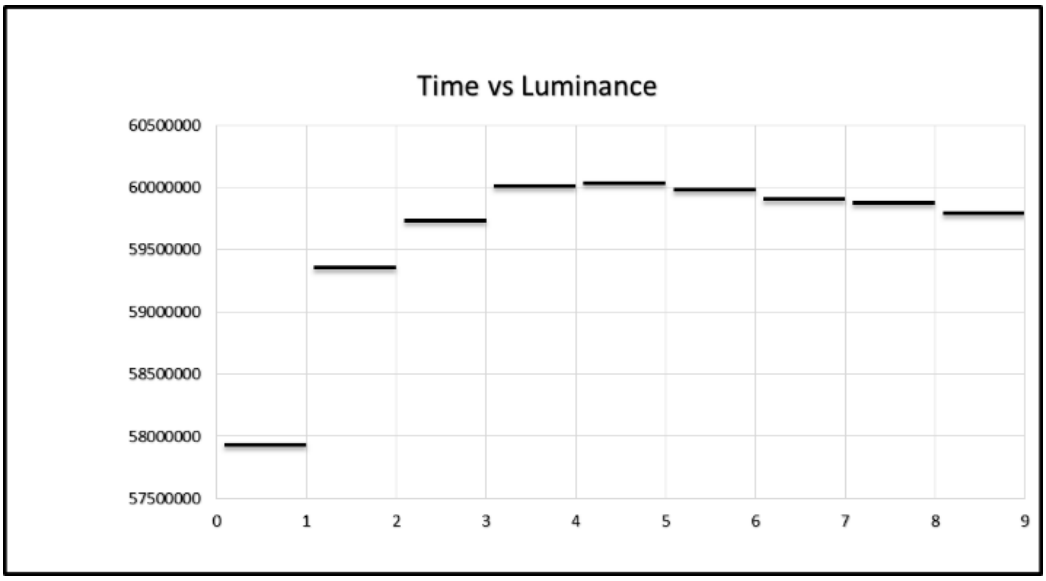

Figure 4.11: Stair step test

Dac count	current mean(mA)	current min(mA)	current max(mA)	data
0	1	0	5	57015870
20000	2	0	15	58047813
0	2.5	0	5	57011909
25691	3.5	0	15	59511626
0	1	0	5	57016278
31382	3.5	0	10	59854288
0	2.5	0	10	57018102
37073	6	0	10	60136388
0	1	0	5	57019928
42764	15.4	10	23	60128670
0	0.5	0	5	57014823
48455	13.6	5	28	60089575
0	0	0	0	57015087
54146	19.8	10	28	59996490
0	2	0	10	57022414
59837	22	15	35	59951980
0	2	0	10	57017280
65528	18.5	10	28	59888523

Table 4.1: Stair step table

4.5 DVI

The SLEDs system is capable of running in the DVI mode, similar to any other functional projector. In order to get the system to the DVI mode, a couple of steps are required. After the system is turned on, the DACs need to be initialized and then the correct bit file should get uploaded to the system. At this point, the system should be ready but in order to send any input to the SLEDs array, the non-uniformity correction(NUC) table should be loaded. A batch file has been written in order to automate the given steps. The batch file does the following:

- Initializes the camera
- Initializes the DACs
- Loads the bit file
- Loads the NUC table

The extras step in the beginning is important since that will allow us to look at the array as we are sending inputs through the DVI. Since the resolution of the SLEDs array is 512x512 when a computer is connected, only a 512x512 portion of the display is sent to the array.

Figure 4.12 shows that the only portion of the display sent to the array is always the top left 512x512 pixels of the screen. The input of the system only takes the top left corner of the input display each time, and for this reason we can write tests in order to test the DVI output.

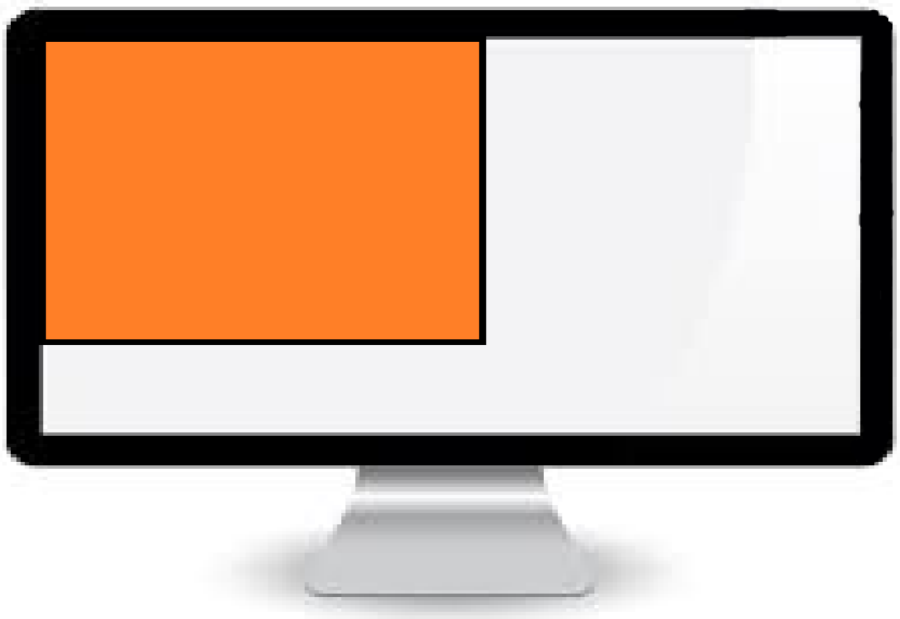

Figure 4.12: DVI screen input to the array

As mentioned above, we know where the DVI is taking its input from each time, so a python test was written to test the DVI functionality of the system. The code is under development, but at this stage it still does all the core functionalities that were required for this test. The code will create a 512x512 borderless window in the top left corner of the main display. A command prompt screen will open up as well which will let the user choose the test that needs to be run on the created window.

Currently there are 8 options to choose from and each option is fully customizable, from the size of the object to the location and the color all can be set when an option is chosen. Figure 4.13 shows the window created by this test and Figure 4.14 is the command prompt that allows the users to choose their tests.

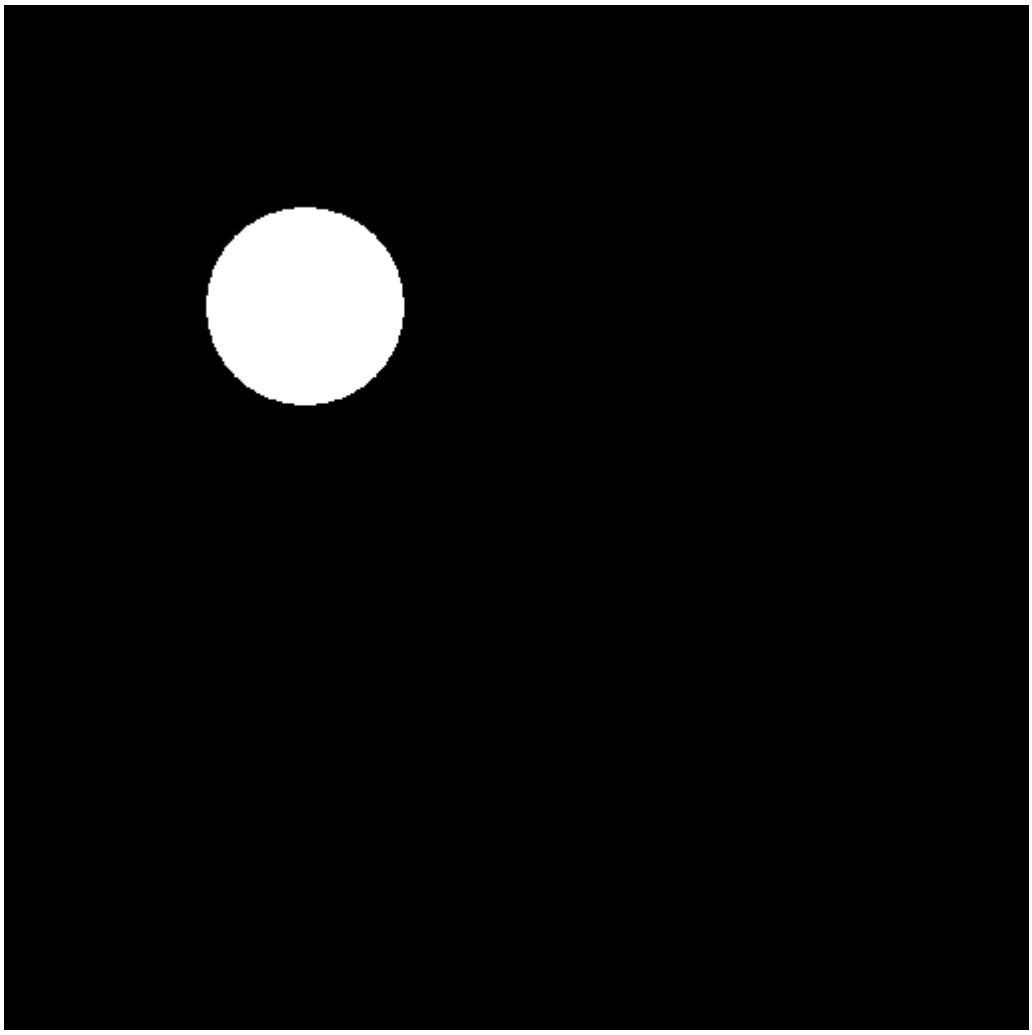

Figure 4.13: DVI test screen

Figure 4.13 is demonstrating option 1 at location x = 100, y =100, and the diameter of 100. The user has the ability to choose a value for the color of the object which is represented by three, 2 bit values for red, green and blue. In this case, all three colors have been set to the max value 255. The size of this window is exactly the same size as it shown in the picture, 512 x 512 pixels. The test was written with next

generation systems in mind, and just changing the width and height variables in the code that will allow the window to change its size.

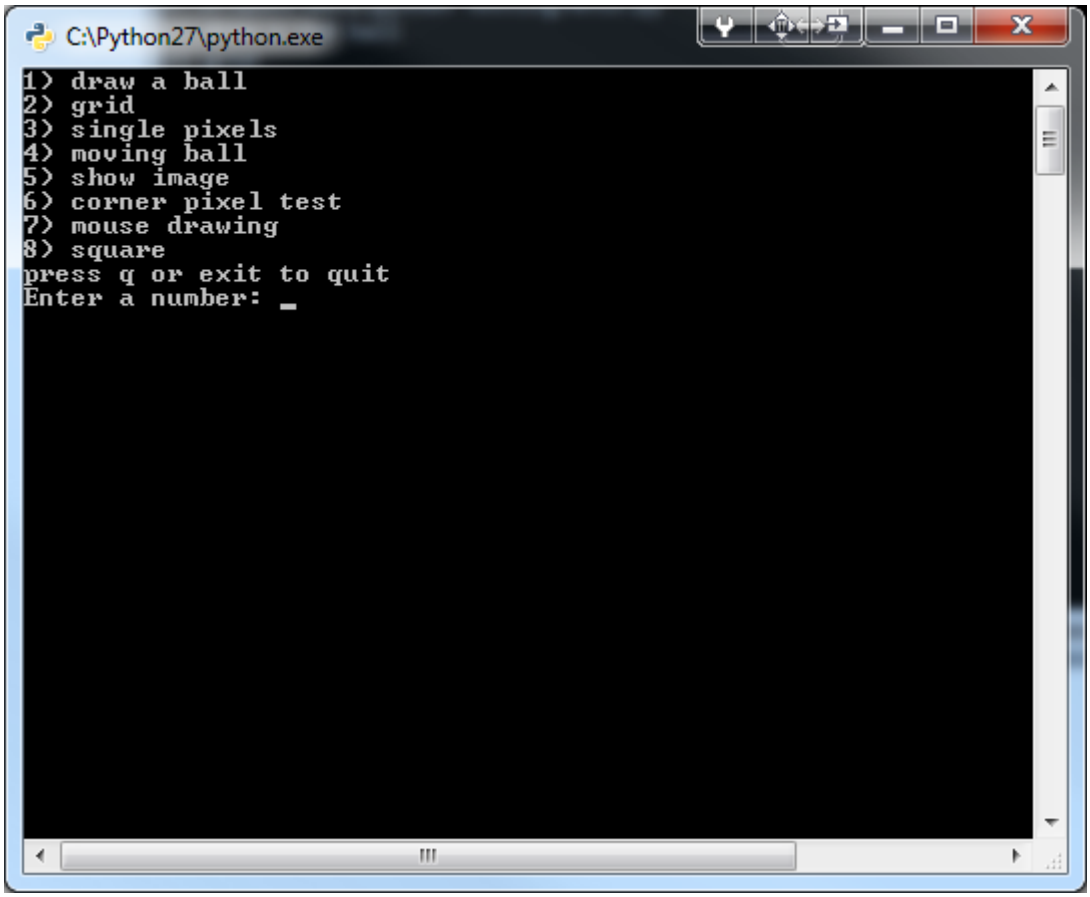

Figure 4.14: Command prompt for the DVI test screen

Previously it was noticed that when the system is running in the DVI mode, the last column and the first column of the array were misbehaving. In order to find and resolve this issue, the corner pixel test was used. A single led was lit up in each corner, one at a time, and it was checked by the camera to make sure that they light up. The

camera showed the pixel, however the dvi output was not showing the top right corner pixel which is at location x = 511, y = 0.

A code was developed to read the DVI buffer and display its output into an excel file, and then the results were compared to the results seen on the camera and the DVI output screen. These results were used to solve the previously seen problem in the DVI mode.

4.6 Single Element Detector

Single Element Detectors (SED are basically low resolution with high accuracy cameras, that can be used for variety of reasons. The purpose of using a SED in our testing is to verify the data taken from the camera is reliable. In many cases the data taken from the FLIR camera was different than what we thought we should get and so the usage of a single element detector seemed to be a great alternative to the camera, and a source to verify whether the data taken from the camera is correct or not.

The single element detector used for testing the 100HZ system is a ls-040-E-LN4 module. This module has a bandwidth of 2500 Hz, a 60-degree nominal field of view, can hold liquid nitrogen for up to 12 hours and the detector type is a InSb photodiode [15]. Figure 4.15 shows the single element detector and figure 4.16 shows the amplifier made for this detector.

Figure 4.15: Single element detector

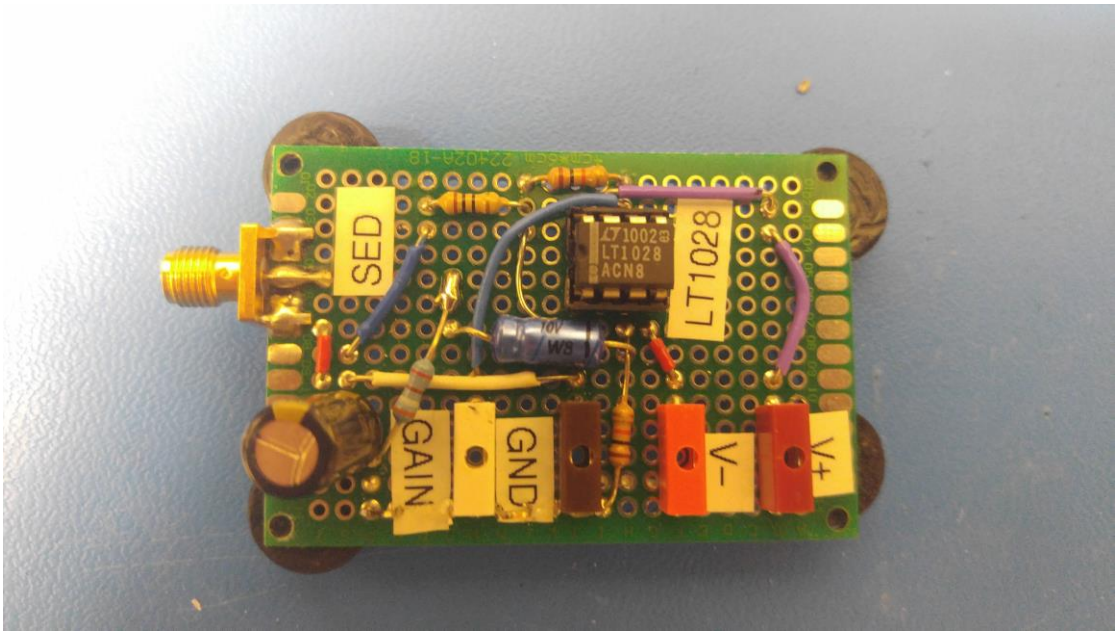

Figure 4.16: Amplifier for the single element detector

The SED has a DC coupled gain which means optical choppers are not required to operate the single element detector however output saturation can cause damage to the amplifier [17]. This SED can work with wavelengths in the range of 2 to 6 microns. Since the wavelength of the LEDs in the 100 Hz system is 4.6 microns this single element detector was chosen [16].

Using the single element detector multiple data sets were recorded to see if they do match up with the previous results taken from the camera. Different size squares at 100 Hz with 40000 dac-counts were used to produce the taken data from the SED. Figures 4.17 to 4.21 show the results of the taken data from the single element detector. All data was taken using pixels near location 257, 257 in the array.

Figure 4.17: 5x5 square

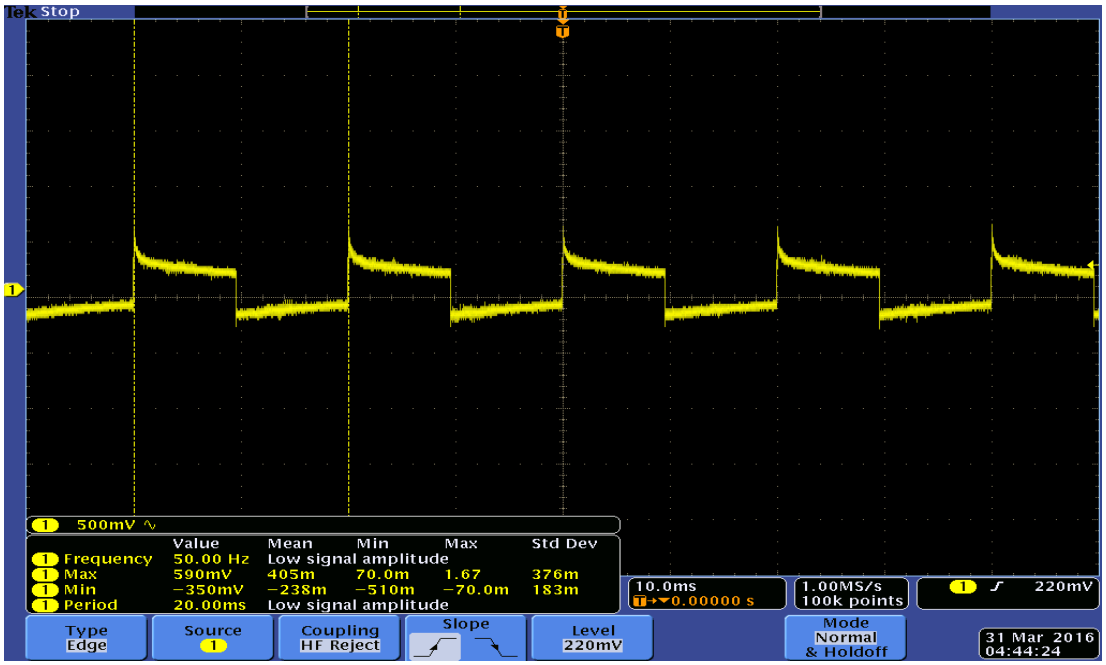

Figure 4.18: 4x4 square

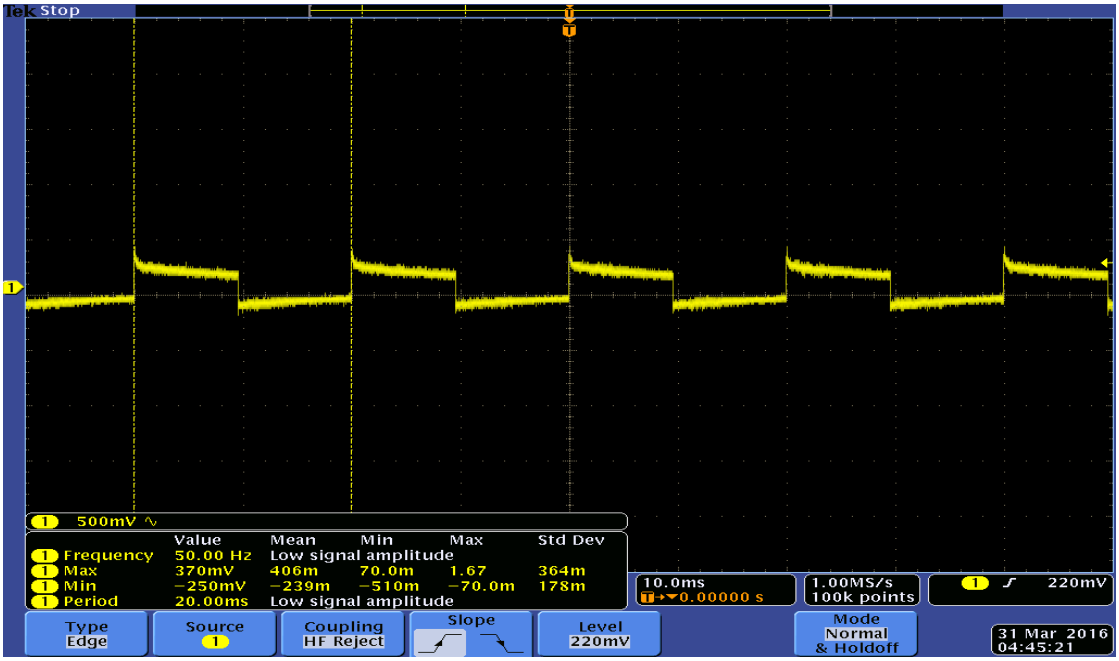

Figure 4.19: 3x3 square

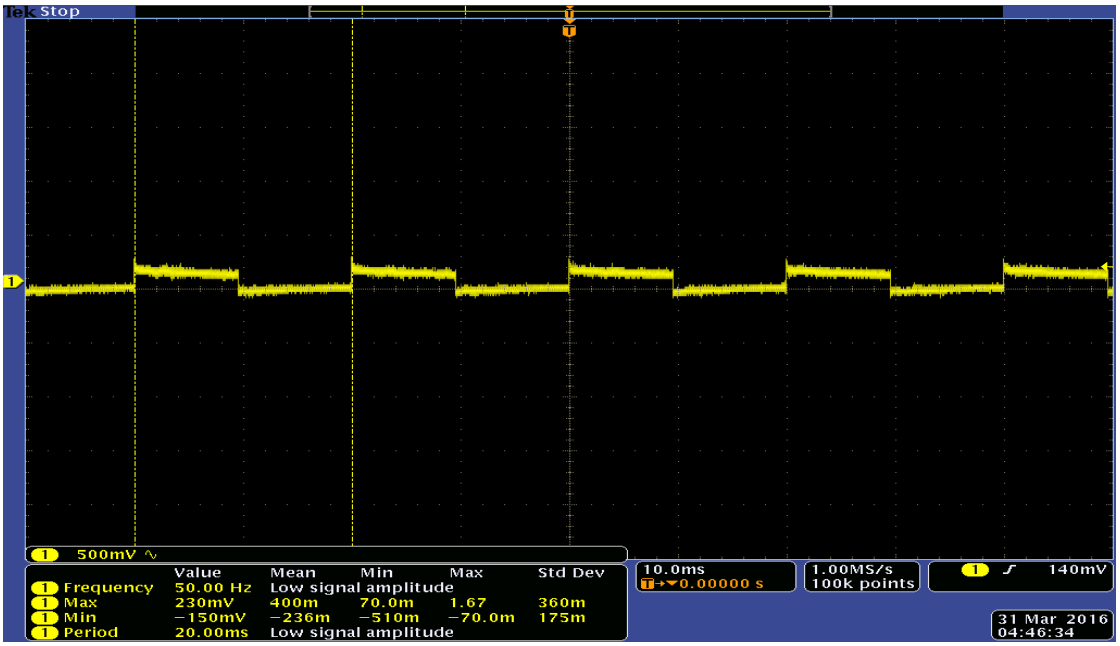

Figure 4.20: 2x2 square

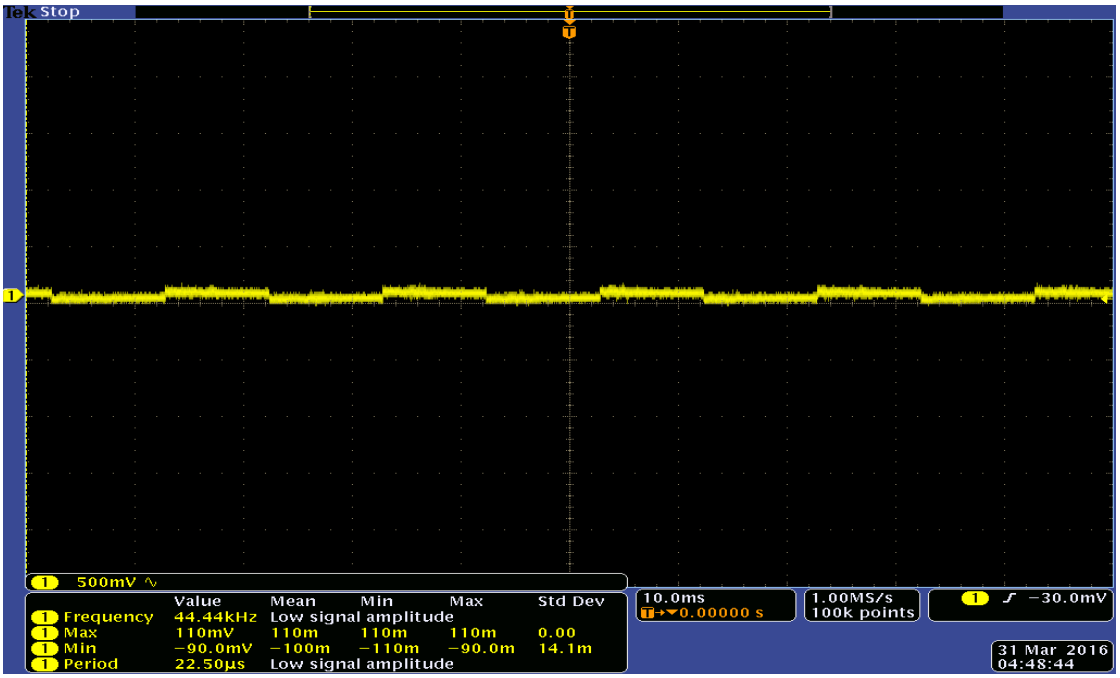

Figure 4.21: Single pixel

The results were compared with the reading from the single element detectors at the ATEC company and the results were promising. The curves were almost a perfect match. The results also seem to be matching the results taken using the camera which was the ultimate goal of this test.

Further tests will be done and the results will be taken into consideration for future comparison and resources.

Chapter 5

ADDITIONAL CAPABILITIES

5.1 1000HZ Frame Recording

The SLEDS System is capable of running at 1000HZ, for small frames like 512 x 12. For testing purposes, we would only need to capture a single pixel in a 192 x 192 and so running a single pixel at 1000 Hz was not a challenge for us.

The challenge started when we started recording the data. At 1000 HZ you can test the system 10 times faster or get 10 times more data in the same amount of time as 100 Hz, and that was our main reason for moving towards this speed. When I started testing the system at 1000 HZ, I found out that we were missing some frames. I tried the same process many times however the results were the same. Each test had missing frames but at different locations. Figure 5.1 shows the system running at 100 HZ and Figure 5.2 shows the same exact test at 1000 Hz.

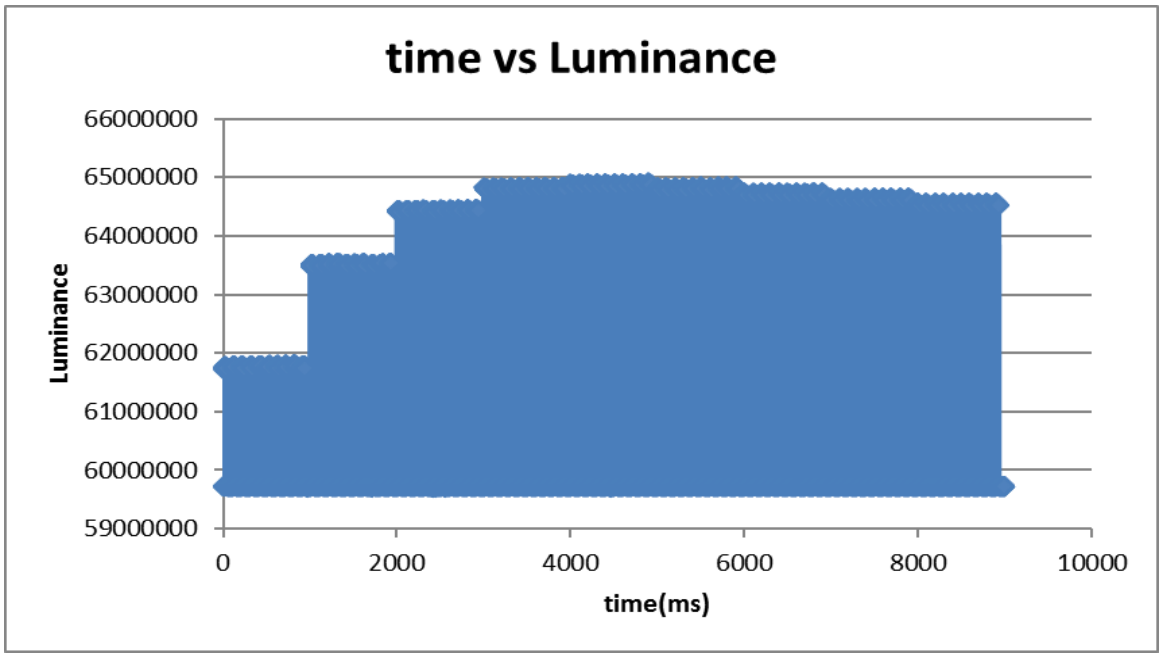

Figure 5.1: 50% duty cycle test at 100 Hz

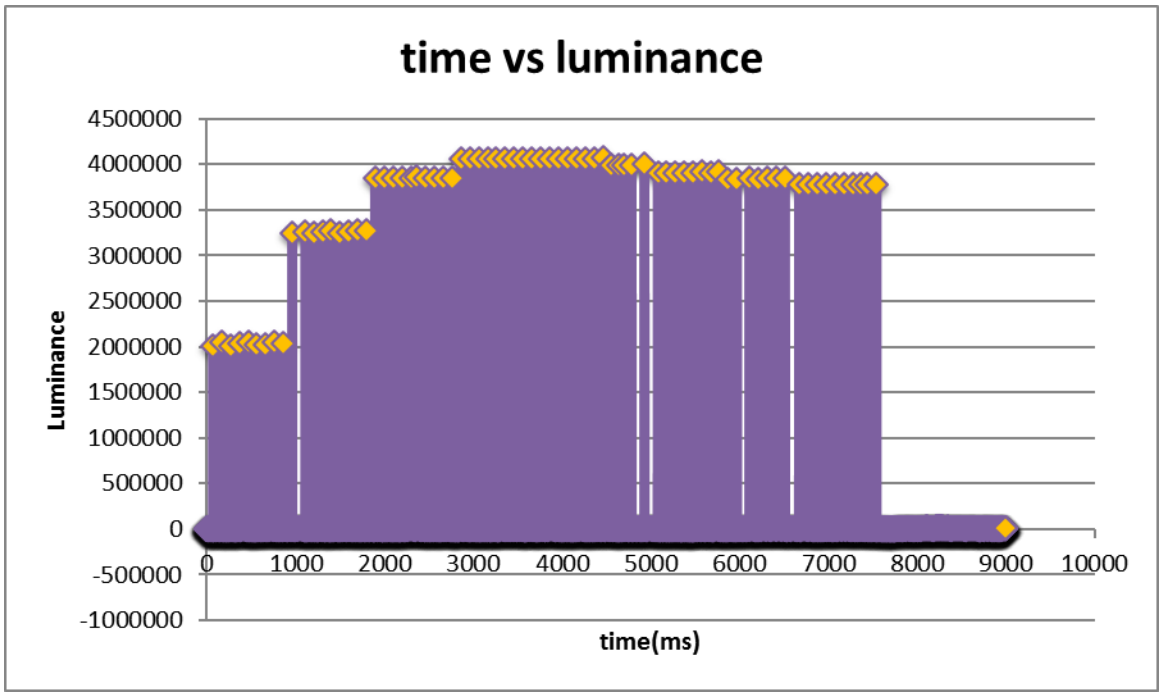

Figure 5.2: 50% duty cycle test at 1000 Hz

Figure 5.2 clearly shows that at 1000 Hz, the system drops a lot of frames and as it appears most frames are being dropped towards the end.

In our testing we used the Vision link F4 camera link frame grabber. After many tests and troubleshooting, I came to the conclusion that the F4 card is dropping the frame, not the camera. I tested my theory by changing our camera but after getting the same exact result with a different camera, I knew the problem was that the tests are just running too quick for the F4 card. I ran a test where I captured 9000 frames at 1000Hz without saving them, and I found that the F4 card was capable of accomplishing that without a problem. I concluded that the time outs happen during the saving process.

In order to eliminate this issue, I started to save the results in the SSD drive and also increased the usable buffer in the F4 card to its maximum amount which is 256 MB [11]. After running the tests again, I saw major differences in the results but I was still missing about 50-60 frames each time. As my last test, I created a ram disk of size 10GB and started to save the results in the ram disk which solved this problem entirely. Figure 5.3 shows the results of the same test as Figure 5.2, running at 1000 Hz after solving the problem.

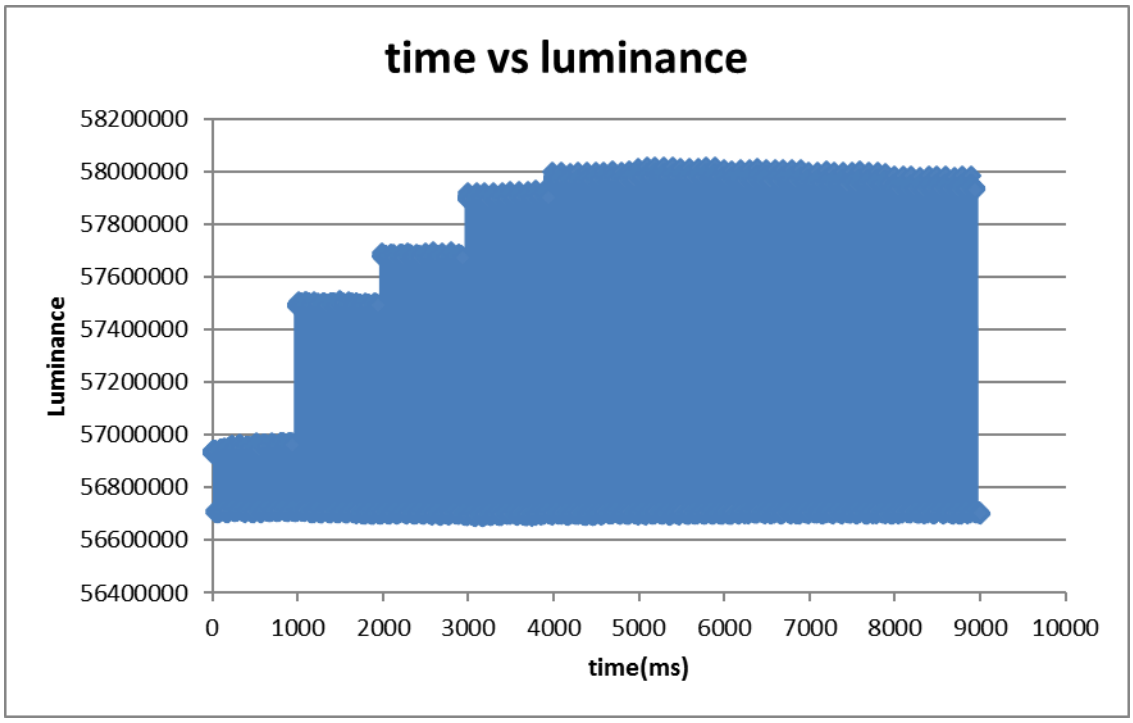

Figure 5.3: 50% duty cycle test at 1000 Hz, after solving the issue

5.2 Super Framing

Super Framing is a technique used to capture and save multiple frames into a single image file. There are many advantages in using this technique, such as less dependency on the computer itself and more dependency on the camera capture card. This technique allows us to use the on board buffer of the capture card to save the frames in and then save all frames in to one image at a time, cutting down the number of the interrupts that the system need to deal with in order to save the images.

The main reason for us to move to this technique was the fact that this will allow us to capture the frames at a higher speed. Currently the system is only capable of running at about 1000 Hz, but in the next generation system we will be able to increase number significantly. However, the system will not be able to catch up with

the speed unless we use the super framing technique. Figure 5.4 and 5.5 show the results of a 50 percent duty cycle test using a single frame in an image, and Figure 5.6 and 5.7 show the same test done using 10 frames in an image.

Figure 5.4: Single pixel at 50% duty cycle

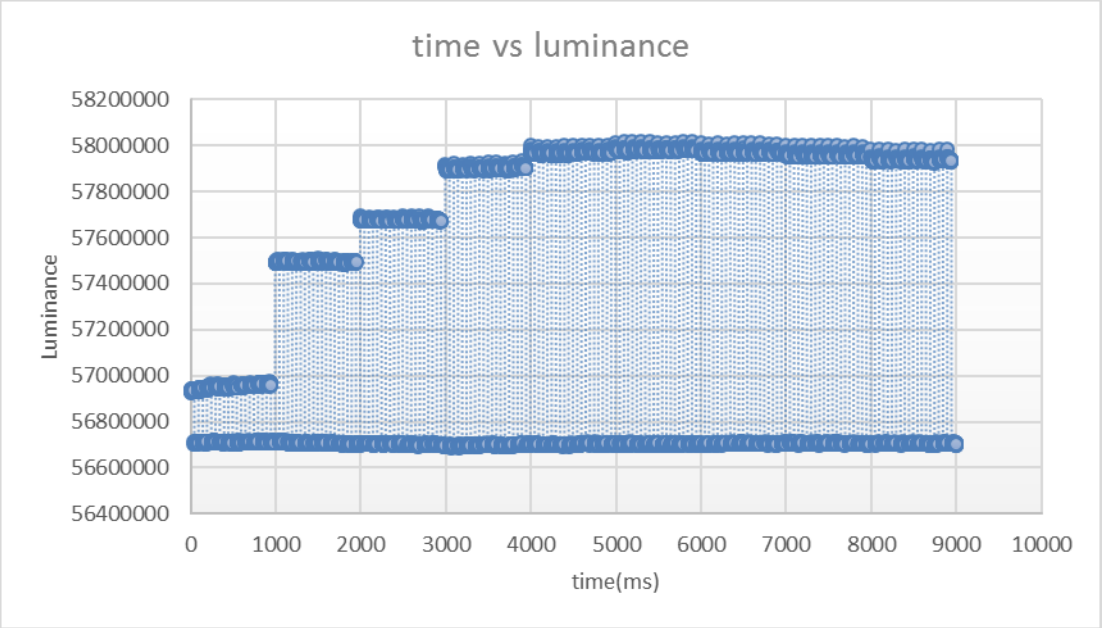

Figure 5.5: 50% duty cycle test without super framing

Figure 5.6: 10 frames in a single image

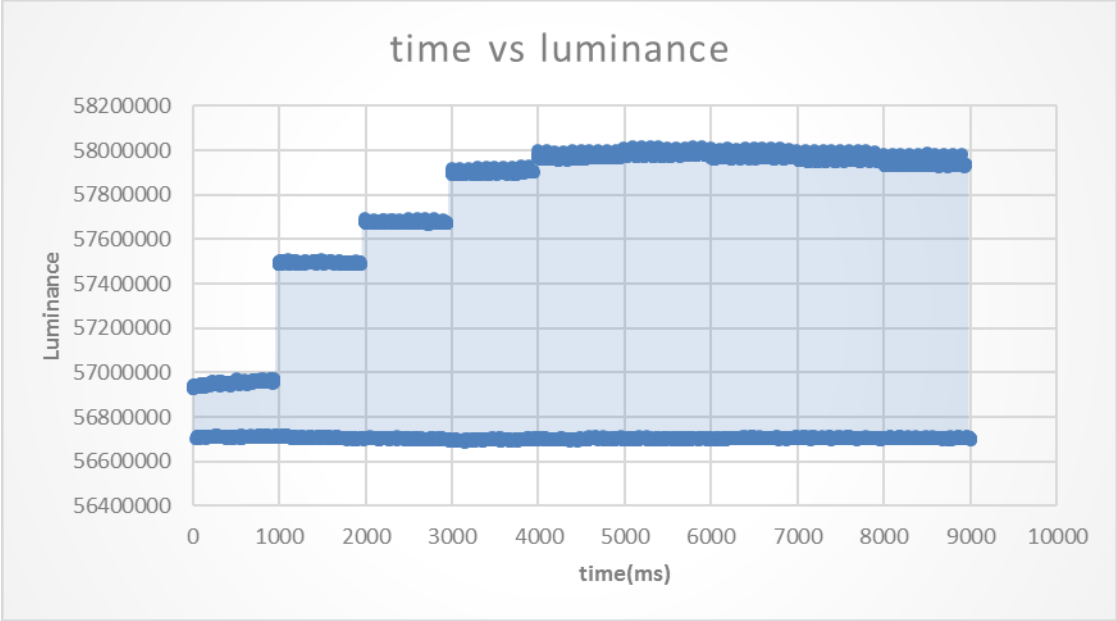

Figure 5.7: 50% duty cycle test with super framing

As seen in the figures above, the results are identical even though the techniques used in capturing the data are different. A python code was developed to process the captured images, and the images captured are cut down into a single frame before getting processed.

5.3 Image Processing

The data captured using the FLIR camera is outputted into RAW images, which means they need to be processed to get the graphs given in the previous sections.

In order to process the data, each image is loaded into a numpy array and then the first row is removed since that row is inserted by the camera and has information such as time, date and the number of pixels, which are user inputs and will not be useful to us. After removing the first row, each pixel in the image is added to other pixels in an array and a number is received. The very first image in every test is a background image that contains nothing but a black background. The same process is applied to the background image and the number received is saved as the background image variable which is then subtracted from other images and the true value of each image is calculated. The code goes through all the images in the folder and subtracts the background image from each one and the result is saved in an excel file, and then graphed as well.

For instance, Figure 5.8 shows a single pixel at full brightness. After removing the first row and adding all its pixels together, the value of 58,000,000 is achieved.

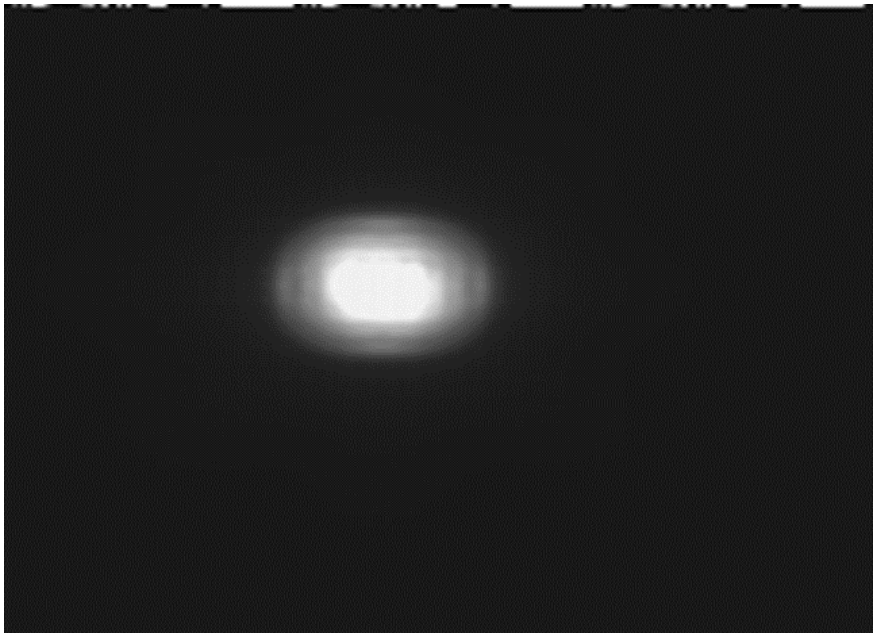

Figure 5.8: Single pixel at full brightness

Background subtraction can be applied, but it is not necessary since the graph will look the same, however the values will be bigger. The end result after processing many images like Figure 5.8 will look similar to Figure 5.7.

Currently all image processing is done automatically after the data is recorded. The code is embedded in the system code and all the user needs to do is to choose the location where the images are saved which can be done using the file explored that shows up on the screen after recording of the data is completed.

Chapter 6

CONCLUSION

The 100 Hz system has proven that our research group has the ability to design and operate an IR LED projector. As the SLEDs projector was the first IR projector based on LEDs, further improvements are required to better the system. The tests have proven that that the current technology of the IR LEDs will not be good enough to proceed with the higher resolution systems and so a research is being done to improve the quality and the efficiency of the IR LEDs.

In addition to the LEDs, other components of the system such as the dac boards, interface board, amplifier boards and the code for the FPGA board are being worked on and being improved. Once all the improvements are in place then we can improve the efficiency of the system and even run the system at the room temperature and even eliminate the DEWAR.

A NUCing algorithm is being developed that can fix all non-uniformity issues and can even take the issue with the DVI into consideration and help improve the quality of images being drawn in the projector. It is my hope that the experience outlined in this thesis will provide a base for the next generation system as well as a guide for new graduate and undergraduate students who will be working on this and next generation IR LED projectors.

REFERENCES

1. Rodney McGee, "Design, fabrication, iteration, and testing of the 68x68 su-perlattice led infrared projections system and associated electronics," *Master's Thesis*, University of Delaware, Department of Electrical and Computer Engineering, June 2010.

2. Christopher Kerwien, "Design and characterization of 12V analog trans-impedance amplifier for superlattice LED projector". Bachelor's University of Delaware, Department of Electrical and Computer Engineering.

3. Norton, D. T., Olesberg, J. T., McGee, R. T., Waite, N. A., Dickason, J., Goossen, K. W., Kiamilev, F. ... & Boggess, T. F. (2013). 512 512 Individually Addressable MWIR LED Arrays Based on Type-II InAs/GaSb Superlattices. Quantum Electronics, IEEE Journal of, 49(9), 753-759

4. Lange, C., McGee, R., Waite, N., Haislip, R., & Kiamilev, F. E. (2011, May). System for driving 2D infrared emitter arrays at cryogenic temperatures. In SPIE Defense, Security, and Sensing (pp. 801507-801507). International Society for Optics and Photonics.

5. Flip Chip bonding of 68 x 68 MWIR LED Arrays, Naresh Das, Monica Taysing-Lara, Kimberley Olver, Fouad Kiamilev, J. Prineas, J. Olsberg, E. Kroepeck, L. Murray and T. Boggess, IEEE Trans. on Elect. Packaging Manufacturing, Vol. 32, No. 1 (January 2009)

6. John P. Uyemura. CMOS Logic Circuit Design. Kluwer Academic Publishers, 2002.

7. C. Kerwien, "Design and characterization of 12V analog trans-impedance amplifier for superlattice LED projector," Honors Bachelors Thesis, University of Delaware, Department of Electrical and Computer Engineering, June 2013.

8. Jacob Benedict, "Design and characterization of a mixed-signal pcb for digital-to-analog conversion in a modular and scalable infrared scene projector," Master's Thesis, University of Delaware, Department of Electrical and Computer Engineering, June 2015.

9. K. Nabha, “100 Hz 512x512 SLEDS system design,” Master’s Thesis, University of Delaware, Department of Electrical and Computer Engineering, June 2014.

10. FLIR Advanced Thermal Solution Website. http://www.flir.eu/science/display/?id=45674, March 2016.

11. Camera Link Frame Grabber for PCI Express / x4. http://edt.com/product/visionlink-f4/, March 2016.

12. J. Lawler, “L-I-V-DAC Count Testing of IR LED Array,” ATEC - HDILED - Jul Update - Jul. 2015. (unpub.)

13. J. Benedict, R. McGee, J. Marks, K. Nabha, N. Waite, G. Ejzak, J. Dickason, H. Ahmed, M. Hernandez, P. Barakhshan, T. Browning, J. Volz, T. Lassiter, F. Kiamilev, T. Boggess, “512x512, Two-color Infrared LED Scene Projector.” GOMACTech 2016. (unpub.)

14. Z. Marks, N. Waite, J. Marks, J. Dickason, R. McGee, F. Kiamilev, K. Goossen, J. Lawler, “Advanced Packaging for Infrared Scene Projectors.” GOMACTech 2016. (unpub.)

15. Electro - Optical Systems Inc., Cryogenic photoreceiver , July. 2013. http://www.eosystems.com/uploads/2/0/1/3/20135707/is-040-e-ln7.pdf, March, 2016.

16. Electro - Optical Systems Inc., Insb relative spectral response, July. 2013. http://www.eosystems.com/uploads/2/0/1/3/20135707/is_series_spectral_response.pdf, March, 2016.

17. Electro - Optical Systems Inc., L-series operating instructions, July. 2013. http://www.eosystems.com/uploads/2/0/1/3/20135707/l_series_op_instructions.pdf, March, 2016.

AppendixA

CALCULATIONS AND TABLES FOR SECTION 4

$$\frac{full\ scale\ current\ (A)}{bits\ of\ resolution} \times load\ resistance\ (ohms) = LSB\ step\ size\ (V)$$

$$\frac{31.7mA}{16\ bits} \times 50\ ohms = 24.2\mu V$$

16-bit value	Voltage across 50 ohm load (mV)	Current output (mA)
0	0 -100	1.01
6553	144 - 152	2.99
13107	296	5.98
19660	440	8.89
26214	584 - 592	11.88
32767	736 - 744	14.95
39321	896	18.1
45874	1048	21.17
52428	1200	24.24
58981	1360	27.47
65535	1540	31.11

Table A.1: Measured and calculated values for DAC linearity

Equation for calculation of values in "Current output" column of Table A.1:

$$\frac{voltage\ across\ load\ (V)}{load\ resistance\ (ohm)} = current\ output\ (A)$$