The process\_instruction() function should be able to simulate the instruction-level execution of the following subset of entire RV32I instructions:

|  |  |
| --- | --- |
| Instruction type | instruction |
| R | add, slt |
| I | addi, slli |
| S | sw |
| SB | bne |
| U | auipc |
| UJ | jal |

A table with numbers and letters

Description automatically generated

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **Funct7** | **Rs2** | **Rs1** | **Funct3** | **Rd** | **Opcode** | **Assembly** |
| add | 0000000 |  |  | 000 |  | 0110011 |  |
| slt | 0000000 |  |  | 010 |  | 0110011 |  |

Table 1:R type instructions.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Instruction | Imm[11:0] | **Rs1** | **Funct3** | **Rd** | **Opcode** | **Assembly** |
| addi |  |  | 000 |  | 0010011 |  |
| slli |  |  | 001 |  | 0010011 |  |

Table 2: I type instructions.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | Imm[11:5] | **Rs2** | **Rs1** | **Funct3** | Imm[4:0] | **Opcode** | **Assembly** |
| sw |  |  |  | 010 |  | 0100011 |  |

Table 3:S type instructions.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | Imm[12|10:5] | **Rs2** | **Rs1** | **Funct3** | Imm[4:1|11] | **Opcode** | **Assembly** |
| bne |  |  |  | 001 |  | 1100011 |  |

Table 4:SB type instructions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Instruction** | Imm[20|10:1|11|19:12] | **Rd** | **Opcode** | **Assembly** |
| auipc |  |  | 0010111 |  |

Table 5:U type instructions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Instruction** | Imm[31:12] | **Rd** | **Opcode** | **Assembly** |
| jal |  |  | 1101111 |  |

Table 6:UJ type instructions.