ATMega128 Timer/Counter1

Prof. Ken Short

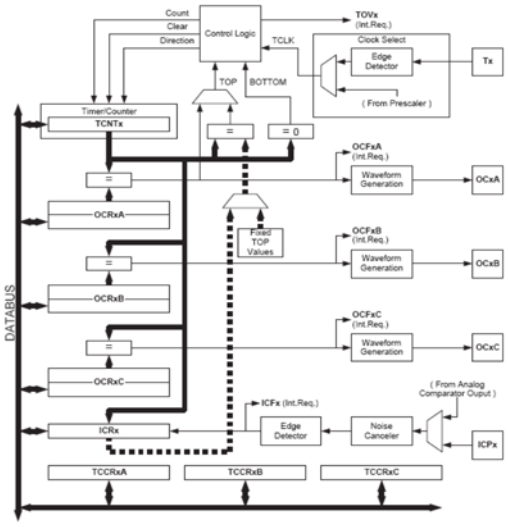
Focus on Timer/Counter1

- The ATMega128 has two 16-bit timer/counters: Timer/Counter1 and Timer/Counter3. These counters are similar in features and operation.
- The focus of the remainder of this lecture is on Timer/Counter1. It is also representative of timer/counter3
- The general concepts covered for Timer/Counter1 provide the background necessary to understand the data sheet and application note descriptions of both the 16-bit timer/counters

Timer/Counter1 Features

- 16-bit counter and compare registers
- Three independent output compare units
- Double buffered Output Compare Registers
- One input capture unit
- Input capture noise canceler
- Clear timer on compare match (auto reload)
- Glitch-free, phase correct pulse width modulator (PWM)
- Variable PWM period
- Frequency generator
- External event counter
- Five independent interrupt sources (TOV1, OCF1A, OCF1B, OCF1C, ICF1)

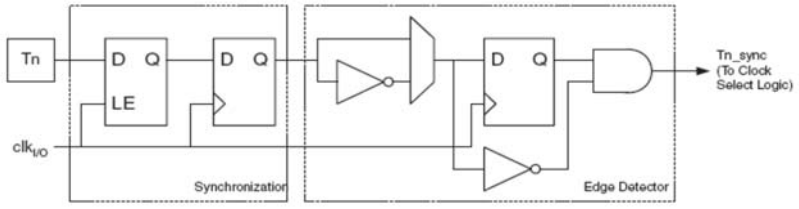
Timer/Counter1 Block Diagram



Timer/Counter1 Clock

- Timer/Counter1 can be clocked:
  - Externally by a signal at pin T1 (PD6)
  - Directly from the system clock
  - From the system clock divided by a prescaler
  - No clock – timer/counter is stopped

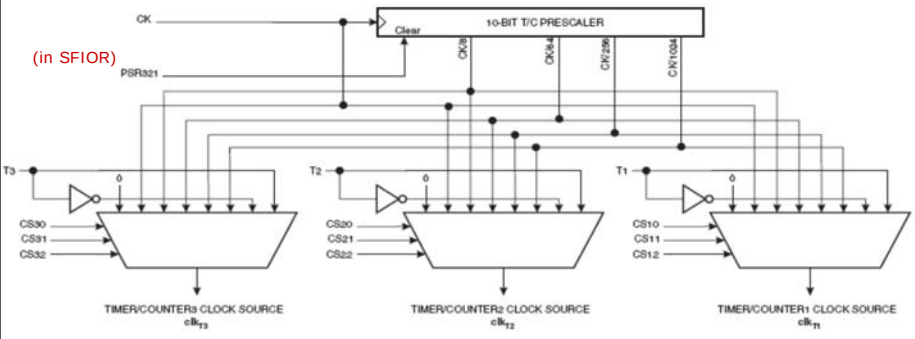
T1 Pin Sampling Functionally Equiv. Ckt.



T1 Pin Sampling

- The T1 pin is sampled once every system clock cycle by the pin synchronization logic
- The sampled signal is passed through an edge detector
- The edge detector generates one clkT1 pulse for each positive (CS12:0 = 7) or negative (CS12:0 = 6) edge it detects
- The clock pulse is delayed by 2.5 to 3.5 clock cycles for each edge detected
- To be detected, the external clock's frequency must be less than half the system clock frequency. The recommended maximum is fsys/2.5
- Enabling and disabling of the clock input must be done when Tn has been stable for at least one system clock cycle, otherwise it is a risk that a false Timer/Counter clock pulse is generated.

Prescaler for Timer/Counters 1, 2, and 3



TCCR1B – Timer/Counter1 Control Register B

Bit	7	6	5	4	3	2	1	0	
	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- Bit 7 – ICNC1: Input Capture Noise Canceller
- Bit 6 – ICES1: Input Capture Edge Select
- Bit 4:3 – WGM13:2: Waveform Generation Mode
- Bit 2:0 – CS12:0: Clock Select

Clock Select Bit Description

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/1 (No prescaling
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

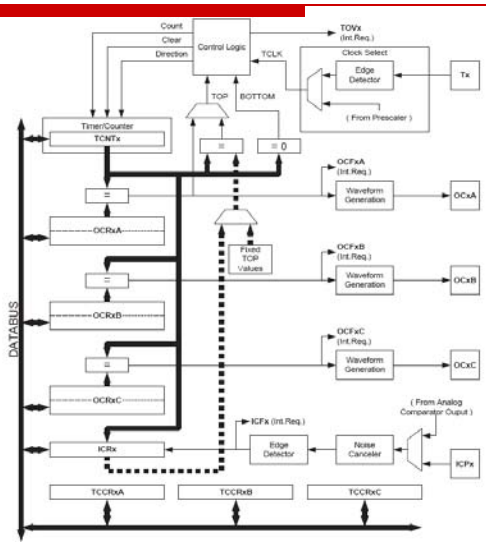
- Making CS12,CS11,CS10 = 0,0,0 stops the counter

Resetting Prescalars Using PSR10 Bit in SFIOR

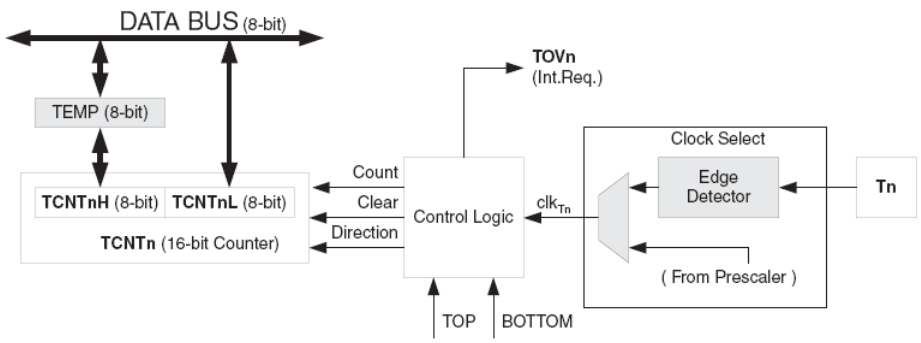
Bit	7	6	5	4	3	2	1	0	
	TSM	–	–	–	ACME	PUD	PSR0	PSR321	SFIOR
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- Setting the PSR10 bit in the SFIOR register resets the prescalars for Timer/Counter0 and Timer/Counter1

Timer/Counter1



Timer/Counter1 Unit Block Diagram



Accessing 16-bit Registers

- The TCNT1, OCR1A/B/C, and ICR1 are 16-bit registers that can be accessed by the AVR CPU via the 8-bit data bus.
- The 16-bit timer/counter has a single 8-bit register TEMP for temporarily storing the high byte during a 16-bit access
- TEMP is shared between all 16-bit registers within the 16-bit timer
- Accessing the low-byte triggers a 16-bit read or write operation
- When the low-byte of a 16-bit register is read by the CPU, the high byte is automatically copied into TEMP in the same clock cycle
- **So, to read a 16-bit register, the low-byte should be read first and then the high byte should be read**

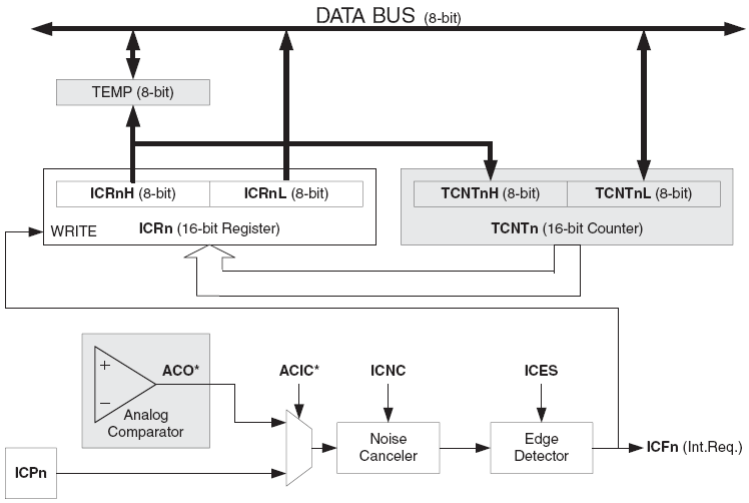
Accessing 16-bit Registers (cont.)

- When the low-byte of a 16-bit register is written by the CPU, the high byte stored in TEMP and the low-byte are automatically copied into the 16-bit register in the same clock cycle
- **So, to write a 16-bit register, the high-byte should be written first and then the low byte should be written**

Input Capture Unit

- The Timer/Counter incorporates an Input Capture unit that can capture external events and give them a time-stamp indicating time of occurrence.
- The time-stamps can then be used to calculate frequency, duty-cycle, and other features of the signal applied. Alternatively the time-stamps can be used for creating a log of the events.

Input Capture Unit Block Diagram



Input Capture Unit (cont.)

- The input capture unit can respond to an external event on the ICP1 pin (or alternatively, for Timer/Counter1 only, the analog comparator unit) by storing a copy of the 16-bit count in TCNT1 in the 16-bit Input Capture Register (ICR1) and setting the Input Capture Flag (ICF1) in TIFR
- The ICES1: Input Capture Edge Select bit in TCCR1B is used to select for rising edge (ICES1 = 1) of falling edge (ICES1 = 0)
- If enabled (TICIE1 = 1, in Timer/Counter Interrupt Mask Register, TIMSK), an interrupt is generated
- The ICF1 flag is automatically cleared when the interrupt is executed. Alternatively the ICF1 flag can be cleared by software by writing a logical one to its I/O bit location.

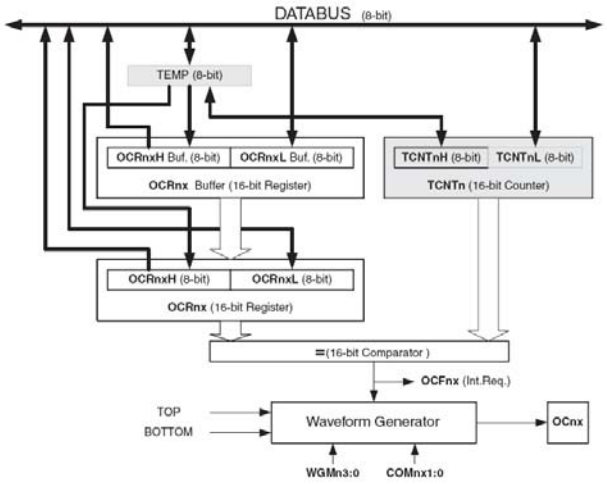
Output Compare Unit

- Timer/counter1 has three output compare units: A, B, and C. They are shown in the Timer/Counter1 block diagram
- Each unit has a *Output Compare Register* (OCR1x), where x is A, B, or C.
- The 16-bit comparator continuously compares TCNT1 with the *Output Compare Register* (OCR1x). If TCNT1 equals OCR1x the comparator signals a match.
- The OCR1x Register is double buffered when using any of the twelve *Pulse Width Modulation* (PWM) modes. For the normal and *Clear Timer on Compare* (CTC) modes of operation, the double buffering is disabled. The double buffering synchronizes the update of the OCR1x Compare Register to either TOP or BOTTOM of the counting sequence. The synchronization prevents the occurrence of odd-length, non-symmetrical PWM pulses, thereby making the output glitch-free.

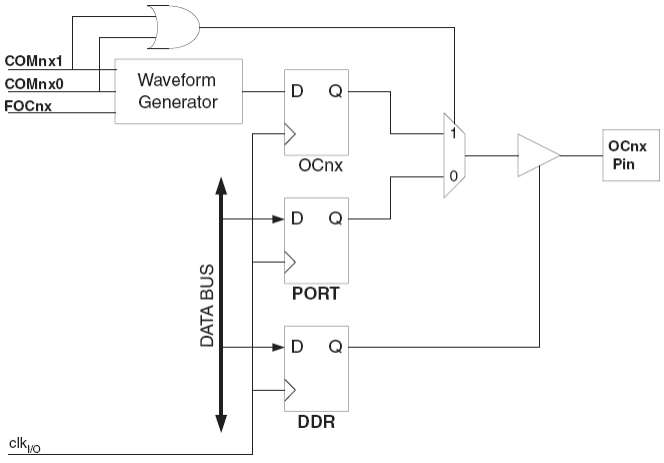
Output Compare Unit (cont.)

- A match will set the *Output Compare Flag* (OCF1x) at the next timer clock cycle. If enabled (OCIE1x = 1), the output compare flag generates an output compare interrupt. The OCF1x flag is automatically cleared when the interrupt is executed.
- Alternatively the OCF1x flag can be cleared by software by writing a logical one to its I/O bit location.
- The Waveform Generator uses the match signal to generate an output according to operating mode set by the *Waveform Generation mode* (WGMn3:0) bits and *Compare Output mode* (COMnx1:0) bits.

Output Compare Unit Block Diagram



Compare Match Output Unit



Timer/Counter1 Interrupts

- TIMER1 CAPT Timer/Counter1 Capture Event
- TIMER1 COMPA Timer/Counter1 Compare Match A
- TIMER1 COMPB Timer/Counter1 Compare Match B
- TIMER1 COMPC Timer/Countre1 Compare Match C
- TIMER1 OVF Timer/Counter1 Overflow

Summary of Timer/Counter1 Registers

- TCCR1A – Timer/Counter1 Control Register A
- TCCR1B – Timer/Counter1 Control Register B
- TCCR1C – Timer/Counter1 Control Register C
- TCNT1H:TCNT1L – Timer/Counter1
- OCR1AH:OCR1AL – Output Compare Register 1 A
- OCR1BH:OCR1BL – Output Compare Register 1 B
- OCR1CBH:OCR1CL – Output Compare Register 1 C
- ICR1H:ICR1L – Input Capture Register 1
- TIMSK – Timer/Counter Interrupt Mask Register
- TIFR - Timer/Counter Interrupt Flag Register

TCCR1A – Timer/Counter1 Control Reg. A

Bit	7	6	5	4	3	2	1	0	
	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- The simplest mode of operation is the normal mode
- In this mode WGM13:0 = 0
- In this mode the timer/counter overflows when it is incremented past its maximum value of $FFFF and rolls over to $0000
- On overflow, the Timer/Counter Overflow Flag (TOV1 in TIFR) is set
- Using normal mode to generate waveforms is not recommended, since it occupies too much CPU time

Atmel's Notation for a Sequence of Bits

- In the previous slide the statement "In this mode WGM13:0 = 0" is given
- Following some common conventions this might be interpreted as fourteen bits WGM13, WGM12, … WGM0 all being equal to 0
- Following Atmel's convention for denoting a set of bits in a register this actually means bits 3 down to 0 of the set of bits WGM1
- That is only for bits are being referred to not 14 and the four bits are associated with timer/counter1, thus the 1 in WGM1

Compare Output Mode – Non PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	Toggle OCnA/OCnB/OCnC on compare match.
1	0	Clear OCnA/OCnB/OCnC on compare match (set output to low level).
1	1	Set OCnA/OCnB/OCnC on compare match (set output to high level).

Compare Output Mode – Fast PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	WGMn3:0 = 15: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC on compare match, set OCnA/OCnB/OCnC at BOTTOM, (non-inverting mode)
1	1	Set OCnA/OCnB/OCnC on compare match, clear OCnA/OCnB/OCnC at BOTTOM, (inverting mode)

Compare Output Mode - Phase Correct and Phase and Frequency Correct PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	WGMn3:0 = 9 or 11: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC on compare match when up-counting. Set OCnA/OCnB/OCnC on compare match when downcounting.
1	1	Set OCnA/OCnB/OCnC on compare match when up-counting. Clear OCnA/OCnB/OCnC on compare match when downcounting.

Note: 1. A special case occurs when OCRnA/OCRnB/OCRnC equals TOP and COMnA1/COMnB1//COMnC1 is set. See “Phase Correct PWM Mode” on page 128. for more details.

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Waveform Generation Mode Bit Description

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation(1)	TOP	Update of OCRnx at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCRnA	TOP	BOTTOM

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Waveform Generation Mode Bit Description

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation[1]	TOP	Update of OCRnx at	TOVn Flag Set on
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

Note: 1. The CTCn and PWMn1:0 bit definition names are obsolete. Use the WGMn2:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

TCCR1B – Timer/Counter1 Control Register B

Bit	7	6	5	4	3	2	1	0	
	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- Bit 7 – ICNC1: Input Capture Noise Canceller
- Bit 6 – ICES1: Input Capture Edge Select (1 for rising edge)
- Bits 4:3 – WGM13:2: Waveform Generation Mode
- Bits 2:0 – CS12:0: Clock Select

TCCR1C – Timer/Counter1 Control Register C

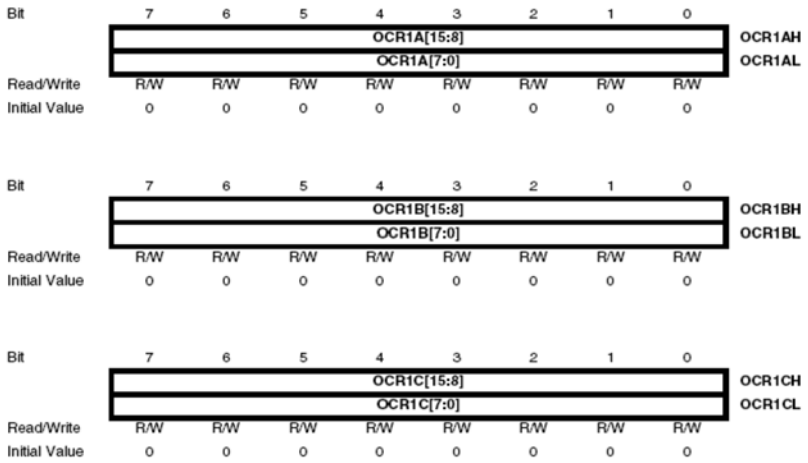
Bit	7	6	5	4	3	2	1	0	
	FOC1A	FOC1B	FOC1C	–	–	–	–	–	TCCR1C
Read/Write	W	W	W	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- Bit 7 – FOCnA: Force Output Compare for Channel A
- Bit 6 – FOCnB: Force Output Compare for Channel B
- Bit 5 – FOCnC: Force Output Compare for Channel C

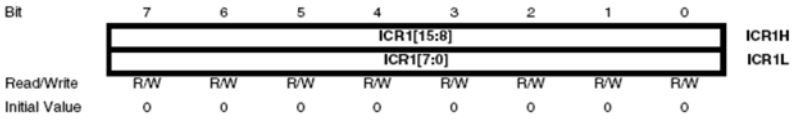
TCNT1H:TCNT1L

Bit	7	6	5	4	3	2	1	0	
	TCNT1[15:8]								TCNT1H
	TCNT1[7:0]								TCNT1L
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Output Compare Registers



ICR1H:ICR1L Input Compare Register1



TIMSK – Timer/Counter Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Note: This register contains interrupt control bits for several Timer/Counters, but only Timer1 bits are described in this section. The remaining bits are described in their respective timer sections.

- This register contains interrupt enable control bits for all the timer/counters
- Bits for timer/counters other than Timer/Counter1 are shaded
- Bit 5 – TICIE1: Timer/Counter1, Input Capture Interrupt Enable
- Bit 4 – OCIE1A: Timer/Counter1, Output Compare A Match Interrupt Enable
- Bit 3 – OCIE1B: Timer/Counter1, Output Compare B Match Interrupt Enable
- Bit 2 – TOIE1: Timer/Counter1, Overflow Interrupt Enable

TIFR – Timer/Counter Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Note: This register contains flag bits for several Timer/Counters, but only timer 1 bits are described in this section. The remaining bits are described in their respective timer sections.

- These flags (status bits) are set when the corresponding event occurs
- Bit 5 – ICF1: Timer/Counter1, Input Capture Flag
- Bit 4 – OCF1A: Timer/Counter1, Output Compare A Match Flag
- Bit 3 – OCF1B: Timer/Counter1, Output Compare B Match Flag
- Bit 2 – TOV1: Timer/Counter1, Overflow Flag

References

- ATMega128 Data Sheet, pages 112 through 143 (on Blackboard).