LCD Hardware

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Intro

- Display choice is application dependent
- There are a wide range of displays available

Agenda

- Displays
- LCD Display Organization
- LCD Display Modules
- LCD Display Controllers

Common Display Types for Small Embedded Systems

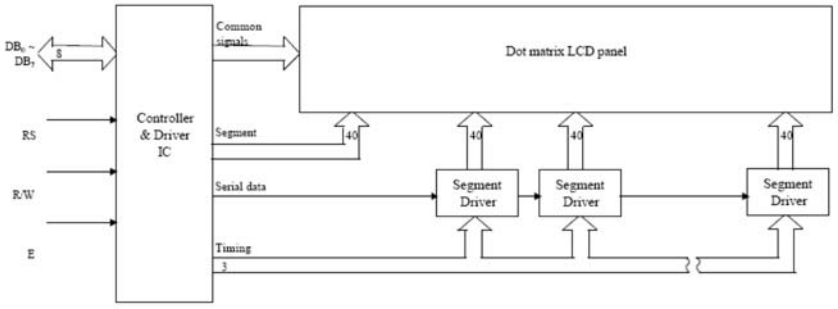
- Discrete LEDs
- Seven segment LEDs
- LCD character displays
- Vacuum fluorescent character displays
- LCD graphics displays

LCD Character Display Module

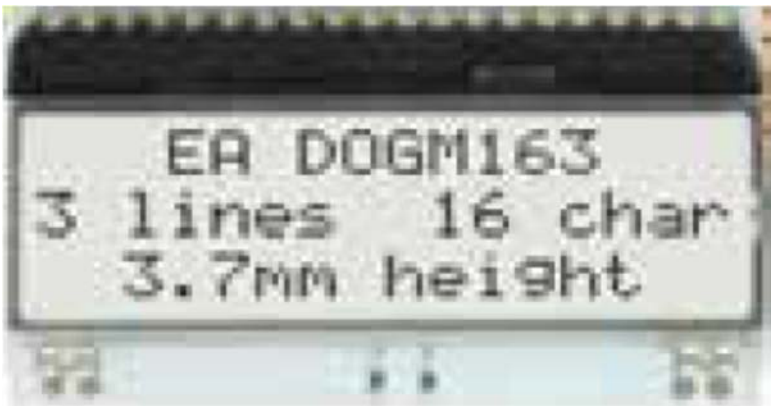
- Consists of LCD panel and CMOS controller and driver mounted on a small pc board
- Some common organizations of the display – rows x characters per row
  - 1 X 8
  - 1 x 16
  - 2 X 16
  - 3 x 16
  - 4 x 16
  - 1 x 20
  - 2 x 20
  - 4 x 20
  - 1 x 32
  - 2 x 32

2-Line 16 Character LCD Display Parallel Interface

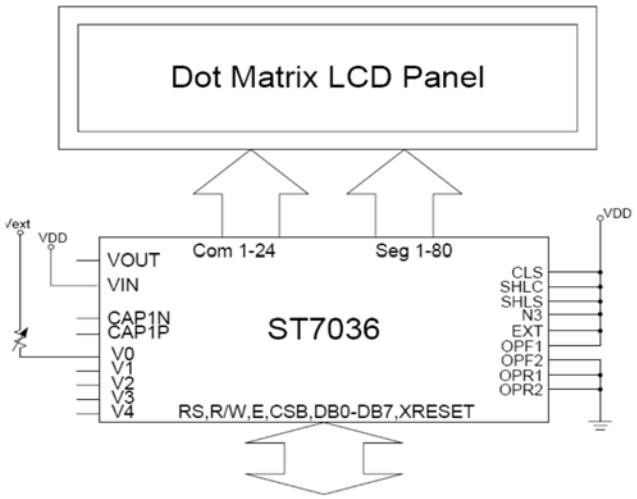
LCD Display Module – Parallel Interface



Electronic Assembly's DOG Module



Dot Matrix LCD Controller/Driver



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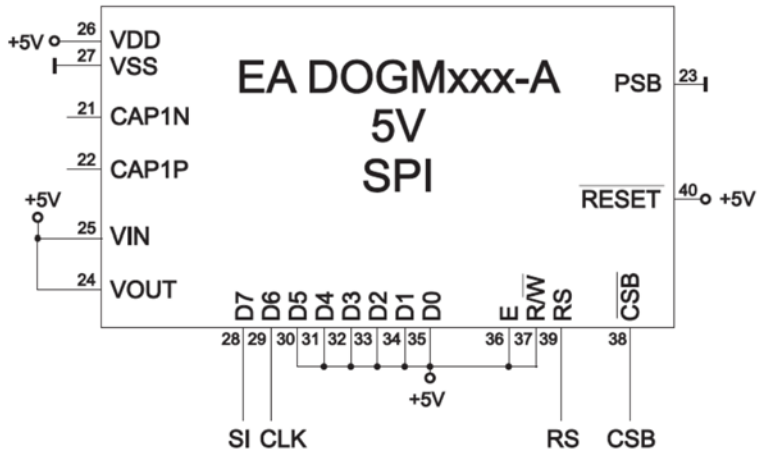
Connections to DOG Module's SPI



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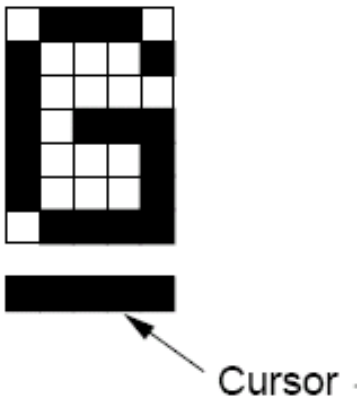
5 x 7 Dot Matrix Character and Cursor Position



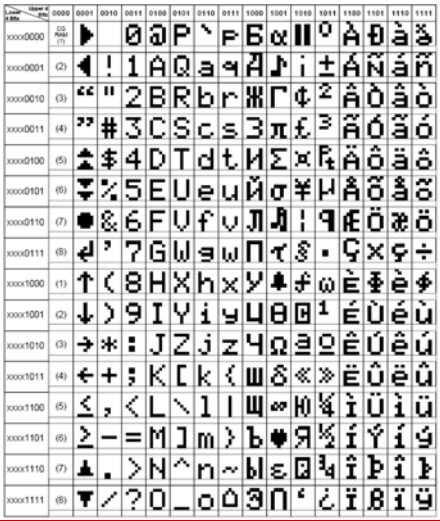
Character Patterns

- The dot patterns to form all the different characters that can be displayed are stored in a ROM (Character Generator ROM – CGROM) in the controller
- A character code is used as a starting address for a sequence of 8 words in the ROM that store the dot pattern for the corresponding character
- Different sets of characters are available in different controllers that use different CGROMs

Character Codes and Character Patterns

Note: The user can specify any pattern for character-generator RAM.

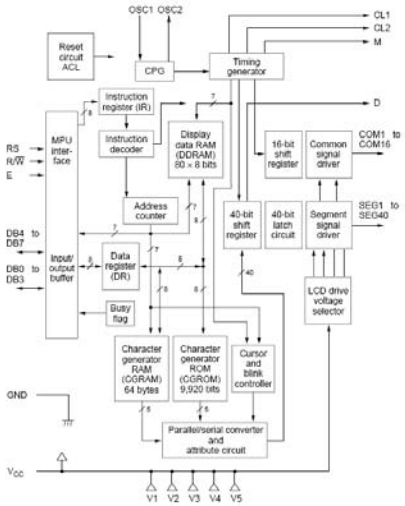
A More Extensive Set of Characters



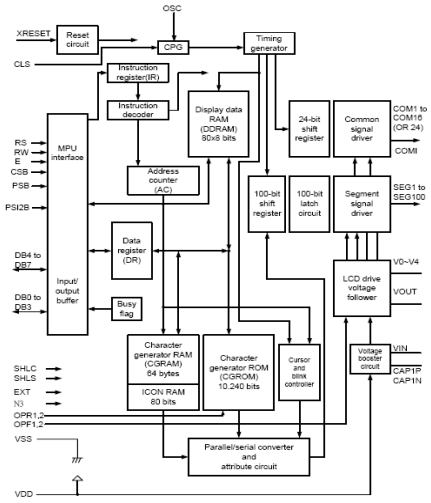
Controller and Driver IC(s)

- The first IC controller/driver for dot matrix character LCDs was the 44780
- Second sources for the 44780 and later versions all used essentially the same controller architecture
- As a result, most 1, 2, and 4 line dot matrix character LCD modules have the same bus interface and can be operated by the same driver software
- Later controller/driver ICs support serial as well as parallel interfaces

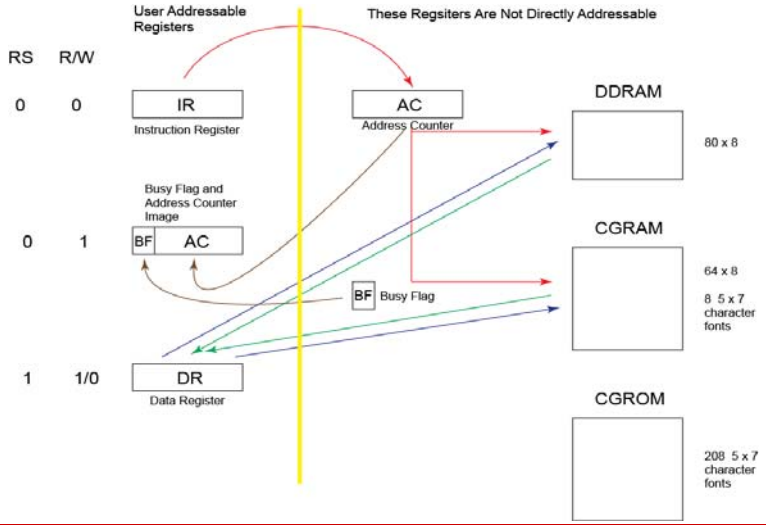
Hitachi HD44780U Parallel Interface Controller and Driver



ST7036 Parallel and Serial Interface Controller and Driver



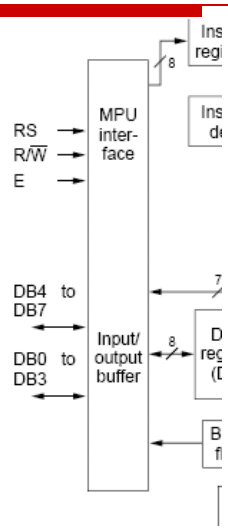
Simplified View of Controller Registers



Bus Interface

- The controllers' parallel bus interface is designed to allow the display controller to be connected to a microcontroller with either a 4-bit or 8-bit data bus
- The parallel bus control signals are "Motorola style"
- The serial bus interface is Serial Peripheral Interface (SPI) compatible

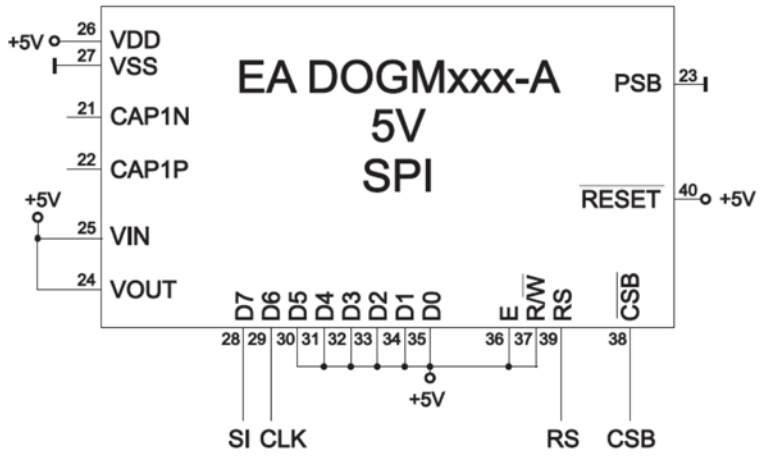
Parallel Bus Interface Block Diagram



Parallel Bus Interface Signal Definitions

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write.
DB4 to DB7	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB7 can be used as a busy flag.
DB0 to DB3	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.

SPI Serial Connections to DOG Module



Instruction Register

- The controller has two 8-bit registers, the instruction register (IR) and the data register (DR)
- The register select (RS) input selects the IR when RS = 0 and the DR when RS = 1
- The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DDRAM) and character generator RAM (CGRAM)
- The IR can only be written from the MPU.

Instructions - ST7036 Execution Times

➢ **instruction table at "Normal mode"**
(when "EXT" option pin connect to VDD, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380kHz	OSC= 540kHz	OSC= 700kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 µs	18.5 µs	14.3 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 µs	18.5 µs	14.3 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 µs	18.5 µs	14.3 µs

Instructions (cont.) - ST7036 Execution Times

Function Set	0	0	0	0	1	DL	N	X	X	X	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 µs	18.5 µs	14.3 µs
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	26.3 µs	18.5 µs	14.3 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	26.3 µs	18.5 µs	14.3 µs

Data Register

- The DR temporarily stores data to be written into DDRAM or CGRAM and temporarily stores data to be read from DDRAM or CGRAM
- Data written into the DR from the MCU is automatically written into DDRAM or CGRAM by an internal operation
- The DR is also used for data storage when reading data from DDRAM or CGRAM. When an address is written into the IR, data is read from the address and then stored into the DR from DDRAM or CGRAM by an internal operation
- Data transfer to the MCU is then completed when the MCU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read cycle.

Busy Flag (BF)

- When the busy flag is 1, the controller is performing an internal operation, the next instruction will not be accepted
- When RS = 0 and R/W = 1, the busy flag is output to DB7
- The next instruction must not be written until after ensuring that the busy flag is 0.
- When using 4-bit mode, the busy flag must be checked only after both nibbles are transferred.

Address Counter

- The address counter (AC) provides addresses to both DDRAM and CGRAM
- When an instruction containing an address is written into the IR, the address information is sent from the IR to the AC. Selection of either DDRAM or CGRAM is also determined concurrently by the instruction.
- The AC can be written using either the Set DDRAM Address instruction or the set CGRAM Address instruction
- The AC can be read, returning the Read Busy Flag and Address instruction

Address Counter (cont.)

- After writing into or reading from DDRAM or CGRAM, the AC is automatically incremented by 1 or decremented by 1 (determined by the I/D bit in the Entry Mode Set instruction
- The AC contents are output to DB0 to DB6 when RS = 0 and R/W = 1

Character Generator (CG) ROM

- The character generator ROM (4096 x 5) generates 5 x 8 dot or 5 x 10 dot character patterns from 8-bit character codes
- It can generate 160 5 x 8 dot character patterns and 32 5 x 10 dot character patterns (Optrex)
- User defined character patterns are also available by mask-programmed ROM.

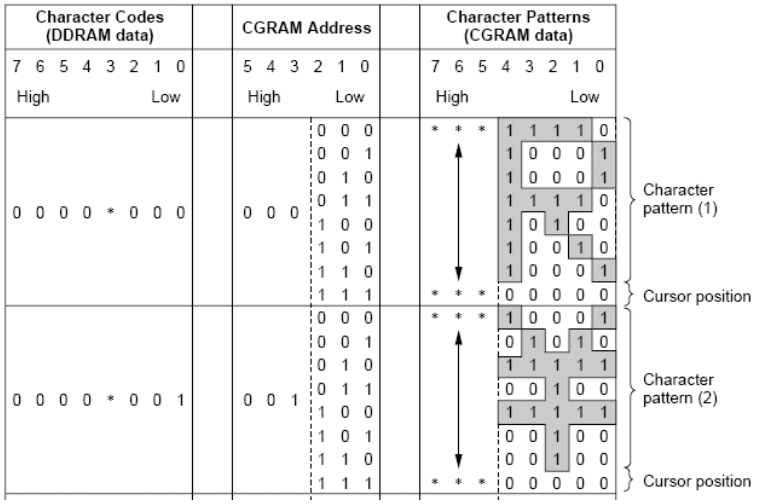
Correspondence Between CG ROM Address and Character Pattern

EPROM Address												Data					
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	LSB O0	
								0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← Cursor position

Character Generator (CG) RAM

- The CGRAM is a 64 x 8 RAM in which the user can program custom patterns
- In the character generator RAM, the user can write user defined character patterns. For 5 x 8 dots, eight character patterns can be written, and for 5 x 10 dots, four character patterns can be written
- The Set CGRAM Address instruction is used to load the AC with the address of the CGRAM location to be written or read
- To display previously programmed CGRAM characters the character codes $00 to $07 are used
- Areas in the CG RAM that are not used for display can be used as general data RAM.

Correspondence Between CG RAM Address and User Defined Character Pattern



Data Display RAM

- Display data RAM (DDRAM) stores display data represented in 8-bit character codes
- Its capacity is 80 x 8 bits, or 80 characters
- The area in DDRAM that is not used for display can be used as general data RAM. For example in a 2 x 16 display, 48 locations in DDRAM are not used for displaying characters
- The DDRAM address (ADD) is set in the address counter (AC) as hexadecimal.

Correspondence Between DDRAM and Character Position for a Two Line Display

Display position	1	2	3	4	5	.....	39	40
DDRAM address (hexadecimal)	00	01	02	03	04	.....	26	27
	40	41	42	43	44	.....	66	67

- When the number of display characters is less than 2 x 40, the two lines are displayed from the head of the DDRAM
- Note that the first line end address and the second line start address are not consecutive

Correspondence Between DDRAM and Character Position on 2 x 16 Display

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

HD44780U display | Extension driver display

Shift of Display Contents

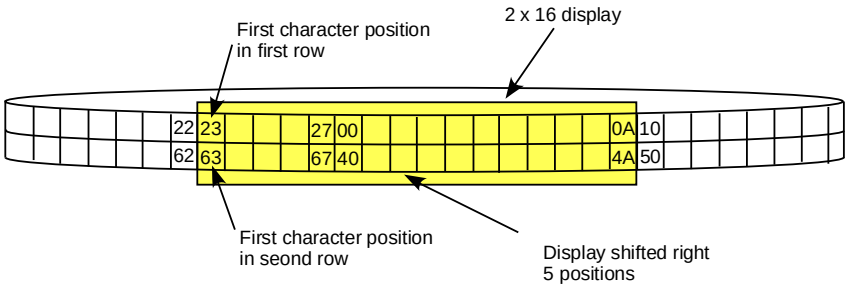
For shift left

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

For shift right

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

2 x 16 Display Shifted Right 5 Positions



Instruction Set

- Clear Display
- Return Home
- Entry Mode Set
- Display ON/OFF Control
- Cursor or Display Shift
- Function Set
- Set CGRAM Address
- Set DDRAM Address
- Read Busy Flag & Address
- Write Data to CG or DD RAM
- Read Data from CG or DD RAM

Summary of Instruction Set

Instruction	Code										Description	Execution time (max.) when fcp or fosc is 250 kHz
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	15.2ms
Return Home	0	0	0	0	0	0	0	0	1	x	Sets DD RAM address 0 in address counter. Also returns shifted display to original position. DD RAM contents remain unchanged.	15.2ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift or display. These operations are performed during data write and read.	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Moves cursor and shifts display without changing DD RAM contents.	40µs
Function Set	0	0	0	0	1	DL	N	F	x	x	Sets interface data length (DL), number of display lines (N) and character font (F).	40µs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40µs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40µs
Read Busy Flag & Address	0	1	BF	AC							Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40µs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40µs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40µs
	I/D=1 : Increment I/D=0 : Decrement S=1 : Accompanies display shift S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right										DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : CG RAM address ADD : DD RAM address. Corresponds to cursor address. AC : Address counter used for both	Execution time changes when frequency changes. Example: When fcp or fosc is 270kHz:

Instruction Set Coding

Instruction	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 270 kHz)
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 µs

Instruction Set Coding (cont. 1)

Instruction	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 270 kHz)
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Instruction Set Coding (cont. 2)

Instruction	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Write data to CG or DDRAM	1	0	Write data								Writes data into DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
Read data from CG or DDRAM	1	1	Read data								Reads data from DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 8 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DDRAM: Display data RAM CGRAM: Character generator RAM ACG: CGRAM address ADD: DDRAM address (corresponds to cursor address) AC: Address counter used for both DD and CGRAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 250 kHz, $37\ \mu s \times \frac{270}{250} = 40\ \mu s$

Note: — indicates no effect.

* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

A Slow Controller

- Most LCD controller/drivers are relatively slow
- A bus read or write requires and enable pulse (E) that is a minimum of 450 ns long
- Execution time of the fastest instructions is approximately 40 microseconds. Execution time of the longest instructions is approximately 1.64 milliseconds
- Driver software can be written so that the same software operate almost any 1, 2, or 4 line display

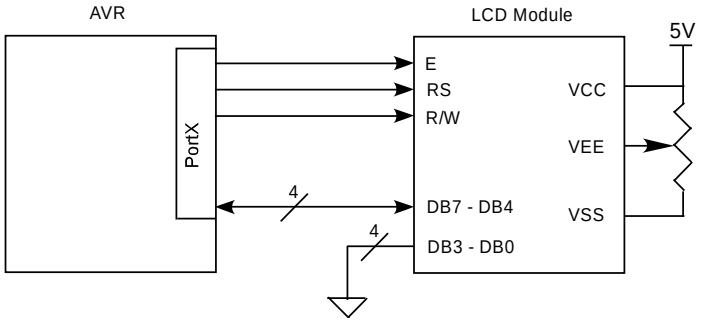
Parallel Bus Interface Pinouts

Pin Number	Symbol
1	V_{ss}
2	V_{cc}
3	V_{ee}
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7

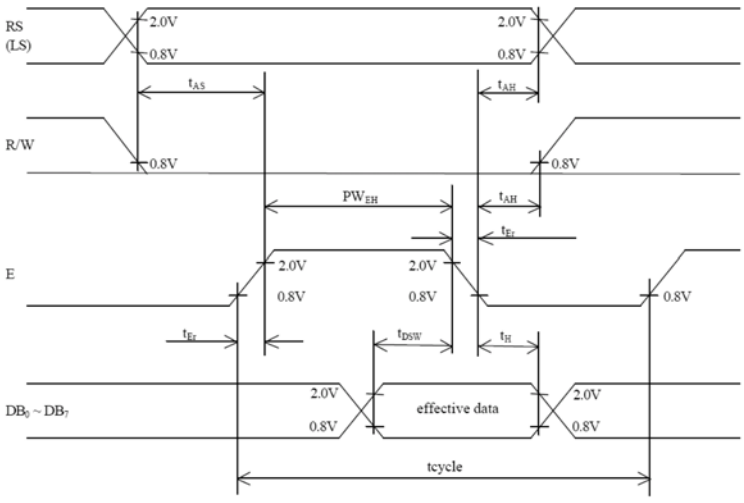
Bus Mode

- Display can be operated in 4-bit or 8-bit mode
- When operating in 4 bit mode, data is transferred in two 4 bit operations using data bits DB4 - DB7. DB0 - DB3 are not used and should be tied low.
- When using 4 bit mode, data is transferred twice before the instruction cycle is complete. First the high order nibble is transferred then the low order nibble. The busy flag should only be checked after both nibbles are transferred.
- When operating in 8 bit mode, data is transferred using the full 8 bit bus DB0 - DB7

4-Bit Interface



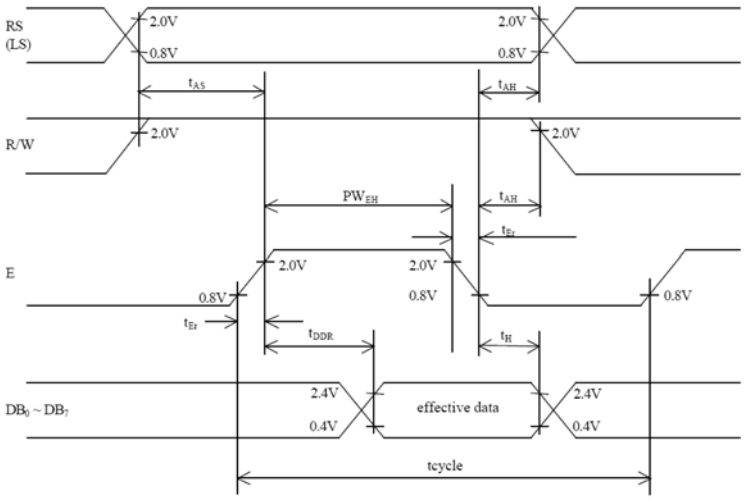
Data Write Timing



Data Write Timing Values (Optrex)

Item		Symbol	Specs. Value		Unit
			Min.	Max.	
Enable cycle time		tcycle	1000	-	ns
Enable pulse width	"High" level	PW_{EH}	450	-	ns
Enable rising, falling time		t_{Er}, t_{Ef}	-	25	ns
Set up time	RS, R/W-E	t_{AS}	140	-	ns
Address hold time		t_{AH}	10	-	ns
Data set up time		t_{DSW}	195	-	ns
Data hold time		t_H	10	-	ns

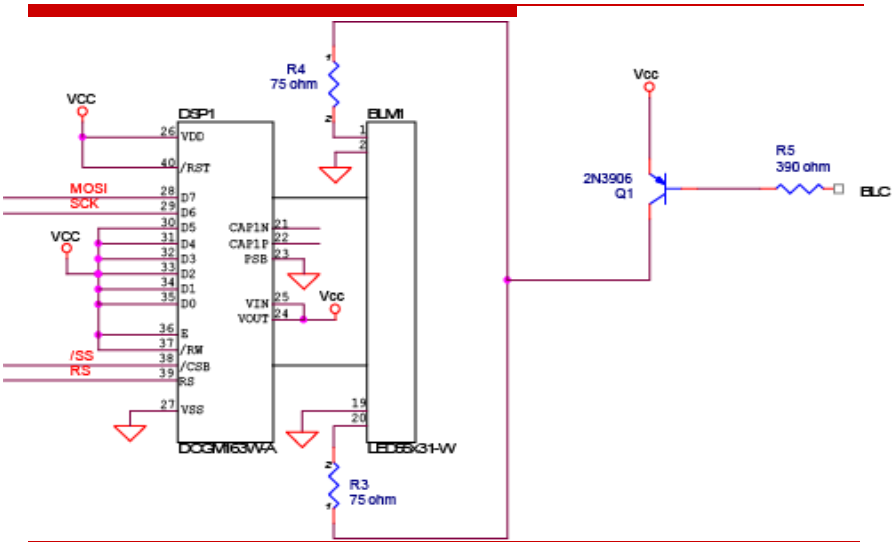
Data Read Timing



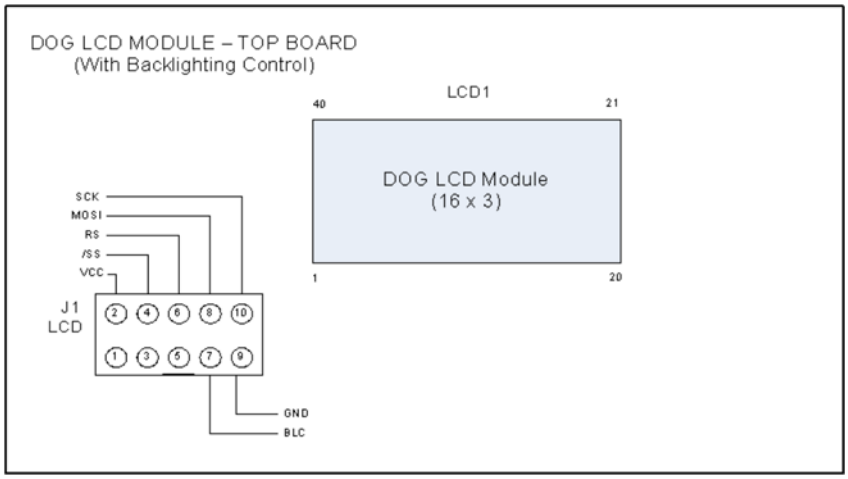
Data Read Timing Values (Optrex)

Item		Symbol	Specs. Value		Unit
			Min.	Max.	
Enable cycle time		tcycle	1000	-	ns
Enable pulse width	"High" level	PW_{EH}	450	-	ns
Enable rise, fall time		t_{Er}, t_{Ef}	-	25	ns
Set up time	RS, R/W-E	t_{AS}	140	-	ns
Data delay time		t_{DDR}	-	320	ns
Data hold time		t_H	20	-	ns

DOG Module with Backlight



DOG Module Breadboard Layout



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Display Positions in ST7036 DDRAM

	1	2	3	4	5	6		14	15	16
DDRAM Address (hexadecimal)	00	01	02	03	04	05	.....	0D	0E	0F
	10	11	12	13	14	15	.....	1D	1E	1F
	20	21	22	23	24	25	.....	2D	2E	2F

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Character Codes and Character Patterns

SPI Timing Waveform for ST7036