MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT AND ENGINEERING

(Affiliated to NMIMS Deemed to be University, Mumbai)

DIGITAL LOGIC DESIGN PROJECT

On

Priority Encoder

Submitted by

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Semester/Year: VII/IV		

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2023-2024

PRIORITY ENCODER

INDEX

INTRODUCTION

An encoder has 2^n input lines and n output lines. The output lines create the binary code equivalent to the input value. So, a priority encoder is a circuit that executes the priority function. It is designed to efficiently manage a multitude of input lines (2^n) and transform them into a corresponding binary code on n output lines. In essence, it prioritizes the inputs based on their relative significance, ensuring that when multiple inputs are active simultaneously, the one with the highest priority takes precedence.

Understanding priority encoders is fundamental for comprehending advanced digital systems and forms the basis for optimizing various functionalities within electronic devices. This report delves into the foundational principles, design considerations, simulation, and applications of priority encoders, shedding light on its indispensable role in digital circuitry and its broad spectrum of real-world applications.

THEORY

To overcome the disadvantages of binary encoders, priority encoders were developed. We have 2^n : n priority encoder, but we will be focusing on 4:2 priority encoder.

4:2 Priority Encoder

4:2 priority encoder stands as a significant component within the family of encoders. With a capacity to handle four input lines and produce a two-bit binary output, this encoder is designed to discern and encode the highest priority active input among the available options.

The third output is ‘E’, which is considered as enable and it is set to 1 when more than one input line is high or active (1). If the enable bit is equal to ‘0’, then all the inputs are ‘0’. In our case, the other 2 output lines are considered as don’t care conditions denoted by ‘X’.

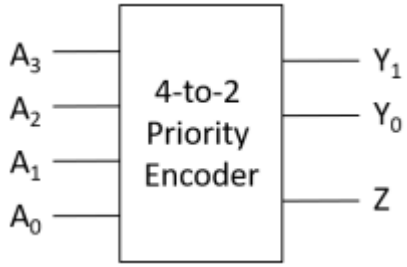
Let’s say D3, D2, D1, D0 are the inputs; Y1 and Y0 are the outputs and E is the enable bit indicator. Here, D3 input is the highest priority input and D0 is the lowest priority input. So, when the input D3 is active high (1), which has the highest priority irrespective of all other input lines, then the output of the 4-bit priority encoder is Y1(1) and Y2(1). When the D3 input is low and the D2 is high then D2 has the next highest priority irrespective of all other input lines, so the output is Y1(1) and Y2(0). Similarly, when D1/D0 will be active high and rest active low, the same will occur.

The simplified output expressions (Y1, Y2) can be obtained for a 4-bit encoder with the help of a Karnaugh map (K-map). From the output expressions, the 4:2 priority encoder circuit diagram is illustrated with logic gates.

The circuit diagram of 4:2 priority encoder is drawn with 2 OR gates, and the combination of AND gate and the NOT gate represent the enable bit, which is used when more than one input is logic high (1). Thus, four inputs with two outputs are encoded based on the assigned priority to the inputs.

DESIGN & PRINCIPLES

Symbol



Truth table

Inputs				Outputs		
D3	D2	D1	D0	Y1	Y0	Enable
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Expanded truth table (with don't care values)

Inputs				Outputs		
D3	D2	D1	D0	Y1	Y0	Enable
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

K-map for Y1

D1 D0 \ D3 D2	00	01	11	10
00	X	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

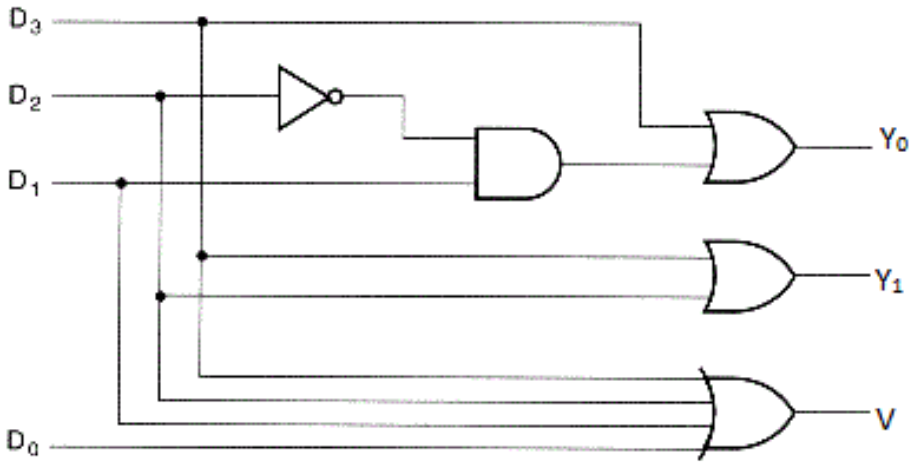
Y1 = D3 + D2

K-map for Y0

D1 D0 \ D3 D2	00	01	11	10
00	X	0	1	1
01	0	0	1	1
11	1	0	1	1
10	1	0	1	1

Y0 = D1.D2' + D3

Circuit Diagram



SIMULATION & TESTING

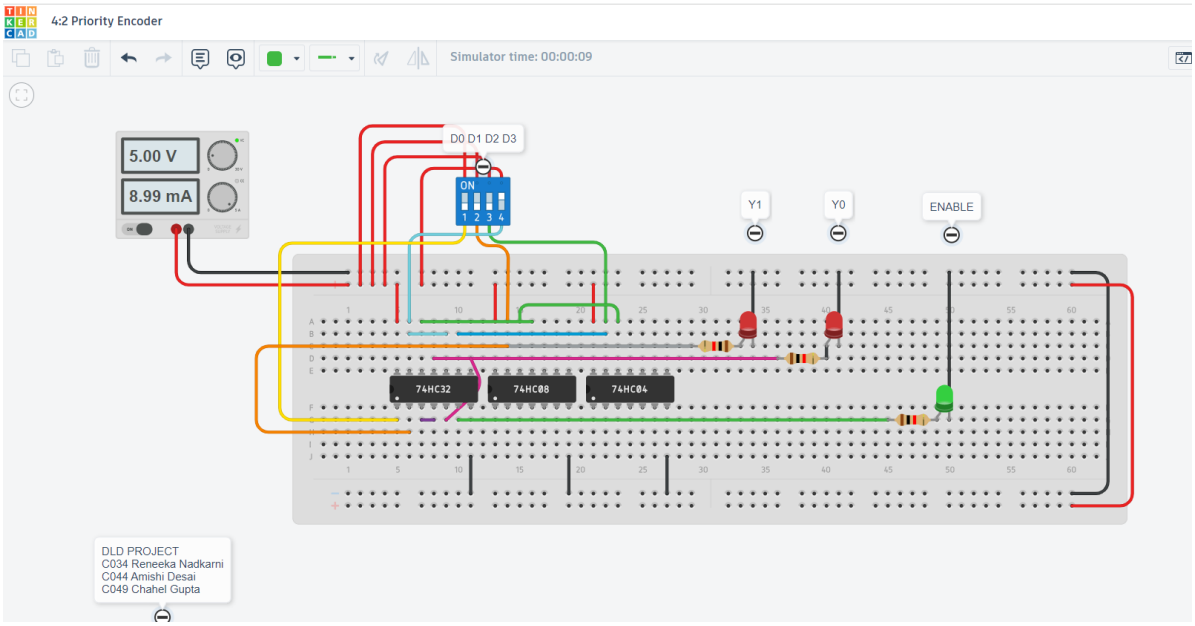
DLD Project - 4:2 Priority Encoder

https://www.tinkercad.com/things/bm26KhEuhHY-copy-of-4-to-2-priority-encoder/editel?sharecode=e2S26zOZ6Lh441NYPSdu0KaVlgRUhMuK6xNZe8z0RIA

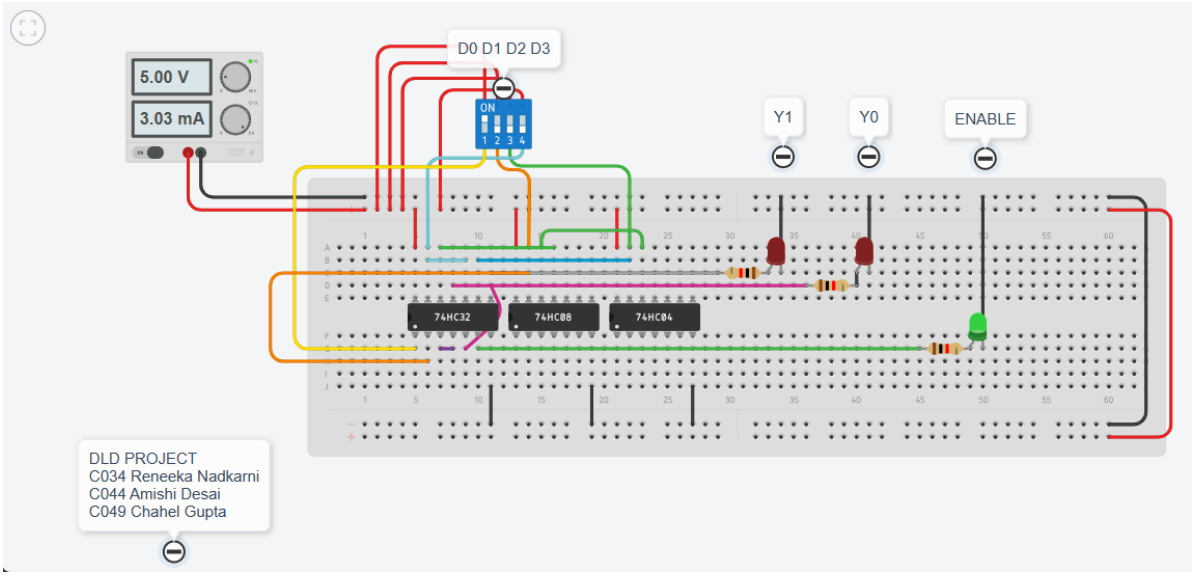
Component List

Name	Quantity	Component
P1	1	5, 5 Power Supply
U1	1	Quad OR gate
U2	1	Quad AND gate
U3	1	Hex Inverter
R1, R2, R3	3	1 kΩ Resistor
D1, D3	2	Red LED
D2	1	Green LED
SW1	1	DIP Switch SPST x 4

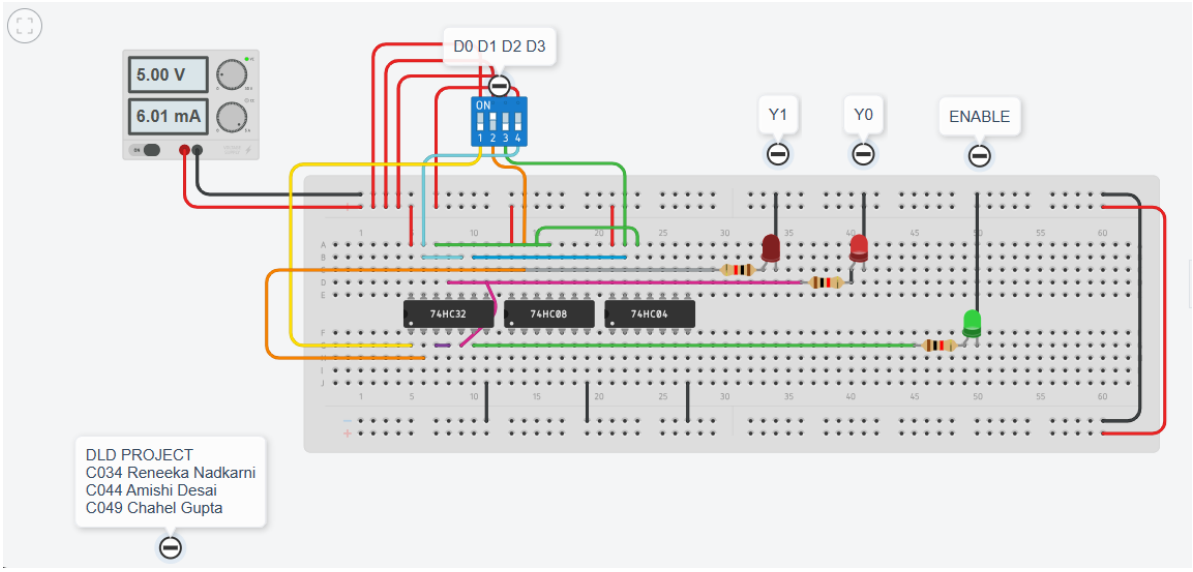
Simulation

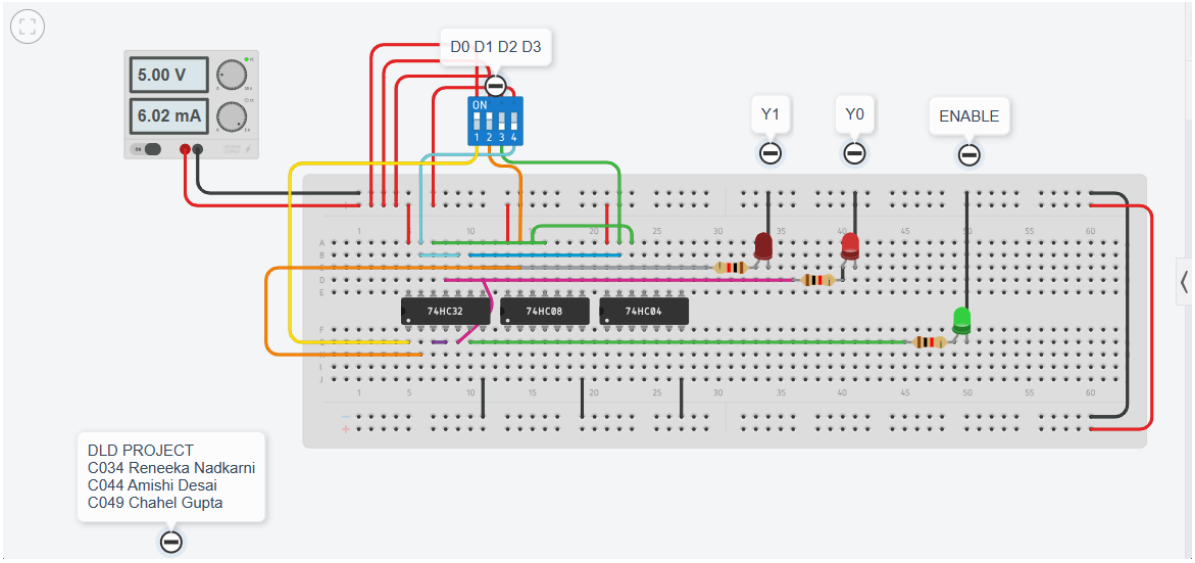


When D0=1

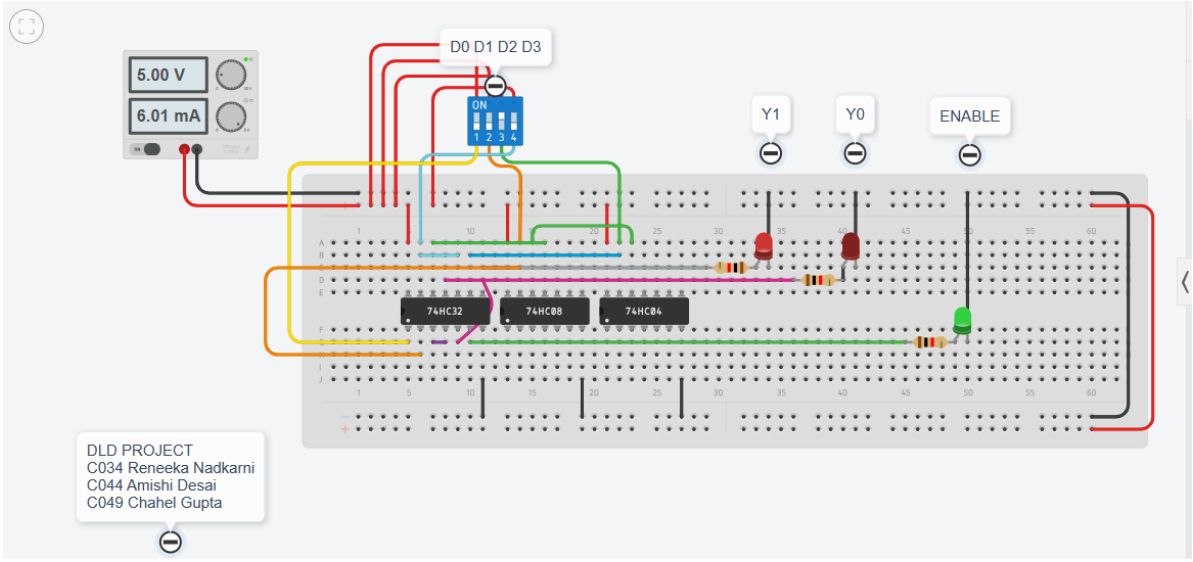


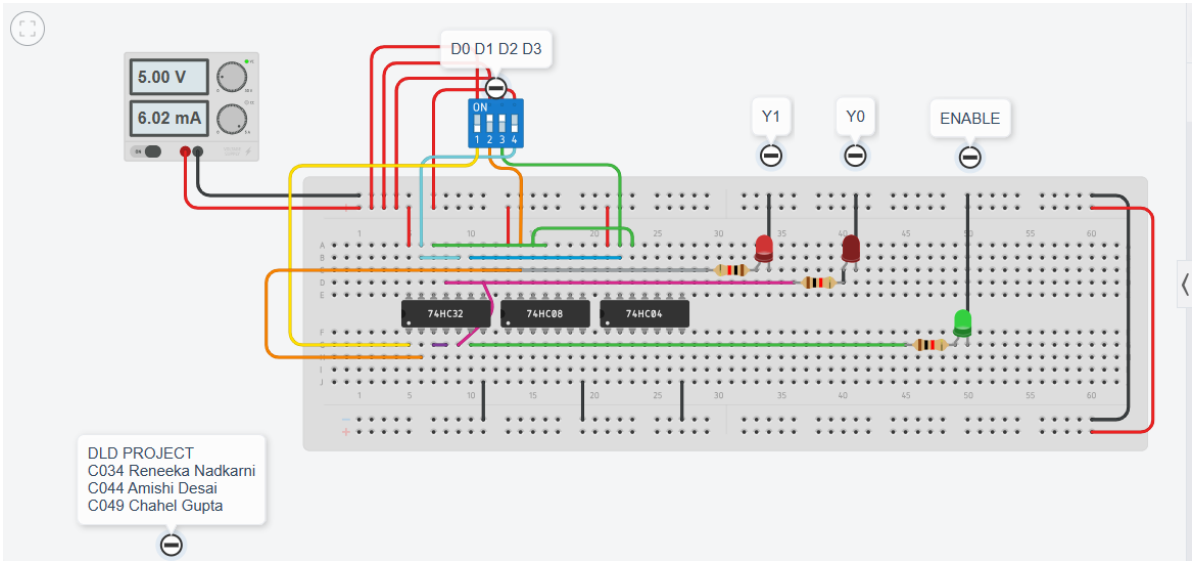
When D1=1





When D2=1




5.00 V
6.02 mA
D0 D1 D2 D3
ON
1 2 3 4
Y1
Y0
ENABLE
74HC32
74HC08
74HC04
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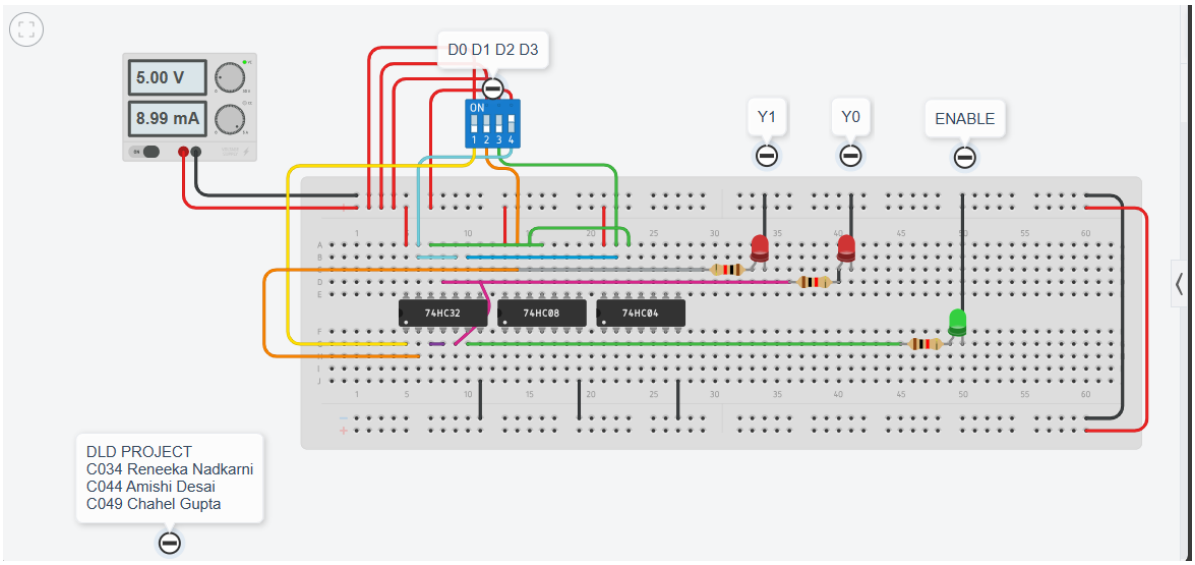
C044 Amishi Desai
C049 Chahel Gupta

When D3=1


5.00 V
8.99 mA
D0 D1 D2 D3
ON
1 2 3 4
Y1
Y0
ENABLE
74HC32
74HC08
74HC04
DLD PROJECT
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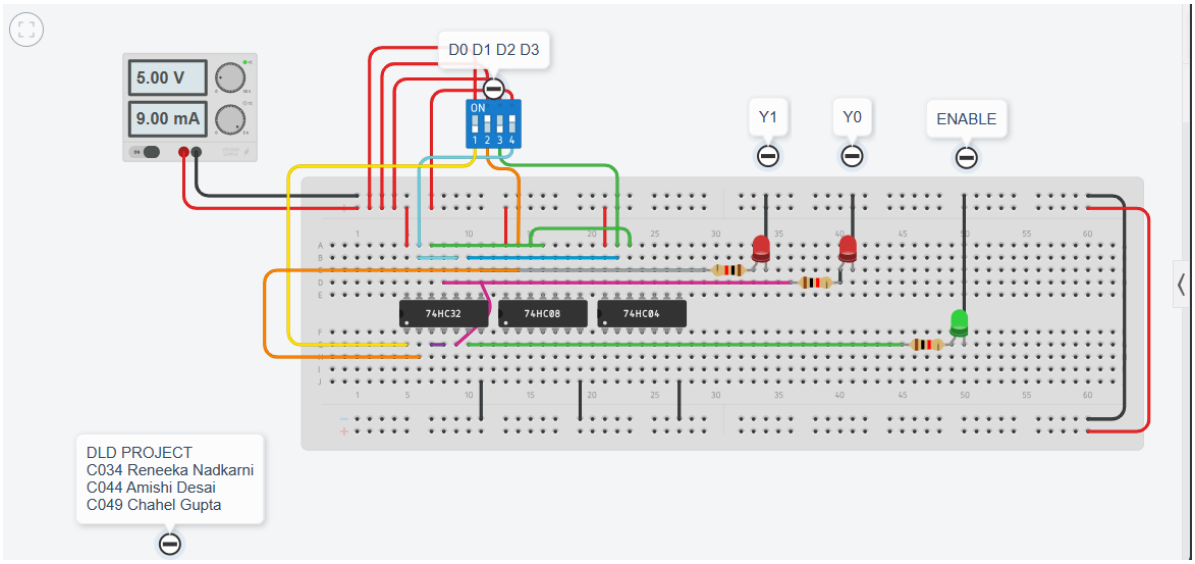
C044 Amishi Desai
C049 Chahel Gupta


5.00 V
9.00 mA
D0 D1 D2 D3
ON
1 2 3 4
Y1
Y0
ENABLE
74HC32
74HC08
74HC04
DLD PROJECT
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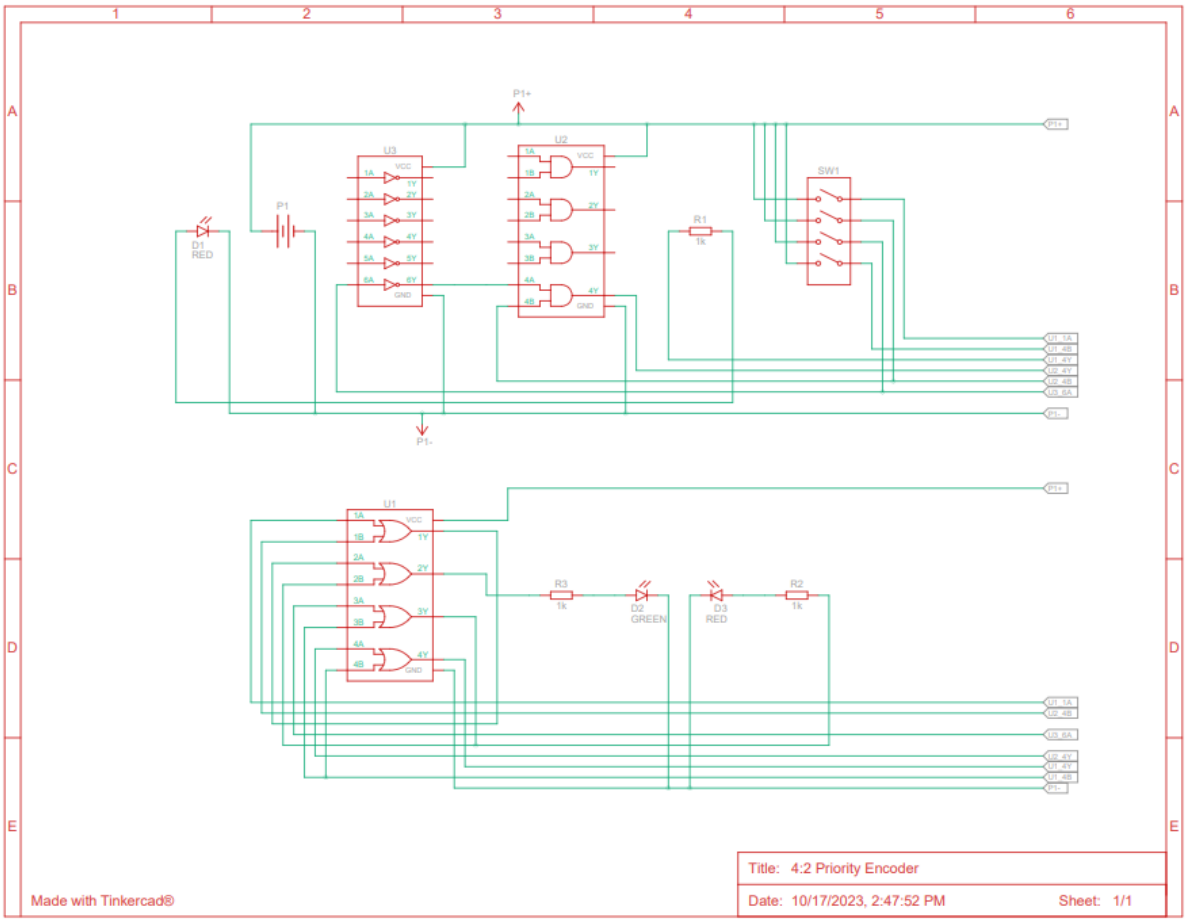
Schematic Diagram of circuit



APPLICATIONS

Priority encoders, fundamental components of digital circuits, find extensive applications across various domains due to their ability to efficiently manage and encode inputs based on predefined priority levels. Some applications include:

1. Interrupt Handling in Microprocessors

Priority encoders are used to manage interruptions in microprocessors, where various devices or processes may simultaneously request a service. It helps prioritize these requests, ensuring that the most critical tasks are addressed first.

2. Network Routing

In computer networks, includes devices such as routers and switches, priority encoders are employed to prioritize incoming data packets based on factors like quality of service, ensuring efficient data routing and allocation of network resources.

3. Traffic Light Control Systems

Priority encoders are also utilized in traffic light control systems to manage traffic flow. Different traffic lanes or routes are assigned priorities, allowing for the smooth movement of vehicles and pedestrians through intersections.

4. Real-time Systems

In real-time systems where immediate and time-critical responses are necessary, priority encoders help to manage multiple inputs/events, ensuring that the most critical tasks are processed first and within specified timeframes.

5. Data Compression and Encryption

Priority encoders optimise compression and encryption processes by assigning priorities to different data packets or segments based on their importance or characteristics.

CITATIONS

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