CO200 - Computer Organization and Architecture

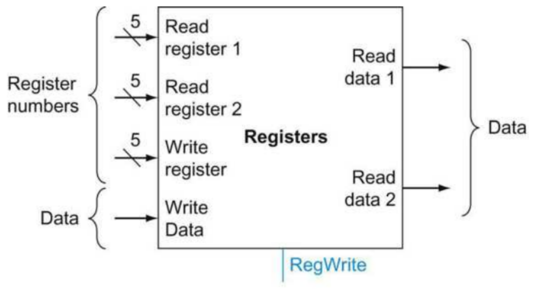
A2 - ALU and Register File Design in Verilog

Points to Note

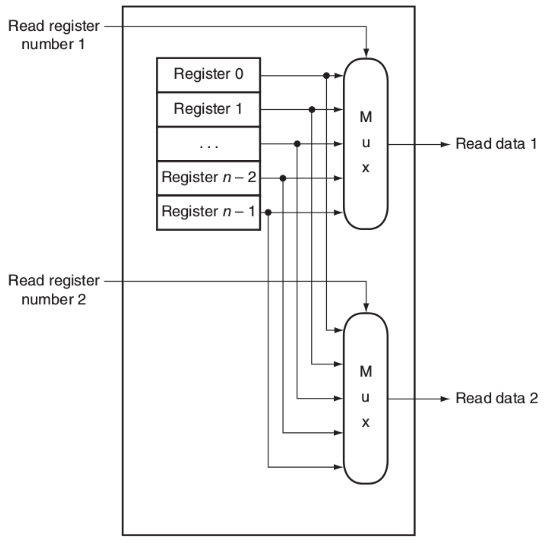
Deadline: Oct., 25, 9AM.
Submission guidelines: Same as A2.

Modules

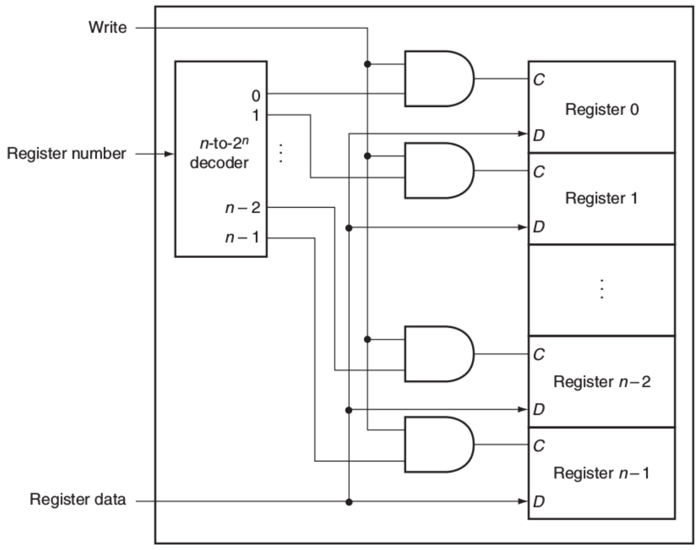
1. **1-bit ALU**. Build a 1-bit ALU that was designed in the class. The ALU should perform the following logical and arithmetic operations: AND, OR, NAND, NOR, ADD, SUBTRACT. The ALU should generate a flag to indicate if the result of the ALU operation is zero (Z). *Hint:* Reference implementation is described in Section in 4.4. *Patterson and Hennesy, Computer Organization and Design - RISC-V Edition, MK.*
2. **64-bit Integer ALU Design.** Extend the 1 bit ALU to support the same tasks on 64-bits.
3. **ALU Control.** Design the ALU control for the above 64-bit Integer ALU. The control unit takes in 2 inputs: (a) A 2-bit input that distinguishes the nature of operation to perform – R-type (2'b10), Add operation instructions (2'b00), Subtract operation instructions (2'b01). (b) Minimal bits from the `funct3` and `funct7` bits of the instruction to identify the operation. You are free to deviate from the design shown in the class/textbook to achieve the objectives.
4. Build an complete 64-bit ALU unit instantiating the previous 2 modules. *The testbench should task the ALU on all possible operations, corner cases (min/max values of operands) in each operation and also a sufficient number of typical cases.*
5. **Register File**. Use the register designed in A1 to implement a 32 register Register file with two read ports and one write port. Block diagram in Section 4.3, Fig. 4.7a, PH-RISC-V, Page 245 (Page 490 in the PDF). The block diagrams of the two read ports and the write port are shown separately (Figures B.8.8 and B.8.9).



3 Port Register File



(a) Register File with two read ports.



(b) Write port implementation in the Register File.

Hint: For the block diagrams and design of the Register File refer Section B.8 of *Patterson and Hennesy, Computer Organization and Design, 5e, MK.*