KANDULA CHAITANYA RAMANJANEYULU

VLSI engineer

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○ github.com/dashboard

CAREER OBJECTIVE

Aspiring VLSI engineer with strong fundamentals in EDC, ECA, STLD, and EMWTL. Keen to apply my skills in digital design, along with basic knowledge in full stack and data analytics. Committed to growth and excellence with a CGPA of 9.16.

WORK EXPERIENCE

Data Analytics Internship, *Brainwave Matrix Solutions*   03/2025 – Present
                                                                              Virtual

- Analyzed Amazon sales data using Pandas and NumPy to identify trends, seasonal patterns, and key performance metrics.
- Cleaned, processed, and visualized large datasets to extract actionable business insights.
- Conducted Sentiment Analysis on social media data to evaluate customer opinions and brand perception.
- Built data pipelines and generated reports to support data-driven decision-making.

EDUCATION

B.Tech, Electronics and Communication, *Vishnu Institute Of Technology*   2023 – 2027

Senior Secondary (XII), Board Of Intermediate Education, Andhra Pradesh,   2023
Sri Chaitanya Jr College
Percentage: 97.00%

SKILLS

- Python
- HTML
- CSS

- Verilog
- C Programming
- Data Analytics

TRAININGS / CERTIFICATIONS

Very Large Scale Integration, *Hindustan Private Limited, Virtual*   01/2025 – Present
Completed fundamentals in CMOS digital design, ASIC, and FPGA as part of my VLSI course at HCL. Gained practical knowledge in Verilog coding, and developed an understanding of digital design, including circuit synthesis and implementation in ASIC/FPGA environments.

EXTRA CURRICULAR ACTIVITIES

- Participated in hackathons, creating innovative solutions and collaborating with teams. Delivered presentations at Research Day events and seminars, showcasing strong communication and technical skills. Actively participated in branch-wise cricket tournaments, gaining recognition for bowling skills. Engaged in various technical and non-technical events, demonstrating leadership, teamwork, and time management.