**ECE 6370: ROM Homework**

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**Memory controller Verilog code:**

// ECE 6370

// Author: Chaitanya Narayanavaram, 6728.

`timescale 1ns/10ps

module ROMController(Data\_In, Address, Data\_Out, Clk, Rst);

input [3:0] Data\_In;

output [5:0] Address;

reg [5:0] Address;

output [3:0] Data\_Out;

reg [3:0] Data\_Out;

input Clk, Rst;

always @(posedge Clk) // One-procedure

begin

if(Rst == 0)

begin

Address <= 0;

end

else

begin

case(Address)

0,1,2,3,4,5,6,7,8,9,10: begin

if(Data\_In == 4'b1111) // 1111 (or) 15 is the ending word

begin

Address <= 12;

end

else

begin

Data\_Out <= Data\_In;

Address <= Address + 1'b1;

end

end

12: begin

Data\_Out <= 0;

end

default: begin

Address <= 0;

end

endcase

end

end

endmodule

**Testbench Code:**

// ECE 6370

// Author: Chaitanya Narayanavaram, 6728.

`timescale 1ns/10ps

module MyROMTestbench();

wire [3:0] Data\_s;

reg Clk\_s, Rst\_s;

MyRomTopModule DUT\_MyRomTopModule(Clk\_s, Rst\_s, Data\_s);

always

begin

Clk\_s = 0;

#10;

Clk\_s = 1;

#10;

end

initial

begin

#3 Rst\_s <= 0;

@(posedge Clk\_s);

#3 Rst\_s <= 1;

@(posedge Clk\_s);

@(posedge Clk\_s);

@(posedge Clk\_s);

@(posedge Clk\_s);

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@(posedge Clk\_s);

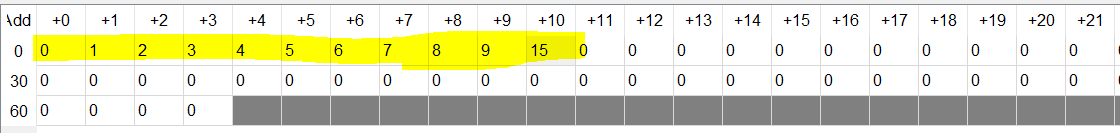
@(posedge Clk\_s);

end

endmodule

**ROM details:**

The ROM that I have chosen has 64 words and each word is 4-bits long.



**Waveform:**

