PROJECT 2 REPORT

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Introduction:

This project deals with the modelling of a shifter which can perform logical left shift, logical right shift, arithmetic left shift, arithmetic right shift, cyclic left shift, and cyclic right shift with the shifting bits from 1 to 4. These shift operations are performed using three bits which decide what type of bit shift operation to be performed and two bits deciding how many numbers of bits to be shifted. This shifter is a combinational shifter rather than a sequential shifter which shifts the bits based on the combinational circuits rather than using latches, flip-flops etc., the modelling of the shifter is done using Cadence Virtuoso schematic and the analysis was done for power and delay. The delay optimization is done using minimal delay analysis. The shifter checks and power analysis is performed from the MATLAB which implemented the test cases with the results captured from virtuoso and exporting the results to a csv file. Below is the screen shot of the successful implementation of the checker.

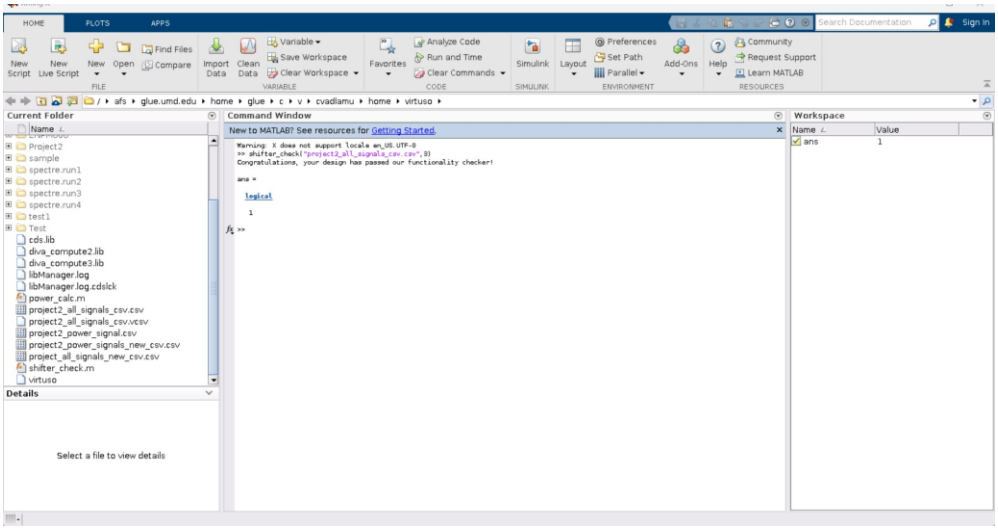

Fig:1 shifter check

The power analysis is done through obtained power results from the waveform tool in virtuoso and performed the power analysis through MATLAB. Below is the screen shot of the power analysis.

```
>> power_calc("project2_power_signal.csv")

ans =

   1.5081e-09
```

Fig:2 power analysis

The delay analysis has been performed at 10ns and 30ns where all transitions of output signals take place. Below are the results of the delay analysis.

Propagation delay for	Transition 1(10ns)	Transition 2(30ns)
Y0	364.4E-12	426.4E-12
Y1	347.9E-12	364.3E-12
Y2	425.3E-12	364.3E-12
Y3	425.3E-12	432.0E-12

Table:1 Delay analysis

The above delay analysis shows the worst-case delay is 432.3 E-12. The detailed analysis of these results will be discussed in the Results and Discussion section.

From the results we can see that the implementation of design should be in such a way that we should extend our functional implementation with the objective of obtaining the optimized one. For the power analysis we are required to maintain minimum number of transitions and most of the times muti stage design will not work for power optimization. For delay optimization, we can optimize through minimizing resistance and capacitance. It is advisable to properly analyze the logical and electrical efforts of each stage for better delay optimization.

Design:

The design is performed hierarchically. I have analyzed the problem algorithmically. I have designed a 3-8 decoder to know what type of shift operation must be performed. Based on the decoder output, we will know what type of operation is to be performed. To know how many bits to shift I have utilized a 4-1 Mux to output the required result to the appropriate bit. At the end we will have a 6 input OR(NOR-INV) which takes the output from the various mux to output a single result.

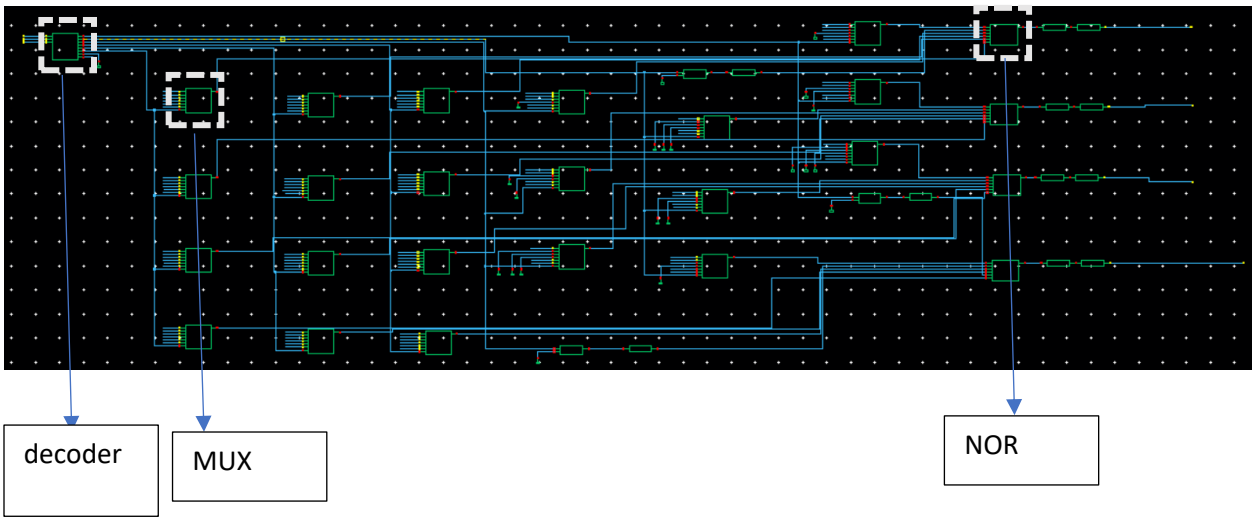

Fig:3 Design of the circuit with 3-8 decoder, MUX and NOR

The main components involved in the circuit are the decoder, MUX and NOR gate. To optimize the circuit either through power or delay, it is required to design this circuit efficiently according to the necessary performance metric which we want to analyze. I have taken the option of minimizing the delay. In delay optimization, it is required to analyze the logical effort and electrical effort. For the 3-8 decoder, I have

utilized a 3 input NAND gate with an inverter with the normal transistor sizes according to the unit inverter. Below is the circuit of a 3-8 decoder.

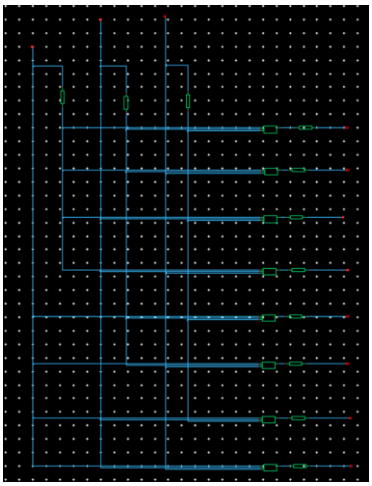

Fig:4 3-8 decoder design

For designing 4-1 MUX, I have opted the designing 4-1 MUX using three 2-1 MUX. Since this Mux must provide its output only when the appropriate type of operation selected, I have used NAND gate as an enable for the MUX. The design of 2-1 MUX was done as an Inverting Mux to reduce the number of transistors and RC delay.

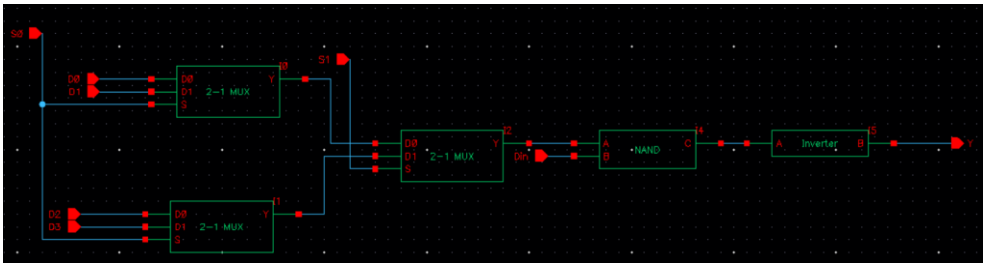

Fig:5 4-1 Mux design

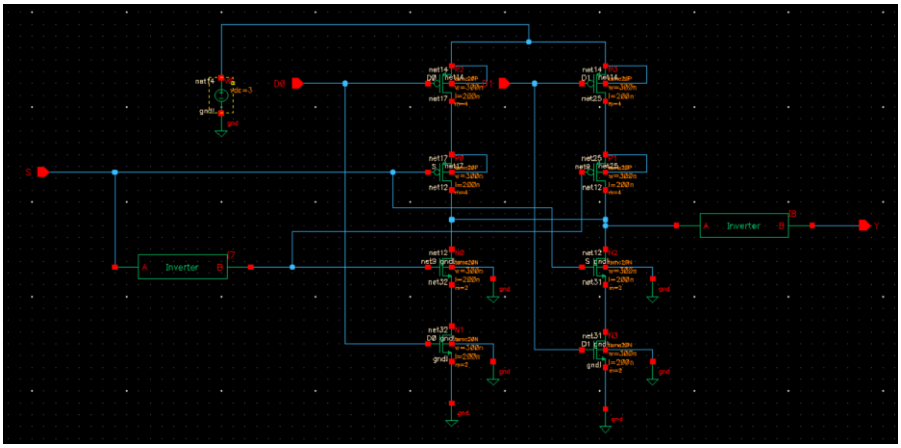

Fig:6 2-1 Inverting Mux design

For designing 6 input NOR gate there are various design options which are available. I have implemented the NOR gate with minimum possible NOR gates. Various design options are made and choose the below the best possible design.

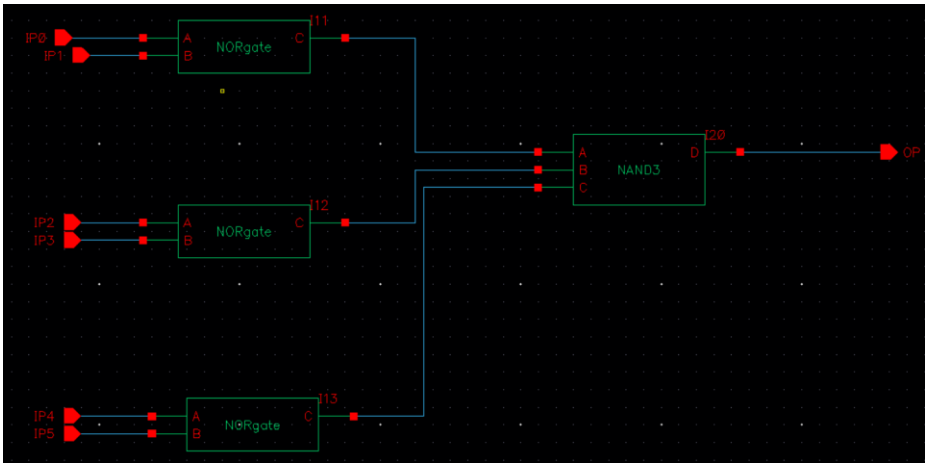

Fig:7 6 input NOR gate

To further minimize the delay, the transistor width of the final inverter is chosen to get the minimum delay. Since the resistance play a prominent in the delay optimization where we have seen in the Elmore's delay calculation. The resistances are added and then multiplied with capacitance. Therefore, it is important to decrease the resistance, and this can be done by adjusting the transistor widths accordingly.

Results and Discussion:

Based on the above implementation, we have calculated the delay accordingly. Below is the figure demonstrating the maximum transition delay obtained.

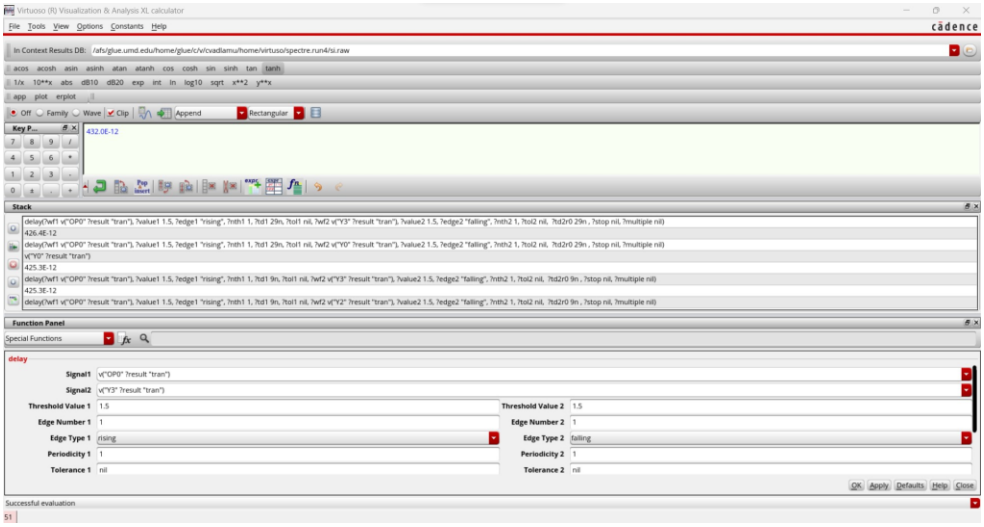

Fig:8 demonstrating the maximum delay output

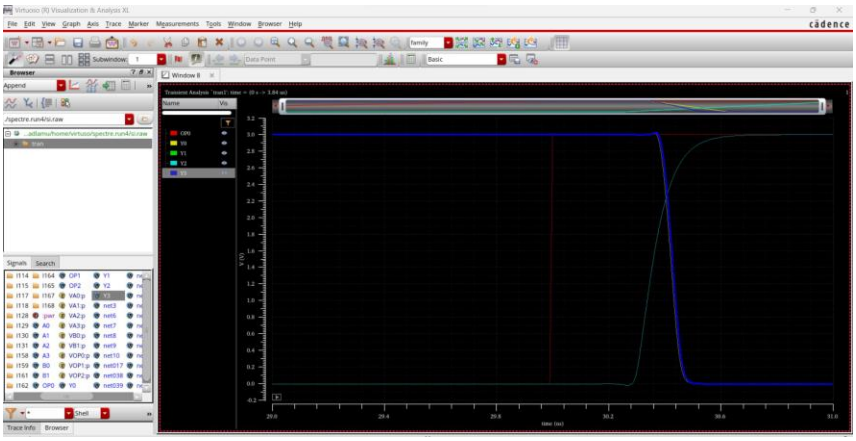

Fig:8 Transitioning delay graphs.

To further reduce the delay, we must resize the transistors to get the minimum delay. We can further minimize the delay and power if we have implemented the circuit directly from the min or max terms from the combinational logic by modelling them through complex complementary CMOS design. This design which was implemented provides us enough room to choose various optimized MUX, decoder and NOR gates. You will be having various permutations and combinations. This design also provides scalability, you can enhance this design to perform a greater number of operations by just replacing a decoder or MUX according to your design. We can change the inverter load to adjust the electrical effort to minimize the delay accordingly.

For power optimization, it is advisable to go with the minimum number of gates and minimum number of transitions. So, it is advisable to go with combinational circuit directly from the min or max terms instead of implementing through algorithmically.

The results which were obtained were demonstrated in figure 2 and Table 1.

Conclusion:

Through the above design, we can achieve a much more scalable design with minimum delay. A further reduction in delay can be made by reducing the resistance to the cost of increased area and reducing the number of branches. For power analysis it is always advisable to use a minimum number of transistors. Path delay analysis is good to perform to obtain a better outlook of number of stages to be selected and the transistor sizes for delay optimization.