Final Project Report – Neuron Spike detection/Sorting **-Chaithanya Krishna Vadlamudi**

Analysis of signals:

We can differentiate the input electrode signals are 5 different voltage levels.

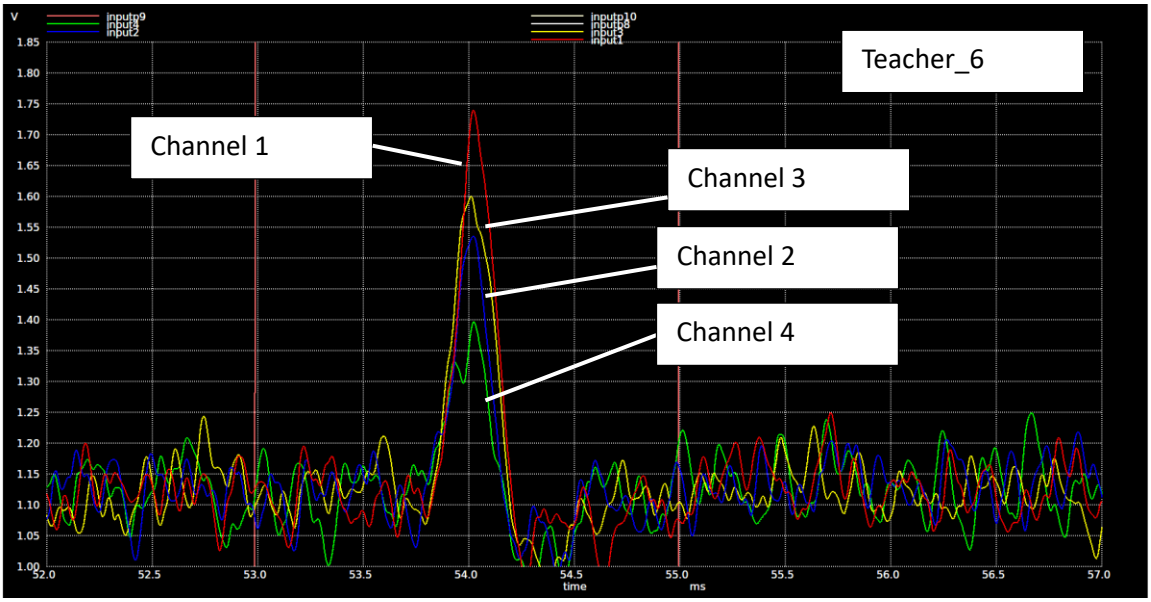


Fig:1 signal graph for Teacher_6

These are the 4-electrode signals which are represented in the above figure. This is at Teacher 6 pulse. We can see 4 of the different voltage levels in this signal.

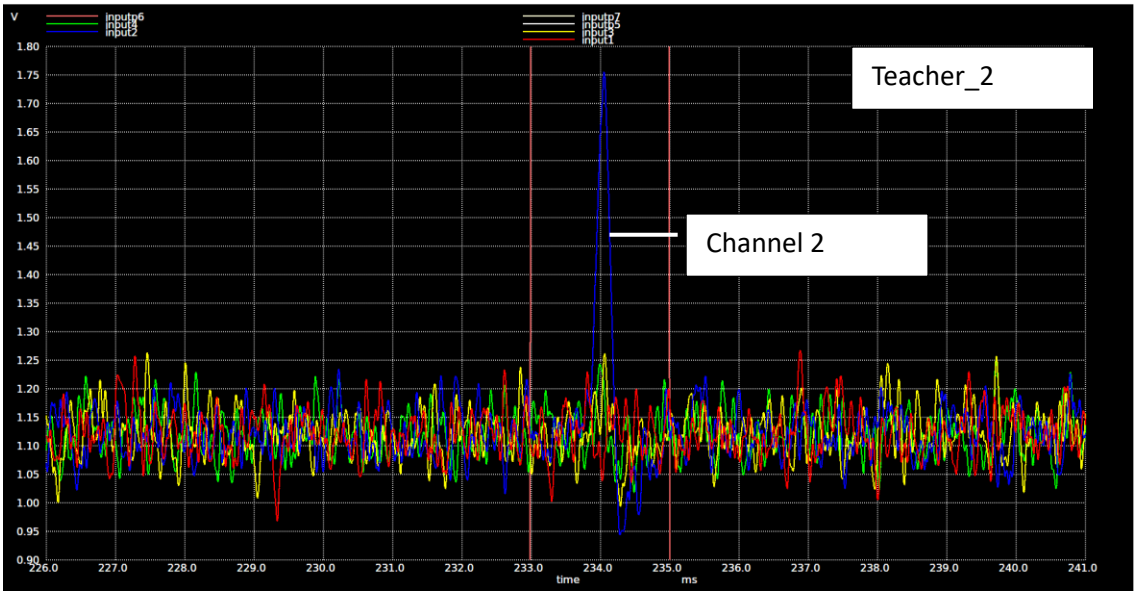


Fig:2 signal graph for Teacher_2

The above signal in here demonstrates the noise voltage which are at the voltage range 1.25-1.15

Project High level Design and construction:

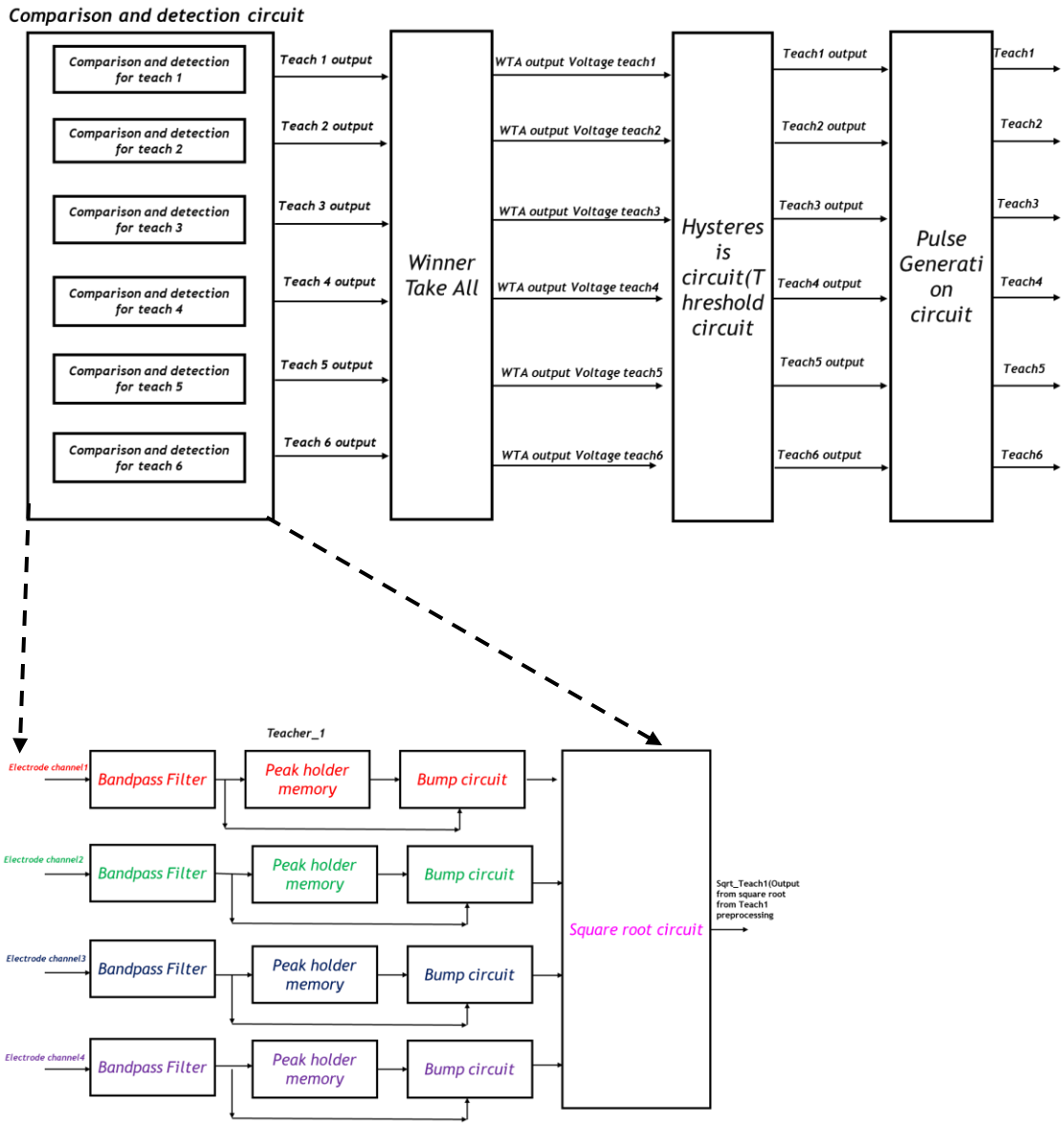
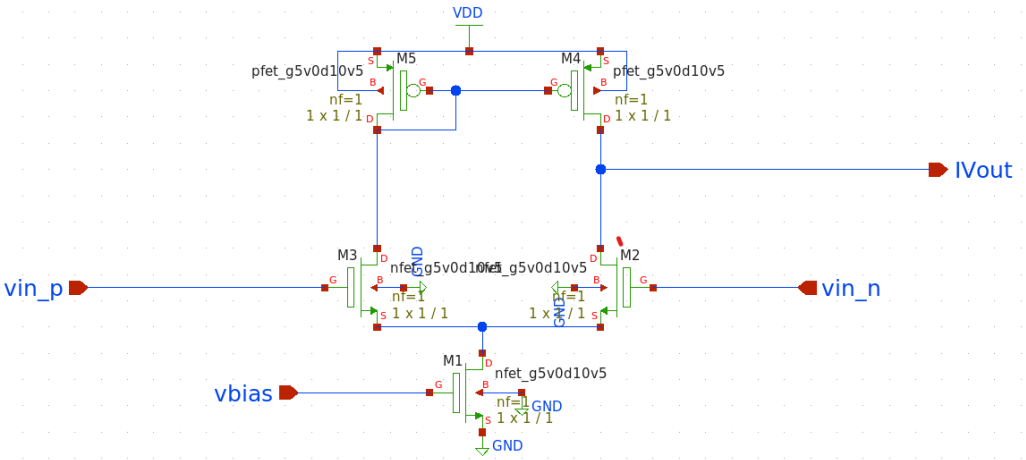


Fig:3 High level design

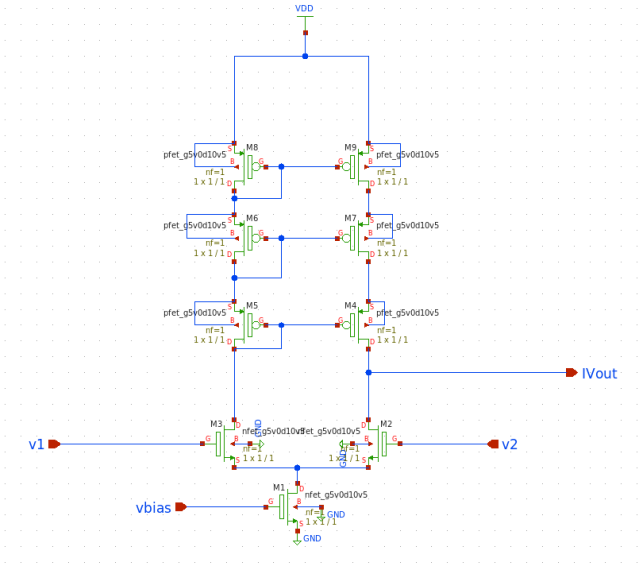
Before going into the actual circuits. I want to provide circuit designs of transamp circuits.

Circuit diagram of Transamp1:

Wherever you see Transamp1 it implies the below circuit:



Circuit diagram of Transamp2:



Transamp2 circuit is used whenever I want to get the accurate value with less early effect.

Comparison and detection circuit:

The comparison and detection circuit consists of several blocks 1) Bandpass filter 2) Peak holder memory 3) Bump circuit 4) Square root circuit.

Bandpass filter: The Bandpass filter is built from a high pass filter in conjunction with a low pass filter. The high pass filter is designed to eliminate the 60hz signal which is being obtained from the environment. The low pass filter is combined with high pass filter. The low pass filter is designed to eliminate high pass frequencies which have less magnitude. These high pass filter frequencies are selected through Fourier analysis. Below is the circuit of the bandpass filter.

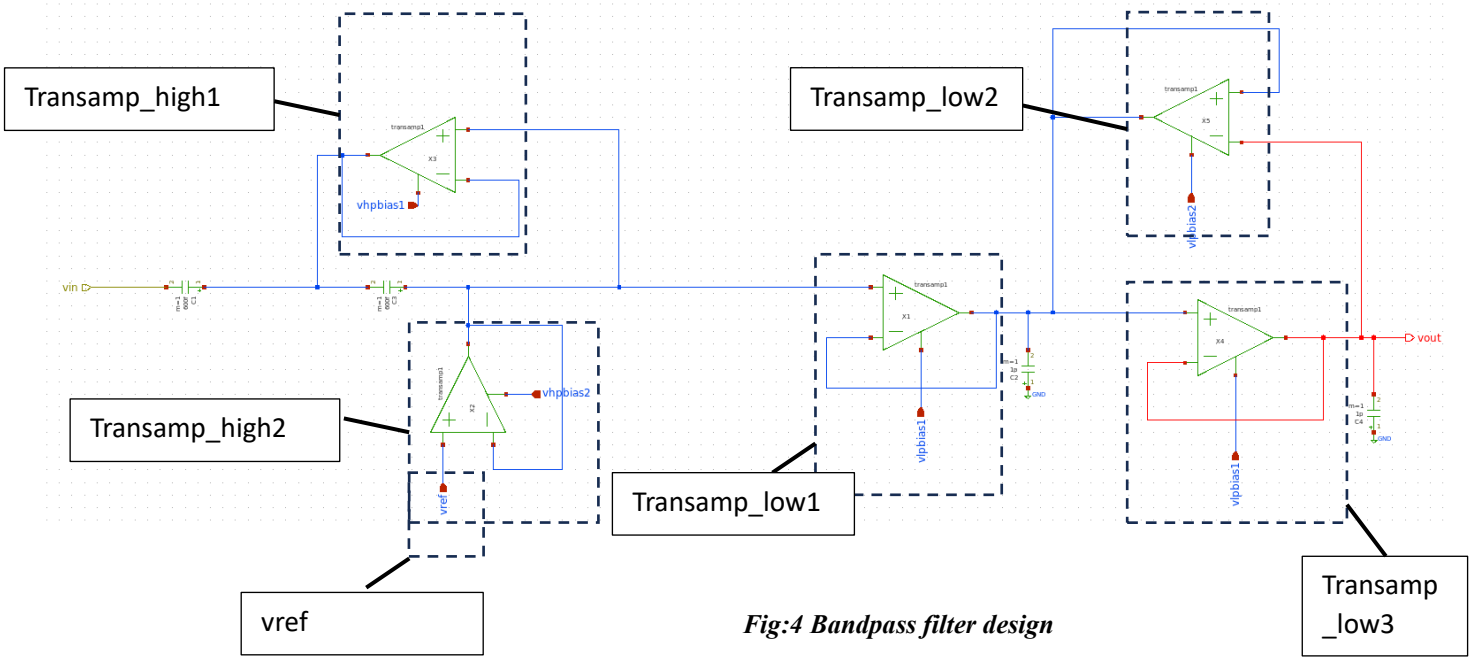


Fig:4 Bandpass filter design

The capacitors values chosen for the high pass filter were 600f and for the low pass filters 1p. Below are the values chosen for the band pass filter.

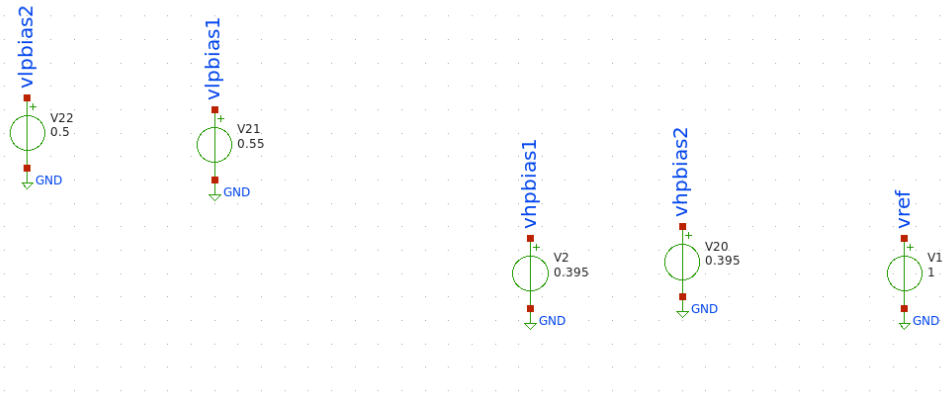


Fig:4 Bandpass design input values

Inputs for the bandpass filter:

Voltage Label	**Value**	**Representation in circuit**
Vlpbias1	0.55	Transamp_low1, Transamp_low3
Vlpbias2	0.5	Transamp_low2
Vhpbias1	0.395	Transamp_high1
Vhpbias2	0.395	Transamp_high2

Vref	1	Vref

Vlpbias1= low pass bias 1 voltage which was used for both transamp_low1, transamp_low3 = 0.55

These values are chosen by applying the following equations for the transamp

$$Gm = \frac{I_b \times k}{2V_T}$$

Where Gm indicates Transamp conductance. Ib is the bias current, k is kappa, V_T is thermal voltage.

From the above equation, we can obtain current Ib and providing appropriate Vbias voltage.

$$v_b = \frac{v_T}{k} \ln\left(\frac{I_b}{I_0}\right)$$

Or other you can model the nFET in the simulator and check for the current vs voltage graph by changing the gate voltage.

Below is the carried-out **Fourier analysis** in Ngspice:

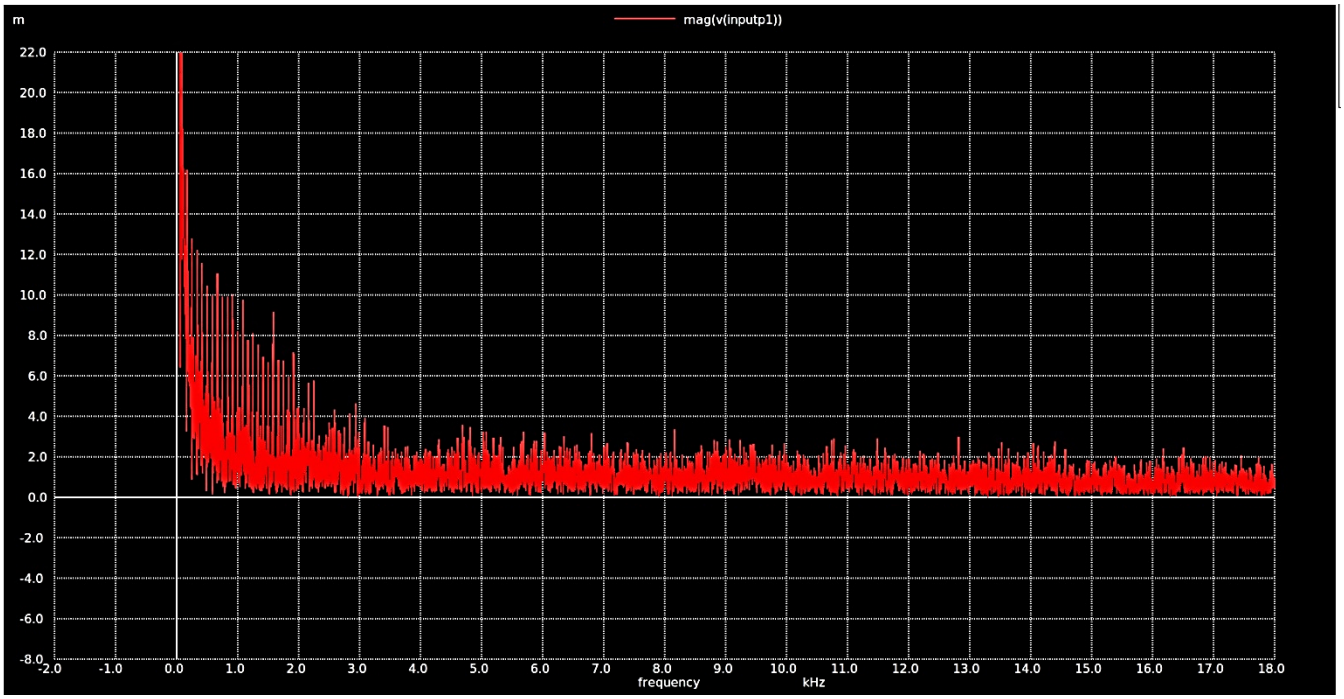


Fig:5 Fourier analysis

The above graph is the zoomed in version to khz

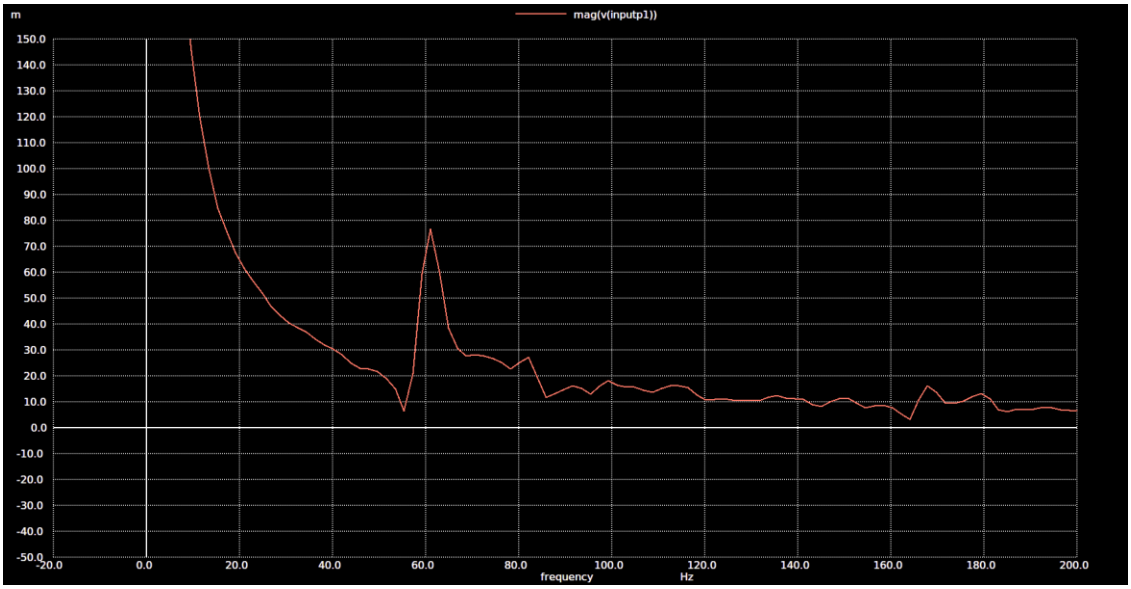


Fig:6 Voltage amplitude peak at 60Hz

This spike in voltage occurs at 60hz which is at low frequency.

Below is the frequency response analysis of the bandpass filter which was used:

Frequency response magnitude plot:

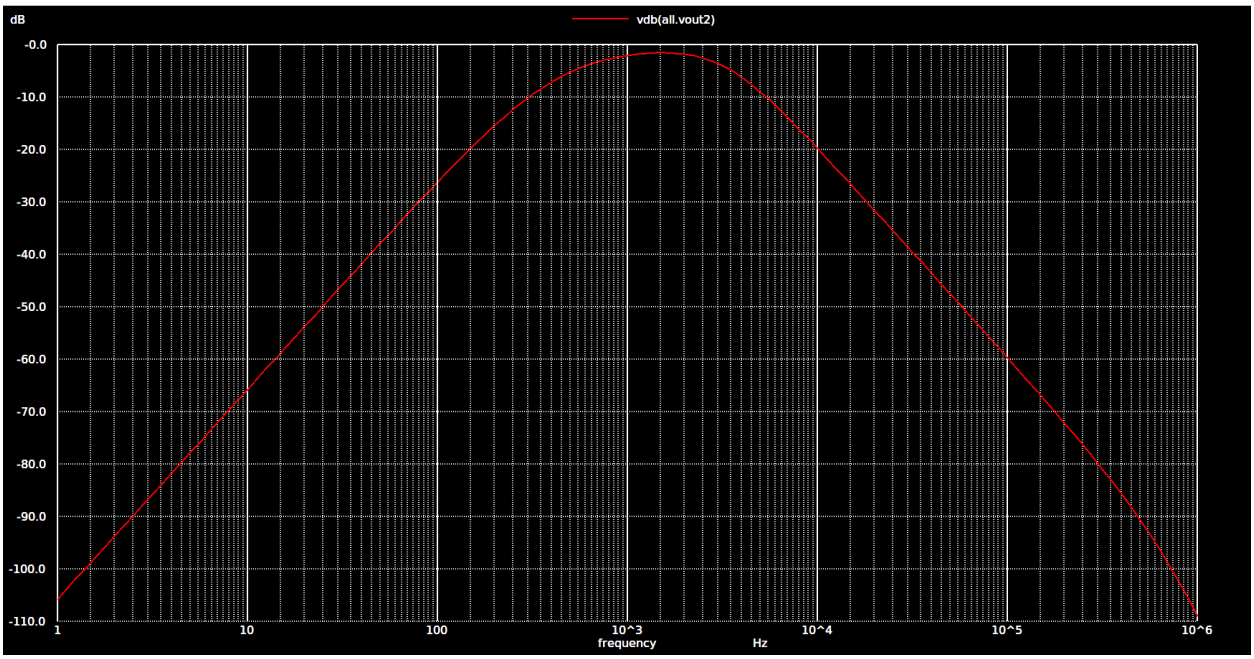


Fig:7 Frequency response magnitude plot

By looking at the magnitude plot here, we can say almost most of the 60Hz magnitude got filtered and high frequency values of more than 7-8KHz got filtered.

Frequency response phase plot:

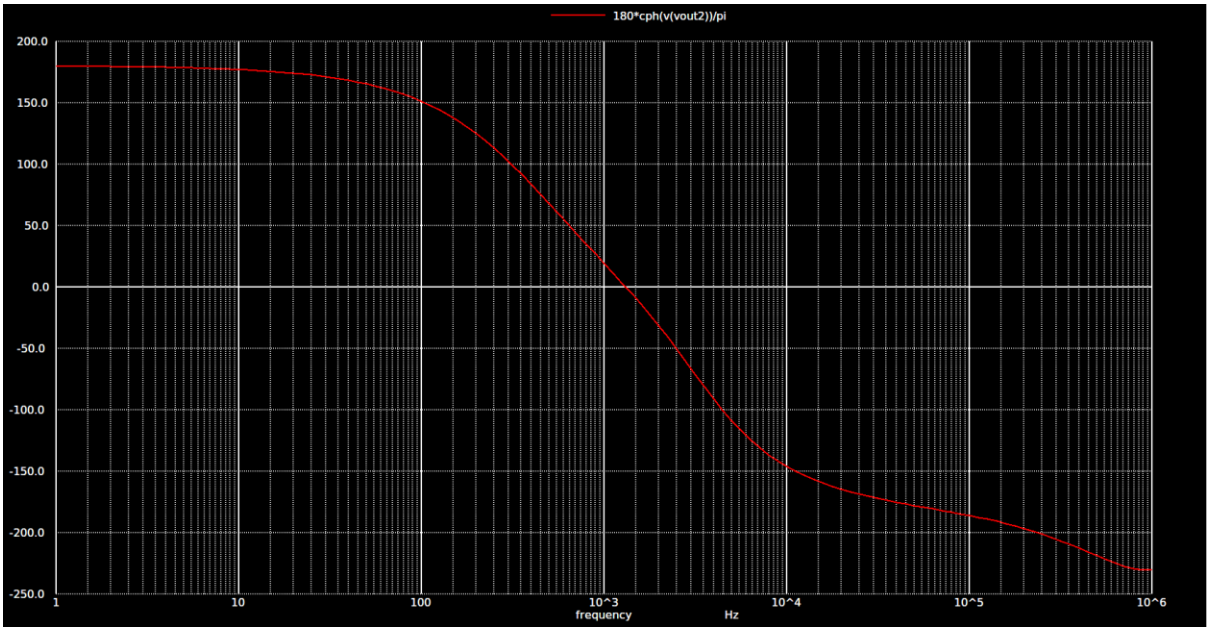


Fig:8 Frequency response phase plot

The phase is mostly not changing too much between the range in which are measuring the signal.

Transient response analysis from the Bandpass filter of electrode channel1:

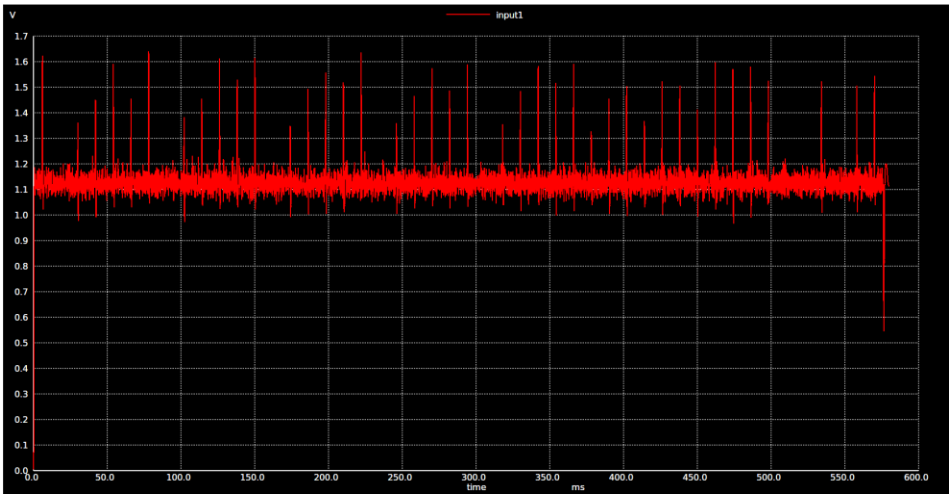


Fig:8 Transient response output

We can see most of the 60Hz waveform and the high frequency waveforms got filtered. The above graph shows the electrode channel one filtering transient response.

Peak Holder Memory Circuit:

For Peak Holder Memory Circuit I used the pFET based peak detection circuit. The reason why I did not choose nFET based peak detection circuit is because of overshot in voltage due to the diffusion capacitance. I used the extreme version of the memory circuit as it provides sample averaging. Below is the circuit diagram of the peak holder memory circuit.

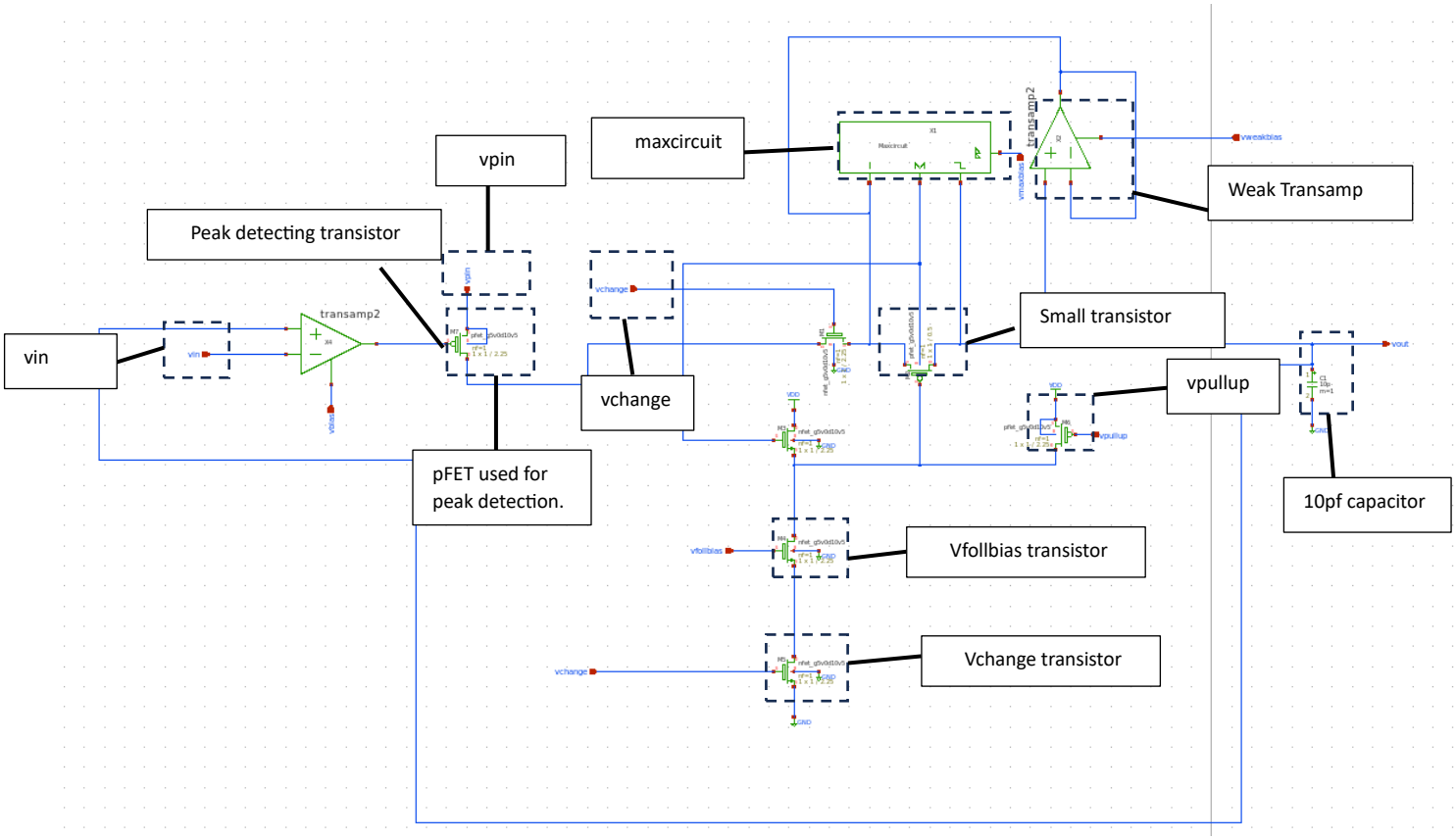


Fig:9 peak holder memory circuit

Here the capacitor is 10pF and we will be controlling the charging of the capacitor with two tunable parameters vpin(supply voltage for the peak detecting nFET voltage) and vfollbias(One of the pulling transistors of the small size transistor). You can also choose any other degree of freedom vpullup if we require. The values are tuned with those specified parameters in such a way that the valid sample average value need to be stored in the 10pf capacitor.

Working: The input voltage from the band pass filter is applied to the vin (negative side of the input of the transamp) and the positive side is connected to the 10pF capacitor which stores the peak of the signal at the corresponding teacher signal. These teacher signals are applied as inputs to vchange and vpullup. When the input value is less than the stored value of the capacitor, the output of the transamp is pulled down then peak detecting transistor gets turned. Supply voltage to the peak detecting

transistor is determined by how fast and how much charge you want to store in the capacitor. nFETs which are being provided with Vchange gate voltage get turned on which makes the capacitor to charge. How much charge you want to impart into the capacitor is determined by how hard you want to pull the small transistor. The conducting pFET transistor is chosen as small (in the sense area is small) to reduce the charge injection during switching. The max circuit is there to hold the capacitor without any leakage and appropriately conduct the current when the vchange signal is provided. For the weak transamp we will provide very low bias voltage in order not to flow not much current. If it gets much current the input voltage which is being provided to the capacitor might not be that accurate.

Max circuit:

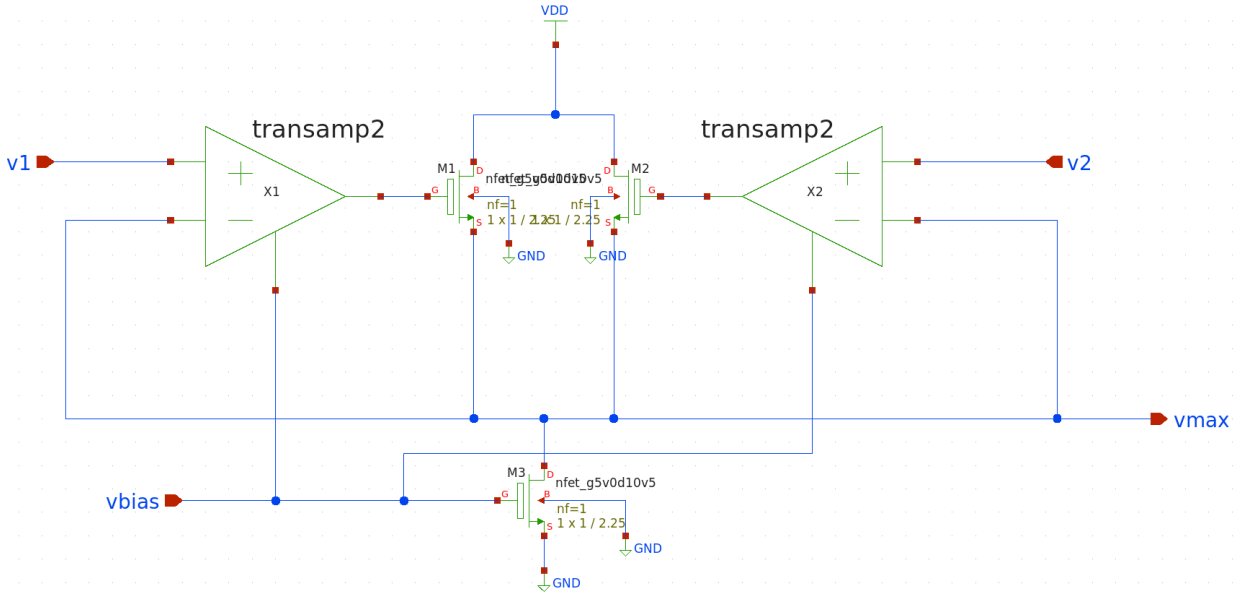
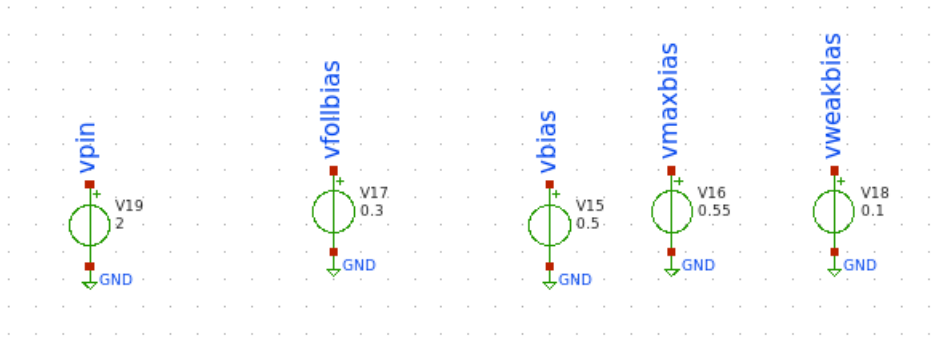


Fig:10 Max circuit

This max circuit brings the maximum of the two voltages which basically works with the intuition of Transamp circuit.

Inputs provided to the peak holder memory circuit:

Transistor name	**Input**	**Representation in Figure**
Peak Detecting transistor	Input	vin
Vpin	2	Vpin
Vchange	Teacher signal input	Vchange
Vpullup	Teacher signal input	Vpullup
vfollbias	0.3	Vfollbias transistor
vweakbias	0.1	Weak transamp bias



Transistor sizes used for peak hold circuit and Max circuit:

All the nFET are of 1*1*2.25 except the small transistor which is of 1*1*0.5. For the max circuit all the nFETs are of 1*1*2.25 and for the transamp2, all the pFETs and nFETS are of size 1*1*1.

Inputs provided to the Max circuit:

For the max circuit one of the inputs comes from the stored capacitor and the other input is from the input and the max circuit output is provided to the body of the weak transistor. This approach provides the minimum leakage as the input, output and body will be at the same voltage as a result we will get very minimal drain leakage.

Signal output signals from the peak detection:

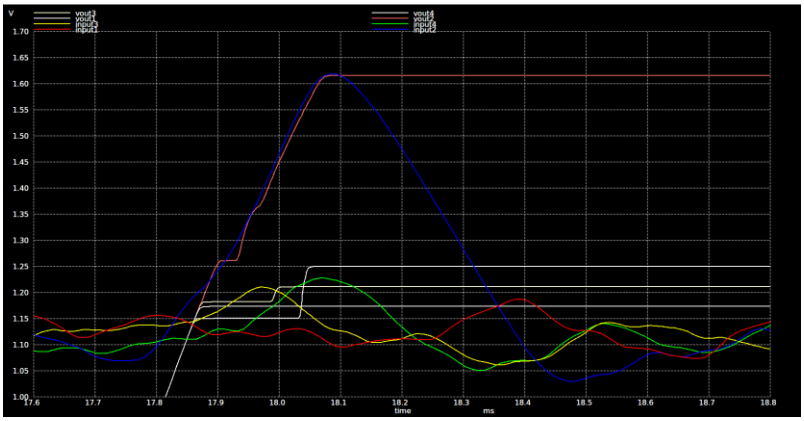


Fig:11 peak detection output Zoomed in version

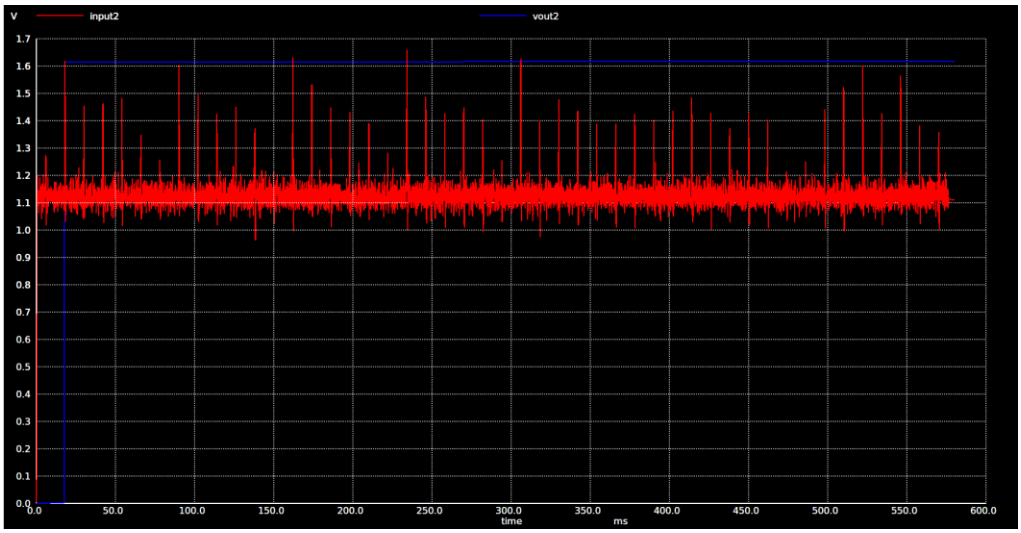


Fig:12 peak detection output zoomed out version

Bump Circuit:

Bump Circuit is basically used for the comparison of the stored value with the actual value from the bandpass filter. If the two values are matched, then we get a bump in the current which tells you that the voltages are matched at that bump value of the current.

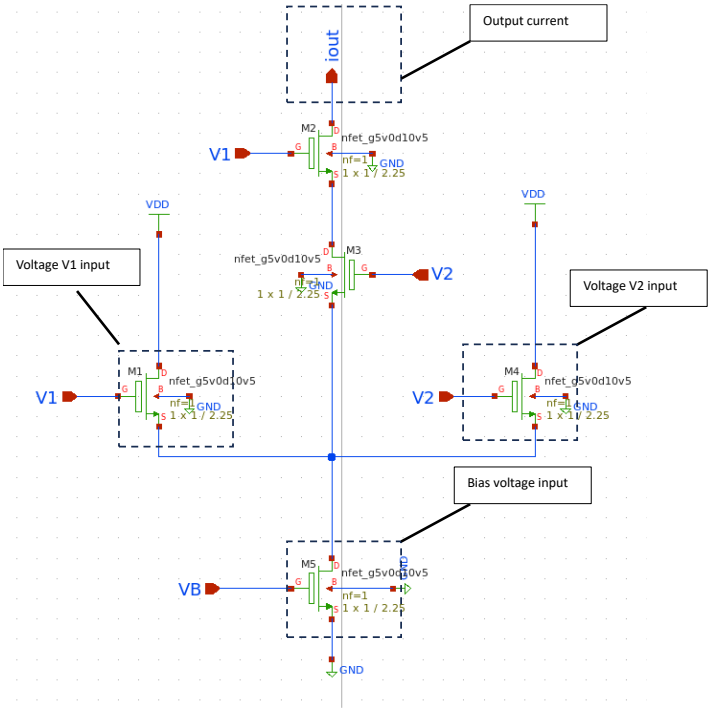
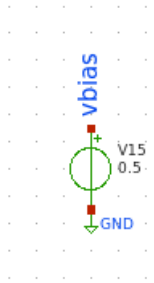


Fig:13 Bump Circuit

Inputs/Outputs from the bump circuit:

Voltage Label	Value	Figure representation
V1	Input from the peak holder circuit	Voltage V1 input
V2	Input from the bandpass filter	Voltage V2 input
VB	0.5v	Bias Voltage input
iout	Current output to square root circuit	Output Current



Transistor sizes used for Bump circuit:

All the nFETs are of size 1*1*2.25.

Sample Output from the bump circuit:

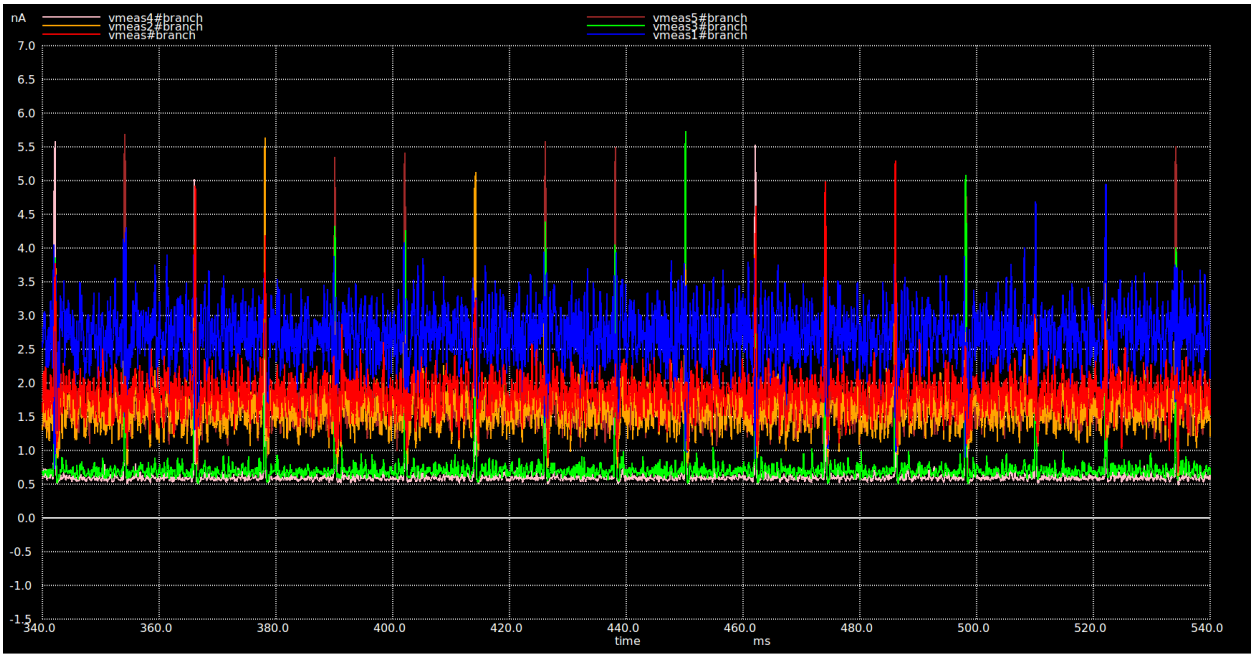


Fig:14 Bump Circuit output

This is the bump circuit output adding all the 4 electrode signals value for one of the teacher signals. As we can we are getting a peak when all the 4 electrode channel signals are matched which gives us the highest current. Since providing this much current is not advisable we will be using a square root circuit. The current is provided to the square root circuit through pFET current mirror, or you can directly take the current from the bump circuit.

Square root circuit:

To bring down the voltage, I am using a square root circuit at each corresponding teacher signal output. So, I will be using six square root circuits in my design.

Circuit diagram:

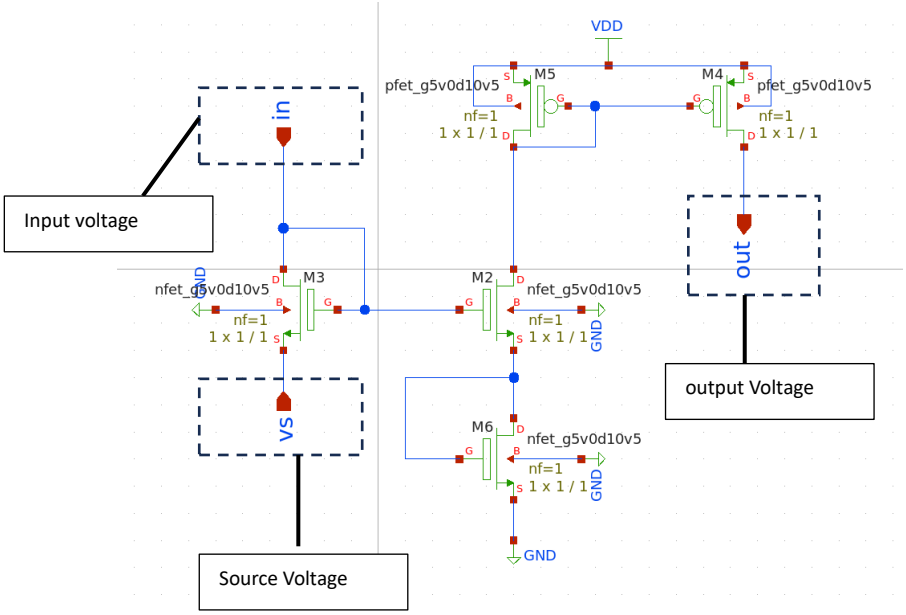
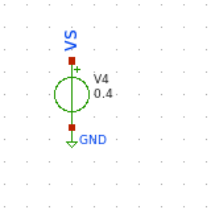


Fig:15 square root circuit

Inputs provided for the square root circuit:

Voltage Label	Value	Figure representation
vs	0.4v	Source Voltage
in	Input voltage from bump circuit	Input voltage
out	Output voltage to square root circuit	Output Voltage



Used Equations:

$$Iout = I_0^{\left(\frac{1}{I+k}\right)} I_0^{\left(\frac{k}{I+k}\right)} e^{v_s/v_T\left(\frac{k}{I+K}\right)}$$

I assumed k=0.7 $I_2 = I_0^{0.588} I_1^{0.411} e^{\frac{0.411 v_s}{v_T}}$. By providing these values I choose to bring the current values

Below is the sample output from the square root circuit.

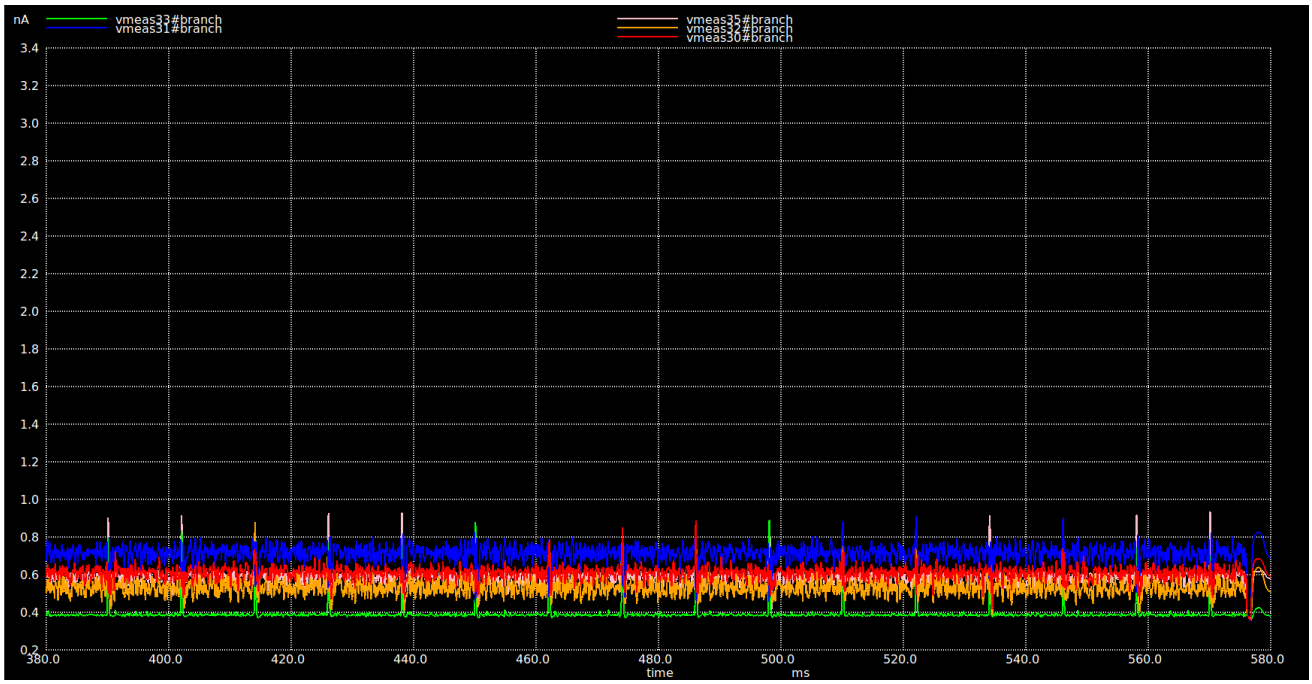


Fig:15 square root circuit

With the help root circuit, we could be able to compress the current values in the 0-1nA from 0.5-5.5nA. As a result of this we will not burden winner take all circuit

Transistor sizes used for square root circuit:

All the nFETs and pFETs are of the same size which is 1*1*1.

Winner Take All circuit:

Winner Take All circuit takes the 6 input signals from the square root circuit.

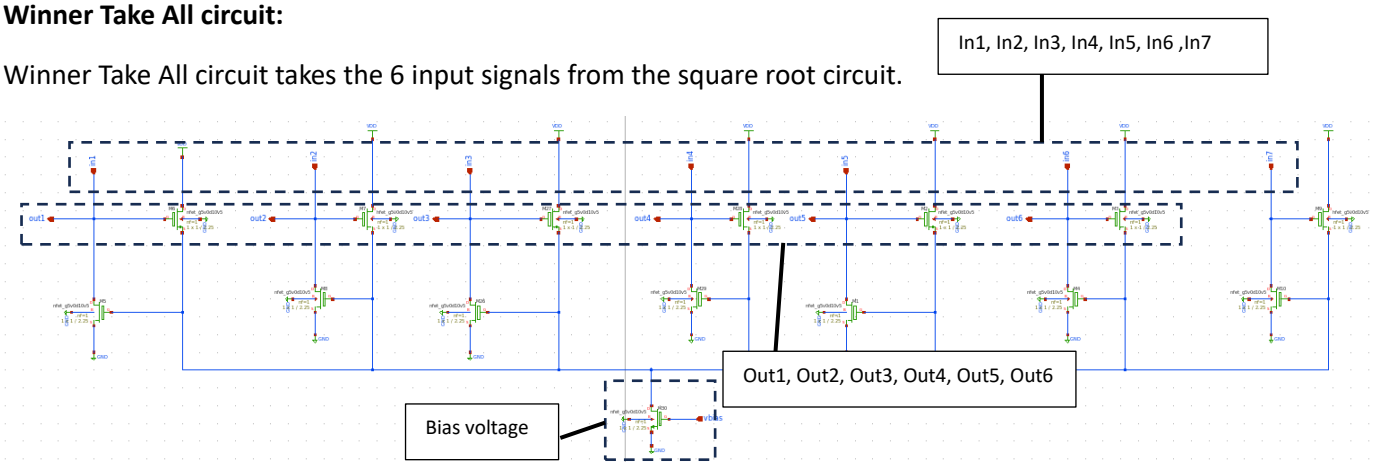


Fig:16 Winner Take all circuit diagram

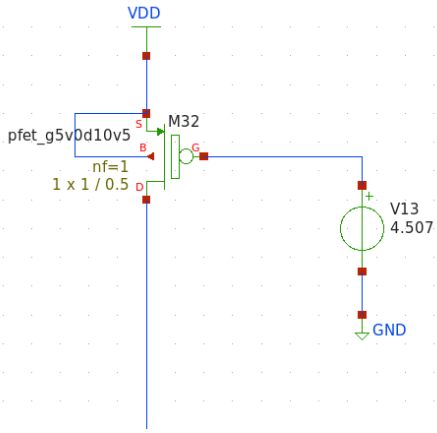
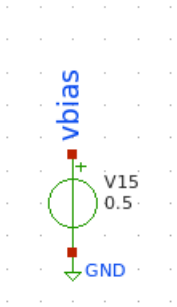


Fig:17 Constant current producing branch

Inputs/outputs for the winner take all circuits:

Voltage Label	Value	Figure representation
In1,In2,In3,In4,In5,In6	Inputs from the square root circuits each for each teacher signal	In1,In2,In3,In4,In5,In6
In7	Input voltage provided from a constant current source (here pFET with gate voltage 4.507)	In7
out1, out2, out3, out4, out5, out6	Output voltage provided to the threshold/hysteresis circuit	out1, out2,out3,out4,out5,out6
vbias	0.5	Bias voltage



We will be getting output from each one of the six output signals from the square root circuit and these output signals are provided as inputs for 6 branches and for the 7th branch we will provide a constant current source to suppress the current which is wining at all the time.

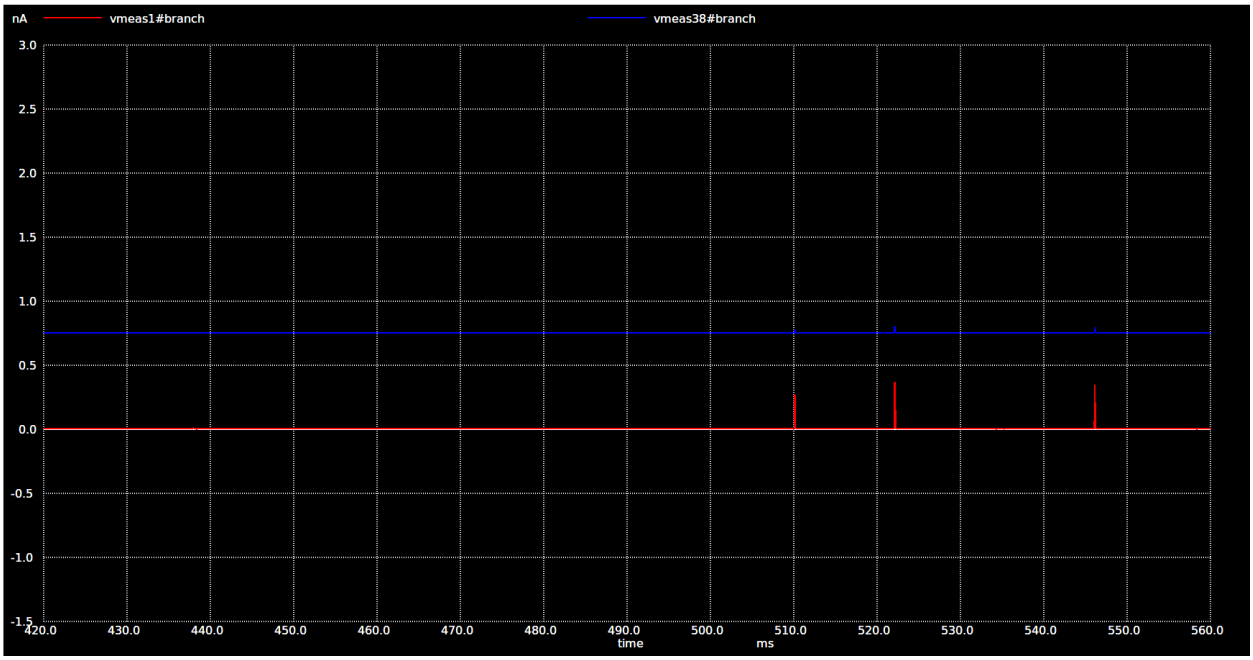


Fig:16 Suppressing the current which is wining every time

The current output from the teacher signal 2 is winning most of the time. So, we have compressed that by providing pFET gate voltage of 4.507 which provides constant noise current.

output taken from the node voltages from the corresponding branches.

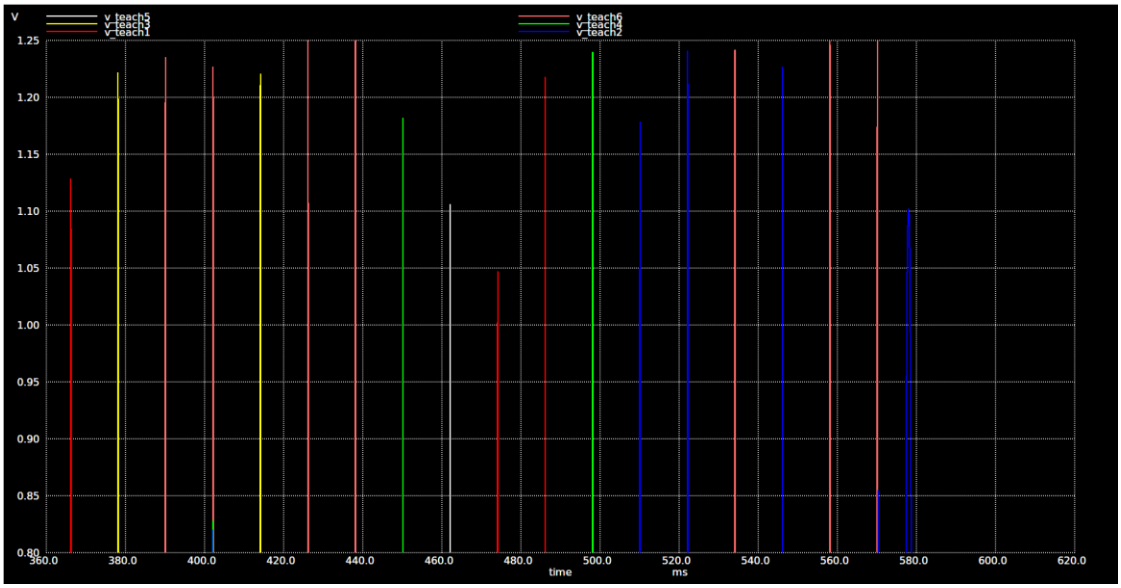


Fig:17 Winner Take all output zoomed in version from 360 to 580ms

Transistor sizes used for Winner take all circuit:

All the transistors which are nFETs are of the same size which are 1*1*2.25. For the seventh branch, we will provide a constant current source using pFET which is of size of 1*1*0.5. There is not very much to use the same size for pFET but we can use different sizes as well, accordingly we need to change the gate voltage.

Threshold/hysteresis circuit:

After obtaining six gate voltages (we will be ignoring the seventh branch as it is only used to suppress the current) from the corresponding bias current flowing branches of the winner take circuit. We will provide the output to threshold/hysteresis circuit which then produces the output which is greater than the certain threshold voltage fixed to that teacher signal.

Circuit diagram for the threshold/hysteresis circuit:

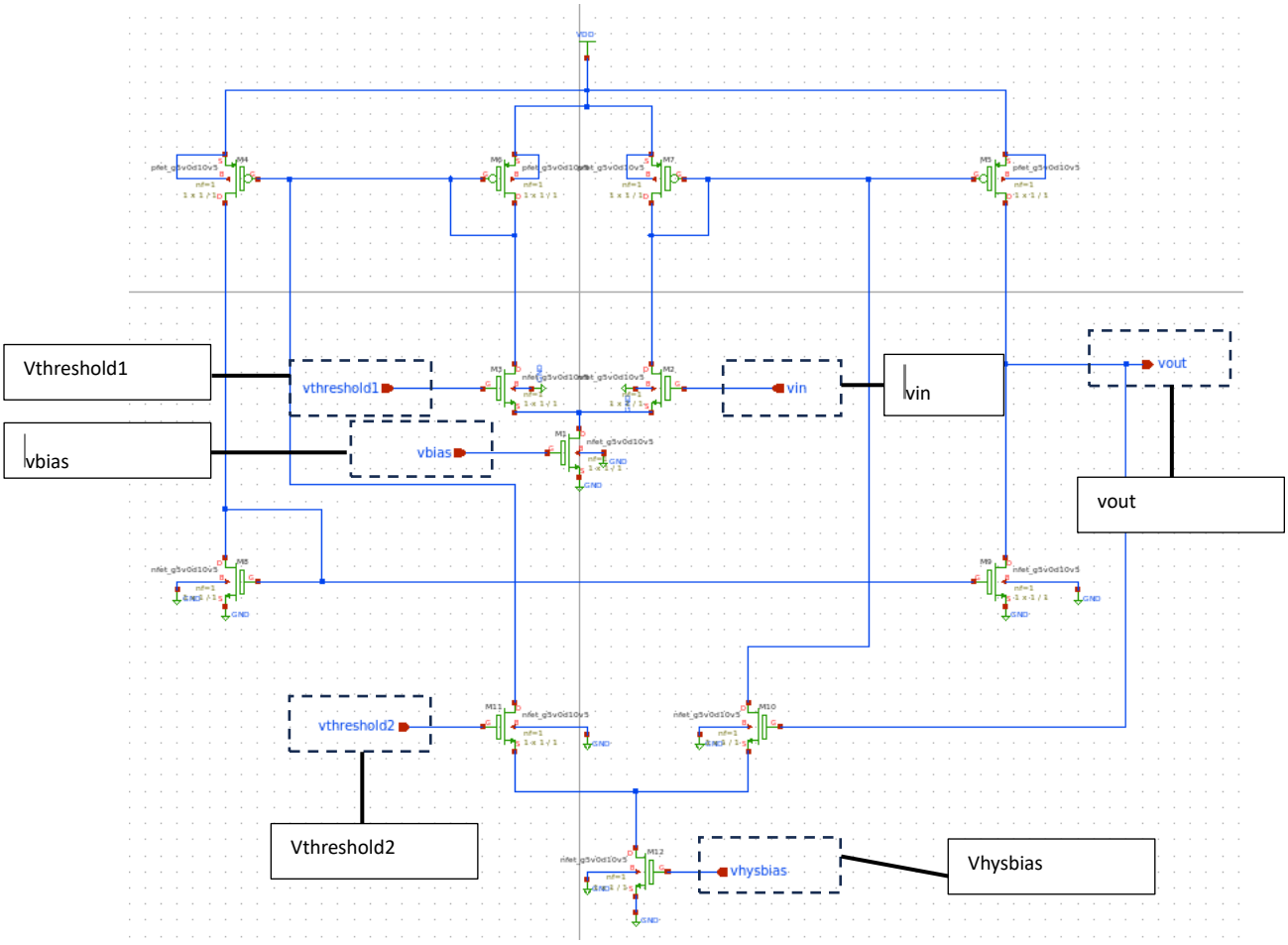


Fig:18 Hysteresis/Threshold circuit

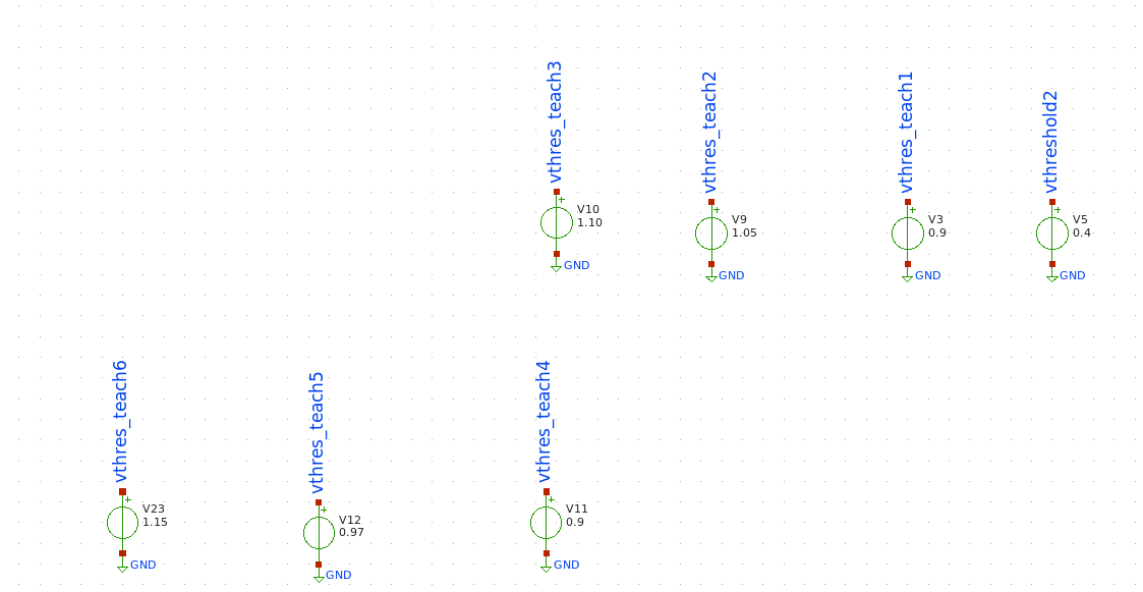
We will provide threshold voltages for each of the teacher signal output based on the branch voltages taken from the winner take all circuit. Vthreshold1 provides the maximum voltage threshold i.e.., when the input voltage reaches to that voltage, we will get the output voltage. V_threshold2 states the minimum voltage that the input voltage should reach to be pulled to zero.

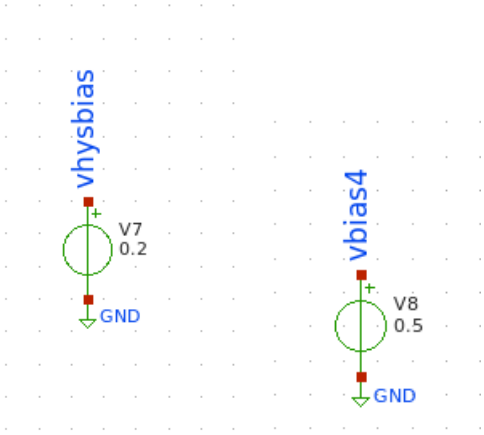
I have used six threshold voltage circuits for six teacher signals output each with different threshold voltage requirement for better comparison (We can also one threshold with exact filtering averaging, but I not guaranteed to know whether it works outside of the evaluation dataset. So, I used six different threshold voltages). Before that I used six buffers to place the voltage onto six threshold/hysteresis circuits.

Inputs/outputs for the threshold/hysteresis circuit:

Voltage Label	Value	Figure representation
V_threshold1	V_threshold1 for teacher1 signal=0.9(vthres_teach1), V_threshold1 for teacher2 signal=1.05(vthres_teach2),	Vthreshold1

	v_threshold1 for teacher3 signal=1.10(vthres_teach3),v_threshold1 for teacher4 signal(vthres_teach4) = 0.9,v_threshold1 for teacher5 signal=0.97(vthres_teach5), v_threshold1 for teacher6(vthres_teach6)=1.15	
V_threshold2	0.4	Vthreshold2
Vbias	0.5(vbias4)	Vbias
Vhysbias	0.2	Vhysbias
Vout	Output to pulse generation circuit	vout





Output signals from the threshold/hysteresis circuit:

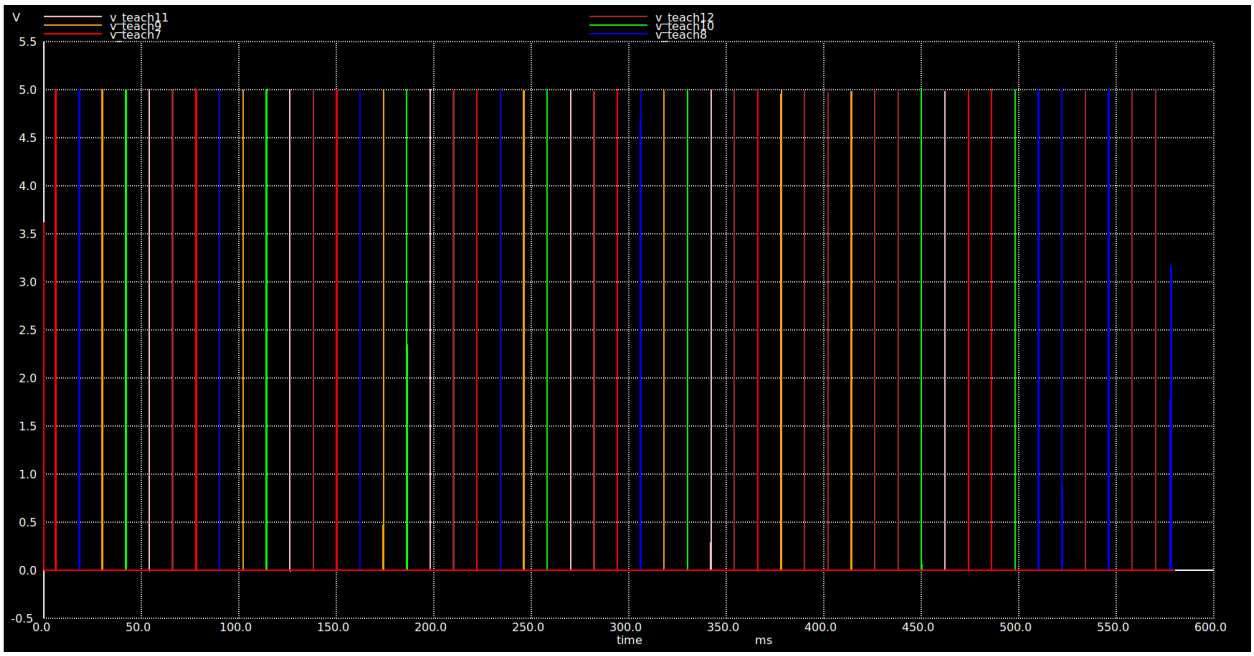


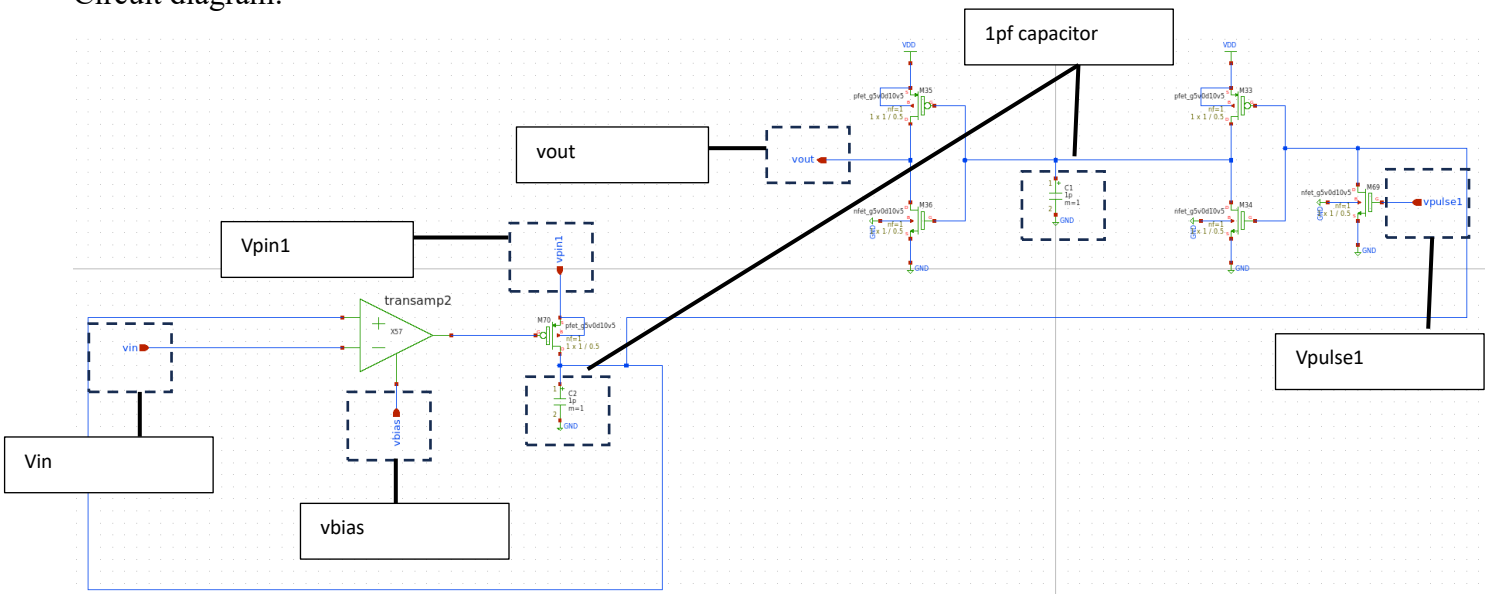
Fig:18 Spikes produced from threshold/hysteresis circuit.

Transistor sizes used for Hysteresis or threshold circuit:

All the nFETs and pFETs are of the same size which are 1*1*1.

Pulse generation circuit:

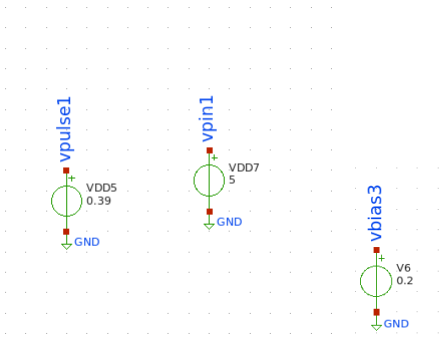
Circuit diagram:



Since the inputs are coming as spikes, I want to hold the spike value for a considerable amount of time. As a result, I have used a peak detector with supply voltage VDD and then after I need to set the vpulse1 value in such a way that how much time the pulse width must be. I thought of pulse width around 1.5ms to 2ms. Accordingly, I have chosen the vpulse1 value to 0.39. After that delay circuit to get the output pulse (adjusting capacitor value also changes the pulse width). We will use six of these circuits for each teacher signal output.

Inputs/outputs of pulse generation circuit:

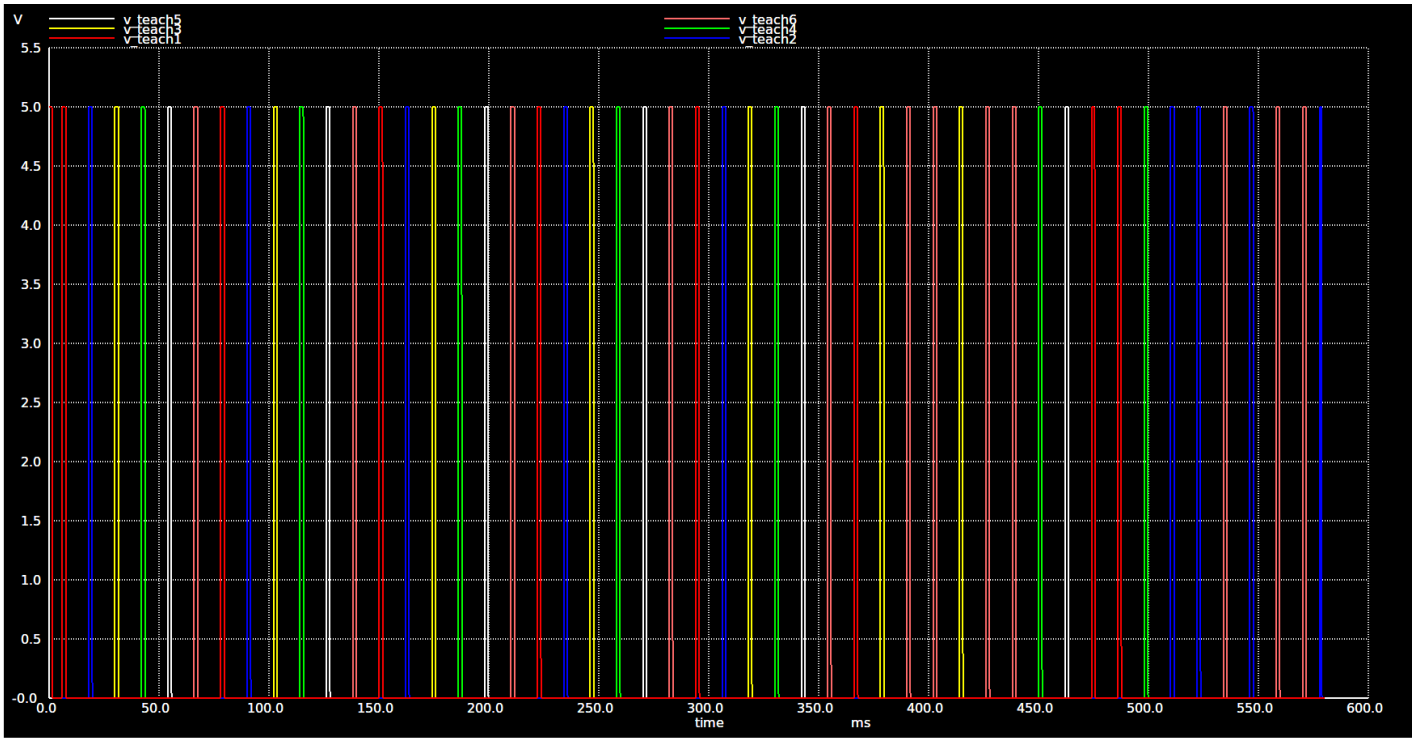
Voltage Label	Value	Figure representation
Vin	Input spike threshold/hysteresis circuit	Vin
vpin1	5	Vpin1
Vbias	0.3(vbias3)	Vbias
Vpulse1	0.39	Vpulse1
Vout	Teacher signal	vout



Transistor sizes used for pulse generation circuit:

All the nFETs and pFETs are of the same size which are 1*1*0.5.

Output from the pulse generation circuit:



Detected signals and timing:

366ms-368ms – teach1 signal

378ms-380ms – teach3 signal

390ms-392ms – teach6 signal

402ms-404ms – teach6 signal

414ms-416ms – teach3 signal

426ms-428ms – teach6 signal

438ms-440ms – teach6 signal

450ms-452ms – teach4 signal

462ms-464ms – teach5 signal

474ms-476ms – teach1 signal

486ms-488ms – teach1 signal

498ms-500ms – teach4 signal

510ms-512ms – teach2 signal

522ms-524ms – teach2 signal

534ms-536ms – teach6 signal

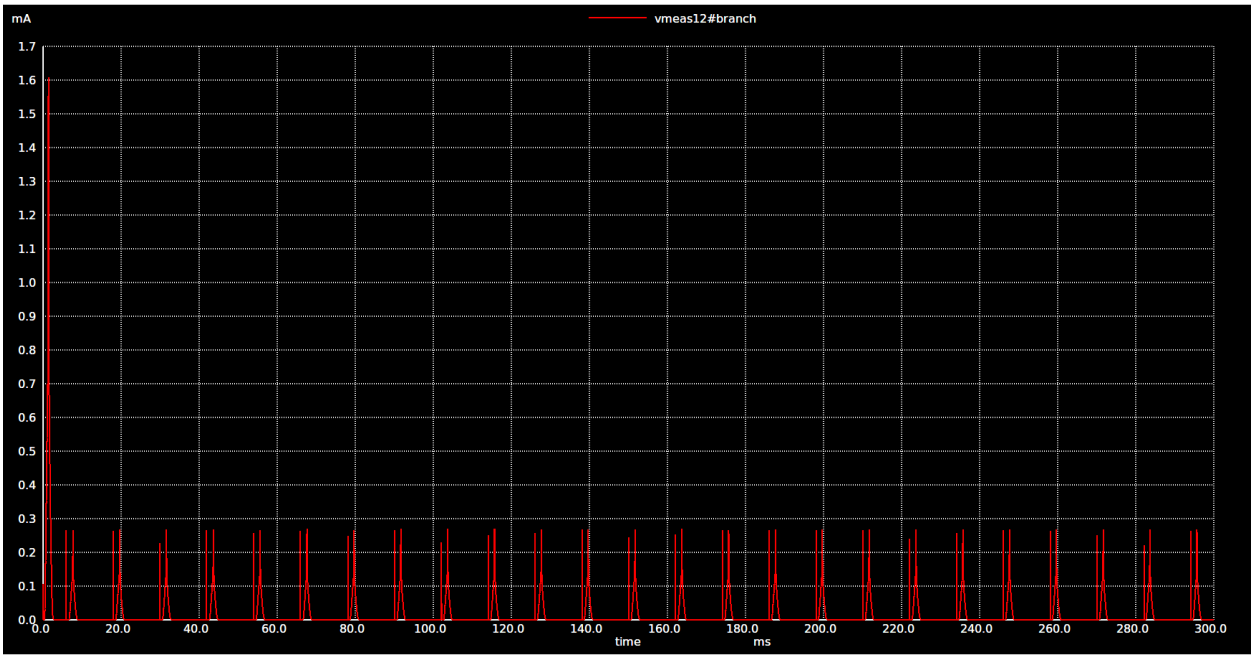
546ms-548ms – teach2 signal

558ms-560ms – teach6 signal

570ms-572ms – teach6 signal

577.5ms-580ms – teach2 signal

Plot of power supply current:



Total power: $1.366735*10^{-5} * VDD = 6.833*10^{-5}$ W

Total Transistor count:

Circuit	Number of transistors	Area
Bandpass filter	25	25 square microns
Peak holder memory circuit	47	56.75 square microns
Bump circuit	5	11.25 square microns
Current mirror	2	1 square microns
Square root circuit	5	5 square microns
Winner take all circuit	16(including constant current source branch)	34.25 square microns
Individual transamp to present voltage to peak hold circuit	9	9 square microns

Hysteresis and threshold circuit	12	12 square microns
Peak holder circuit	15	12 square microns

Total area: (Bandpass filter*4) +(peak holder memory circuit*24) +(Bump circuit*24)+(Current mirror*24)+(Square root circuit*6)+(Winner take all circuit*1)+(Individual transamp*6)+(Hysteresis and threshold circuit*6)+(Peak holder circuit*6) = 2018.25 square microns

Other approach Idea:

I have another approach of comparing with the peak value instead of analog value. In that case we need to use a peak detector for comparing with the stored value and discharge time will be output of the pulse. Due to time constraints, I am holding this design.