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Modeling of Busbars in High Power Neutral Point Clamped Three-Level Inverters

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Abstract: The busbars in high power neutral point clamped three-level inverters are modeled using the Maxwell Q3D Extractor software, which is based on the partial element equivalent circuits method. The equivalent circuits of the busbars and devices model are simulated in the electric simulator PSIM to analyze the effects of the parasitic inductance on the switching characteristics of the integrated gate commutated thyristor (IGCT) in different topology positions. The simulation results agree well with the measured impedance analyzer results and the IGCT test results, which proves the effectiveness of the modeling method for the large, complex busbars.

Key words: busbars; parasitic inductance; partial element equivalent circuits; switching characteristics

Introduction

In power electronic equipment, more and more interconnections use busbars, which reduces the wiring inductance compared to cables[1]. However, for high power NPC three level inverters, the long distances between components depending on the power rating and the heat transfer make the busbar inductances large. Semiconductor devices with high currents and voltages produce very high di/dt during commutations, so the busbar inductance may create overvoltages. As a result, the switching losses and electromagnetic interference increase inside the inverters[2,3].

The parasitic effects on the circuit operation must be analyzed to guarantee high reliability and good inverter performance. This can be accomplished by modeling the busbars[4]. Conventionally, electromagnetic field simulation tools[5], which employ the finite element analysis (FEA) to solve Maxwell's differential field equations, are used to obtain the parasitic parameters. However, when the busbar physical structures become more complex, the FEA method entails more extensive computations and sometimes shows poor convergence. The partial element equivalent circuits (PEEC) method[6], which uses Maxwell's integral equations instead of the differential equation, has been successfully used to model the interconnects of small, lower power converters[7,8]. In this paper, the PEEC technique is applied to large, high-power inverters. The Maxwell Q3D Extractor software based on the PEEC method is used to develop the equivalent busbar circuits in a 1250 kW/6 kV diode neutral point clamped (NPC) three-level inverter. The busbar model is combined with the models of the capacitors, resistors, integrated gate commutated thyristors (IGCTs)[9], and diodes in a PSIM simulator to analyze the effects of the wiring inductance on the turn-off switching characteristics of IGCTs in different positions. The simulation and experimental results are compared to validate the modeling method.

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1 High Power NPC Three-Level Inverter

Figure 1 shows the schematic diagram of the inverter. This inverter is equipped with 4.5 kV/630 A reverse conducting IGCTs (5SHX08F4502)[10] and fast recovery diodes (5SDF03D4502)[11]. The snubber inductors (L_{i1} and L_{i2}) are used to limit the turn on di/dt of the IGCTs. The snubber diodes (D_{CL1} and D_{CL2}), the resistances (R_{CL1} and R_{CL2}), and capacitors (C_{CL1} and C_{CL2}) are used to clamp the maximum turn off voltages of the IGCTs and diodes.

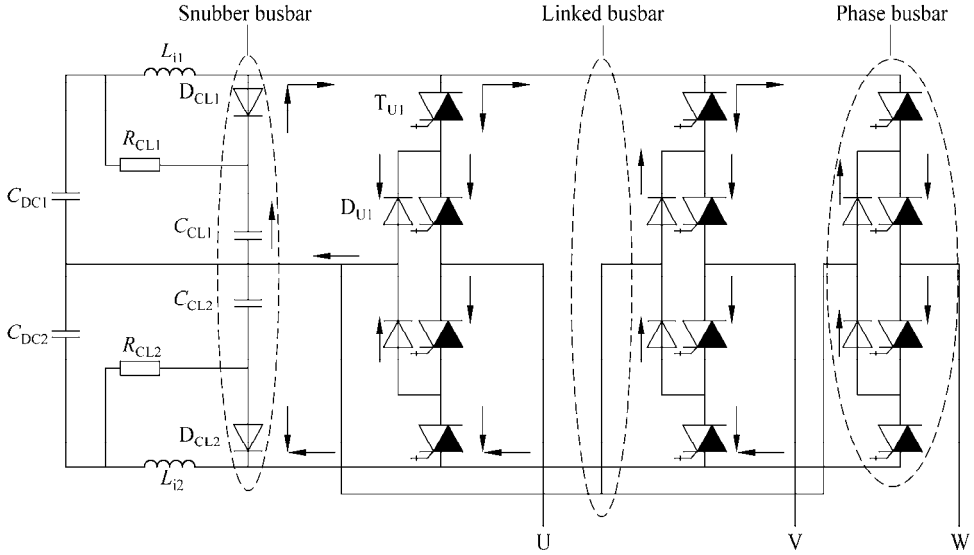


Fig. 1 Inverter circuit topology

Due to several industrial considerations, such as maintenance and cooling, the semiconductor devices and air heat sinks are pressed together in one stack. The entire structure of the busbars must comply with the constraints of this press-pack mechanical structure. Besides the heat transfer, the heat sinks also act as conductors and become a part of the busbars. Three types of busbars are shown in Fig. 1. The snubber circuit busbars connect the snubber capacitors and the snubber diodes. The role of the phase busbars is to associate the four IGCTs and two diodes for the neutral point clamping in phase. The linked busbars are employed for the interconnections among phase bridges and snubber circuits. Table 1 lists the components used in the inverter. ESL and ESR are the equivalent series inductance and resistance.

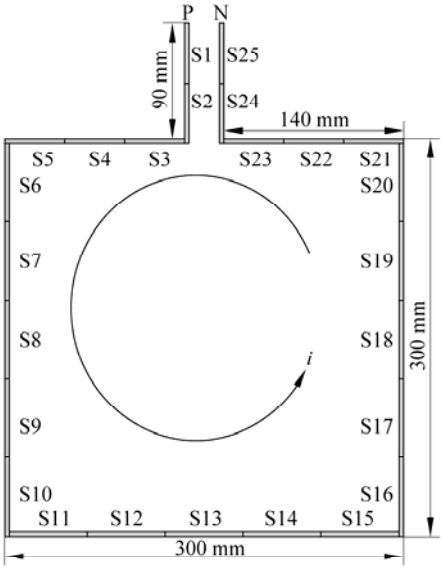
Table 1 Inverter components

Component	Values
L_i/μH	10.7
R_{CL}/Ω	1.2
C_{CL}/μF	2
C_{DC}/μF	2300
ESL of R_{CL} (μH)	2
ESL of C_{CL} (nH)	67
ESR of C_{CL} (mΩ)	3
ESL of C_{DC} (μH)	3
ESR of C_{DC} (mΩ)	9
Copper busbars (width/thickness) (mm)	40/2
Small heat sinks (length/width/ thickness) (mm)	149/160/64
Large heat sinks (length/width/ thickness) (mm)	149/160/99

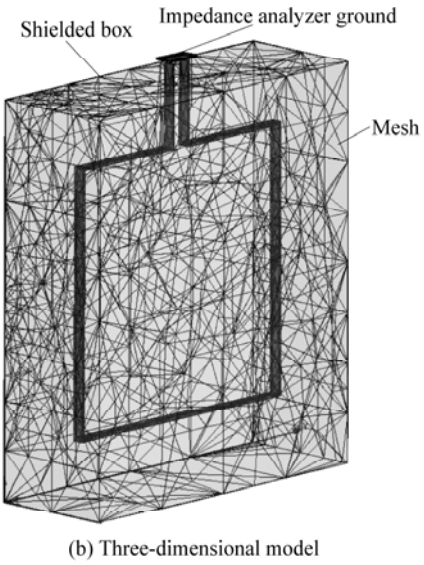
2 Model Development

2.1 Parasitic parameter extraction and validation

The impedance measurements for the busbars are quite difficult because of the complexity, size, and decentralization of the busbar. Thus, the busbar geometry was simplified to a simple rectangular cross-section (12.5 mm ×3.0 mm) copper busbar as shown in Fig. 2a to prove the feasibility of the PEEC method.



(a) Physical model



(b) Three-dimensional model

Fig. 2 Rectangular cross-section busbar

The parasitic parameters have been measured using time domain reflectometry (TDR) based measurements[12] and impedance analyzer measurements[13]. The TDR method requires complicated experimental measurements, special hardware (TDR/sampling head) and software. The impedance measurement is more straightforward and simpler; therefore, an impedance analyzer (HP4395A) was used in these tests. The measurement impedance curve across ports P and N from 100 kHz to 180 MHz is shown in Fig. 3. The first resonance point occurs at about 50 MHz, which is chosen as the highest frequency (f_c) for the modeling.

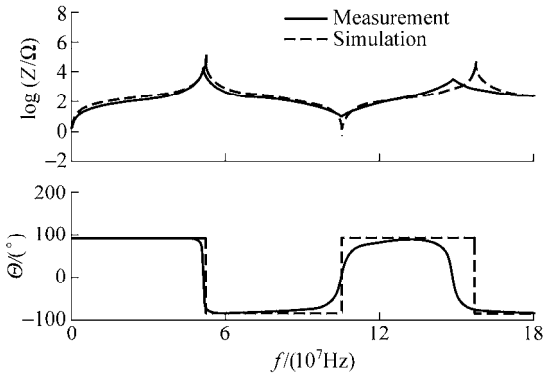


Fig. 3 Test busbar impedance curves

The PEEC method requires only the geometric and material information. The modeling process using Maxwell Q3D Extractor includes four basic steps.

Step 1 Drawing the model geometry and assigning material characteristics.

To ensure equal voltages at all points on the bus, the maximum point-to-point distance d in the busbar model is defined as in Ref. [4]

$$d < 0.01\lambda \tag{1}$$

where $\lambda = c/f_c$ is the corresponding electromagnetic wavelength of f_c. The longest length in the busbar should then be less than 60 mm and the busbar should be divided into 25 segments (S1-S25) as shown in Fig. 2a.

Step 2 Identify nets to determine the segments needed to calculate the parameters.

The source and sink terminals are assigned to the nets according to the direction of the current through the busbar. An independent current source is attached to each pair of terminals for the electromagnetic field analysis. Current enters the source terminal and leaves the sink terminal. The shielded box and the impedance analyzer ground are treated as ground nets.

Step 3 Divide the structure into finite elements as illustrated in Fig. 2b.

To include the skin and proximity effects, a nonuniform current distribution is realized by creating a series of layers and gradings based on the skin depth. The skin depth, δ, is calculated based on the permeability, μ, and the conductivity, σ, of the materials and the frequency.

$$\delta = \frac{1}{\sqrt{\pi f_c \mu \sigma}} \tag{2}$$

Step 4 Solve the resistance, inductance, and capacitance (RLC) matrix of the busbars.

Q3D Extractor computes the full electromagnetic field pattern using the specified mesh and the electrical parameters from the computed field quantities. The parasitic inductance and capacitance results of segments S1 to S6 are shown in Table 2 and Table 3. The diagonal elements in Table 2 are the self-inductance, while the non-diagonal elements are the mutual inductance between segments. The diagonal elements in Table 3 are the capacitances-to-ground, while the non-diagonal elements are the capacitances between segments.

Table 2 Busbar inductance matrix (nH)

Segment	S1	S2	S3	S4	S5	S6
S1	19.43	7.51	0.35	0.25	0.22	2.01
S2	7.51	20.59	0.92	0.33	0.26	2.33
S3	0.35	0.92	20.92	7.86	3.98	1.56
S4	0.25	0.33	7.86	20.72	7.6	1.41
S5	0.22	0.26	3.98	7.6	20.79	1.65
S6	2.01	2.33	1.56	1.41	1.65	31.07

Table 3 Busbar capacitance matrix (pF)

Segment	S1	S2	S3	S4	S5	S6
S1	1.38	33.60	0.03	0.00	0.00	0.00
S2	33.60	0.57	0.86	0.03	0.00	0.01
S3	0.03	0.86	0.65	33.63	0.02	0.02
S4	0.00	0.03	33.63	0.77	33.62	0.06
S5	0.00	0.00	0.02	33.62	0.73	0.83
S6	0.00	0.01	0.02	0.06	0.83	0.79

To obtain the simulated impedance curve, the entire RLC matrix is imported into the electric simulator PSpice to create an equivalent circuit for the busbar. Each inductance or resistance matrix entry is divided into two series inductors or resistors and placed in the circuit to create a balanced circuit as shown in Fig. 4.

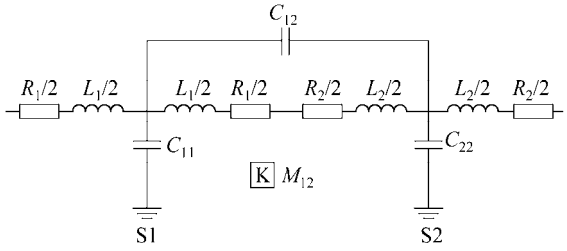


Fig. 4 Balanced equivalent circuit

The simulated impedance curve shown in Fig. 3 agrees well with the measurement results for both magnitude and phase. Therefore the PEEC method can effectively model the large busbar.

2.2 Modeling of the busbars in NPC three-level inverter

The inverter structure is not only large but also quite complicated, which makes the three-dimensional (3-D) geometric description rather difficult. For simplicity, the impact of the surrounding cables, the screws in the copper busbars, and the holes in the heat sinks are neglected in the model.

For the inverter, the highest critical frequency is associated with the turn-off current fall time (t_f) of the semiconductor device. The IGCT fall time is about 300 ns, resulting in a maximum frequency of

$$f_c = \frac{1}{2\pi t_f} = 530 \text{ kHz} \quad (2)$$

Thus, the maximum length in the busbar model is 500 mm. In addition, the busbars, which are located in different circuit positions or have geometric discontinuities, are individually modeled as segments with a total of 50 segments. The 3-D modeling result for the inverter busbars is shown in Fig. 5.

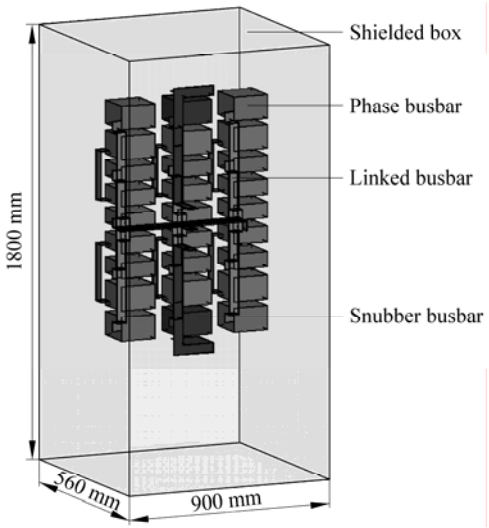


Fig. 5 Busbars geometric model

The shielded box is modeled as the ground nets. The source and sink terminals of each segment are defined according to the current shown in Fig. 1. The parameter matrices were exported after performing the mesh operations and parametric analysis. Table 4 lists the inductance results for the snubber circuit busbars.

Table 4 Important parasitic self-inductances (nH)

Segment	L_{S1}	L_{S2}	L_{S3}	L_{S4}	L_{S5}	L_{S6}
L_{S1}	24.13	−14.45	−8.76	−2.57	−1.70	0.78
L_{S2}	−14.45	99.91	24.29	7.26	3.95	−1.82
L_{S3}	−8.76	24.29	158.79	9.03	6.84	−2.92
L_{S4}	−2.57	7.26	9.03	159.00	22.41	−6.83
L_{S5}	−1.70	3.95	6.84	22.41	87.61	−7.63
L_{S6}	0.78	−1.82	−2.92	−6.83	−7.63	6.54

An equivalent circuit of busbars was then obtained based on the parasitic parameters. Because of the geometric symmetry, only the equivalent circuits for phases U and V are shown in Fig. 6. Only the inductances are included for clarity.

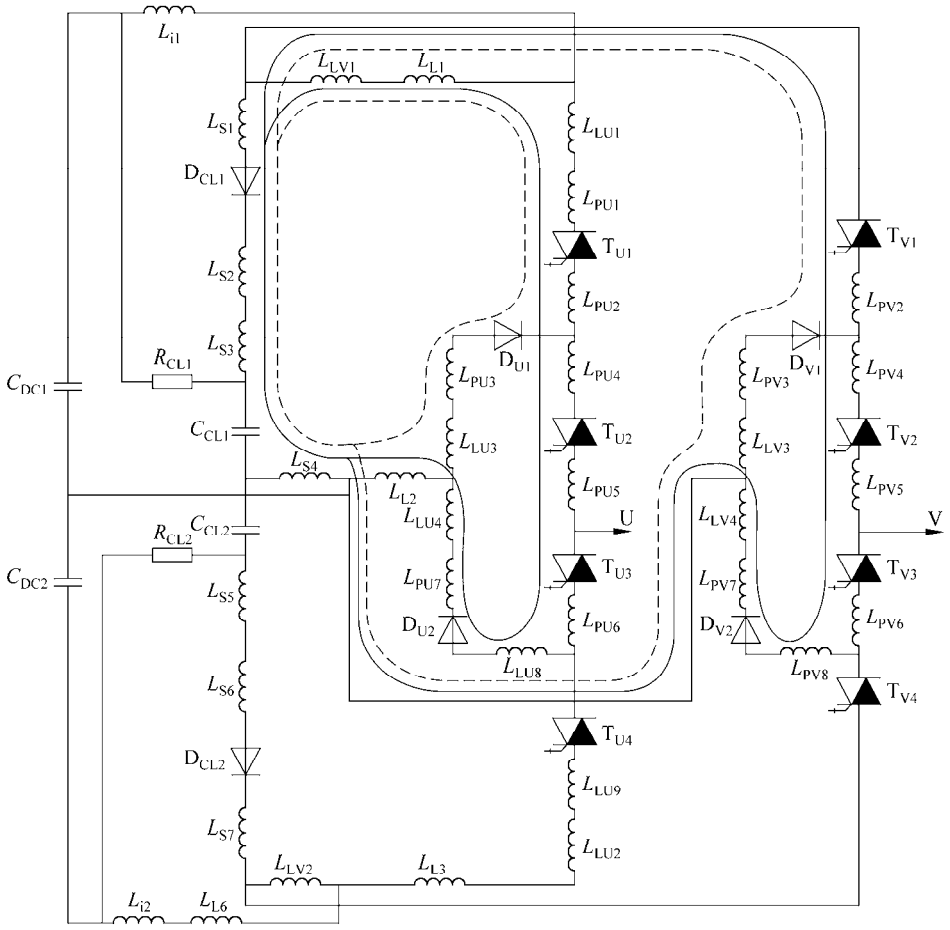


Fig. 6 Equivalent electrical circuit of the busbars

3 Simulation and Experiment

The equivalent circuit of the busbars is introduced into PSIM with the models of the other devices for the simulation. The IGCT and diode models are functional models, which treat the devices as a "black box" to describe the externally observed behavior without detailed consideration of the physical effects inside the device[14]. The capacitor models are simply equivalent circuits incorporating the ESL and ESR.

A buck type circuit (Fig. 7), the basic commutation cell in the inverter, is usually used to analyze the IGCT switching characteristics. Four typical commutation cells (dashed and solid line in Fig. 6) for T_{U1}, T_{U3}, T_{V1},

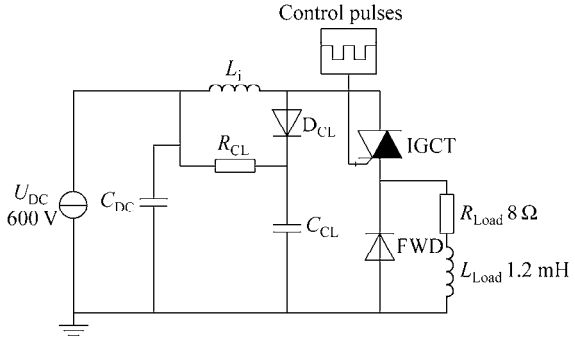


Fig. 7 IGCT test circuit

and T_{V3} were used in this simulation. For safe operation of the test system, the DC link voltage and the load current were reduced. The switching frequency was 2 kHz, the duty ratio was 75%, and the number of control pulses was 80.

The control board for the test platform was based on a DSP (TMS320LF2407A), which is used to output the optical control pulses to the IGCT. The experimental waveforms were recorded on an oscillograph (YOKOGAWA DL750). The simulation and experimental voltage waveforms across IGCTs (U_{TU1}, U_{TU3}, U_{TV1}, and U_{TV3}) are shown in Fig. 8. The first peak voltage (U_{DSP}) across the IGCT is one of the most important performance factors for the turn-off transient process, which is mainly influenced by the parasitic inductance in the busbars. Figure 8 shows that the simulated values of U_{DSP} agree well with the measured values, thus the busbar modeling method presented in this paper can effectively model the parasitic effects.

The curves of the first voltage peak values versus the load current are shown in Fig. 9. The turn-off characteristics of the inner IGCTs are worse than those of the outer IGCTs in one phase. Moreover, the IGCTs in the same topology positions for different phases have

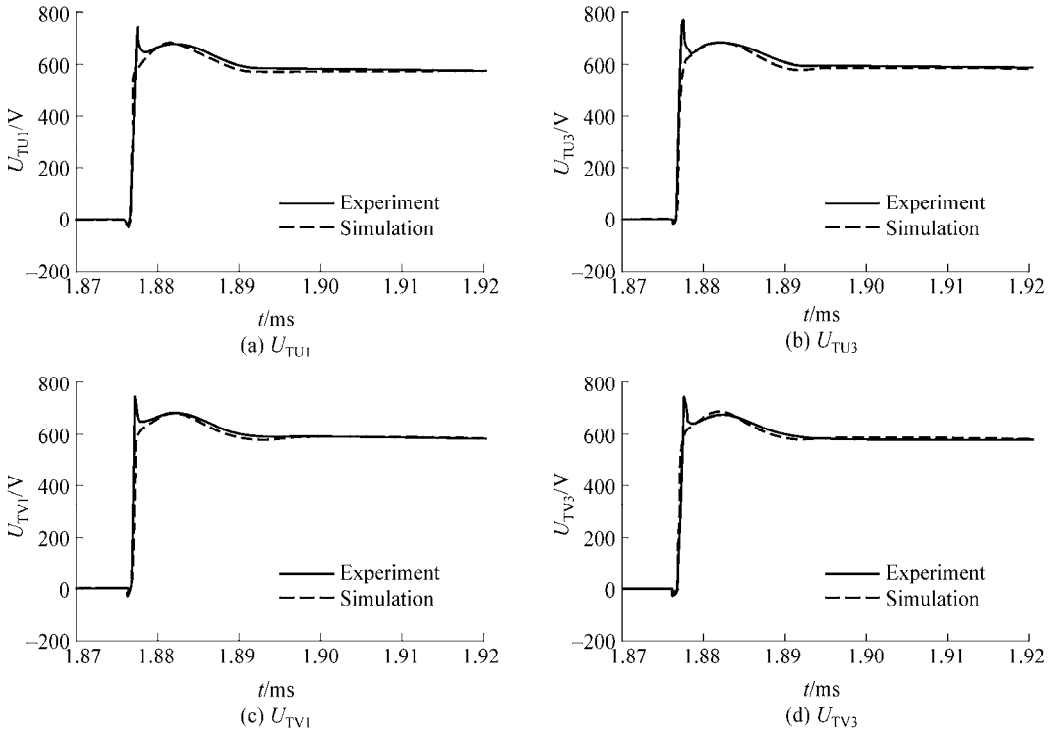


Fig. 8 Turn-off voltage waveforms across the IGCTs

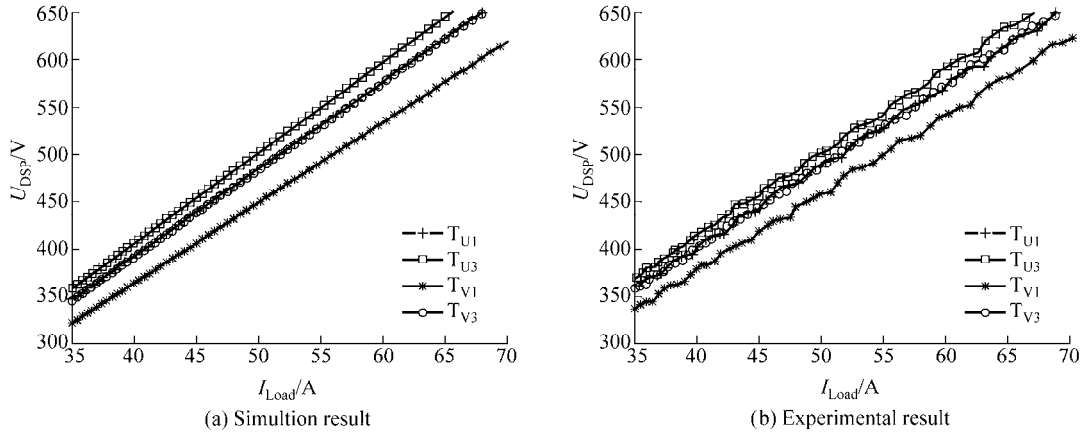


Fig. 9 First peak voltage curves

different turn-off characteristics. The IGCTs in phase V have better dynamic behavior than those in phase U because the snubber diode is directly connected to the T_{V1} by the heat sink.

4 Conclusions

Parasitic inductances can result in significant increases of the voltage stresses in semiconductor devices and EMI problems. In this paper, the PEEC method has been used for parameter extraction for the large busbars with complicated structures. The simulations, which included the parasitic parameters of the busbars, is a practical method to predict the turn-off over voltage and to investigate the switching characteristics of IGCTs in different positions. These results can be used to ensure that semiconductor devices work in their safe operating areas and to provide guidelines for the optimization of inverter designs.

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