Dayananda Sagar College of Engineering

Department of Electronics and Communication Engineering

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(An Autonomous Institute affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)

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AAT

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A Report on

"Voltage Controlled Oscillator (VCO) using CMOS design"

TOPIC

Submitted by

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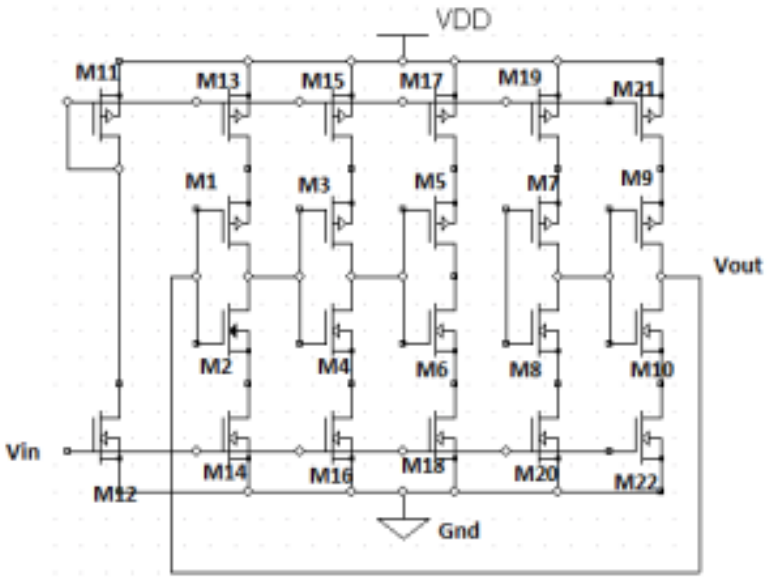
1. INTRODUCTION

- CMOS is also sometimes referred to as complementary symmetry metal oxide semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistor (MOSFETs) for logic functions. A voltage controlled oscillator or VCO is an electronic oscillator designed for producing oscillation frequency by a controlled input voltage. The frequency of oscillation is varied by the applied controlled voltage. A voltage controlled oscillator or VCO is an electronic oscillator designed for producing oscillation frequency by a controlled input voltage. The frequency of oscillation is varied by the applied controlled voltage. A VCO plays a vital role in communication system, providing a periodic signal required for digital circuit and also a frequency transmission in digital circuit. Their output frequency is a function of control input voltage. An ideal VCO is a circuit whose output frequency is a linear function of its control voltage. Most of the application as required a variable control input voltage as they required different frequency.
- The voltage-controlled oscillator (VCO) plays a very important role in communication systems due to low power consumption, wide frequency range of operation and its high integration capability. It is an electronic device that uses amplification, feedback, and a resonant circuit to generate a repeating voltage waveform at a particular frequency. The frequency, or rate of repetition per unit time, is variable with an applied voltage. VCOs are important integral part of phase locked loops, clock recovery circuits, frequency synthesizers and in almost all digital and analog systems.
- Phase locked loops (PLLs) are common applications for VCOs based frequency synthesizer is usually used in RF transceivers. PLLs can be used for clock generations, such as in a microprocessor, clock and Data recovery, such as in an optical transmission system, or frequency synthesis, such as in a wireless radio. The general characteristic for VCOs used in PLL is wide tuning range so that the entire frequency range is covered. Also,
- the phase noise requirement of the VCO can be loosened due to that when the loop is locked, the noise generated by the VCO at the center of oscillation frequency will be filtered out by the loop bandwidth. As a result, PLLs generally use wide tuning range and noisier ring topology VCO.

2. CIRCUIT DIAGRAM



circuit diagram of VCO.

- Working principle:

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Figure 7, it is observed that MOSFETs M1 and M2 operate as an inverter, while MOSFETs M13 and M14 operate as current sources. The current sources, M13 and M14, limit the current available to the inverter M1 and M2. In other words, the inverter is starved for the current. The MOSFETs M11 and M12 drain currents are the same and are set by input control voltage. The currents in M11 and M12 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M11 and source voltage is applied to the gates of all low NMOS Transistors. The bias circuit is used to provide correct polarization for transistor M13 and M14. The benefit of this configuration is that the oscillation frequency can be tuned for a wide range by changing the value of control voltage.

3. RESULT ANALYSIS

- Software tool used: **Cadence virtuoso**

  Cadence Virtuoso is a comprehensive **Electronic Design Automation (EDA)** tool suite used for the design, simulation, verification, and layout of integrated circuits (ICs), particularly **analog**, **RF (radio frequency)**, and **mixed-signal** ICs. Virtuoso is one of the leading tools used in the semiconductor industry for designing custom ICs and is especially well-suited for designing and simulating **analog circuits** and **custom layouts**.

  - Procedure:

Creating a **VCO (Voltage-Controlled Oscillator)** schematic in **Cadence Virtuoso** for a **180nm technology node** involves several steps, including designing the circuit, selecting the appropriate components, performing simulations, and verifying the layout. Below is a step-by-step guide on how to create a VCO schematic in Cadence Virtuoso.

Step-by-Step Procedure to Create a VCO Schematic in Cadence Virtuoso (180nm):

1. Set Up Cadence Virtuoso Environment

Before you start designing, make sure the Cadence Virtuoso environment is set up correctly.

1. **Launch Cadence Virtuoso**:
   a. Open **Cadence Virtuoso** by running the **Virtuoso Layout Editor** or **Virtuoso Schematic Editor**.
   b. Set up your design environment using the **Library Manager**.
2. **Create a New Library**:
   a. Open the **Library Manager** and create a new library for your VCO design.
   b. You will need to associate your library with the **180nm process technology**. This is typically done by specifying the **Technology File** or **PDK (Process Design Kit)** provided by your foundry (e.g., TSMC, UMC).
3. **Create a New Cell View**:
   a. In the Library Manager, create a new **cell** under your library (e.g., VCO).
   b. Choose **Schematic** as the cell type and click **OK**.

2. Design the VCO Schematic

Now, let's start designing the VCO circuit. We'll design a simple **CMOS VCO** as an example, which is a common architecture for voltage-controlled oscillators in analog IC design.

1. **Open the Schematic Editor**:
   a. Open the schematic editor by selecting your newly created cell (e.g., VCO).
   b. Click **Create** > **Instance** to add components to your schematic.
2. **Select Components for the VCO Design**: You can design a simple **CMOS VCO** using the following components:
   a. **MOSFETs** (n-channel and p-channel) for the oscillator core.

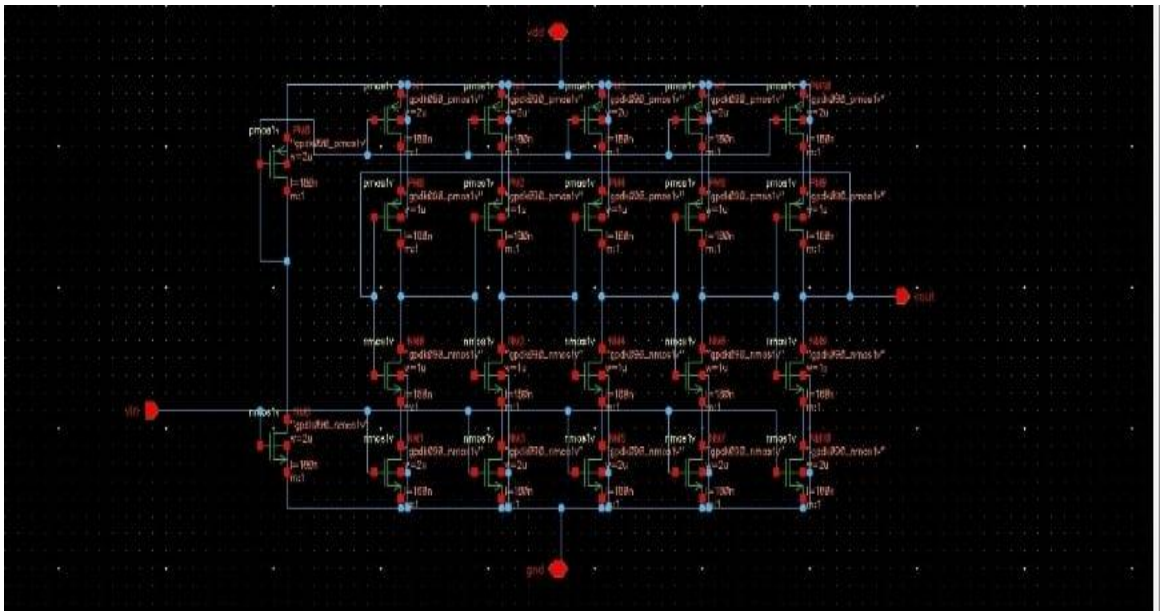
b. **Resistors** and **capacitors** for the tank circuit.
c. **Voltage source** (V_control) to control the oscillation frequency.
d. **Biasing components** (e.g., resistors, current sources) to set the operating points of the transistors.

To add these components:

e. Click **Create** > **Instance**.
f. Search for the components you need in the **Library** (e.g., `nmos`, `pmos`, `resistor`, `capacitor`).
g. Place the components on the schematic sheet.
h. For an **RC VCO**: You would replace the inductor with a **resistor** to determine the frequency.

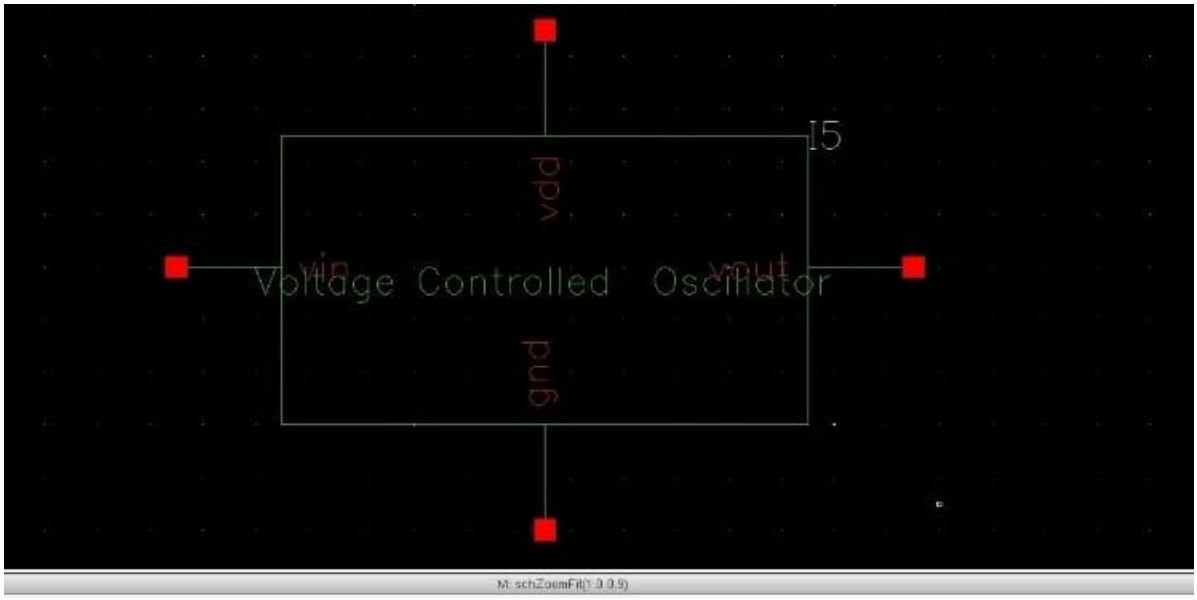
3. **Connect the MOSFETs in a Negative Feedback Loop**:
   a. Use **nMOS** and **pMOS** transistors to create the **oscillator core**.
   b. Connect the drain of the **nMOS** transistor to the capacitor and the positive feedback loop to the **gate** of the **pMOS** transistor.
4. **Add Control Voltage**:
   a. The control voltage (V_control) is connected to the **gate** of one of the MOSFETs (typically the **nMOS** transistor). This will control the frequency of the VCO by adjusting the gate voltage and thus the operating point of the transistors.
5. **Output Node**:
   a. The output of the VCO can be taken from the drain of the **nMOS** transistor or the **pMOS** transistor.
   b. You can add an output buffer (e.g., a **CMOS inverter**) to ensure the signal is clean and stable.

- Schematic:

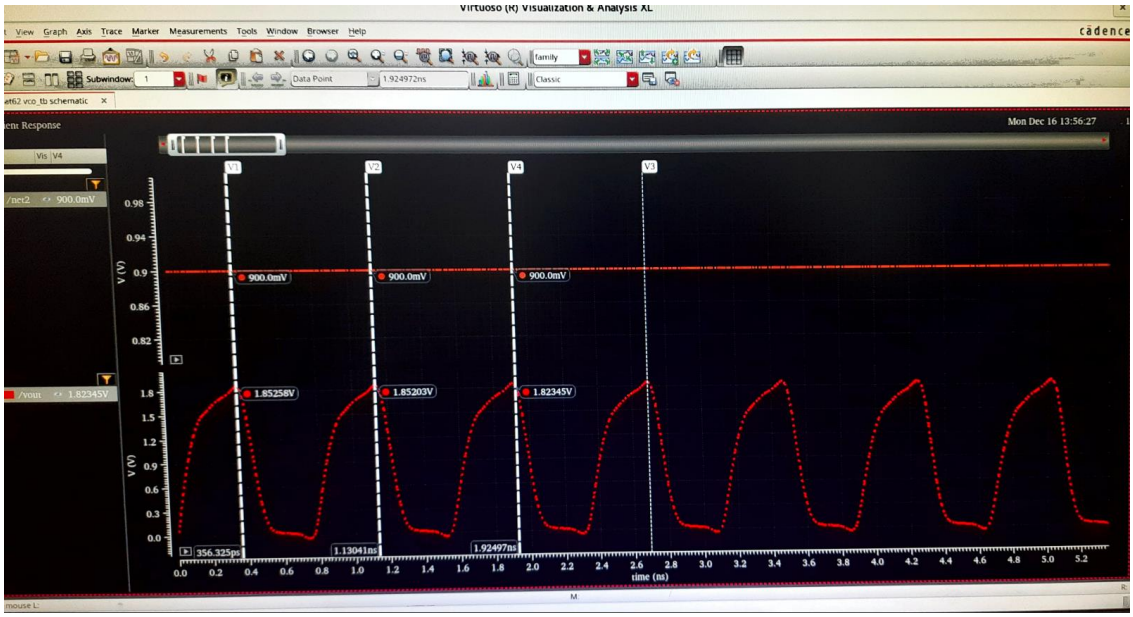


schematic of VCO in cadence virtuoso

Symbol creation of the schematic:



- Outputs/Results
  1. For vin=0.9v.



t = t2-t1

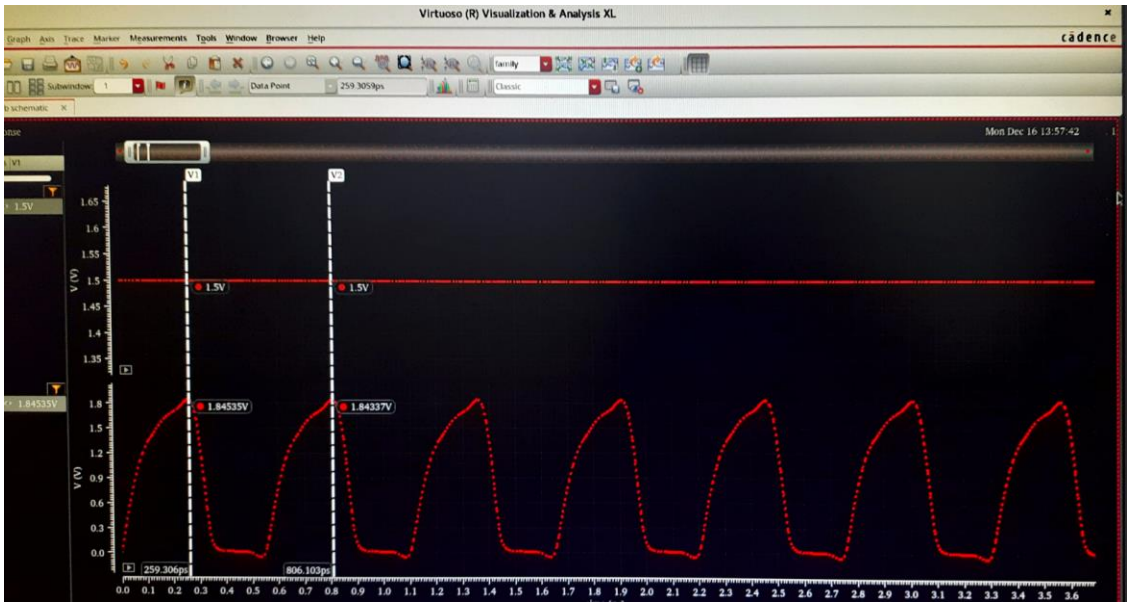
= (1.13041n-356.525p)s

F=1/(t)

F=1/7.74e-10

F=1.29G Hz.

2. For vin=1.5v



t = t2-t1

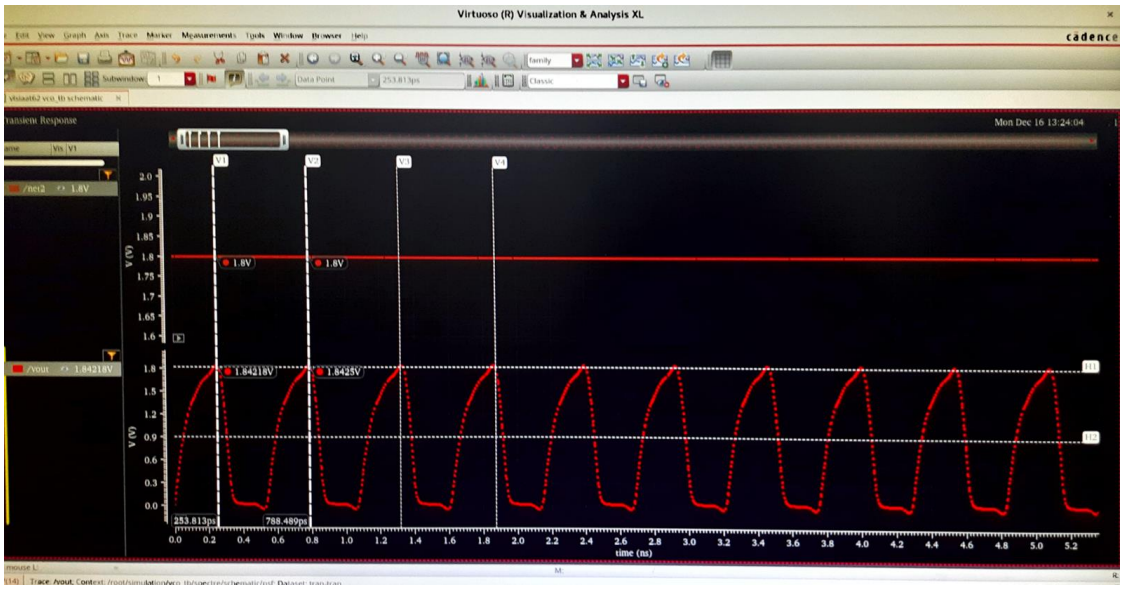
= (806.103p-259.306p)s

F=1/t

=1/ 546.797e-12

=1.82G Hz

3. For vin=1.8v



t = t2-t1

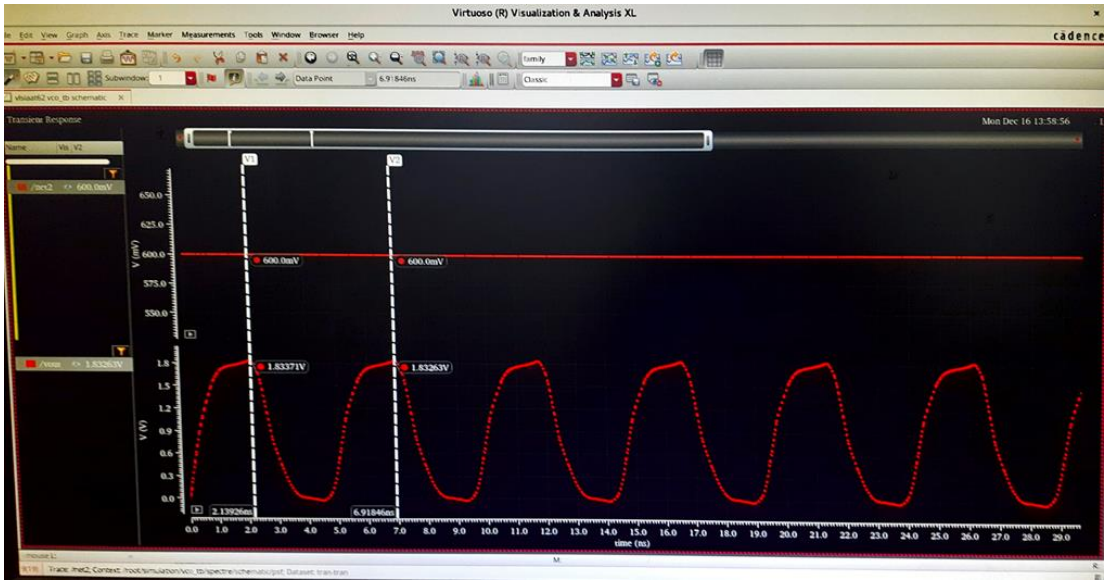
= (788.49p-253.813p)s

F=1/t

=1/534.677e-12

=1.87G Hz.

4. For vin=0.6v



t = t2-t1

= (6.91846n-2.1392n)s

F=1/t

=1/(4.7796e-9)

=209M Hz

Similarly for different voltages we get different frequencies.

From this we can conclude thar with increase in voltages, increases the frequency.

Sl. No.	Voltages	Frequency
1.	600mV	209M Hz
2.	900mV	1.29G Hz
3.	1.5V	1.82G Hz
4.	1.8V	1.87G Hz

4. REFERENCES

[1] Zainabkazemi, SajjadShalikar, A.M.buhari, Seyed Abbas MousaviMaleki ,"Design of Current Starved Ring Oscillator for Phase Locked Loop",International Journal of Electrical, Electronics and Data Communication, ISSN:

2320-2084 Vol-3, Issue-1, Jan.-2015.

[2] AtulKhode, AbhaGaikwad-Patil, Prof. Shubhangi Dhengre, Abha Gaikwad-Patil, "Current Starved VCO

Verses Source Coupled VC International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 7, Jul- 2015.

[3] Varun J. Patel,MehulL.Patel, "Low Power Wide Frequency Range Current Starved CMOS VCO in 180nm,

130nm and 90nm CMOS Technology", International Journal of Engineering Research and Development e-

ISSN: 2278-067X, p-ISSN: 2278-800X, www.ijerd.com Vol 7, Issue 4,May- 2013.

[4] Deepika, R.C. Gurjar, "Low Phase Noise, Current Starved Ring VCO with Wide Tuning Range and Improved

Linearity", International Journal of Innovative Research in Computer and Communication Engineering(An ISO 3297: 2007 Certified Organization),Vol. 4, Issue 7, Jul-2016.

[5] ZainabKazemi, Mamun Bin IbneReaz, and FazidaHanim Hashim3, "Low Power Five Stage Current Starved

Voltage Controlled Oscillator in 0.18 µm CMOS Technology Towards Green Electronics", International Conf. on Advances in Science, Engg., Technology &

Natural Resources (ICASETNR-15) Aug- 2015.

[6] Design of Voltage Controlled Oscillator in 180 nm CMOS Technology Sandhiya.S[1], Revathi.S[2], Dr.B.Vinothkumar[3] Volume: 05 Issue: 03 | Mar-2018

AAT Evaluation Rubrics

Description	Marks (10)
Report	4
Simulation	4
Viva	2