



DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute affiliated to Visvesvaraya Technological University (VTU), Belagavi,
Approved by AICTE and UGC, Accredited by NAAC with 'A' grade & ISO 9001 – 2015 Certified Institution)
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560 111, India



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Open ended experiment Report submitted for the subject

Digital Communication Systems – 22EC53

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Evaluation

USN	Name		Simulation & Analysis -10 Marks	Presentation & Report -10 Marks
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CERTIFICATE

This is to certify that Open ended experiment entitled “**Generate PN- Sequence using shift register**” as part of **Digital Communication Systems – 22EC53** is a bonafide work carried out by Chaitra Krishna Gouda (1DS22EC054), Chithrashree G S (1DS22EC058) & Deepthi S R (1DS22EC059) as 30-marks component in partial fulfillment for the 5th semester of Bachelor of Engineering in Electronics and Communication Engineering of the Visvesvaraya Technological University, Belagavi during the year 2024-2025. The Open ended experiment report has been approved as it satisfies the academic requirements prescribed for the Bachelor of Engineering degree.

Signature of Faculty
Prof. Navya Holla K
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Signature of HOD
Dr. Shobha K R

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DECLARATION

We declare that we abide by the ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. The work submitted in this report of **Digital Communication Systems – 22EC53**, V Semester BE, ECE has been compiled by referring to the relevant online and offline resources to the best of our understanding and in partial fulfillment of the requirement for the award of the degree of Bachelor of Engineering in Electronics and Communication Engineering, at Dayananda Sagar College of Engineering, an autonomous institution affiliated to VTU, Belagavi during the academic year 2024-2025. We hereby declare that the same has not been submitted in part or full for other academic purposes.

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Place: Bengaluru

Date: 09-12-2024

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AIM:

To generate a Pseudo-Noise (PN) sequence using a Linear Feedback Shift Register (LFSR) with feedback defined by (3,1)

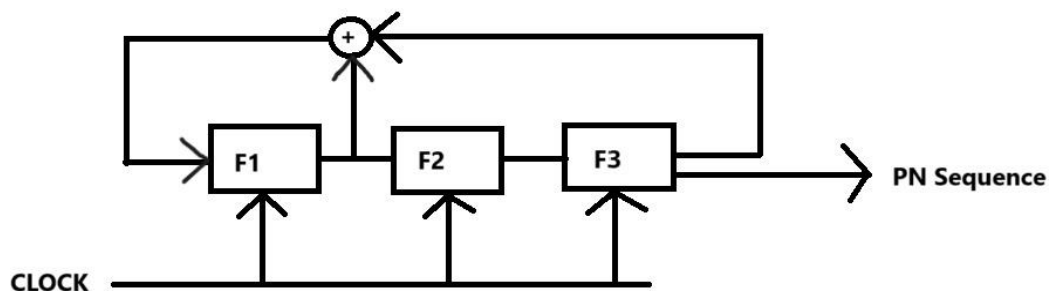
INTRODUCTION:

A Pseudo-Noise (PN) sequence is a deterministic binary sequence that exhibits properties similar to random noise. Despite its deterministic nature, the sequence appears random and uncorrelated over short periods, making it ideal for various applications in communication and digital systems. PN sequences are widely used in applications like spread-spectrum communication, cryptography, and pseudo-random number generation.

The sequence is generated using a fixed algorithm, ensuring repeatability for a given initial state. For an n -bit Linear Feedback Shift Register (LFSR), the length of a PN sequence is $2^n - 1$, which is the maximal length achievable for n bits. The sequence does not include an all-zero state.

The sequence appears random but follows a predictable pattern. It satisfies the balance property (equal number of ones and zeros in a period), the run-length property (distribution of consecutive bits), and the autocorrelation property (low cross-correlation).

BLOCK DIAGRAM:



WORKING:

➤ **LFSR:**

- An LFSR is a shift register whose input bit is a linear function of its previous state.
- For this, the feedback is generated using XOR of the outputs from flip-flop 3 and flip-flop 1.
- For n flip-flops, the sequence length is $2^n - 1$
- The feedback taps (3,1) define the connections used for feedback.

➤ **Maximal Length:** The PN sequence generated with (3,1) achieves the maximal length of $2^3 - 1 = 7$

➤ **Feedback Calculation:** The feedback bit is computed as
Feedback = $\text{LFSR}[3] \oplus \text{LFSR}[1]$ where \oplus is the XOR operation

➤ **Initial State:** The LFSR is initialized to {1,0,1}.

The state must be non-zero to avoid the LFSR being stuck at zero.

➤ **Shifting:** The bits in the LFSR are shifted to the right. The feedback bit is inserted into the first flip-flop.

➤ **Generated Sequence:** Output sequence for {1,0,1}: 1 0 1 0 0 1 1

C CODE :

```
#include <stdio.h>

#define N 7

void generatePNSequence();

int main() {

    generatePNSequence();
```

Generation of PN Sequence

```
    return 0;

}

void generatePNSequence() {

    int lfsr[3] = { 1, 0, 1 };

    int pnSequence[N];

    int feedback, i, j;

    printf("Initial LFSR state: ");

    for (i = 0; i < 3; i++) {

        printf("%d ", lfsr[i]);

    }

    printf("\n");

    for (i = 0; i < N; i++) {

        pnSequence[i] = lfsr[2];

        feedback = lfsr[2] ^ lfsr[0];

        for (j = 2; j > 0; j--) {

            lfsr[j] = lfsr[j - 1];

        }

        lfsr[0] = feedback;

    }

    printf("Generated PN sequence:\n");

    for (i = 0; i < N; i++) {
```


Generation of PN Sequence

```
printf("%d ", pnSequence[i]);  
  
}  
  
printf("\n");  
  
}
```

SIMULATION OUTPUT:

```
main.c  
2  
3 #define N 7 // Length of PN sequence = 2^3 - 1  
4  
5 void generatePNSequence();  
6  
7 int main() {  
8     generatePNSequence();  
9     return 0;  
10 }  
11  
12 void generatePNSequence() {  
13     int lfsr[3] = {1, 0, 1}; // Initial state of the LFSR (can be  
14                             // any non-zero state)  
15     int pnSequence[N];  
16     int feedback, i, j;  
17     printf("Initial LFSR state: ");  
18     for (i = 0; i < 3; i++) {  
19         printf("%d ", lfsr[i]);  
20     }  
21     printf("\n");  
22 }
```

Output
Initial LFSR state: 1 0 1
Generated PN sequence:
1 0 1 0 0 1 1
--- Code Execution Successful ---

MANUAL CALCULATION:

- For (3, 1)
Where 3=no of flip flops,
1s= the output of the flip flop 1 is connected
as intermediate
- Length = $2^n - 1$
 $= 2^3 - 1$
 $= 7$

NO. of Shifts	Flip Flop Content			PN Sequence
	F1	F2	F3	
0	1	0	1	→ 1
1	0	1	0	→ 0
2	0	0	1	→ 1
3	1	0	0	→ 0
4	1	1	0	→ 0
5	1	1	1	→ 1
6	0	1	1	→ 1
7	1	0	1	→ 1

RESULTS AND DISCUSSIONS:

The experiment successfully generated a Pseudo-Noise (PN) sequence using a 3-bit Linear Feedback Shift Register (LFSR) with feedback defined by (3,1). The output sequence, derived from the initial state {1,0,1}, was determined to be:

Generated PN Sequence: 1 0 1 0 0 1 1

This sequence exhibits the desired properties of a PN sequence:

1. **Balance Property:** The sequence has an approximately equal number of 1s and 0s over a period.
2. **Run-Length Property:** The distribution of consecutive 1s and 0s adheres to the expected pattern.
3. **Autocorrelation Property:** The sequence demonstrates low cross-correlation, resembling random noise over short periods.

The manual calculations and simulation results align perfectly, confirming the correctness of the algorithm and implementation.

ADVANTAGES AND APPLICATIONS:

ADVANTAGES

1. **Deterministic yet Random-Like:** PN sequences provide the benefits of randomness while being fully reproducible, aiding debugging and analysis.
2. **Efficiency:** Simple hardware implementations like the LFSR make PN sequence generation resource-efficient.
3. **Maximal Length:** Achieving a sequence of length ensures efficient use of the register.
4. **Noise-Like Properties:** Ideal for applications requiring randomness, such as cryptography or spread-spectrum communication.

APPLICATIONS

1. **Spread-Spectrum Communication:** Used for direct-sequence spread spectrum (DSSS) to reduce interference and improve security.
2. **Cryptography:** Employed in generating pseudo-random keys for secure data transmission.
3. **Error Detection:** Helps generate test patterns in built-in self-test (BIST) circuits for digital systems.

Generation of PN Sequence

4. **Radar and Sonar Systems:** PN sequences are used for signal modulation to enhance resolution and accuracy.
5. **Pseudo-Random Number Generation:** A critical component in simulations and randomized algorithms.

CONCLUSIONS:

The experiment successfully demonstrated the generation of a PN sequence using an LFSR with feedback defined by (3,1). The simulation output matched the theoretical expectations, validating the properties of the PN sequence. PN sequences are indispensable in communication systems, cryptography, and digital signal processing, offering deterministic yet random-like properties. Their efficient generation through simple hardware circuits like the LFSR ensures their relevance across diverse applications.

