**Task 4: Functional Simulation of RISC-V Core (Deadline – 24th January, 2025)**

- **Objective: Perform a functional simulation of the given RISC-V Core Verilog netlist and testbench.**
- **Steps:**
    1. **Download Files:**
        - **Get the Verilog netlist from RISC-V Core Verilog Netlist.**
        - **Get the testbench from Testbench for RISC-V Core.**
    2. **Set Up Simulation Environment:**
        - **Ensure you have a suitable simulation tool (e.g., iverilog, gtkwave).**
        - **Load the Verilog netlist and testbench into the simulator.**
    3. **Run Functional Simulation:**
        - **Simulate the design using the testbench.**
        - **Check the functional correctness of the core by observing the output signals.**
    4. **Capture Waveforms:**
        - **Generate and save waveform snapshots for the executed commands during the simulation.**
    5. **Upload Results to GitHub:**
        - **Update your GitHub repository.**
        - **Upload the waveform snapshots and simulation results to your GitHub.**
        - **Include a brief description of your work in the repository.**
- **Reference Resources:**
    - **Official GitHub repository: RISC-V Core GitHub Repo.**
    - **Use the reference document for additional guidance.**

Please **do not copy/paste** from the sample repository, as your tasks differ from those shown.

All the best