Design of Single Precision Floating Point Arithmetic Logic Unit

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***Abstract*—Floating point numbers are used in many applications such as telecommunications,medical imagining,radar,ete.In top-down design approach,four arithmetic modules,addition, subtraction,multiplication and division are combined to form a floating point ALU unit.Each module is independent to each other.In this paper,the implementation of a floating point ALU is designed and simulated.This paper presents the design of a single precision floating point arithmetic logic unit.The operations are performed on 32-bit operands.The algorithms of addition,subtraction,division and multiplication are modeled in Verilog HDL using ModelSim and an efficient algorithm for addition and subtraction module is developed in order to reduce the no.of gates used.The RTL code is synthesized using Synopsys RTL complier for 180nm TSMC technology with proper constraints. Keywards-floating point number,FPU,overflow.underflow, exceptions,normalization,ete.**

***Index Terms*—component, formatting, style, styling, insert**

I. REFERENCE CIRCUIT

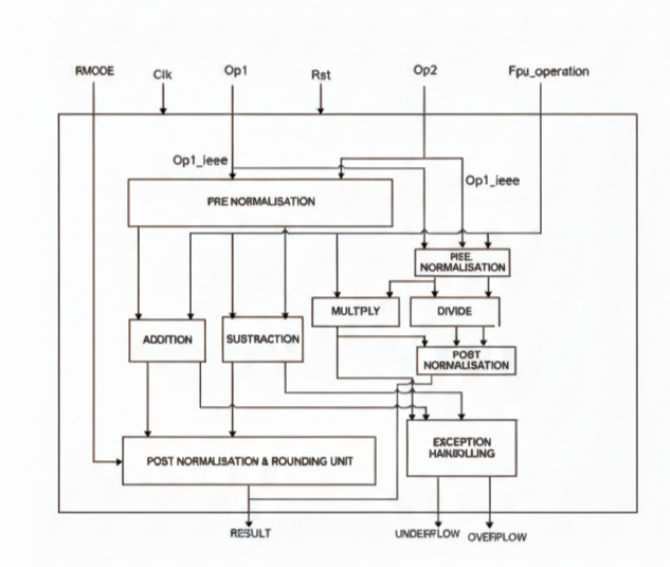

Fig. 1. FLOATING POINT UNIT

II. CIRCUIT DETAILS

Floating-Point Unit (FPU) Circuit Details This block diagram illustrates a Floating-Point Unit (FPU), a specialized processor circuit designed to perform arithmetic operations on floating-point numbers. The unit takes several inputs: two operands (Op1, Op2), a clock signal (Clk), a reset signal (Rst), a rounding mode selector (RMODE), and an operation code (Fpu operation).

The process begins with Pre Normalisation, which aligns the exponents of the input operands (Op1 ieee) before the main arithmetic operation. Based on the Fpu operation input, the circuit directs the data to one of four main arithmetic blocks: Addition, Subtraction, Multiply, or Divide.

After the primary calculation, the intermediate result undergoes further processing. The Op1 ieee and the result from the multiplier feed into another Normalisation block, likely to handle the specific requirements of multiplication and division. The output then proceeds to Post Normalisation, which adjusts the result to fit the standard floating-point format. The final step is the Post Normalisation Rounding Unit, which applies the rounding mode specified by RMODE to produce the final RESULT.

An Exception Handling block monitors the process to detect issues like UNDERFLOW and OVERFLOW, ensuring the FPU responds correctly to invalid operations or results that are too large or too small to be represented

III. REFERENCES

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IV. REFERENCE WAVEFORMS

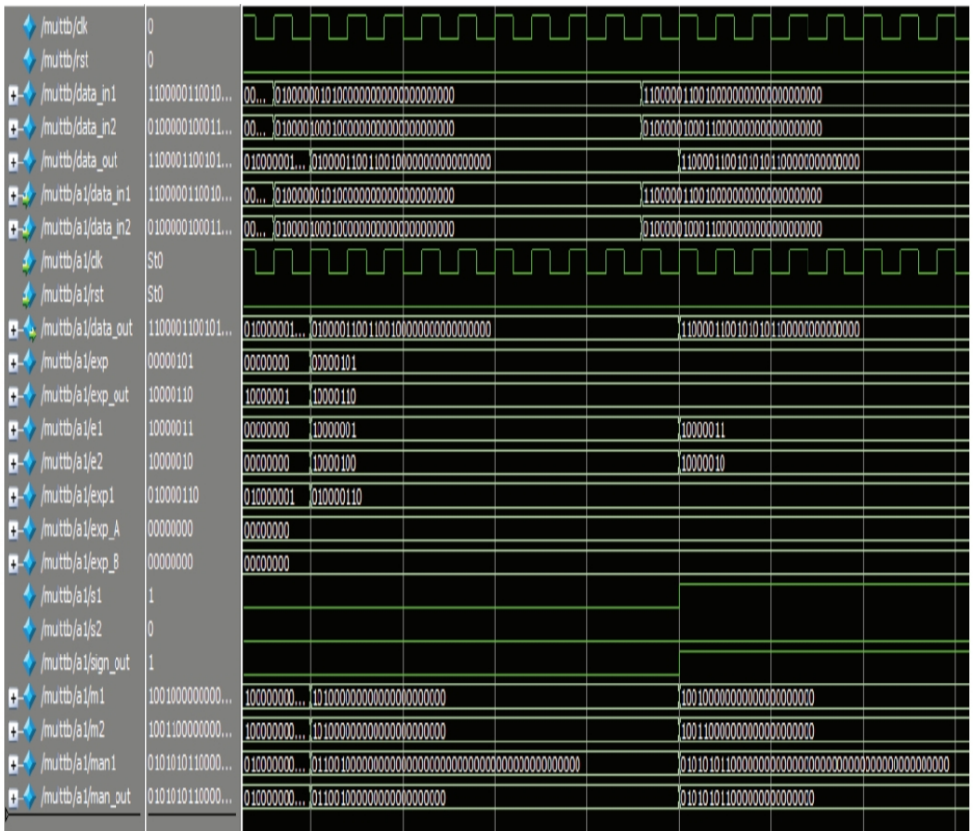

Fig. 2. Caption