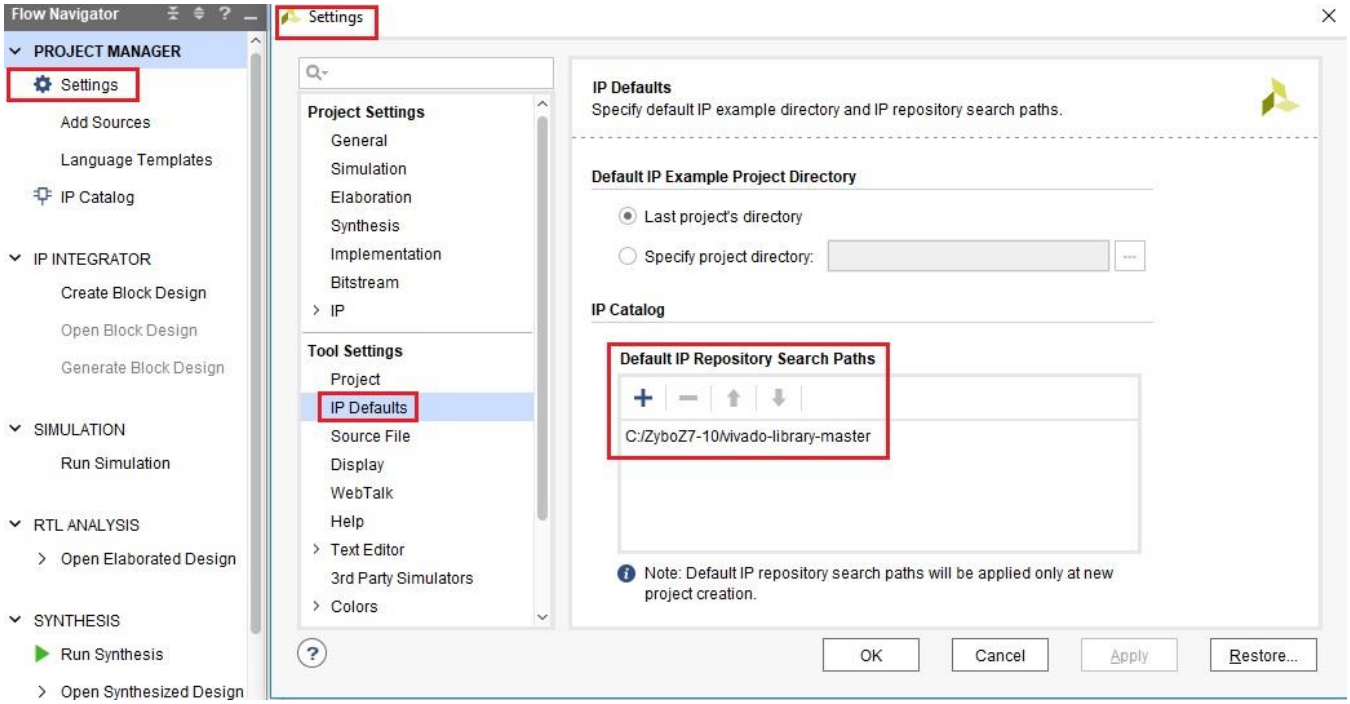
Project: hdmi_pass_through_ZyboZ7-10

1> Xilinx Vivado Installation: Install **Vivado 2017.4** and make sure you have obtained the license.

2> Digilent Board File Installation: The Digilent Zybo Z7-10 board has been used in this project. For Vivado to identify this board, make the necessary changes mentioned in this link. https://reference.digilentinc.com/reference/software/vivado/board-files?redirect=1

3> Get the Digilent Vivado library (IP cores from Digilent GitHub) from https://github.com/digilent/vivado-library and save them C:/ZyboZ7-10/vivado-library-master. You can also choose any location, just make sure to use the same location when you are setting the 'Default IP Repository Search Paths' (shown below in the screen-shot).

In order to get the above IPs listed inside the Vivado IP Catalog, do the following change:

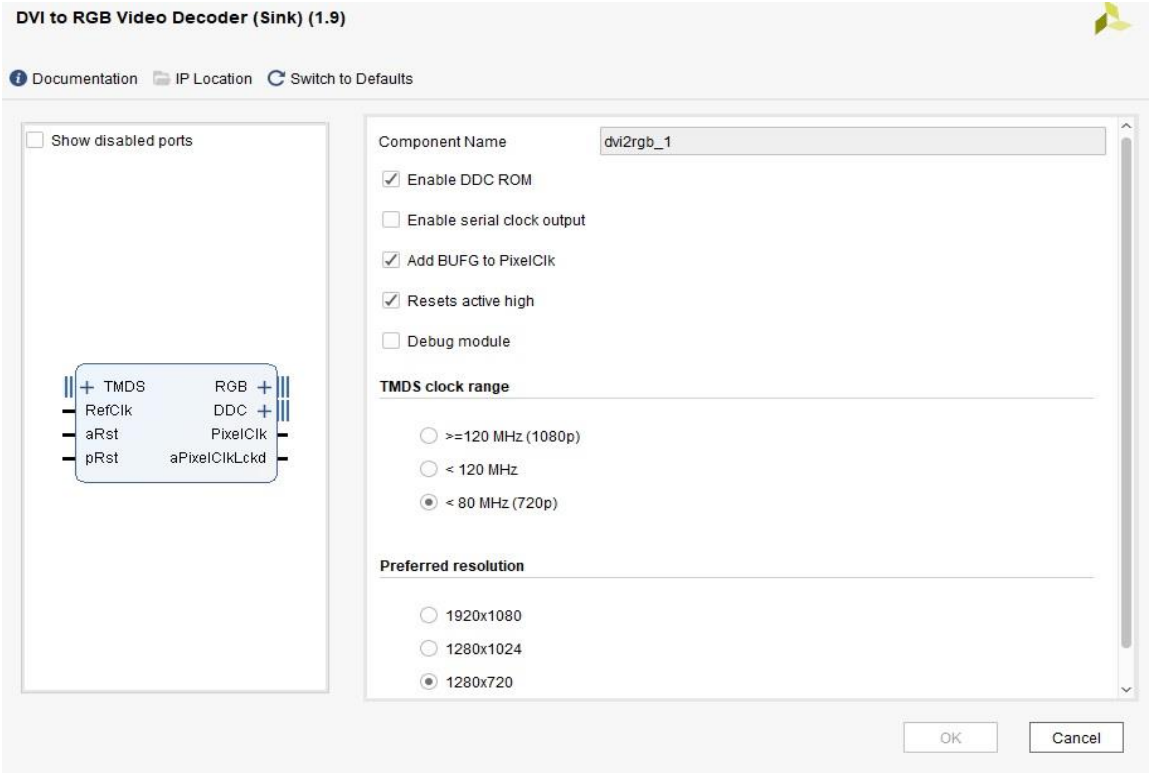


4> Now that our environment is set up, it is time for project creation. I have chosen the project name to be 'hdmi_pass'. Initially just create a blank project with no design data. This will be a VHDL based project.

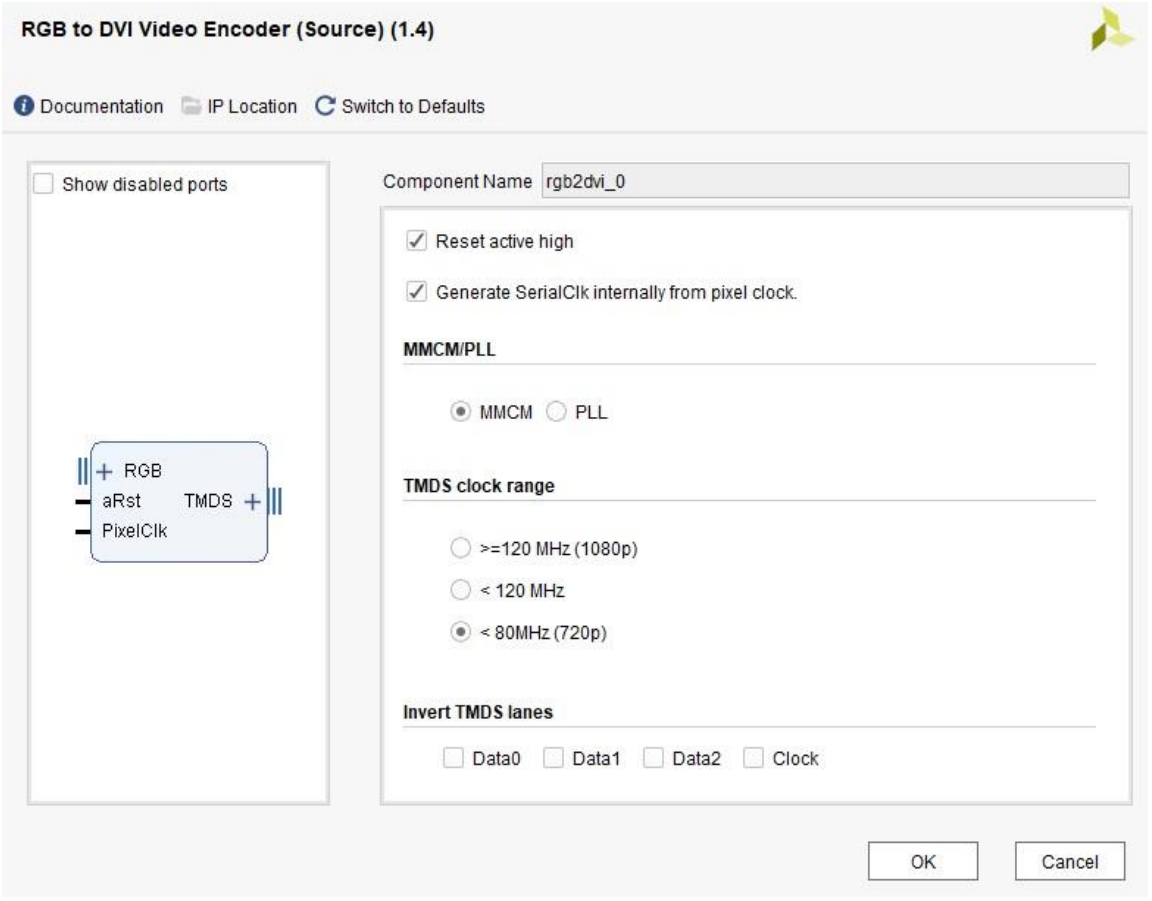
5> Add the following IPs to the project.

a> Xilinx Clocking Wizard: Configure the Clocking Wizard IP such that input clock is 125MHz and output is 200MHz. Choose the 'Primitive' to be PLL and not MMCM.

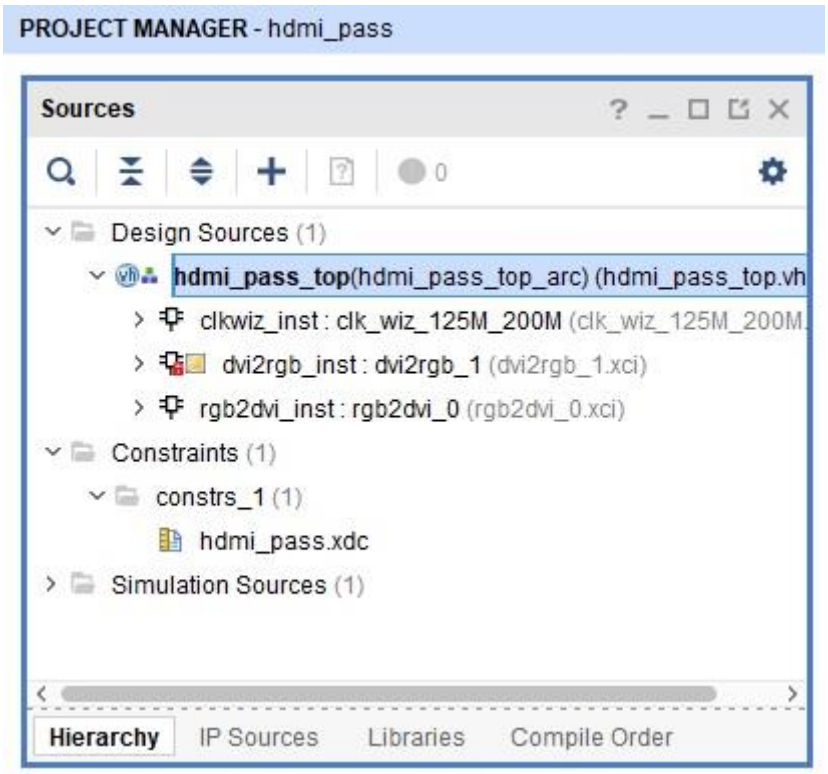
b> Digilent dvi2rgb IP core: Configure the dvi2rgb IP core as shown below.



c> Digilent rgb2dvi IP core: Configure the rgb2dvi IP core as shown below.

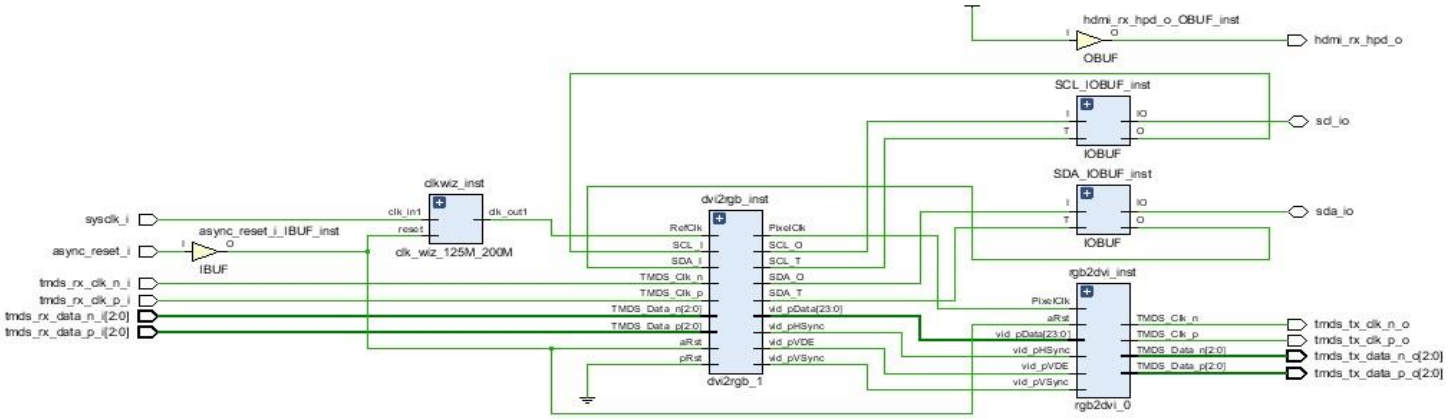


6> Now add the top level VHDL file, *hdmi_pass_top.vhd*, which will instantiate the IP cores and make the necessary connections. For the SCA and SCL connections the IOBUF Xilinx primitive has also been instantiated. In the end add the top level constraints file *hdmi_pass.xdc*. You Sources Window should appear as shown below.



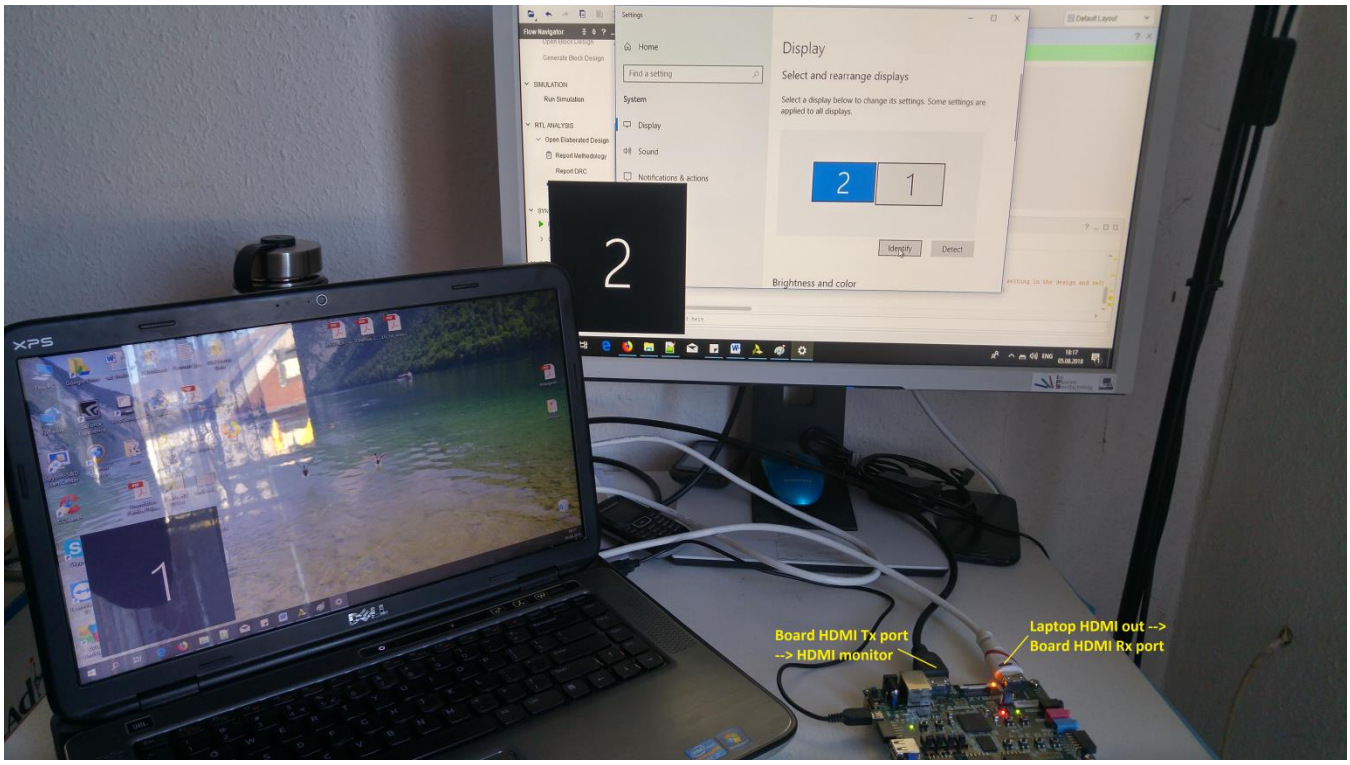
7> Proceed to Synthesis, Implementation and Bitstream generation. There could be some 'Critical warnings' regarding ILA core constraining of the Digilent IP/s. They can be ignored as the IP's debug module is turned-off.

The connectivity of the top-level design should be as shown below. This is the Schematic view of Vivado.



After successful bitstream generation, download the bitstream to the PL section of the FPGA using Vivado's Hardware Manager.

8> Demo in action:
In the picture given below, the display of my laptop is extended to the monitor. You can see that I have allowed Windows to identify the displays ([1] and [2]). The HDMI connections to the Z7-10 board are also marked.



9> **Special Notes**:

a> For the Digilent IPs used here, the HDMI resolution is chosen to be 720p. This is because the Zybo Z7-10 uses a -1 speed grade FPGA which has a FVCO restriction (for other development boards, such as the Z7-20 higher HDMI resolutions can be targeted). Details about this limitation are discussed here: https://forum.digilentinc.com/topic/560-help-with-a-zybo-video-design/

b> If Vivado suggests to upgrade the Digilent IP cores, then do not perform it otherwise the design will not work. The version of the Digilent IP cores used here should be the same as their default downloaded version (Step 3).

c> As 720p is the chosen resolution for the IP cores, the source HDMI signal (i.e. output from my laptop) should also be the same. So it is best to keep the laptop screen resolution to 1280 x 720 and then download the bitstream to the FPGA.