Mr. Chandan Kumar Jha

Personal Details Name: *Mr. Chandan Kumar Jha*
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Research Interests

- Energy Efficient VLSI Architectures, Approximate Computing
  - I am currently working in the area of energy efficient computing. I have worked on the design of approximate circuits for both integer and floating point operations. I am currently looking into the field of approximate architectures which support approximate computing.

Education

- PhD in Electrical Engineering (ongoing, July 2015 onwards)
  Indian Institute of Technology Gandhinagar, India
  CPI 8.87/10
  - A semester of Coursework done at IIT Bombay
    CPI 9.0/10
  - **Semester 1**: **Subjects**: Electronic Devices, Physics of Transistors, VLSI Design, Independent Project Courses.
    SPI : 9.30/10
  - **Semester 2 at IIT Bombay**: **Subjects**: Processor Design, Testing and Verification, VLSI Design Lab, Systems Design.
    SPI : 9.00/10
  - **Semester 3**: **Subjects**: Pattern recognition and Machine Learning, Mathematical Foundations for Computer Vision, Programming Advanced Computer Architectures , Independent Project Courses.
    SPI : 8.26/10
  - **Semester 4**: Internship at Intel India Pvt. Ltd. The work was related to Power Distribution networks.
  - **Semester 5 onwards**: PhD Research
- Bachelor of Technology in Electronics and Communication Engineering
  National Institute of Technology Meghalaya, Shillong, India, 2015
  CGPA 9.38/10
- Higher Secondary School Leaving Certificate
  St. Edmunds College, Shillong, India, 2011.
  Percentage 81.8/100
- Indian Certificate of Secondary Education
  Meghalaya Police Public School, Shillong, India, 2009.
  Percentage 87.4/100

Awards and Fellowships

- Visvesvaraya PhD Fellow
- IITGN Overseas Research Experience Fellowship. I will be interning at ETH Zurich with Prof. Onur Mutlu from (July '19 - Jan '20)
- Richard Newton Young Fellow at Design Automation Conference 2019.
- Intel Research Fellowship 2019

Internships

- Internship at Intel India Pvt. Ltd. The work was related to On Chip Power Distribution networks from 18th January 2017 to 23rd June 2017

  I worked with Yatendra Singh and Bhunesh Kshatri on the design of On-Chip Power Distribution Network. We proposed a methodology for the design of On Chip PDN that leads to 22% reduction in the average IR drop. The work was carried out at Intel.
- Industrial Practical Training conducted by Bharat Sanchar Nigam Ltd. (BSNL) 2013 from 3rd June 2013 to 29th June 2013, Shillong.

  The training mainly consisted of Telecommunication Technologies and Networks, Digital Switching Systems in Telecom, Optical Network and Mobile Communication Systems: GSM,CDMA,3G, RF Concepts.

Teaching

- Teaching Assistant :
  - Embedded Systems(Lab), IITGN, August 2015.
  - VLSI Design, IITGN, August 2016.
  - VLSI Design, IITGN, August 2017.
  - Introduction to Analog and Digital Circuits, IITGN, January 2018
  - Microelectronics Lab, IITGN, August 2018.
  - Embedded Systems, IITGN, January 2019.

Bachelors Publications

- Kumar, Vinay, Chandan Kumar Jha, Gaurav Thapa, and Anup Dandapat. A Novel Methodology for Design of Cyclic Combinational Circuits. Journal of Low Power Electronics 12, no. 3 (2016): 205-217.
  - A methodology for the fast and efficient synthesis of *Cyclic Combinational Circuits* was proposed in this work.

PhD Publications

- C. K. Jha, S. N. Ved, I. Anand and J. Mekie, "Energy and Error Analysis Framework for Approximate Computing in Mobile Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs.
- Jha, Chandan Kumar, and Joycee Mekie. "SEDA-Single Exact Dual Approximate Adders for Approximate Processors." Proceedings of the 56th Annual Design Automation Conference 2019. ACM, 2019.
- Jha, Chandan Kumar, Sumit Walia, Gagan Kanojia and Joycee Mekie. "Floating Point Configurable Approximate Multiplier" (Accepted as Work-in-Progress 56th Annual Design Automation Conference 2019. ACM, 2019.)
- Jha, Chandan Kumar, and Joycee Mekie. "Design of Novel CMOS based Inexact Subtractors and Dividers for Approximate Computing: An In-Depth Comparison with PTL based Designs" (Accepted in EUROMICRO Digital System Design Conference 2019. (DSD))

- Jha, Chandan Kumar, Ankita Nandi and Joycee Mekie. "Quality Tunable Approximate Adder for Low-Energy Image Processing Applications" (Accepted in IEEE International Conference on Electronics Circuits and Systems 2019 (ICECS))
- Nandi, Ankita, Chandan Kumar Jha and Joycee Mekie. "Should We Code Differently When Using Approximate Circuits?" (Accepted in IEEE Asia Pacific Conference on Circuits and Systems 2019 (APCCAS))

Programmes Attended

- 56th Annual Design Automation Conference 2019 from 2nd June to 6th June, 2019
- VLSID Conference from 8th to 10th January, 2018
- GIAN Course on Near/sub-threshold Circuits and Architectures for Microprocessors from 9th to 13th Jan, 2017, IIT Madras.
- Workshop on Workshop on SYNOPSYS EDA Tools under SMDP-C2SD Project from 13th to 17th December, 2016, IIT Gandhinagar.
- IEP on Analog, Mixed-Signal and RF System Design, from 11th to 13th July, 2016, IIT Bombay.
- IEP on CHIP TAPE OUT from 4th to 8th July, 2016, IISc Bangalore.
- GIAN Course on Asynchronous and Synchronous Approaches to Network on Chip Architecture Design from 7th to 18th June, 2016, IIT Gandhinagar.
- VLSI Design and Test (VDAT) Conference from 24th to 27th May, 2016, IIT Guwahati.
- International Workshop on Network on Chip from 10th to 12th December, 2015, MNIT Jaipur.
- System Level Design on Platform FPGAs at from 7th to 9th December, 2015, IIT Delhi.

Other Achievements and Initiatives

- Took initiative to start Circuits and Architecture Research Group meeting under the supervision of Prof. Joycee
- Was awarded Merit Scholarship in B.Tech.
- Managed NanoDC Lab at IIT Gandhinagar (Jointly with Mohit Ganeriwala)

Technical Skills

- Programming: Python, Matlab, C++, Shell, LATEX
- CAD Tools: Cadence Abstract, Cadence Virtuoso, Cadence Liberate, Synopsys Design Compiler
- Hardware Description Language: Verilog
- Operating Systems: Linux and Windows
- Familiar with the ASIC Flow

Course Projects in PhD

- IITB RISC V Pipelined Processor Design.(Prof. Virendra Singh IIT Bombay)
  - A six stage pipelined processor IITB RISC with the data forwarding unit was implemented in Verilog.
- A 4x4 NoC implementation in Verilog.(Prof. Virendra Singh IIT Bombay)
  - A synthesizable single cycle 4x4 NoC was implement Verilog.
- A simulator for Automatic Test Pattern Generator (ATPG) for Combinational Circuits using Python.(Prof. Virendra Singh IIT Bombay)
  - The tool was designed in Python. It would read the netlist of the standard benchmark circuits and report the test vectors required to test the design. It was based on PODEM (Path Oriented Decision Making) algorithm.
- Power analysis of Network on Chip router using Orion 2.0.(Prof. Joycee Mekie IIT Gandhinagar)
  - The tool was used for power analysis of the NoC. An analysis was carried out to study the different components in a router and power consumed by each of the components.
- SPARSE Fast Fourier Transform (Prof. Shanmuganathan Raman IIT Gandhinagar)
  - The Sparse Fast Fourier Transform is used for data sets which are sparse in the frequency domain. The algorithm was implemented in Matlab.

Mentorship

- Worked on Spiking Neural Network using Brian Library with Harshil Shah(Undergrad IITGN)
- Worked on Configurable Floating Point Multipliers with Sumit Walia (Undergrad IITGN)
- Worked on design of Approximate Multipliers with Deepika Soni (Undergrad IITGN)
- Worked on evaluation of deep learning based architectures with Nisarg Ujjainkar (Undergrad IITGN)
- Worked on the design of Approximate Circuits on FPGA with Bishal Banerjee (Undergrad NIT Nagaland)
- Worked on the design of energy efficient data encoding scheme with Shreyas Singh (Undergrad IITGN)
- Worked on the design Approximate Circuits on FPGA with Vinu Sankar (Undergrad IITGN)
- Worked on the design of Approximate Circuits on FPGA with Arun Singh Tomar (M.Tech IITGN)
- Worked on building evaluation frameworks for approximate computing with Kailash Prasad (PhD IITGN)

Collaborations

- Prof. Onur Mutlu, ETH Zurich (Approximate Archietctures)
- Dr. Manu Awasthi, Ashoka University (Energy Efficient Architectures for Approximate Computing)

Relevant Courses

- Processor Design, VLSI Design, Computer Architecture, VLSI Design Lab, Testing and Verification of Digital Circuits, Pattern Recognition and Machine Learning, Graduate Algorithms.