00971

Sri Lanka Institute of Information Technology

B. Sc. Special Honours Degree/ Diploma
in
Information Technology

Final Examination
Year 1, Semester 1 (2016)

IT100 – Computer Fundamentals

Duration: 2 Hours

Instructions to Candidates

- This paper contains 4 questions on 5 pages.
- This paper is preceded by a 10-minute reading period. The supervisor will indicate when answering may commence.
- Each question carries equal marks.
- Answer ALL questions.
- Read all questions before start answering.
- The total marks obtainable for this examination is 100.
- This examination accounts for 60% of the module assessment.
- This is a close book examination.

Question 1 – Data Representation and Number Systems **(25 Marks)**

a) Copy and complete the table below. You have to clearly show all your workings in your answer sheet.

Binary	Decimal	Octal	Hexadecimal
1011011011_2			
		125_8	

(6 Marks)

b) Perform the following subtractions using 2s complementary arithmetic (show all intermediate steps).

i) 126 - 52
ii) 35 - 64

(6 Marks)

c) The reading on a hexadecimal odometer is 34FA. Miles later you see a reading of 8AFC. How far you have gone. Give the answer in decimal.

(4 Marks)

d) Use the binary division and shift and adding methods to solve the following expressions (show all intermediate steps)

i) 27/6
ii) 31 x 14

(6 Marks)

e) Give the decimal number representation of binary number 1011.0011. (show all intermediate steps).

(3 Marks)

Question 2 - Logic Circuits and Controls **(25 Marks)**

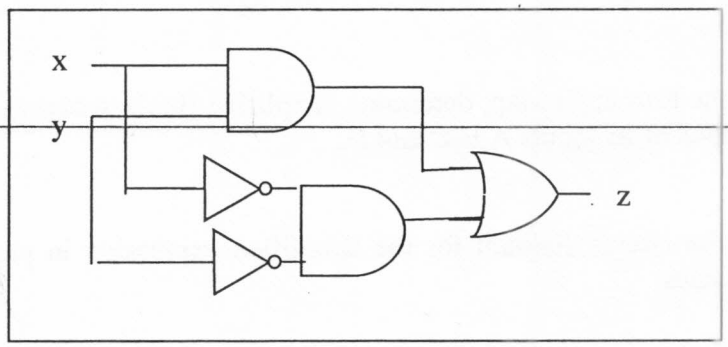
a) Using the laws and rules of Boolean Algebra simplify the following expressions.

i. $F = A.\bar{B}.\bar{C} + \bar{A}.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + \bar{A}.\bar{B}.C + A.B.\bar{C}$

ii. $F = (X + Y).(\bar{X} + Y + Z).(\bar{X} + Y + \bar{Z})$

(8 Marks)

b) Consider the following combinational circuit.

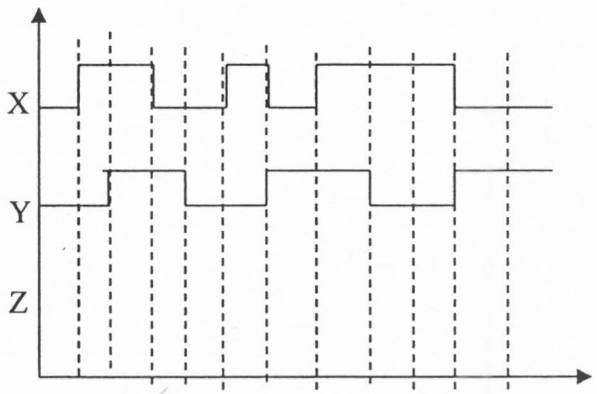


i) Draw the truth table for the above circuit.

(2 Marks)

ii) The inputs of the above circuit are given as X and Y in the following graph. Copy and complete the output of the circuit in the same graph.

(3 Marks)



c) A combinational logic circuit takes 4 binary inputs A, B, C and D where each combination represents a decimal number. Here A is the most significant bit (MSB). For the decimal input 1,2,3,5,7,11 and 13, the output S generates 1 and for all the other inputs, the circuit generates 0.

i) Write down the truth table for the above-mentioned circuit.

(3 Marks)

ii) Using the Karnaugh Map, determine simplified Boolean expression for the output S, in terms of its inputs A,B,C and D.

(5 Marks)

iii) Draw the circuit diagram for the simplified expression in part (ii) using Basic Logic Gates.

(4 Marks)

Question 3 - Logic Circuits and Controls **(25 Marks)**

a) List down two differences between combinational circuits and sequential circuits.

(2 Marks)

b) Compare SR Flip Flop and D Flip Flop with aid of circuit diagrams.

(4 Marks)

c) How do you use a 2-4 Decoder to implement a half adder? Write down the:

i) Circuit Diagram.

ii) Sum and Carry Expressions.

(5 Marks)

d) Draw the block diagram to implement 32X1 Multiplexer by combining 3 relevant types of Multiplexers.

(4 Marks)

e) Draw a Programmable Logic Array to represent the summation of half adder.

(4 Marks)

f) Implement a parallel adder to represent the addition of 01 and 11 binary numbers.

(6 Marks)

Question 4 – Computer Organization and Memory **(25 Marks)**

a) List down 2 classes of Operating Systems and briefly explain each of them.

(2 Marks)

b) List down 2 facts about each of the following topics.
   i) Process Management Services
   ii) Disk Management Services

(4 Marks)

c) Following table illustrates 3 instructions (Ins1, Ins2 and Ins3) which are used to perform the subtraction operation.
   Ex-60-20=40

Address	Memory
9	**Load A 12 (Ins 1)**
10	**Sub A 14 (Ins 2)**
11	**Store A 13 (Ins 3)**
12	60
13	
14	20

- **Ins 1- Load A 12** -Load Accumulator with the content stored in memory location 12
- **Ins 2- Sub A 14** - Subtract the Accumulator content with the content stored in memory location 14
- **Ins 3- Store A 13** -Store the content of the accumulator at memory location 13

Briefly explain the above subtraction process using diagrams.

Hint: Use PC, MAR, MDR, CIR registers, Accumulator and necessary buses.

(10 Marks)

d) Write short notes for the following topics.

   i) Address Bus
   ii) Data Bus
   iii) Control Bus

(6 Marks)

e) Compare and Contrast Static Memory and Dynamic Memory.

(3 Marks)

End of Question Paper