Drake Bridgewater & Ryan Phillips
April 19, 2014
CS 472 HW 3

(3.1)

Why is the program counter a pointer and not a counter?

> It saves a step. If it were a counter, an address would still need to be stored somewhere, and arithmatic on this address would need to be performed using the counter. But since the program instructions are stored sequentially in memory, the address itself can simply be incremented to get the next instruction.

(3.2)

Explain the function of the following registers in a CPU.

a) PC

> The Program Counter. It is incremented after an instruction is fetched. It holds the memory address of the next instruction to be executed.

b) MAR

> The Memory Address Register. It works in tandom with the MDR. It either contains the location of the where the MDR data should be written to, or the location of data which will be read into the MDR.

c) MDR

> The Memory Data Register. It contains the data referred to in the MAR explanation above.

d) IR

Instruction Register. This contains the instruction which is currently being executed. It is fetched from the location pointed to by the PC.

(3.3)

For each of the following 6-bit operations, calculate the values of the C, Z, V, and N flags.

a. 001011 001101 +

b. 111111 000001 +

c. 000000 111111 -

d 101101 011011 +

e 000000 000001 -

f. 111110 111111 +

(3.10)

Why does the ARM provide a reverse subtract instruction RSB r0,r1,r2 that implements [r0] = [r2] - [r1] when the normal subtraction instruction SUB r0,r2,r1 will do exactly the same job?

These two operand only differ by the order of operation, and can be seen as unnecessary as switching the two operands for SUB should suffice. The problem arises when only the second operand can be constant or other special forms. All operations could be done using the SUB operations but additional registers would be necessary as seen in this example: $SUB\ R2,\ R4,\ \#8$ if you wanted to do the exact opposite you would need an an additional register to hold the constant #8, but using RSB it would just be $RSB\ R2,\ R4,\ \#8$

(3.17)

(3.18)

Write one or more ARM instructions that will clear bits 20 to 25 inclusive in register r0. All the other bits of r0 should remain unchanged.

(3.19)

This is a classic problem of assembly language programming. Write a sequence of ARM instructions that swap the contents of registers r0 and r2 without using any additional registers or memory storage (that is, you can't move r1 to a temporary location).

(3.25)

What is the binary encoding of the following instructions?

a) STRB r1, [r2]

b) LDR r3, [r4, r5]!

c) LDR r3, [r4], r5

d) LDR r3, [r4,#-6]!

(3.39)

Write an ARM assembly language program that scans a string terminated by the null byte 0x00 and copies the string from a source location pointed at by r0 to a destination pointed at by r1.

(3.51)

Write an ARM assembly language program to determine whether a string of characters with an odd length is a palindrome (for example, mom) under the following constraints.

a. The string of ASIC-encoded characters is stored in memory.

b. At the start of the program, register r1 contains the address of the first character in the string, and r2 contains the address of the last character. On exit from the program, register r0 contains a 0 if the string is a not a palindrome, and 1 if it is.

References

[1] Alan Clements. *Computer Organization and Architecture.* Global Engineering: Christopher M. Shortt, themes and variations edition, 2014.