A 15Gb/s Wireline Repeater in 65nm CMOS Technology

[1]Weidong Cao, [1,2]Xuqiang Zheng, [1]Ziqiang Wang, [1]Dongmei Li, [1]Fule Li, [2]Shigang Yue, [1]Zhihua Wang
[1]Institute of Microelectronics, Tsinghua University, Beijing, China
[2]School of Computer Science, University of Lincoln, Lincoln, UK
Email: chalvescao@gmail.com

***Abstract*—This paper describes the design of a wireline repeater in 65nm CMOS technology. The T-coil networks with ESD protection are used in both repeater's input and output to realize impendence matching and bandwidth enhancement. Three continuous time linear equalizers (CTLE) placed in the data path are used to compensate for high frequencies loss, while the current mode logic (CML) buffer chain is used to compensate for DC loss. The measurement results show that the repeater could deliver 15 Gb/s data through a 10 inch channel which has a 19.2 dB loss at 7.5GHz. The power consumption is 2.67mW/Gbps under 1.1V supply voltage and the chip area is 0.63mm^2.**

***Keywords*—repeater; T-coil; CTLE; CML buffer**

I. INTRODUCTION

Serializer/Deserializer (SerDes) is widely used in many applications to improve the wireline transmission performance, such as SATA, Hyper TransPort, PCIExpress, InfiniBand treaty and so on. As the data transmission rate of wireline communication systems reaches to tens of Gb/s, the severe channel loss will cause serious inter-symbol interference (ISI), which could degrade jitter performance, signal to noise ratio (SNR) and ultimately worsen the bit error rate (BER) [1]. In this case, equalization is usually applied to remove time-domain ISI, or flatten the frequency response up to Nyquist frequency to compensate for the high frequency attenuation of the channel [2]. One common method is to place a decision feedback equalizer (DFE) in front of receiver to cancel ISI. However, since DFE has the issues of considerable power consumption and high design complexity, feed forward equalizer (FFE) for transmitter is often applied to release the pressure of receiver equalization. Nevertheless, the design of FFE delay cell is difficult at high data rate. On the contrary, for simple and low loss channel, continuous time linear equalizer (CTLE) is a better choice for lower cost. In this paper, we proposed a wireline repeater based on CTLE which could effectively compensate a 10 inch channel with 19.2dB loss at 7.5GHz.

What's more, the problem of electrostatic discharge (ESD) continues to become more critical as the data rate reaching up to tens of Gb/s. As the [4] concludes, high-speed ESD protection circuits must satisfy several difficult criteria. These circuits should: 1) provide a broad bandwidth despite the parasitic capacitance of the ESD protection device itself; 2) occupy a small area with a reasonable aspect ratio so that tens or hundreds of these devices can be integrated on a chip without complicating the layout and routing; 3) create good impedance matching at the input and output to avoid corrupting the high-speed data; and 4) exhibit negligible midband loss. Therefore, T-coil network in [3] is employed in this repeater's design, which is efficient for impendence matching and bandwidth enhancement.

This paper is organized as follows: Section II presents the proposed repeater architecture and building blocks. The measured results are shown in Section III. Conclusions are presented in section IV.

II. ARCHITECTURE

The block diagram of the proposed wireline repeater with TX/RX and channel model is presented in Fig.1. As the Fig.1 shows, the repeater consists of a T-coil with ESD protection at the input, two CTLEs, one CML buffer, one CML buffer chain in the data path and a driver stage at the output. It should be noted that the output driver is a CTLE embed with T-coil and ESD protection.

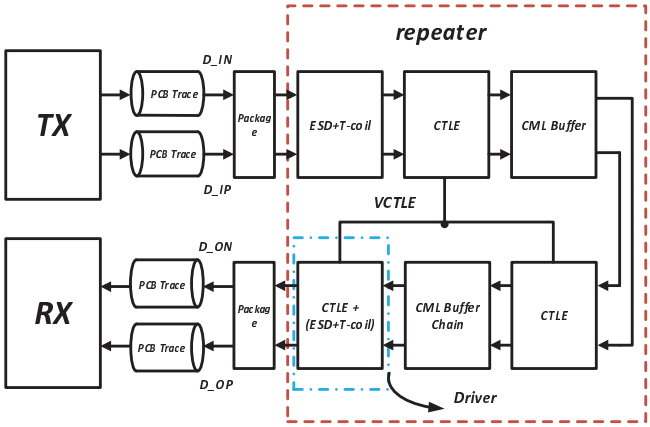

Fig.1. The block diagram of the proposed design

The T-coil networks with ESD protection are placed at both input and output of the repeater, which are employed to enhance the bandwidth and provide good impedance matching. The CTLE stages are used to compensate for the high frequencies loss of signals while the buffer and buffer chain are used to promote the DC gain of signals. By controlling the voltage *VCTLE* on the CTLE, the desired peaking location and gain can be obtained. All of the buffers belonging to current mode logic (CML) provide a strong drive capability and wide

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band.The 15Gb/s differential data coming from TX are delivered to the repeater through a 10 inch printed circuit board (PCB) trace. After being equalized by the repeater, the data will be sent to RX through another 10 inch PCB trace and finally be accepted by RX.

A. ESD and T-coil Circuit

The repeater's input and output termination networks are similar, and the output termination network is shown in Fig.2. As depicted in Fig.2, the T-coil network consists of two coupled inductors L_1 and L_2, which has a coupling coefficient of K and a bridge capacitor C_B. The output is applied to terminal A, while the termination resistor R_D is connected to terminal B, and the load capacitance is tied to terminal X.

As referred in [4], the T-coils offer two attributes which proved to be useful in ESD design. First, if designed properly, the circuit displays a purely resistive input impedance, independent of the frequency and the value of C_L. This can be seen intuitively by observing that L_1 and L_2 short the input to R_D at low frequencies, while at high frequencies C_B plays the same role when L_1 and L_2 are open. It can be proved that the input impedance remains resistive for all frequencies if the following conditions are hold:

$$L_1 = L_2 = \frac{C_L R_D^2}{4}\left(1+\frac{1}{4\varepsilon^2}\right) \quad (1)$$

$$C_B = \frac{C_L}{16\varepsilon^2} \quad (2)$$

$$k = \frac{4\varepsilon^2 - 1}{4\varepsilon^2 + 1} \quad (3)$$

where ε is the damping factor of the network's transfer function. As these equations suggest, ε and k, hence, are chosen to target a desired response, and other T-coil parameters are subsequently determined.

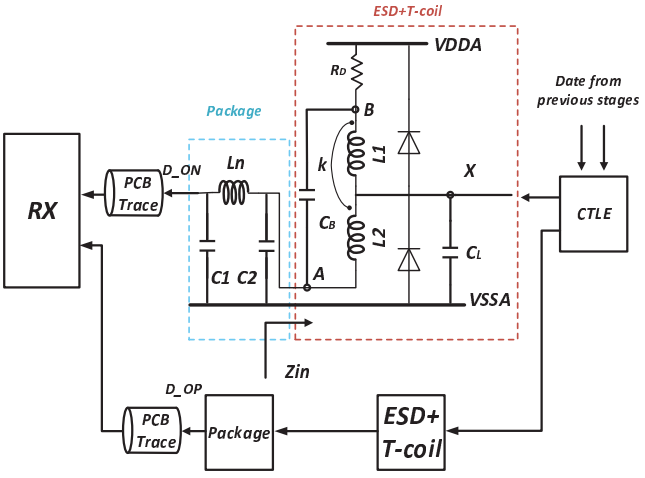

Fig.2. Output termination network of the repeater

In order to keep output resistor constant and group delay uniform, according to [4], we let $C_B=C_T/12$, $C_T=C_L+C_{ESD}$, $k=0.5$. Therefore, in the symmetrical case, it comes as $L_1=L_2=R_D^2C_T/3$. By adjusting the parameters basing on the former calculation, a good impedance matching is obtained and the bandwidth of the circuit is broadened by a factor of 2.5. Specially, the package module is also considered in this design, which is simplified to a π resonant network. The value of L_n should be designed carefully to obtain a higher resonant frequency.

B. CTLE with Manual Coeffcient

In order to equalize 15Gb/s data, the CTLE must provide wide bandwidth and remarkable capability of large boosting at high frequencies. Traditional approach incorporating capacitive degeneration technique to generate tunable boosting can't satisfy the requirements. To further extend the bandwidth and enlarge the boost, each CTLE stage is realized with capacitive degeneration and inductive peeking, as shown in Fig.3.

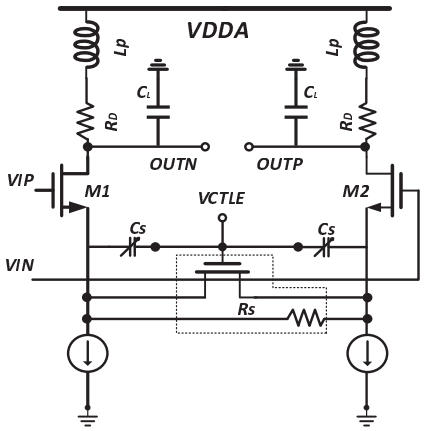

Fig.3. The structure of proposed CTLE

The variable capacitor and resistor are implemented by varactors and a NMOS transistor respectively. By controlling the voltage *VCTLE* on the varactors and the NMOS transistor, the desired peaking location and gain can be obtained. The conclusion in [5] shows that this topology facilitates the equalizing filter's design and makes the 15-20 dB compensation at 7.5GHz become feasible.

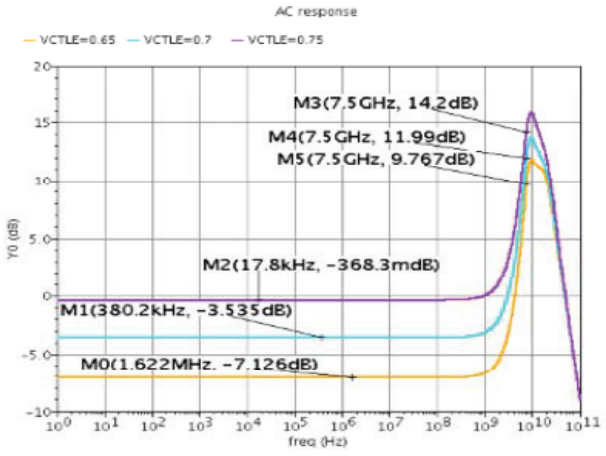

Fig.4 The AC response of proposed CTLE

Fig.4 shows the AC response of the cascaded CTLE when *VCTLE* changes from 0.65V to 0.75V with a 50mV step. Simulation shows that the cascade CTLE stages can make about 11.4dB-22.4dB compensation when *VCTLE* changes from 0.5V to 1.1V.

C. CML Buffer Gain Stage

As the CTLE provides frequency peaking at the cost of attenuating low frequency component, the gain stages are used to compensate for DC loss. To extend the bandwidth even further, we choose the CML buffer with inductive peeking technique, as shown in Fig.5.

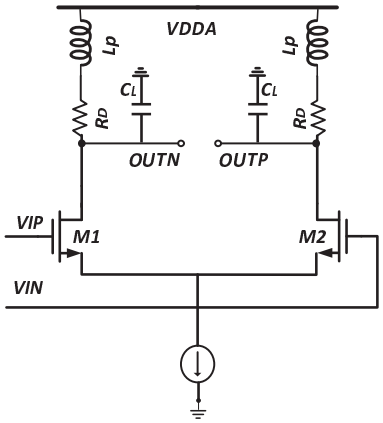

Fig.5. Proposed CML buffer

Simulation shows that the 3-dB bandwidth of the single CML buffer is 20GHz. The single CML buffer and the buffer chain result in a total gain of 9dB, with single buffer 3dB and buffer chain 6dB, respectively。

D. Driver Stage

The repeater's output driver stage is shown in Fig.6, which is actually a CTLE embed with T-coil and ESD protection. Both the CTLE in Fig.6 and Fig.3 have the same structure, as well as the T-coil and ESD protection in the Fig.6 and Fig.2. The difference is that the output of CTLE in Fig.6 is realized by T-coil and ESD protection, which could enhance the bandwidth and provide good impedance matching.

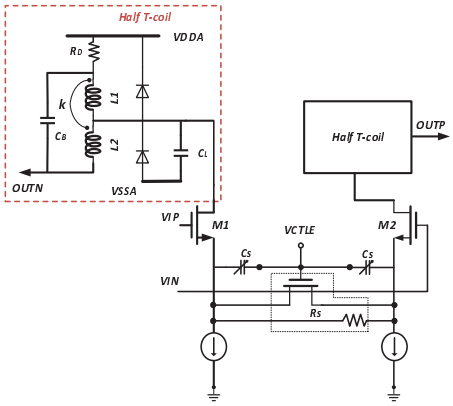

Fig.6. The output driver stage

III. Experimrnt Result

The presented repeater is fabricated in TSMC 65nm CMOS Technology. And the micrograph of the whole chip is shown in Fig.7, which occupies an area of 0.62mm^2.

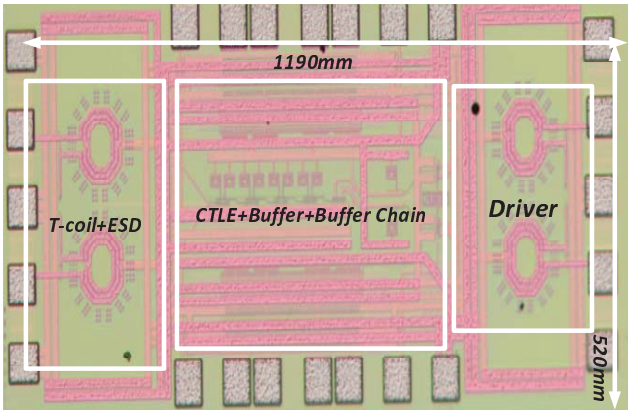

Fig.7 Chip micrograph

The chip is tested by Agilent's DSA-Z634A digital signal analyzer with 63GHz bandwidth and Anritsu MP1800A signal quality analyzer. As the Fig.8 shows, before received by the repeater, the 15Gb/s PRBS7 data will pass through a 10 inch PCB trace, which has a loss of 19.2 dB at 7.5 GHz as the Fig.9 shows.

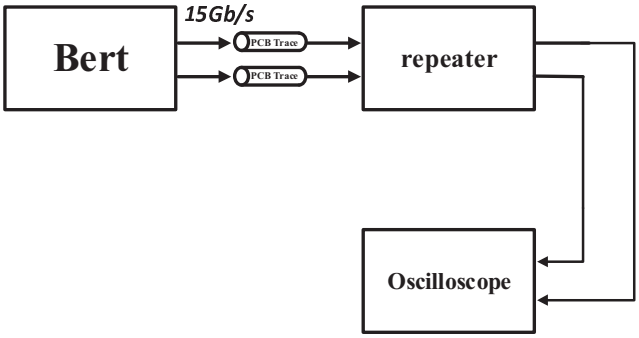

Fig.8 The test setup of repeater

Fig.9 S parameter of PCB trace

Fig.10 depicts the eye diagram of output data equalized by the repeater after the 10 inch PCB trace. The 15Gb/s PRBS7 output has 18ps jitter and 350mV eye opening. Hence, the result suggests that the designed repeater supports 15Gb/s data transmission. Finally, the power of the entire repeater is 40mW under 1.1V supply and the simulated power distribution is presented in Fig.11.

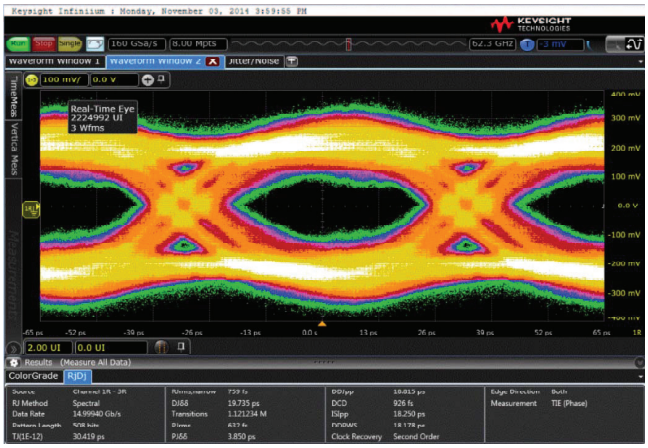

Fig.10 Measured eye diagram at 15Gb/s

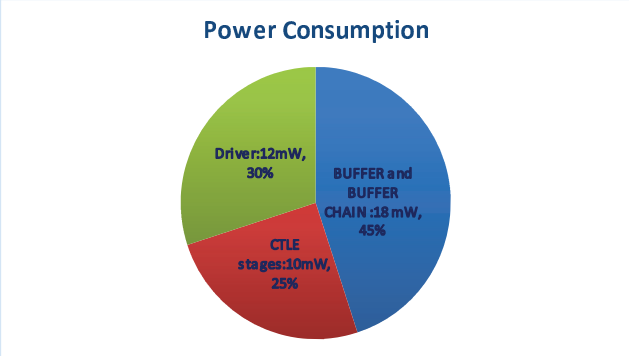

Fig.11 Simulation power distribution

IV. Conclusion

This paper presents a wireline repeater in 65nm CMOS technology. The repeater can compensate a 10 inch channel with 19.2dB loss at 7.5GHz. The power efficiency of the transmitter is 2.67mW/Gbps under 1.1V supply with 350mV output swing.

Acknowledgment

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