Mincheol Cha

mccha@capp.snu.ac.kr | 82+ 010-7599-7679 | github.com/chamchiking

Education

Seoul National University (SNU) — Seoul, Korea
M.Sc. in Electrical and Computer Enginnering; GPA: 3.83/4.3 — Mar 2023 – Present
Graduate Researcher, Computer Architecture and Parallel Processing Lab (CAPP)
Advisor: Professor Hyuk Jae Lee, Ph.D.; Secondary Advisor: Xuan Truong Nguyen, Ph.D.

Seoul National University (SNU) — Seoul, Korea
B.Sc. in Electrical and Computer Enginnering; Total GPA: 3.64/4.3 **(Cum Laude)** — Mar 2016 – Feb 2023

Research Interests

High-performance reconfigurable computing: FPGA, computer architecture, System on Chip (SoC)
Sensor Technologies: Dynamic Vision Sensors (DVS), sensor fusion.
Machine learning and system: ML algorithm/system co-design, 3D Network
Electronic design automation (EDA): high-level synthesis (HLS), physical design

Publications

[Conference]

[C1] ***Mincheol Cha***, Keehyuk Lee, Bobaro Chang, Soosung Kim, Daniel Moon, Taeho Lee, Xuan Truong Nguyen, Taesung Kim, Hyunsurk Ryu, "An Energy-Efficient Daily Surveillance System with DVS-CIS Sensor Fusion and Event-based NPU Triggering," submitted to the 2025 IEEE International Symposium on Circuits and Systems (ISCAS 2025), London, United Kingdom, May 2025 (under review).

[C2] ***Mincheol Cha***, Keehyuk Lee, Bobaro Chang, Soosung Kim, Taeho Lee, Xuan Truong Nguyen, Taesung Kim, Hyunsurk Ryu, "A DVS-CIS Sensor Data Receiver on FPGA with a 10 Gbps MIPI Controller," submitted to the 2025 IEEE International Symposium on Circuits and Systems (ISCAS 2025), London, United Kingdom, May 2025 (under review).

[C3] ***Mincheol Cha***, Keehyuk Lee, Bobaro Chang, Soosung Kim, Taeho Lee, Xuan Truong Nguyen, Taesung Kim, Hyunsurk Ryu, "Live Demonstration: DVS-CIS Sensor Fusion System for Real-Time DNN-Based Object Detection," submitted to the 2025 IEEE International Symposium on Circuits and Systems (ISCAS 2025), London, United Kingdom, May 2025 (under review).

[C4] Soosung Kim, ***Mincheol Cha***, Xuan Truong Nguyen, Hyuk-Jae Lee, "Towards Eight-bit Quantization for 3D U-Net Medical Image Segmentation via ROI-Based Calibration and Background-Aware Shift," IEEE/IEIE International Conference on Consumer Electronics - Asia (ICCE-Asia 2024), Da Nang, Vietnam, November 2024 (accepted).

[C5] Keehyuk Lee, ***Mincheol Cha***, Soosung Kim, Xuan Truong Nguyen, Hyuk-Jae Lee, "A Winograd-Convolution-Based Accelerator on FPGA for Real-time Object Detection with Effective On-chip Buffer Access Patterns," submitted to the 42nd IEEE International Conference on Consumer Electronics (ICCE 2025), Las Vegas, NV, USA, January 2025 (accepted).

[C6] ***Mincheol Cha***, Keehyuk Lee, Xuan Truong Nguyen, Hyuk-Jae Lee, "A Low-Latency and Scalable Vector Engine with Operation Fusion for Transformers," IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), Apr. 2024. [10.1109/AICAS59952.2024.10595857]

[C7] Hyunha Hwang, Se-Hun Kim, ***Mincheol Cha***, Min-Ho Choi, Kyujoong Lee, Hyuk-Jae Lee, "Analysis of the Effect of Feature Denoising from the Perspective of Corruption Robustness," The 38th International Technical Conference on Circuits/Systems, Computers, and Communications (ITC-CSCC), Jun. 2023. [10.1109/ITC-CSCC58803.2023.10212895]

[C8] ***Mincheol Cha***, Hyunha Hwang, Kyujoong Lee, Hyuk-Jae Lee, "Enhancing Neural Networks Corruption Robustness with Convolution Kernel Size Change," in Fall Conf. of the Institute of Electronics and Information Engineers (Conf. of IEIE), Nov. 2023. (in Korean) [View the Full Paper]

[C9] Min-Ho Choi, Se-Hun Kim, Hyunha Hwang, ***Mincheol Cha***, Kyujoong Lee, Hyuk-Jae Lee, "Performance comparison depending on normalization method in single batch training environment," in Summer Conf. of the Institute of Electronics and Information Engineers (Conf. of IEIE), Jun. 2023. (in Korean) [View the Full Paper]

[C10] ***Mincheol Cha***, Sangmin Lee, Xuan Truong Nguyen,, "Implementation of a Convolution Layer Kernel Accelerator using High-Level Design Synthesis," in Fall Conf. of the Institute of Electronics and Information Engineers (Conf. of IEIE), Nov. 2022. (in Korean) [View the Full Paper]

Patents

[P1] **Mincheol, Cha**. 2024. "LOW-LATENCY AND SCALABLE VECTOR SYSTEM WITH OPERATION FUSION" Korean Patent DP240209, filed May 2024.

Technical Experience

Computer Architecture and Parallel Processing Lab (CAPP Lab) Seoul, Korea
Graduate Researcher Jan 2023 – Present

- **Project: Development of SoC for High-Speed Video Recording and Recognition** [C1], [C2], [C3], [C5]
  - Implemented WinoConv-based engine for real-time object detection on Xilinx ZCU106 board.
  - Designed a novel hardware-friendly post-training quantization scheme, achieving less than 1% drop in mean average precision (mAP) for the Tiny-YOLOv3 model.
  - Achieved a latency of 18 ms and a throughput of 362 GOPS at 200 MHz clock frequency realizing 4k 60fps end to end real-time object detection.
- **Project: Efficient 3D U-Net Deployment on NPU for Medical Applications** [C4]
  - Quantized a 3D U-Net model for medical image segmentation, incorporating ROI-based calibration, background shift, and instance normalization folding.
  - Achieved a 0.4% dice score drop on the KITS19 dataset during quantization using integer-only arithmetic.
  - Developed an NPU architecture on the Xilinx Alveo U280 board, leveraging the inherent sparsity of the 3D U-Net model.
- **Project: Vector Processing Unit with Operation Fusion (HLS, Hardware Simulator Integration)** [P1] [C6]
  - Designed and wrote a patent about Vector Processing Unit (VPU) with Operation Fusion and achieved 50% reduction in speed with only 10% area overhead.
  - Implemented VPU IP with HLS and tested on Xilinx ZCU106 board.
  - Aligned real-world DRAM access with simulated DRAM access with less than few clock cycles for more accurate NPU system performance modeling.
  - Added new VPU architectures into STONNE-FLEX(A Simulation Tool for Neural Networks Engines) simulator.
- **Project: Enhancing Corruption Robustness in Model Training** [C7], [C8], [C9]
  - Developed a Laplacian-based sharpening filter integrated after lateral 1x1 convolutions in fpn(feature pyramid network) to enhance feature maps and achieved 7% increase in accuracy for defocus blur with PCB dataset.
  - Tuned gain values for the filter (0 to 0.1), achieving optimal performance at gain 0.05.
  - Implemented anti-aliasing across downsampling operations in the ResNet-50 backbone and applied it to the last two FPN convolution layers.

Neuro-Reality Vision (NRV corp) Dongtan, Korea
Lead Hardware Engineer May 2021 – Present

- **Project: Development of SoC for High-Speed Video Recording and Recognition** [C1], [C2], [C3], [C5]
  - Collaborated with CAPP Lab on the development and implementation of a WinoConv-based engine utilizing a CMOS Image Sensor (CIS) and a Dynamic Vision Sensor (DVS) for real-time object detection on the Xilinx ZCU106 board.
  - Designed up to 13,000 fps DVS(Dynamic Vision Sensor from Samsung) MIPI Rx subsystem IP.
  - Developed a full SoC evaluation platform for DVS sensors, successfully achieving no frame loss up to 4,000 fps with frame size 960x720 on the Xilinx ZCU106 board.
  - Integrated and fully optimized Ethernet 2.5Gbps interface on Xilinx ZCU106 for seamless image sensor bring-up and real-time data transmission.
  - Designed interface boards to connect the DVS sensor with FMC and Infineon CX3 (MIPI CSI-2 to USB Bridge Controller), ensuring efficient data handling and transmission.
  - Automated the installation and configuration of Xilinx PCIe drivers during Linux boot, establishing stable and persistent PCIe connectivity for enhanced data transfer.

Poomang Corp Seoul, Korea
Backend, DevOps Engineer Jan 2021 – Apr 2021

- **Project: Test-Driven Development(TDD) Implementation for Microservice Architecture**

- Implemented TDD using pytest to ensure stability with new changes and reduce manual testing efforts.
- Developed test cases for legacy code and established a consistent, scalable testing structure, stabilizing previously unreliable parts of the system and enabling future development and server expansion.
- Integrated NoSQL DynamoDB to improve database efficiency and reduce service latency.
- Developed and maintained server-side APIs for managing the "Social Relationship" data of over 2 million users, utilizing Django and Django REST Framework (DRF).

Technical Skills

Programming Languages (Advanced): Verilog/SystemVerilog, C/C++, CUDA Programming, Python
EDA Tools (Advanced): Vivado, Vitis, Vitis HLS, Virtuoso, Pspice, OrCAD PCB Editor
Design Frameworks (Advanced): PyTorch, MMDetection, Django, Django Rest Framework (DRF)

Scholarship

BK21 Scholarship, M.Sc. at Seoul National University (Dec 2023)
University Merit Scholarship for Academic Excellence M.Sc. (Dec 2023)
University Merit Scholarship for Academic Excellence B.Sc. (2016 - 2021, 4 semesters)

Leadership and Activities

Team Leader, CAPP, Seoul National University (SNU) Jan 2023 – Present
- Technical leader of a team of two graduate and three undergraduate students in the design and verification of FPGA and hardware-software co-optimization, successfully completing two government-funded projects within one year.

Lead NPU Hardware Team, Neuro-Reality Vision (NRV Corp) Mar 2022 – Present
- Led the verification of NPU functionality on FPGA and played a key role in the development of DVS camera products and various FPGA evaluation platforms.

CEO, Founding Member, Connect Corp Jan 2021 - Jan 2022
- Setup a company for convenient web based reverse purchasing automation.
- Received a project fund from a large private education institution in South Korea, delivering web based education service.

Languages

English: Fluent (TOEFL 105)
Korean: Native
Chinese: Basic conversational

References

Professor Hyuk Jae Lee, Ph.D.
Department of Electrical and Computer Engineering, Seoul National University
Former Chair Person of IEIE, Institute of Electronics and Information Engineers
Email: hjlee@capp.snu.ac.kr

Professor Jong Ho Lee, Ph.D.
Department of Electrical and Computer Engineering, Seoul National University
Former Minister of Science and Technology of Korea
Email: jhl@snu.ac.kr

Professor Xuan Truong Nguyen, Ph.D.
Department of Next Generation Semiconductor Convergence and Open Sharing System, Seoul National University
Email: truongnx@snu.ac.kr

Professor Hyunsurk Ryu, Ph.D.
Department of Next Generation Semiconductor Convergence and Open Sharing System, Seoul National University
CEO of Neuro-Reality Vision Corporation
Former Master of Samsung Electronics, System LSI Business Division
Email: eric.ryu@snu.ac.kr