

디지털 -> 디지털 이더넷

아날로그 -> 디지털 wifi, pc통신, LTE, 5G

디지털-> 아날로그

아날로그 -> 아날로그 라디오

Data Communications

-Digital Transmission (1)-

Ethernet
 $\begin{bmatrix} D \\ A \end{bmatrix} \text{ Data} \Rightarrow \text{Signal} \begin{bmatrix} D \\ A \end{bmatrix}$ *호신 부호화* : 디지털 데이터를 전송하기 위한 신호를 변환하는 기술

2024. 10. 15

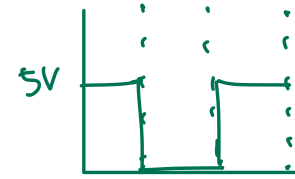
Young Deok Park (박영덕)

Line Coding

회선 부호화

디지털신호를 만드는 기법

1011
1: +5V
0: 0V



- Converting a string of 1's and 0's (digital data) into a sequence of signals that denote the 1's and 0's

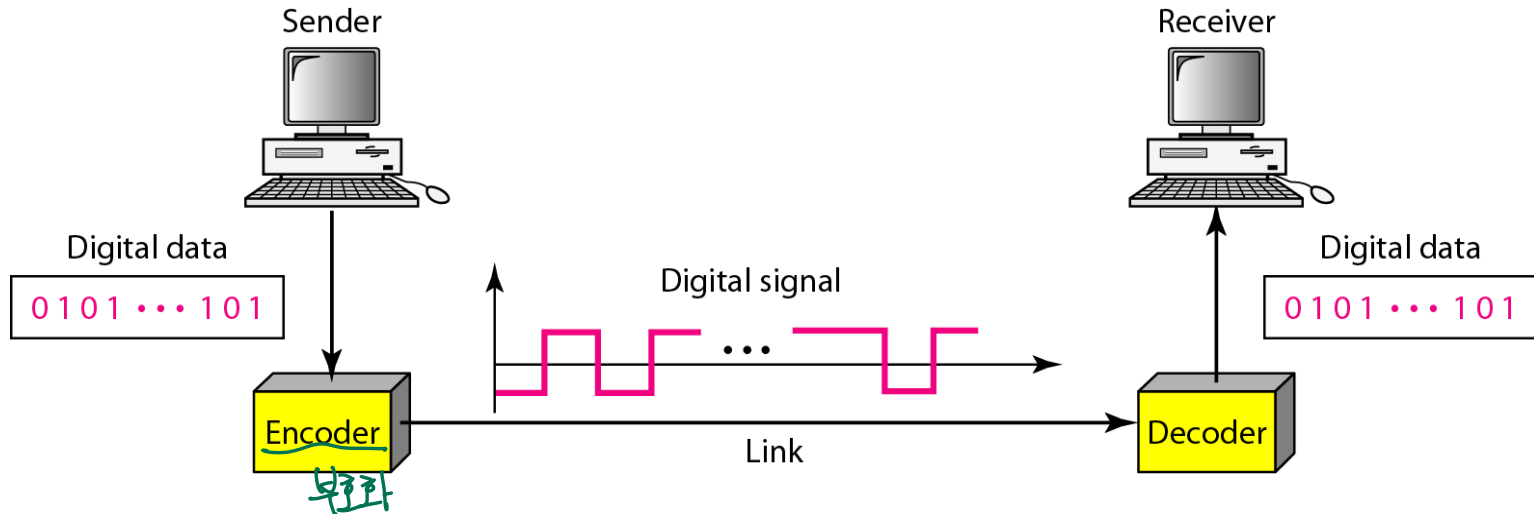
나타내는

Example

- A high voltage level (+V) could represent a "1" and a low voltage level (0 or -V) could represent a "0"

고전압

저전압



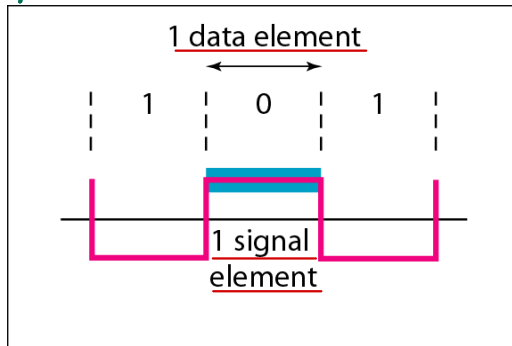
Data Element vs Signal Element

bandwidth, bitrate 비례 관계

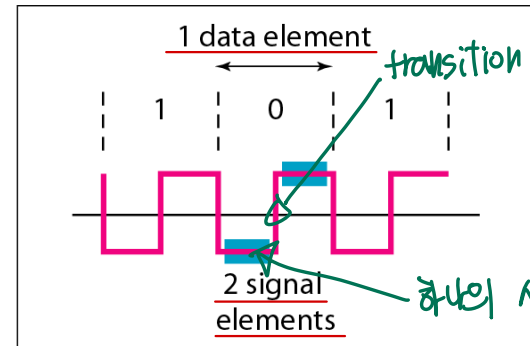
transition 하는 데 bandwidth 2배 더 필요

resource를 많이 잡아먹음 bandwidth = 2

3 bandwidth = 1

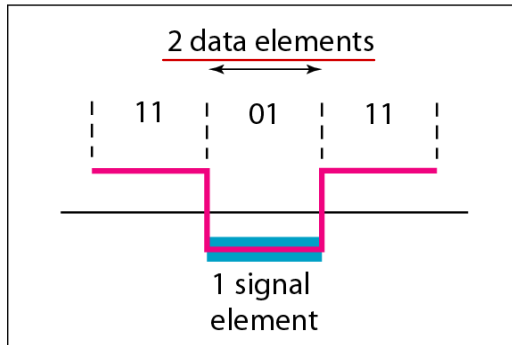


a. One data element per one signal element ($r = 1$)
bandwidth = 1/2

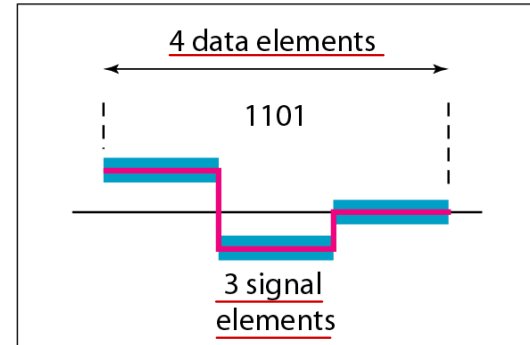


b. One data element per two signal elements ($r = \frac{1}{2}$)
bandwidth = 3/4

data element
signal element



c. Two data elements per one signal element ($r = 2$)



d. Four data elements per three signal elements ($r = \frac{4}{3}$)

Considerations

고저사상

평균 0 : 양의음으로 편향

평균이 0이 아닐때 존재

1 : +5V

0 : 0V

평균 2.5V

DC0

1 : 5V

-1 : -5V

평균 0V

DCX

전압이 일정유지가 되어야함

0V는 전압이 안걸려있기 때문에 X

■ DC components 직류성분

구현이

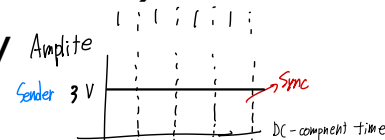
- When the voltage level remains constant for long periods of time, there is an zero frequency of the signal (DC component) 장시간

- Some devices may not support the zero frequency 신호의 주파수

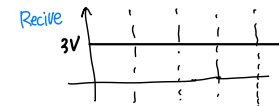
- Encoding scheme without DC component is better 자유V

방식

없는



타이밍을 맞추



동기화에 문제 :
Clock을 강제하여야 하는지
기준이 없어서 동기화를
해줄 방법이 없는지
22444 Syll의 문제가 발생

■ Synchronization 동기화

- To correctly interpret the signals received from the sender, the receiver's bit intervals must correspond 수신자 송신자

수신자

간격

■ Bandwidth

- A encoding scheme requiring less bandwidth is better

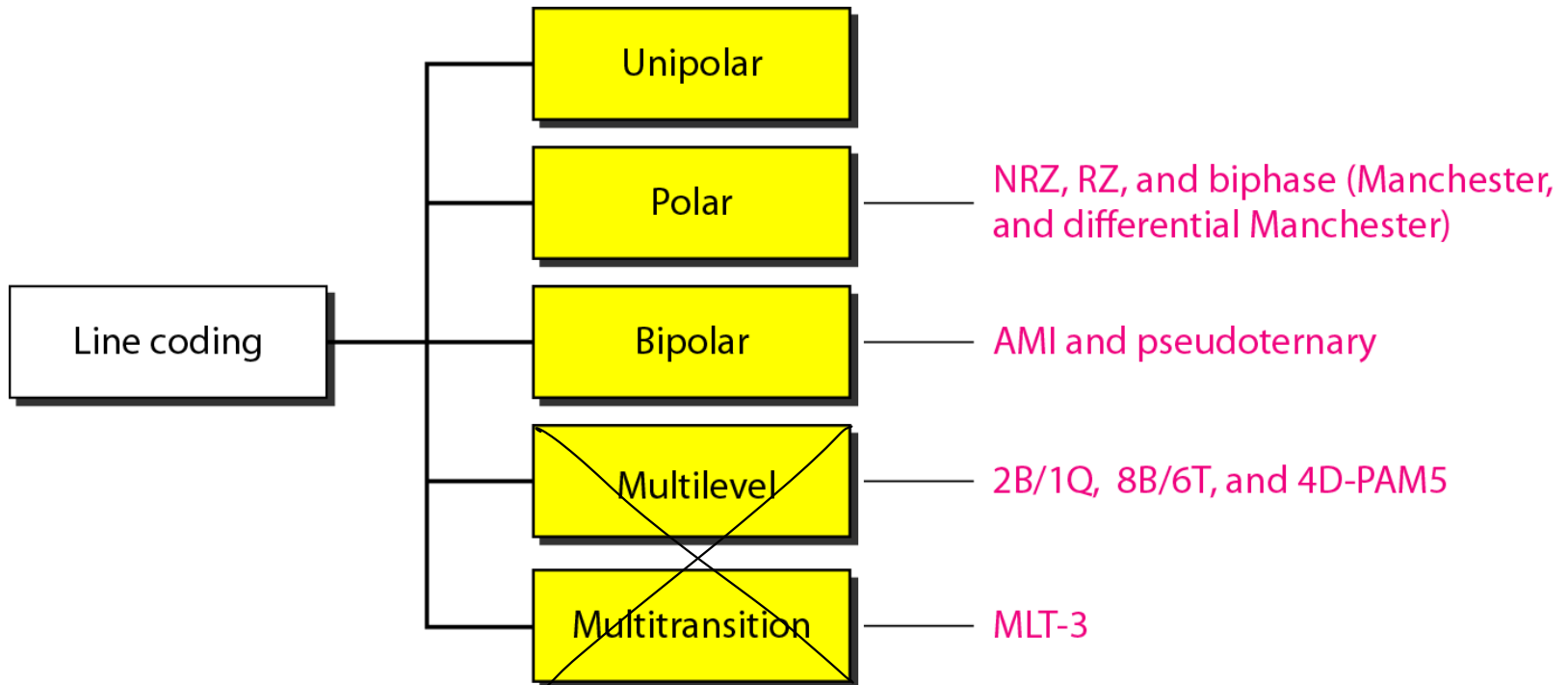
필요V

본

데이터를 전송할 수 있는 최대 용량

초당 비트수, Hz

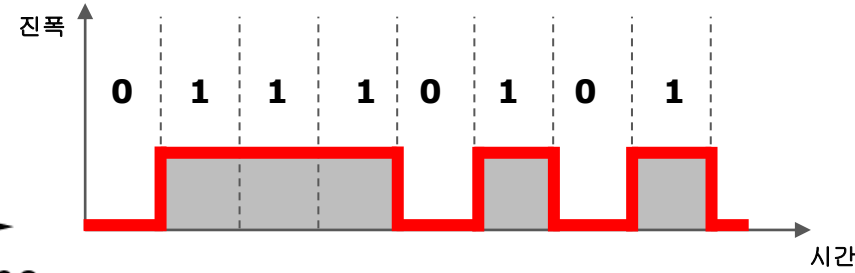
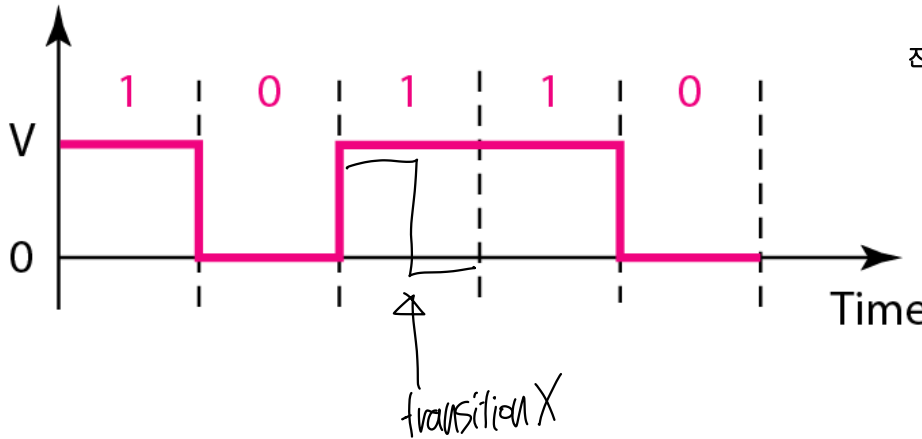
Line Coding Schemes



Unipolar

단극형 (+ or - 하나만 사용해서 표현)

Amplitude



DC component ○
Synchronization X
Bandwidth ↓

- All signal levels are on one side of the time axis - either above or below
아래(음수) : 신호의 전압 레벨이 시간 축의 한쪽에서만 나타남

- Unipolar scheme has DC component

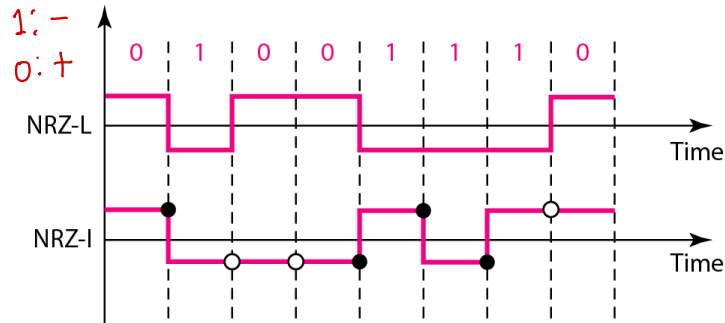
- It has no synchronization capacity
기능

Bandwidth ↓

Polar – NRZ (Non-Return to Zero)

극형

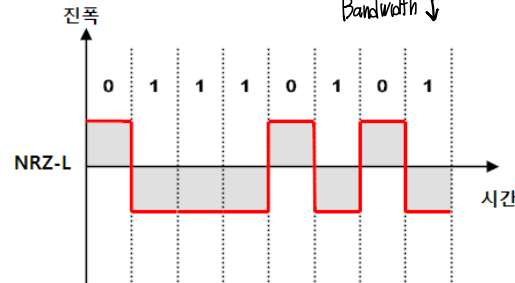
항상 1이거나 0일 때 발생



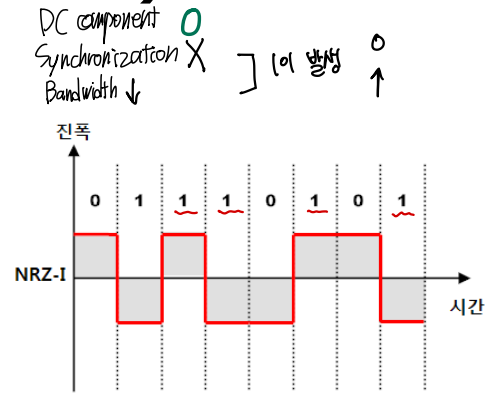
○ No inversion: 0

● Inversion: 1

(이나오면 inversion)



(+) 전압은 0, (-) 전압은 1

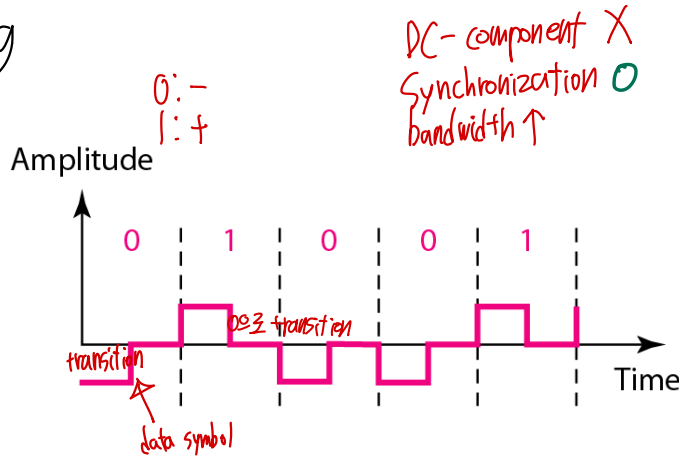


다음 비트가 1이 올 때 신호의 전이가 발생

- The voltages are on both sides of the time axis
전압 양쪽에
- Polar NRZ scheme can be implemented with two voltages
 - E.g. +V for 1 and -V for 0
- Two versions:
 - NRZ - Level (NRZ-L): positive voltage for one symbol and negative for the other
양전압 위계 기호 음전압
 - NRZ - Inversion (NRZ-I): the change or lack of change in polarity determines the value of a symbol
변화 변화X 전압
 - E.g. a "1" symbol inverts the polarity a "0" does not
반전 전압

Polar – RZ (Return to Zero)

self clocking



- The Return to Zero (RZ) scheme uses three voltage values. +, 0, -.
- Each symbol has a transition in the middle. Either from high to zero or from low to zero.
 각 기호 (per symbol) 전압 (voltage) 둘중 하나 (one of two) high → 0
- This scheme has more signal transitions (two per data symbol) and therefore requires a wider bandwidth.
 필요 (needed) 넓은 (wide)
- No DC component
- Synchronization - transition indicates symbol value.
 전환 (switch) 나타나다 (appear) 기호값 (symbol value)
- More complex as it uses three voltage levels
 manchester 보다 복잡 (more complex than Manchester)

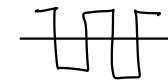
Polar – Manchester and Differential Manchester

DC component X
Synchronization O
Band Width ↑

■ Manchester encoding

- Combining the NRZ-L and RZ schemes
- Every ^{변화}symbol has a level transition in the middle: from high to low or low to high (similar to RZ)
- Uses only two voltage levels (similar to NRZ-L)

low → high high → low



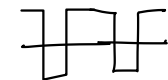
■ Differential Manchester encoding

- ^{차등}Combining the NRZ-I and RZ schemes
- Every symbol has a level transition in the middle (similar to RZ)
- But the level at the beginning of the symbol is determined by the symbol value. / One symbol causes a level change the other does not (similar to NRZ-I)

DC component X
Synchronization O
Band Width ↑



| 1일 때 비트 시작 부분에서 전압이 변화, 0일 때 시작 부분에서 전압 유지

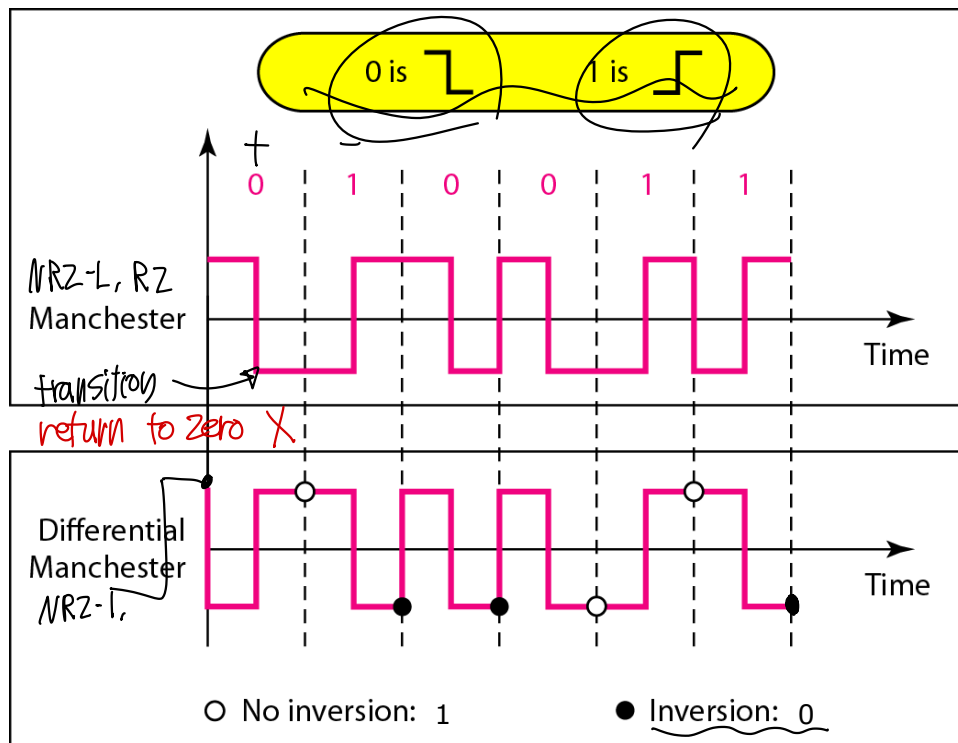


- Manchester/Differential Manchester have more signal transitions (two per symbol) and therefore **require a wider bandwidth than NRZ**
- No DC component**
- Synchronization** - transition indicates symbol value

Polar – Manchester and Differential Manchester

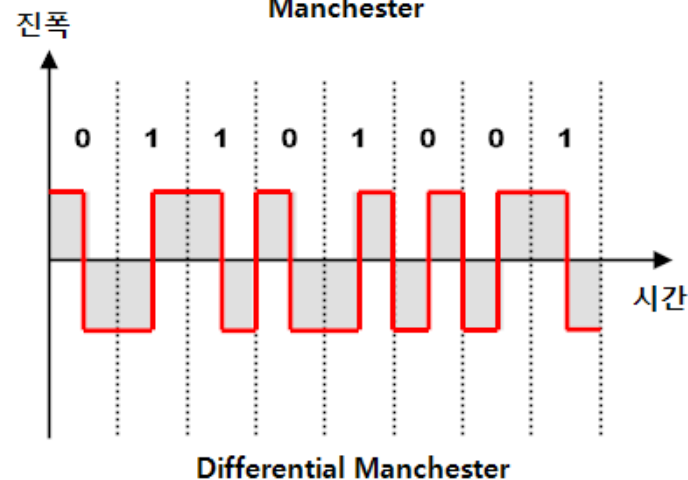
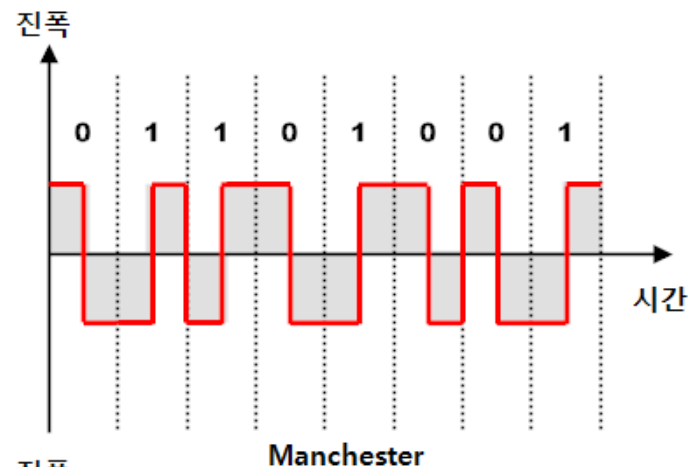
DC X 항상 전위

bandwidth return to zero =



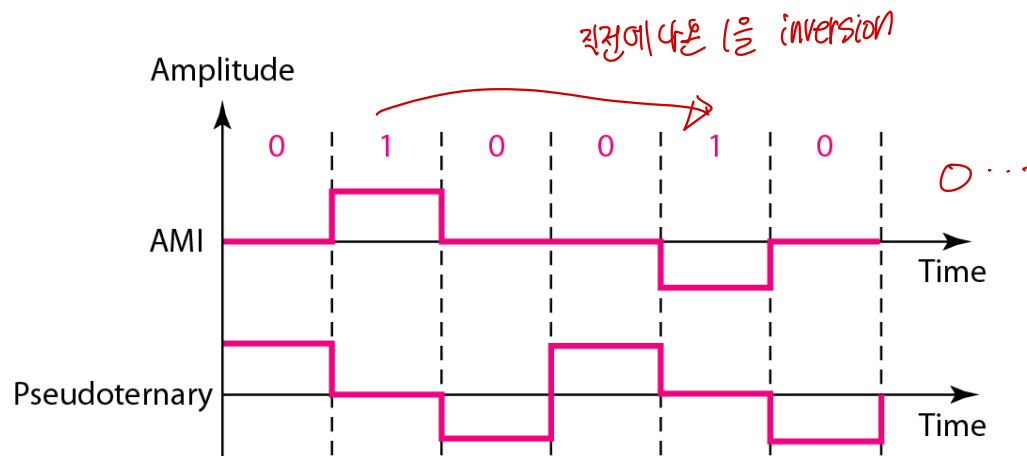
직전 전류 유지

유지 X



Bipolar – AMI and Pseudoternary

- Code uses 3 voltage levels: +, 0, -, to represent the symbols (not transitions to zero as in RZ)
- Voltage level for one symbol is at "0" / and the other alternates between + & -
- Alternate Mark Inversion (AMI) - the "0" symbol is represented by zero voltage and the "1" symbol alternates between +V and -V
- Pseudoternary is the reverse of AMI



0: 0V
1: +, -

DC-component X
SY 문제
bandwidth 작음

- DC component? X
- Synchronization? O

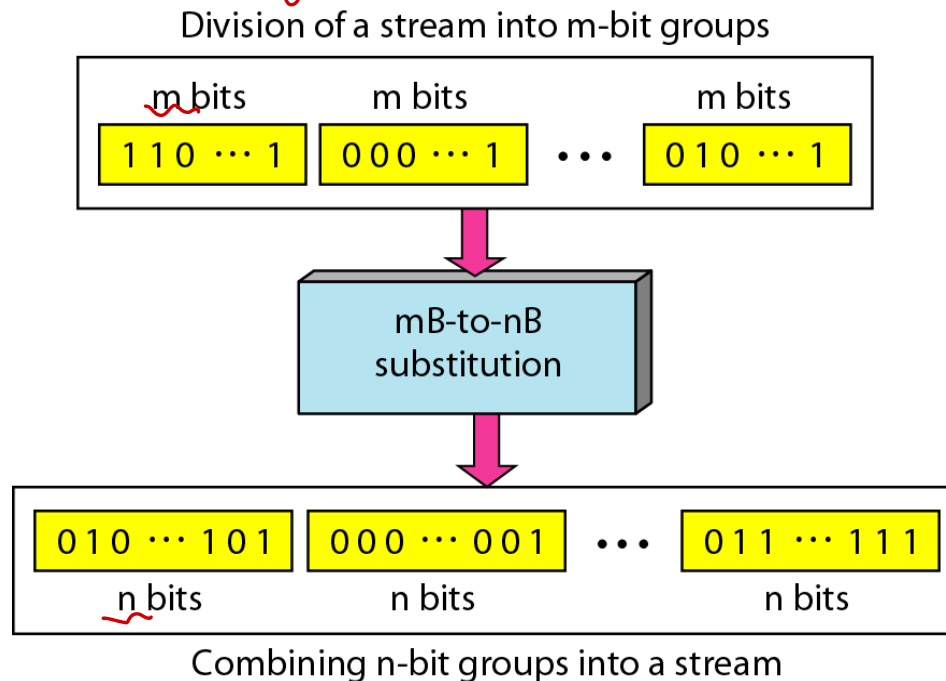
bandwidth ↓

Block Coding *Sy* 원리

- Block coding is normally referred to as mB/nB coding
- It replaces each m-bit group with an n-bit group *지정된다*
- 4B/5B encoding: resolve synchronization issue of NRZ-I (long 0s)
라인화 하다 = encoding

DC-component ??
Sy 문제 bandwidth
0
↑

*4B로 구성된것을
5B로 치환한다.*



Block Coding

4B/5B mapping codes

장점

동기화유지: 추가된 비트 패턴
1과 0의 전환

DC 성분 제거: 0, 1 패턴 조정

평균전압 0
→ DC 성분 해결

단점

대역폭 비효율: 추가된 비트로 인해
대역폭 증가

복잡한 변환 과정: 원본 데이터를 변환할 때
복잡한 연산

10100

제한

데이터 비트 (4비트)	코드 비트 (5비트)	NRZI
0000	11110	
0001	01001	
0010	10100	
0011	10101	
0100	01010	
0101	01011	
0110	01110	
0111	01111	
1000	10010	
1001	10011	
1010	10110	
1011	10111	
1100	11010	
1101	11011	
1110	11100	
1111	11101	

0이 연속되는 횟수는 최대 3번 → SYNC

0연속 크게 문제X

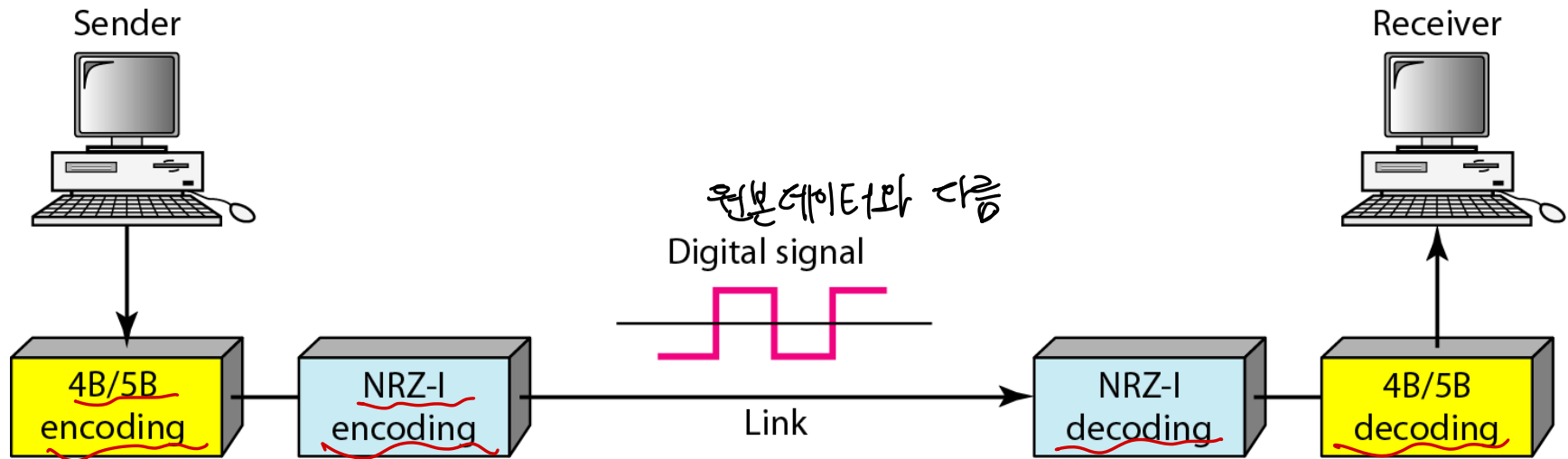
동기화가 완화되는 이유

동기화 문제는 연속된 동일한 비트 패턴으로 인해 발생
block coding은 전환이 없는 연속적인 패턴을 피하도록 설계
연속된 0 or 동일한 비트 패턴이 크게 이어지지 X

DC-component 해결X

0000 → 11110
0001 → 01001
0010 → 10100
0011 → 10101
0100 → 01010
0101 → 01011
0110 → 01110
0111 → 01111
1000 → 10010
1001 → 10011
1010 → 10110
1011 → 10111
1100 → 11010
1101 → 11011
1110 → 11100
1111 → 11101

Block Coding



NRZ-I (0 연속일 때)
동기화 문제, 단점 보완

Scrambling

DC-component 0
Sy 문제 0
bandwidth ↓

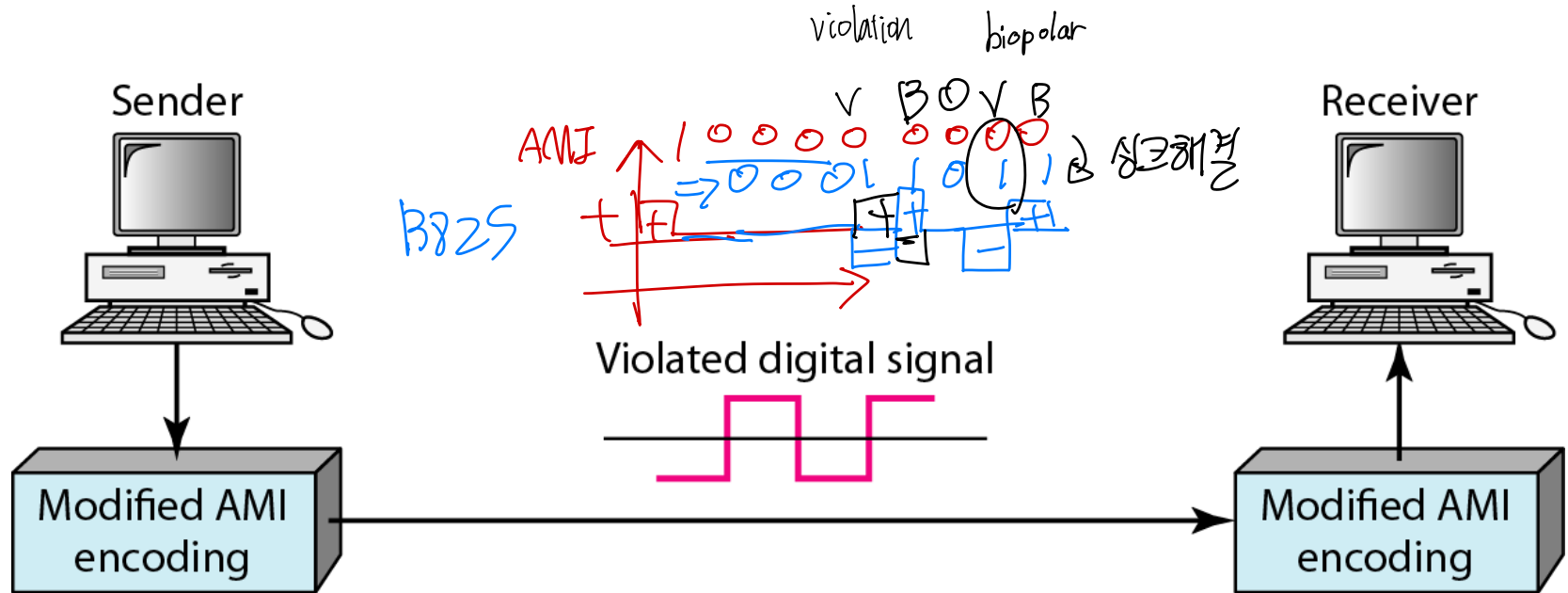
block-coding처럼 안쓰임

기법 불려서 사용

[AMI violation 구분X

-일부러 violation 추가 규칙을 깨고 정보를 변형하는 패턴
→ 동기화 문제 해결

- The best code is one that does not increase the bandwidth for synchronization/and has no DC components
제거하지 않는다
- Scrambling is a technique used to create a sequence of bits that has the required features - synchronization, no DC components, no wide bandwidth

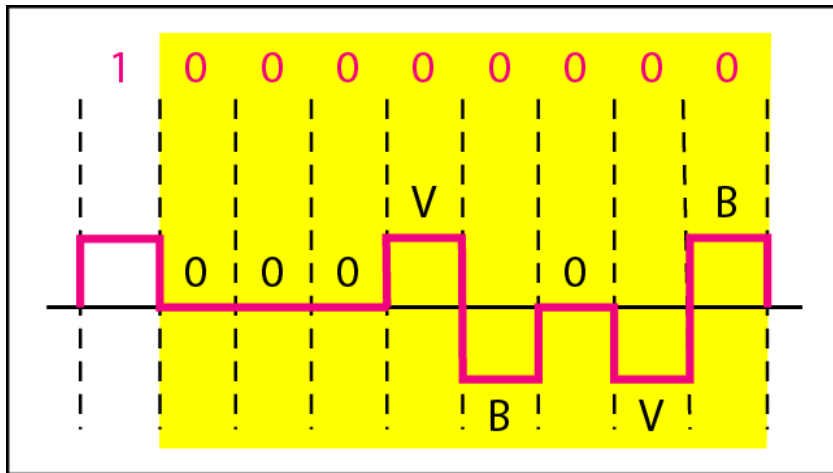


Scrambling – B8ZS (복합) AMI 단점 보완

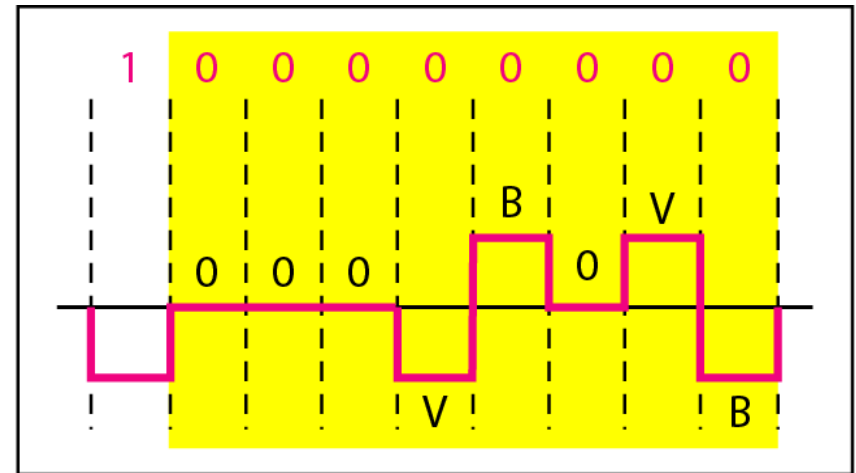
■ Bipolar with 8-zero substitution

- Eight consecutive zero-level voltages are replaced by the sequence 000VB0VB

- V: violation 위반
 - ✓ Non-zero voltage that breaks an AMI rule of encoding (opposite polarity from the previous) 전압 반대 극성 이권다
- B: bipolar 양극성 양극성
 - ✓ Non-zero voltage in accordance with the AMI rule 다른



a. Previous level is positive.



b. Previous level is negative.

장점 : 동기화 문제 해결, 전압 변화를 인위적으로 삽입 → 동기화 문제 해결
 DC성분 제거 연속된 특정 패턴 방지
 대역폭 증가 기존 신호 변형 X, 특정 패턴 나올때만 전압 변화 추가

단점 : 오류 감지 기능 부족 전압 변화만으로 삽입
 복잡한 수신 처리 Scrambling 패턴을 복원하는 과정이 복잡
 비트 패턴 왜곡 원래 데이터 패턴 왜곡