

MID SEMESTER EXAMINATION, September-2016

IT-403: Compiler and Translator Design

Time: 1:30 Hrs

Max. Marks: 20

Note: All questions are compulsory. Assume suitable missing data, if any.

1. Distinguish between compiler and interpreter bringing out clearly the situations in which each of them is more suitable than the other. [4]

2. (a) Consider the below grammar:

$S \rightarrow aB \mid ab$

$A \rightarrow aAB \mid a$

$B \rightarrow ABb \mid b$

Show that this grammar is ambiguous. [2]

- (b) Design a DFA that accepts all strings on $\{0, 1\}$ except those containing substring 011. [2]

3. Construct NFA for the following regular expression using Thompson's construction.

$(a \mid b)^*abb$

Construct the corresponding DFA from the above NFA [4]

4. Consider the following program:

```
int main ()
```

```
{
```

```
    int x, y, z;
```

```
    z = x + y*10;
```

```
}
```

List down the lexemes, tokens and the attributes of the tokens, at the end of the lexical analysis of the above program. [4]

5. Consider the following grammar for regular expressions.

$R \rightarrow R' \mid 'R \mid RR \mid R^* \mid (R) \mid a \mid b$

Modify the grammar to make it LL(1). Generate the predictive parsing table for the resulting grammar. [4]

Total No. of Pages: 1
SEVENTH SEMESTER

Roll No.:
BE(IT)

MID SEMESTER EXAMINATION, September 2016
IT-402: DISTRIBUTED SYSTEMS & COMPUTING

Time: 1½ hrs.

Max. Marks:20

Note: Attempt all questions.

1. What is Inter Process Communication? Discuss the message format that is used to implement IPC using message queues.
 2. Differentiate between the following:
(c) Monolithic kernel and Microkernel.
(d) Pipe and FIFO.
 3. List the various forms of transparency identified by the ISO reference model for distributed systems. Discuss at least two of them. Is complete transparency achievable?
 4. How much replication will be enough for a system to be *k-fault tolerant* to handle fail-stop failures and Byzantine failures? Justify your answer.
 5. Explain the blocking and non-blocking semantics used for synchronization in DCS. Discuss in the context of send/receive primitives.
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Total No. of Page(s): 1
SEVENTH SEMESTER

Roll No.
B.E. (IT)

B.E. MID SEM. EXAMINATION, SEPTEMBER-2016
Internet and Web Engineering (IT-401)

Time: 1:30 Hrs.
Max. Marks: 20

Note: Attempt ALL questions.

1. List some attributes of WebApps which make them different from the attributes of conventional software? (3)
2. Explains the steps required for developing a Web Application? (3)
3. Discuss in brief the following: (3*2=6)
 - (i) How does MIME enhance SMTP
 - (ii) Best effort delivery service
 - (iii) Categories of user WebApps
4. How ARP packet is transferred from source to destination? (3)
5. What is the difference between port address, logical address, physical address and gateway address? (2)
6. Two computers C1 and C2 are configured as follows. C1 has IP address 203.197.2.53 and netmask 255.255.128.0. C2 has IP address 203.197.75.201 and netmask 255.255.192.0. Check whether they are on same network or not? (3)

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Total No. Of page:1

Roll No. _____

B.E. MID SEMESTER EXAMINATION September, 2016
IT-404: Soft Computing & Neural Networks

Time: 1.30 Hours

Max. Marks: 20

Note: Assume suitable missing data, if any.
All questions are compulsory.

Q1. a. Draw a comparison between Hard Computing and Soft Computing techniques.

b. What is a squashing function? Explain different types of squashing functions.

(2*2.5=5 Marks)

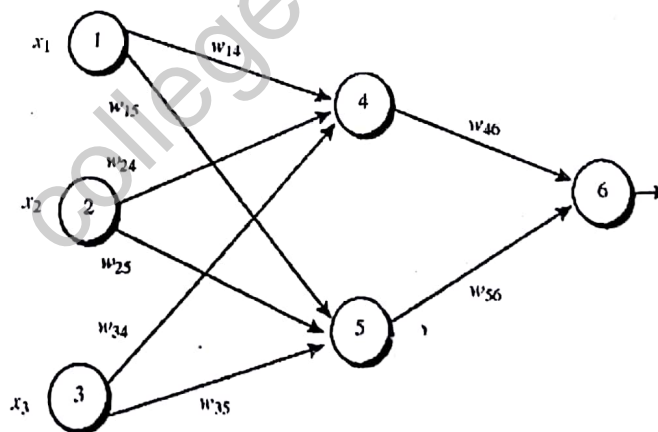
Q2. a. Find the weights required to perform the following classification using perceptron network with initial weights as zero and learning rate as one. The vectors (1,1,-1,-1) and (1,-1,1,-1) belong to class 1 (target value is +1) and vectors (-1,-1,-1,1) and (-1,-1,1,1) belong to class 2 (target value is -1).

b. Implement NOR function with bipolar inputs and targets using Hebb algorithm.

(2*2.5=5 Marks)

Q3. a. Explain the concept of linear separability with respect to artificial neural networks. (2 Marks)

b. Use backpropagation algorithm to update the weights " w_{46} " and " w_{56} " in the following architecture. Assume that the learning rate is 0.9 and the training example is (1,0,1) with class label +1. The initial weights are ($w_{14}, w_{15}, w_{24}, w_{25}, w_{34}, w_{35}, w_{46}, w_{56}$) = (0.2, -0.3, 0.4, 0.1, -0.5, 0.2, -0.3, -0.2). Use unipolar sigmoidal activation function.



(3 Marks)

Q4. Write short notes on any two of the following:

(2*2.5=5 Marks)

- Mc Culloch Pitts Model
- Madaline Networks
- Different types of learnings

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Total No. Pages: 1

Roll No. -----

SEVENTH SEMESTER

B.E. (IT)

MID SEMESTER EXAMINATION, September-2016

IT-404: Elective-II (IT in Marketing Management)

Time: 1:30 Hrs

Max. Marks: 20

Note: All questions are compulsory. Assume suitable missing data, if any.

1. What is consumer behavior? Elaborate the different types of purchase behavior in the purchase of a product, giving suitable two examples. [5]
2. Differentiate between Product concept, Selling Concept and social marketing concept. [5]
3. Write short notes on the following: [2.5x4= 10]
 - (a) Ethical issues in marketing
 - (b) Sales promotion schemes (with examples)
 - (c) Market Segmentation
 - (d) Digital Marketing

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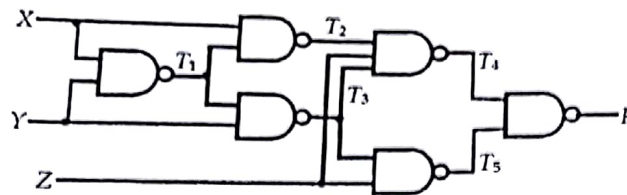
BE (Information Technology) VII SEMESTER
B.E MID SEMESTER EXAMINATION, SEPTEMBER- 2016
IT-405: ADVANCES IN DIGITAL SYSTEM DESIGN
 Max.Marks:20

(167)

Time: 1.30 Hours

Note: Attempt all questions. Assume suitable missing data, if any.

Q.1 Obtain the truth table for the circuit shown below. Draw an equivalent circuit for F with fewer NAND gates. (2)



OR

Q.1) Given the Boolean function $F = xy'z + x'y'z + w'xy + wx'y + wxy$

- Obtain the truth table of the function.
- Draw the gate structure using the original Boolean expression.
- Simplify the function to a minimum number of literals using Boolean algebra.
- Obtain the truth table of the function from the simplified expression and show that it is the same as the one in part (a)
- Draw the gate structure from the simplified expression and compare the total number of gates with the diagram of part (b) (2)

Q.2) Give an algorithmically designed Combinational circuit for 4-bit comparator. Also explain the step involved in designing the algorithm. (3)

Q.3) Complete the design of the BCD-to-seven-segment decoder by performing the following steps.

- Plot the seven maps for the outputs
- Simplify the seven output functions in sum of products form, and determine the total number of gates that will be needed to implement the decoder.
- Verify that the seven output functions give a valid simplification. Compare the number of gates with that obtained in (b). (3)

Q.4) Many offices and buildings use combination locks to control entry. As the design engineer of the Wonderful Door Security Company, you are asked to implement a door security system by using a card reader. There are four inputs to the card reader: inputs X, Y, and Z are used to validate the correct door code, and input V is used to check if the card reader is still valid. After the card reader is being read by the system, there are three outputs to this system: alarm (A), door open (D), and Error (E). Door (D) will only open when the decimal value of the binary inputs (x, y, z) is odd AND the card reader is valid. The Error (E) signal goes on when the code on the card is correct (i.e. decimal value equal to odd) but the card is no longer valid. Finally, the alarm (A) will trigger when the code is incorrect. Show your final design in canonical product of sum form. (3)

Q.5) Design a PLA as 4X4X2 to implement the following two Boolean functions. Minimize the number of product terms. Show all your work, including the Karnaugh maps used in the minimization.

$$F1(A,B,C,D) = \sum(1, 3, 4, 5, 7, 13, 15)$$

$$F2(A,B,C,D) = \sum(0, 2, 3, 6, 7, 8, 10, 11, 12, 14)$$

(3)

Q.6) Explain the performance issues related to static interconnection networks. (3)

Q.7) Solve any TWO

- Explain Flynn's classification of Computer Architecture. (1.5)
- Provide a list of the main advantages and disadvantages of shared-memory and message-passing paradigm. (1.5)
- Write short note on PAL, GAL and FPGA. (1.5)

END