

0 1 3 2

13.8.18

## Advances in Digital System Design

$$F = A + \overline{B}\overline{C}$$

draws the truth table

	F	A	B	C	$\overline{C}$	$\overline{B}\overline{C}$
0	0	0	0	0	1	1
1	0	0	0	1	0	0
2	0	0	1	0	1	1
3	0	0	1	1	0	0
4	1	1	0	0	1	0
5	1	1	0	1	0	0
6	1	1	1	0	1	1
7	1	1	1	1	0	0

draws the K-map and show

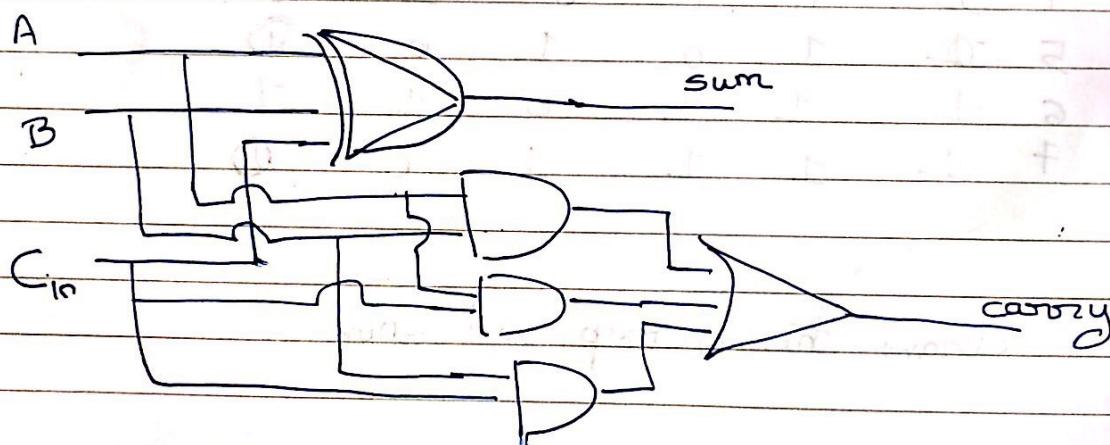
		$\overline{BC}$	00	01	11	10
		MSB to LSB	0	1	1	1
A	B	0				
		1	1	1	1	1

$$F = A + \overline{B}\overline{C}$$

D, D D

## Q 1 bit Full Adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Carry	BC <sub>00</sub>	BC <sub>01</sub>	BC <sub>11</sub>	BC <sub>10</sub>
0	1	1	1	0
1	1	1	1	1

$$AC + AB + BC$$

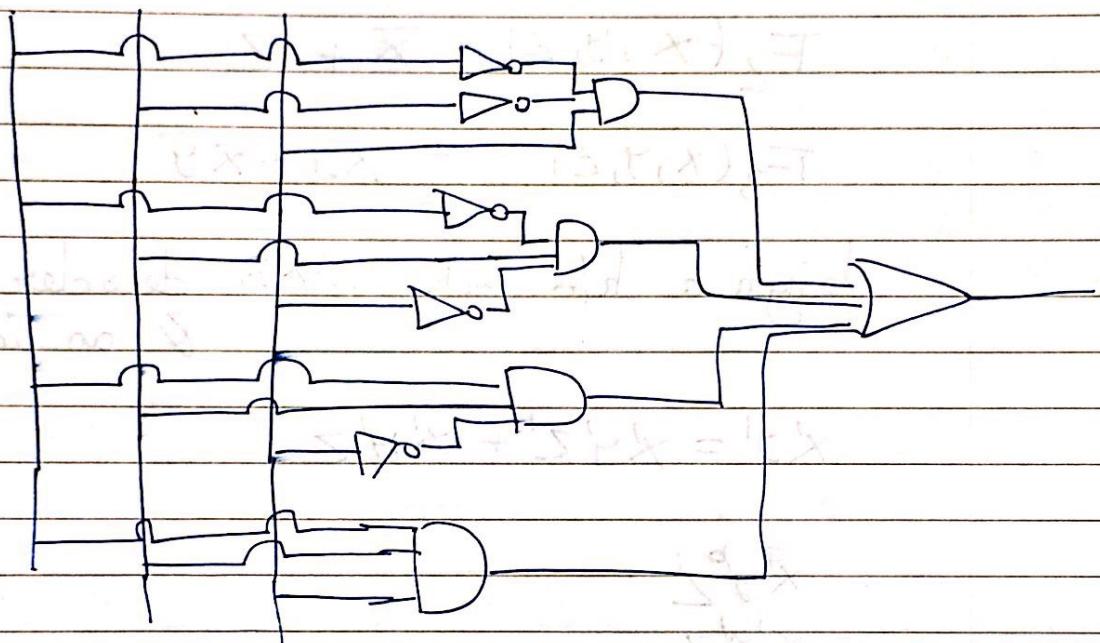
adder

00	01	11	10
0	1	1	1
1	1	1	1

0 0 0  
 0 1 1 0 1  
 1 0 0 1 1  
 1 1 0 0 0

$$\Rightarrow \overline{A} \overline{B} C + \overline{A} B \overline{C} + A \overline{B} \overline{C} + A B C$$

A B C



$$\Rightarrow A(\overline{B}\overline{C} + BC) + \overline{A}(\overline{B}\overline{C} + B\overline{C})$$

$$\Rightarrow A(\overline{B} \oplus C) + \overline{A} (B \oplus C)$$

$A \oplus B \oplus C$

g

A combinational ckt is defined by

$$F_1(x, y, z) = \overline{x}\overline{y} + xy\overline{z}$$

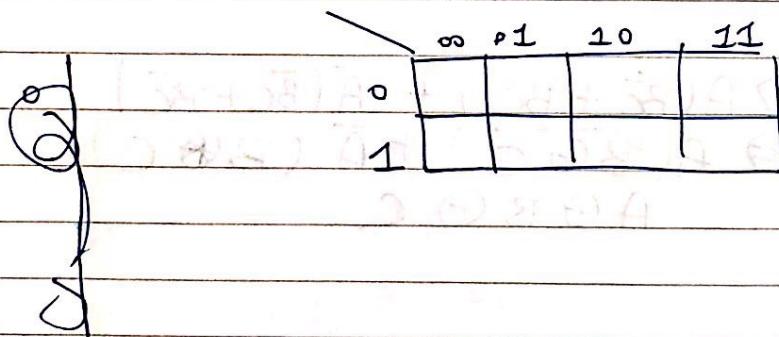
$$F_2(x, y, z) = \overline{x} + z$$

$$F_3(x, y, z) = xy + \overline{x}\overline{y}$$

design a h/lw with 3x8 decoder, 4 Z/p or & an inverter

$$x'y' = x'y'z' + x'y'z$$

$$\begin{array}{c} \oplus \\ \times y' \\ \hline z' \\ \times y' \\ \hline z \end{array}$$



$$F_1 \Rightarrow \overline{x}\overline{y} + xy\overline{z}$$

$$x \quad y \quad z \quad \overline{x}\overline{y}$$

$$\begin{aligned} & X'Z + X'Z' \\ & X'Z + X'Z' \end{aligned}$$

81.8.4

X	Y	Z	$\bar{X}\bar{Y}$	$X\bar{Y}Z$	$X'Y$	$X'Y'$
0	0	0	1	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	1	0
1	1	1	0	0	1	0

$\bar{Y}Z$	$\bar{Y}Z'$	11	10
0	(1 1)		
1		(1)	

$$\Rightarrow \bar{X}\bar{Y} + \cancel{X\bar{Y}Z}$$

$F_3$

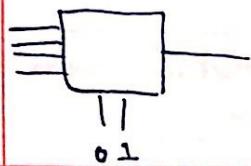
00	01	11	10
0	(1 1)		
1		(1 1)	

$$F_3 \Rightarrow \cancel{\bar{X}Y + X\bar{Y}} \quad \bar{X}\bar{Y} + X\bar{Y}$$

$$F_1 = \textcircled{1} X'Y'Z + \textcircled{2} X'Y'Z' + \textcircled{3} X'YZ'$$

$$F_2 = X'YZ + \textcircled{2} X'Y'Z' + \textcircled{4} \cancel{X'Y'Z} + \textcircled{2} X'Y'Z$$

$$F_3 = \textcircled{1} X\bar{Y}Z + \textcircled{3} X\bar{Y}Z' + \textcircled{2} \cancel{X\bar{Y}Z} + \textcircled{2} \cancel{X\bar{Y}Z'}$$



~~CD~~

~~D~~

$$C + \bar{C}D$$

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Q implement the boolean function  $F(A, B, C, D) = \sum m(4, 6, 7, 8, 12, 15)$   
with  $4 \times 1$  MUX & external gates

		CD	A	00	01	11	10
			00	.	.	.	.
			01	1	1	1	1
			11	1	1	1	1
			10	1			

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

$$\Rightarrow B\bar{C}\bar{D} + A\bar{C}\bar{D} + BCD + \bar{A}BC$$

$$\Rightarrow \bar{C}\bar{D}(A+B) + BC(\bar{A}+D)$$

A	B	C	D	F
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	1
9	1	0	0	0
10	1	0	1	0
11	1	0	1	1
12	1	1	0	1
13	1	1	0	0
14	1	1	1	0
15	1	1	1	1

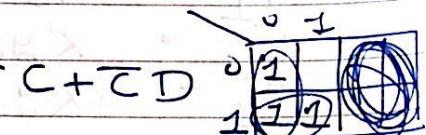
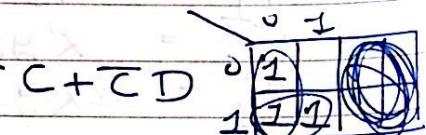
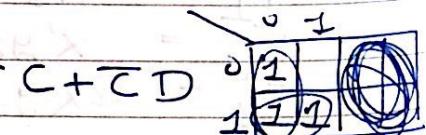
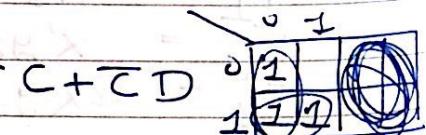
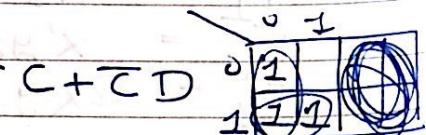
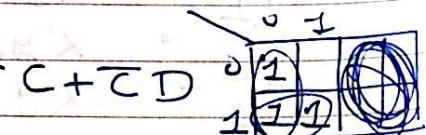
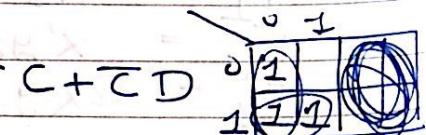
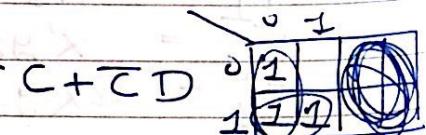
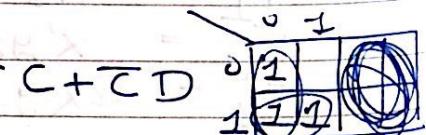
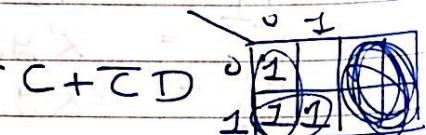
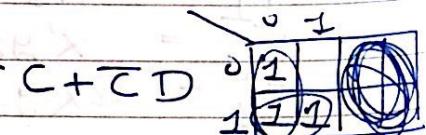
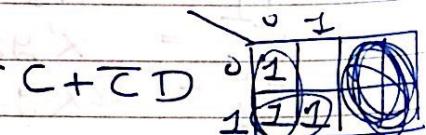
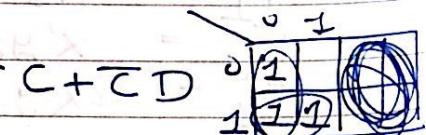
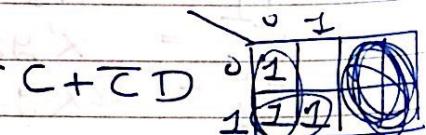
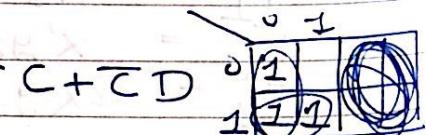
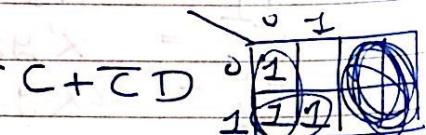
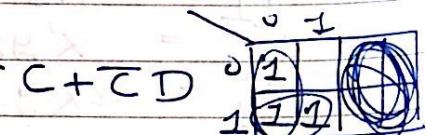
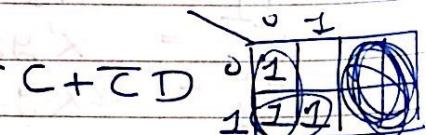
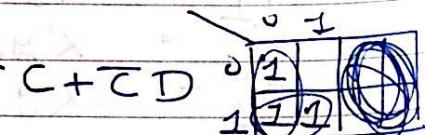
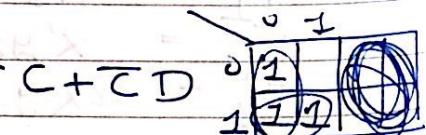
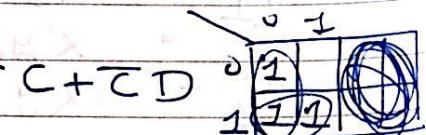
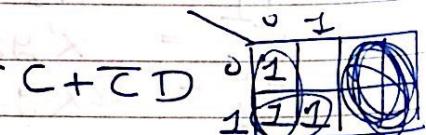
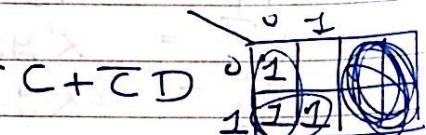
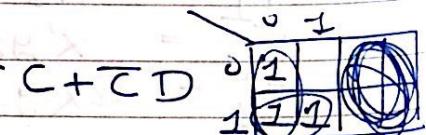
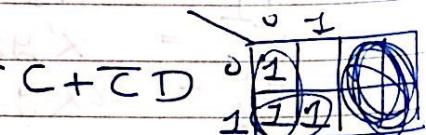
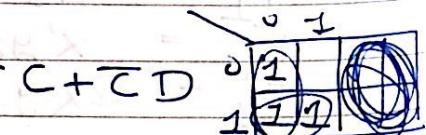
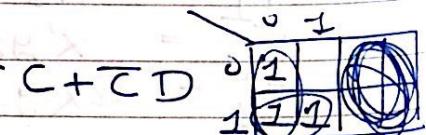
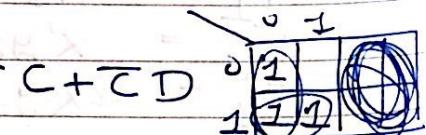
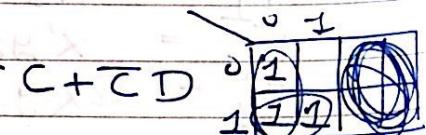
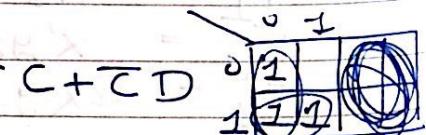
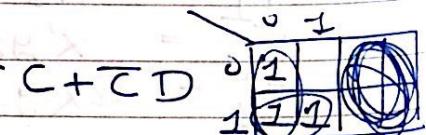
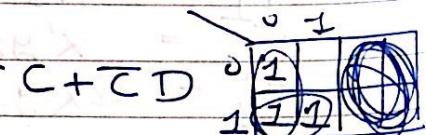
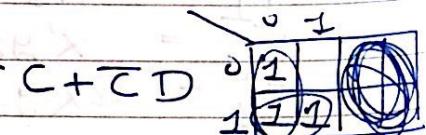
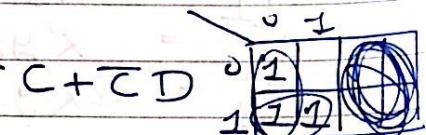
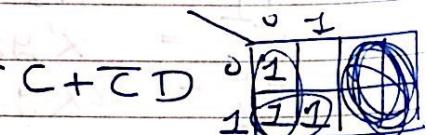
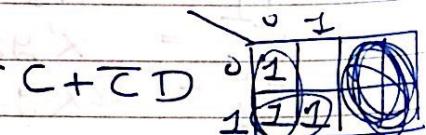
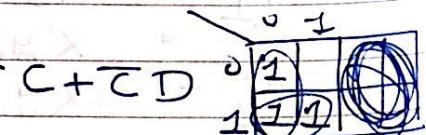
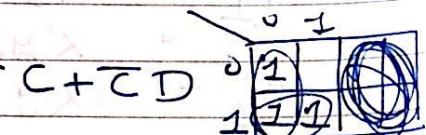
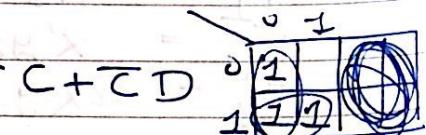
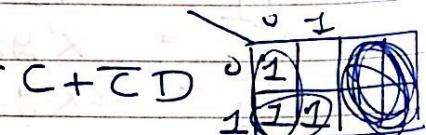
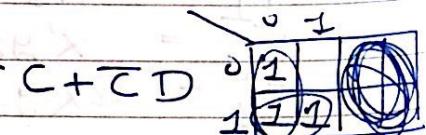
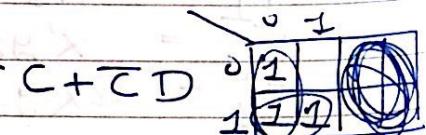
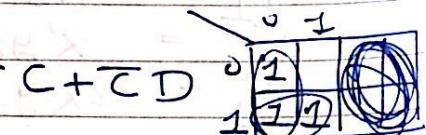
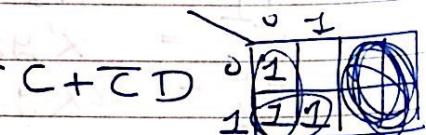
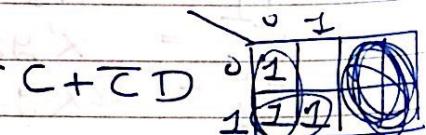
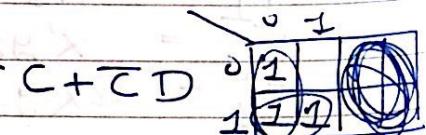
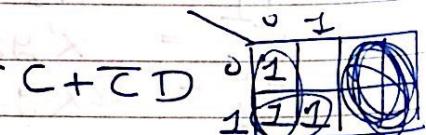
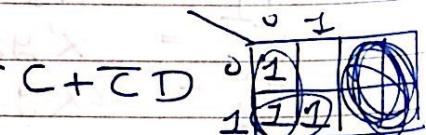
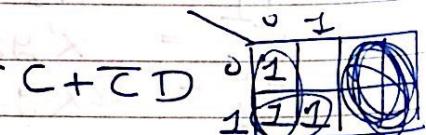
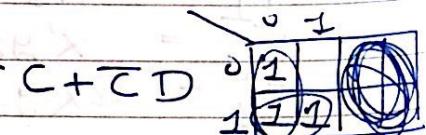
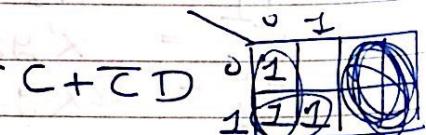
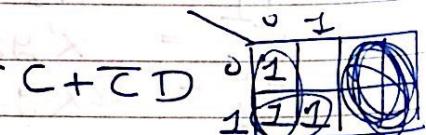
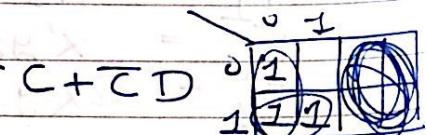
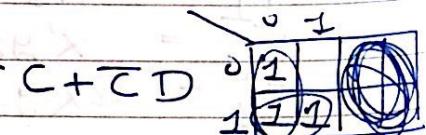
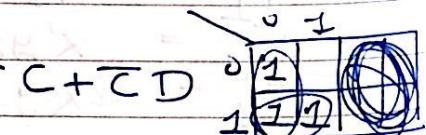
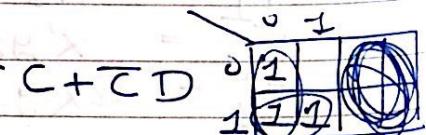
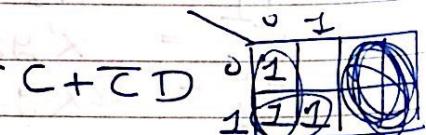
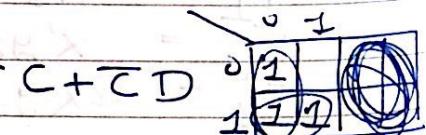
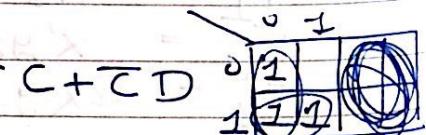
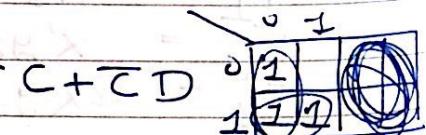
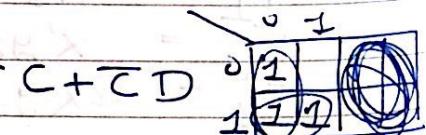
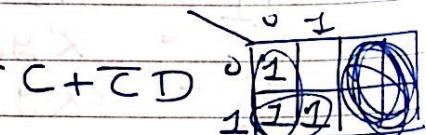
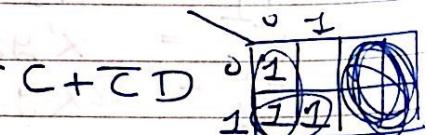
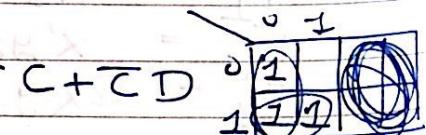
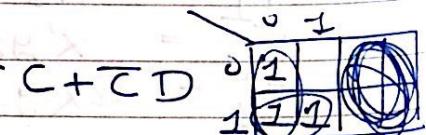
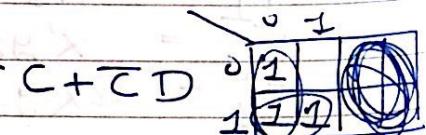
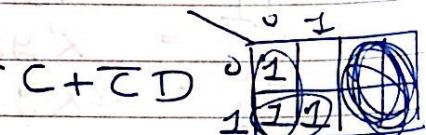
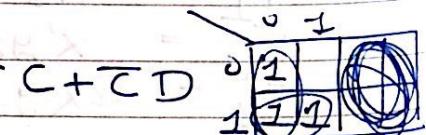
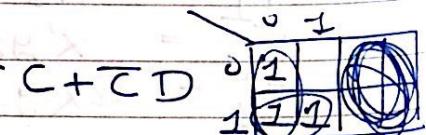
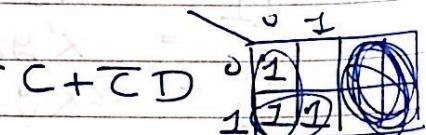
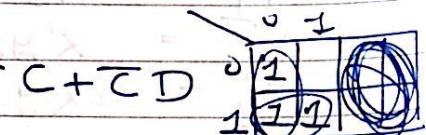
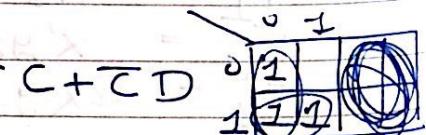
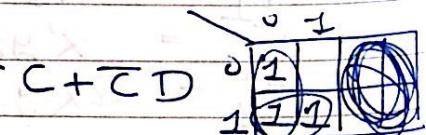
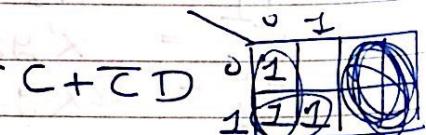
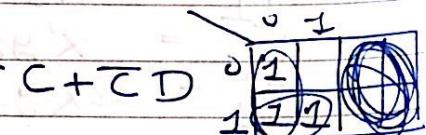
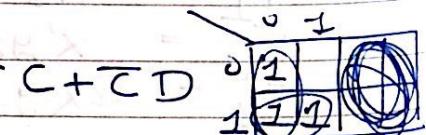
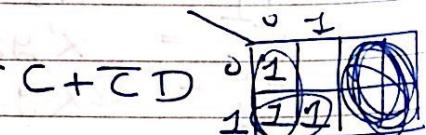
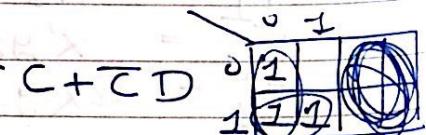
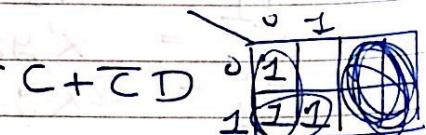
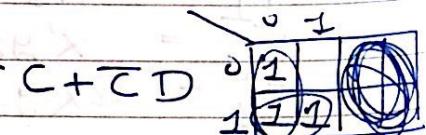
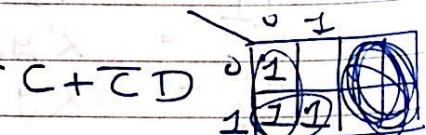
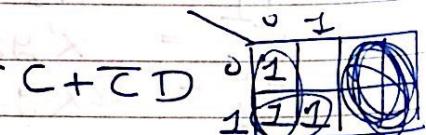
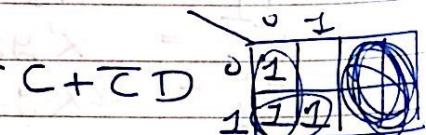
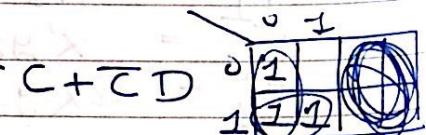
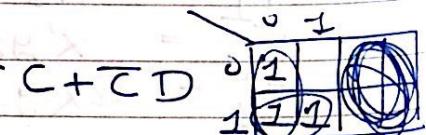
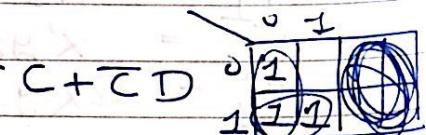
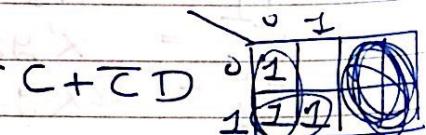
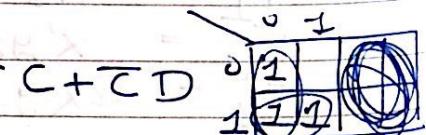
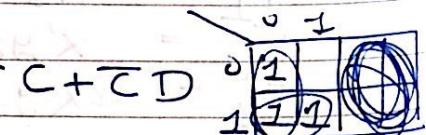
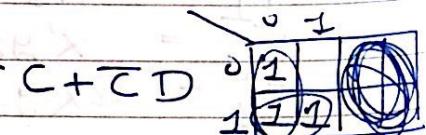
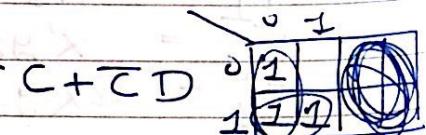
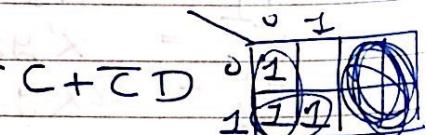
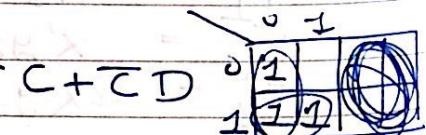
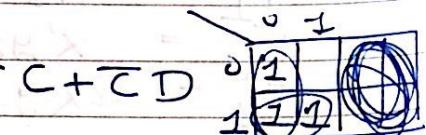
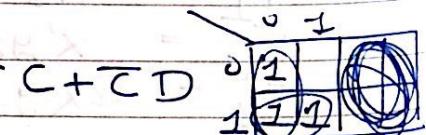
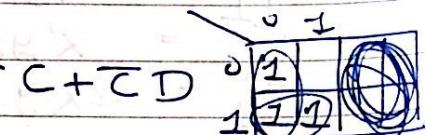
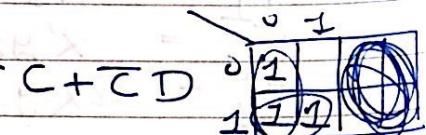
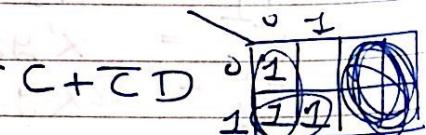
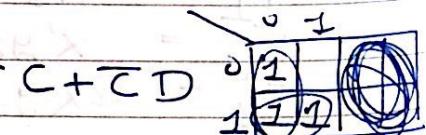
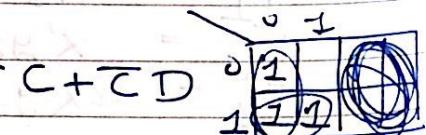
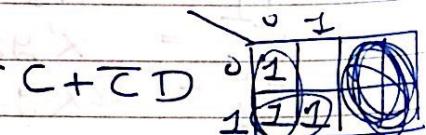
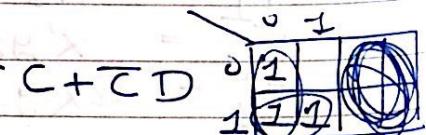
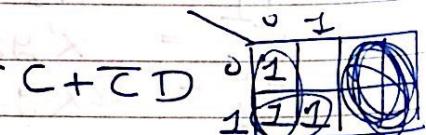
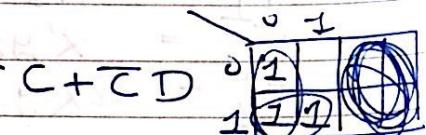
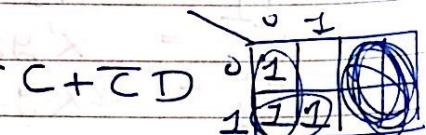
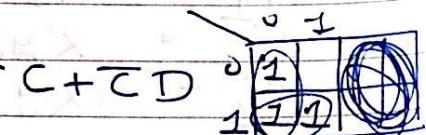
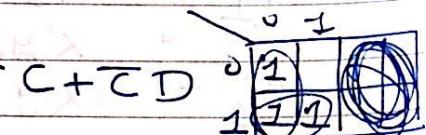
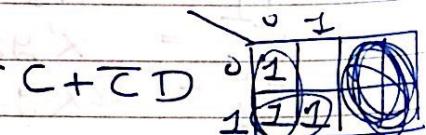
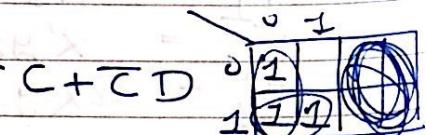
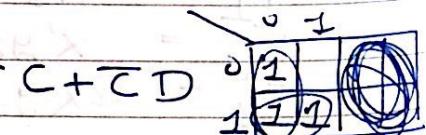
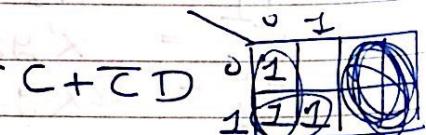
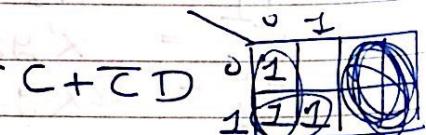
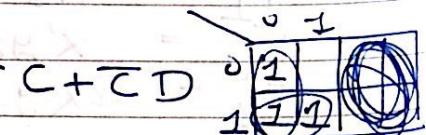
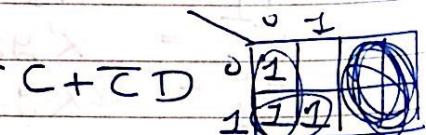
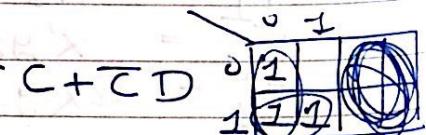
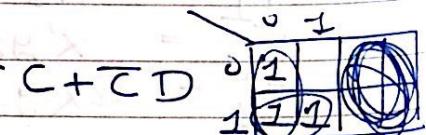
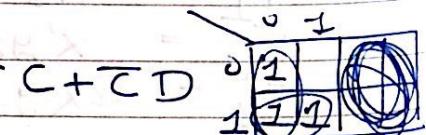
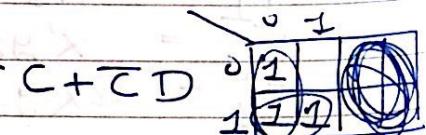
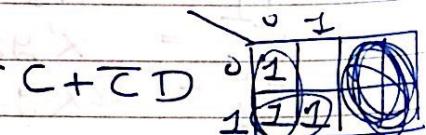
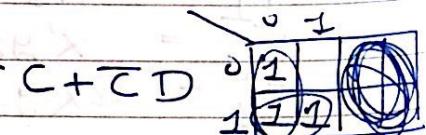
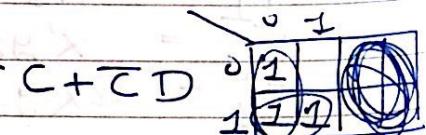
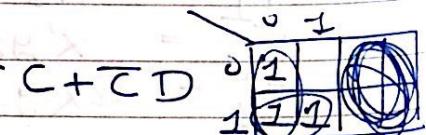
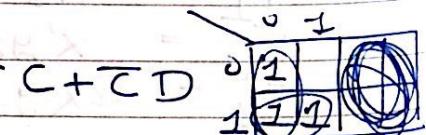
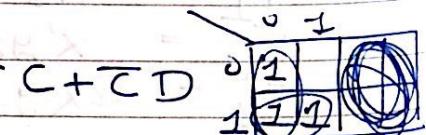
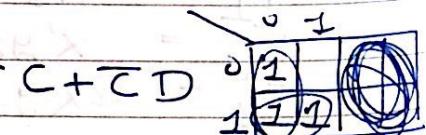
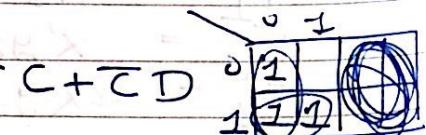
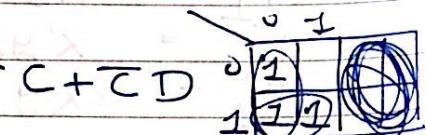
$\bar{C} + \bar{C}D$

$\bar{C}D$

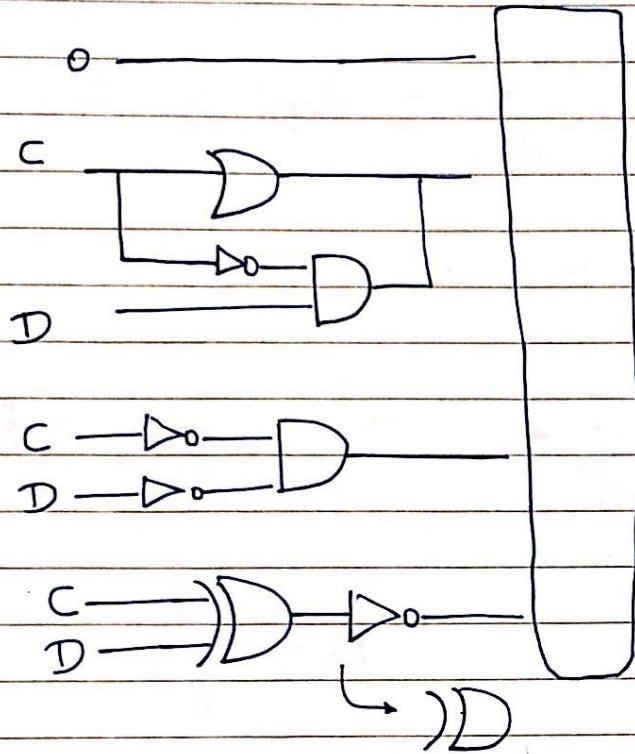
$CD$

$A$        $B$

$C + \bar{C}D$



$$\begin{array}{c}
 \begin{array}{cc}
 A & B \\
 0 & 0 \\
 0 & 1 \\
 1 & 0 \\
 1 & 1
 \end{array}
 \quad
 \begin{array}{c}
 = \bar{A}\bar{B} + A\bar{B} \\
 (\bar{A}\bar{B}) \cdot (\bar{A} + B) \\
 \cancel{\bar{A}\bar{B}} \rightarrow \bar{A} + \bar{A} \\
 \cancel{\bar{A}\bar{B}} \quad \cancel{\bar{A} + \bar{A}}
 \end{array}
 \quad
 \begin{array}{c}
 \text{DOMS} \quad \text{Page No.} \\
 \text{Date} / / \quad / / \\
 \boxed{A+B} \quad \boxed{A \cdot B}
 \end{array}
 \end{array}$$



$$\begin{array}{c}
 \begin{array}{cc}
 0 & 0 \\
 0 & 1 \\
 1 & 0 \\
 1 & 1
 \end{array}
 \quad
 F = \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} \\
 + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}CD
 \end{array}$$

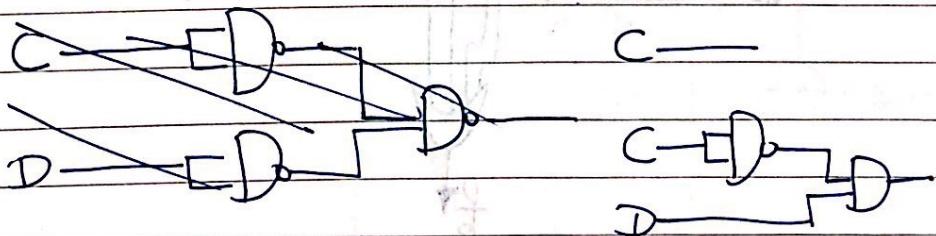
$$F = \bar{A}\bar{B}[0] + \bar{A}B[\bar{C}\bar{D}] + C\bar{D} + \bar{C}D + A\bar{B}[\bar{C}\bar{D}] +$$

$$AB[\bar{C}\bar{D} + CD]$$

$$= \bar{A}\bar{B}[0] + \bar{A}B[\bar{D} + CD] + AB[\bar{C}\bar{D}] + AB[\bar{C}\bar{D} + CD]$$

$\Rightarrow C + \bar{C}\bar{D}$

X NOR



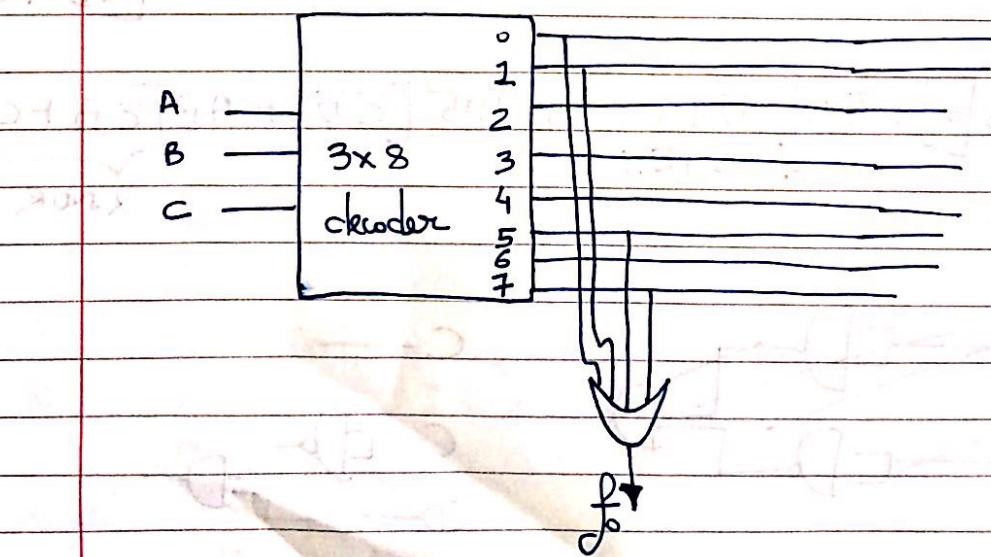
[20.8.18]

Q. Implement the 3 input logic.

$$f = \sum (0, 1, 5, 7)$$

$$f_0 = \sum (0, 1, 2, 6)$$

$$f_1 = \sum (2, 3, 4)$$



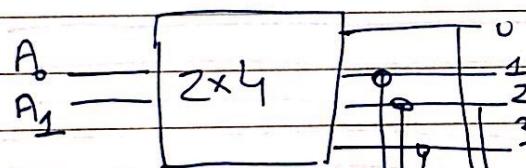
[ROM]

$k$  inputs  $\rightarrow n \times 2^k$  information where  $n$  is  
the no. of outputs

$2^k$  and gates,  $n$  or gates

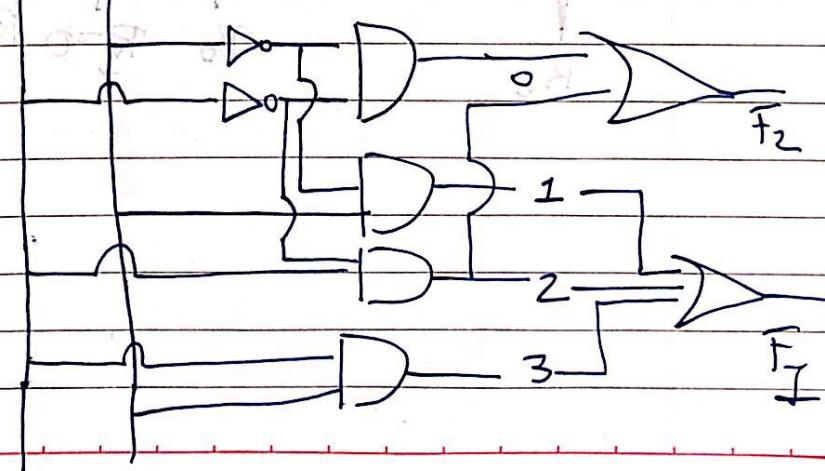
efficiently  
 { data converters       $\rightarrow$  for each address line, I should  
 { data storage          have an output

$$\begin{aligned} F_1 &= \sum(1, 2, 3) \\ F_2 &= \sum(0, 2) \end{aligned}$$



$$\bar{F}_1 \quad F_2$$

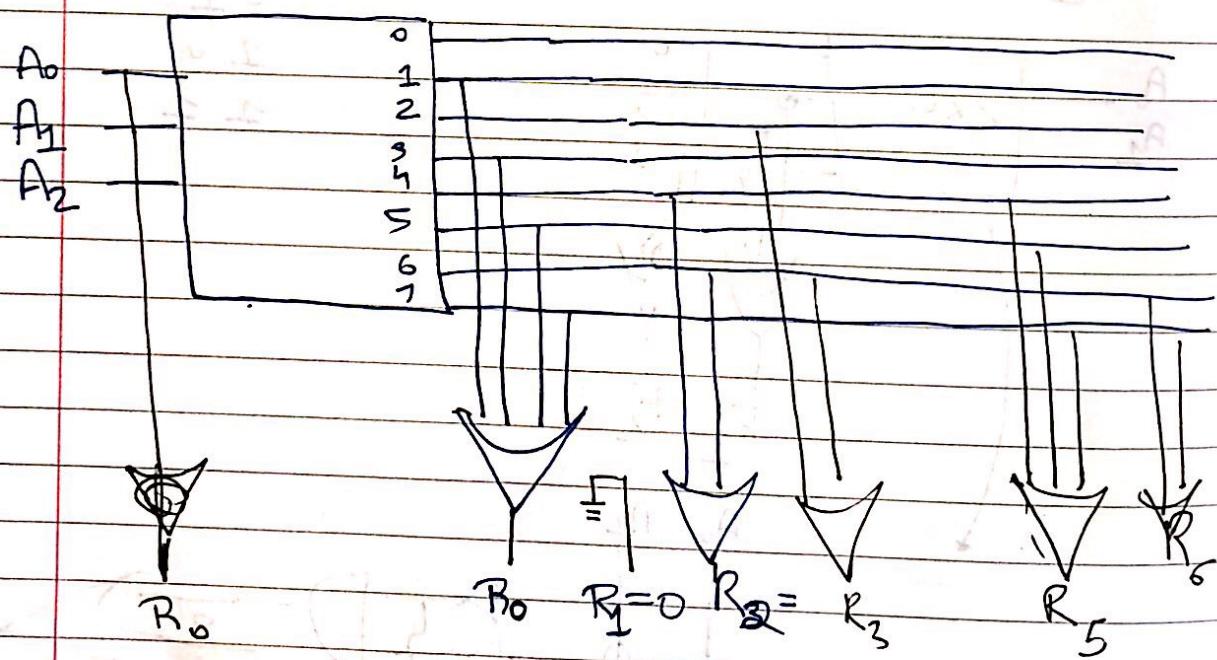
$$A_0 \quad A_1$$



[21.8.18]

Q design a ROM to print/get the square of a 3 bit input number with min no. of AND gates

			2 2 2 2 2 2
0 0 0	0	0	0 0 0 0 0 0
0 0 1	1	1	0 0 0 0 0 1
0 1 0	2	4	0 0 0 1 0 0
0 1 1	3	9	0 0 1 0 0 1
1 0 0	4	16	0 1 0 0 0 0
1 0 1	5	25	0 1 1 0 0 1
1 1 0	6	36	1 0 0 1 0 0
1	1 → 49 → 6 bits		1 1 0 0 0 1



[24.8.18]

ROM

AND gate      OR gate      (I can give diff.  
array            array            inputs to OR function)  
(FIXED)      (programmable) Gate

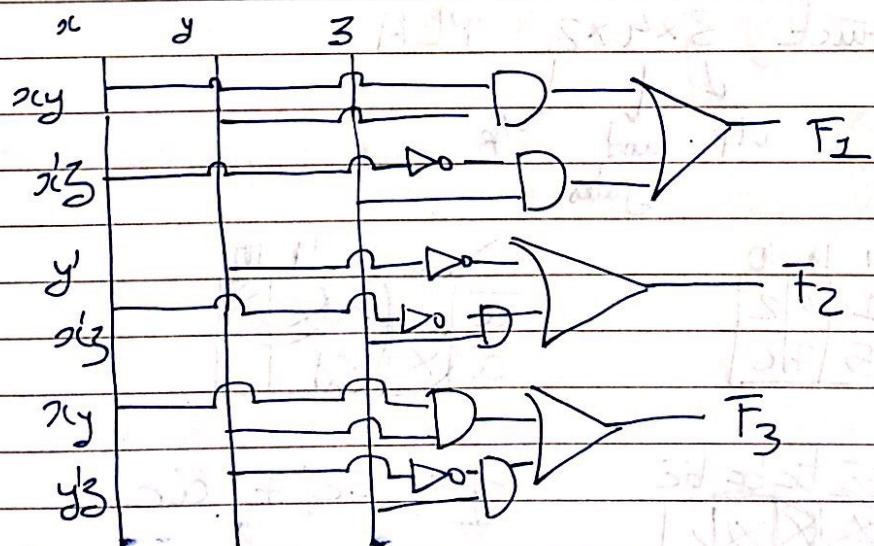
PLA → programmable logic array  
also  
programmable

$$F_1 = xy + x'z$$

$$F_2 = y' + x'z$$

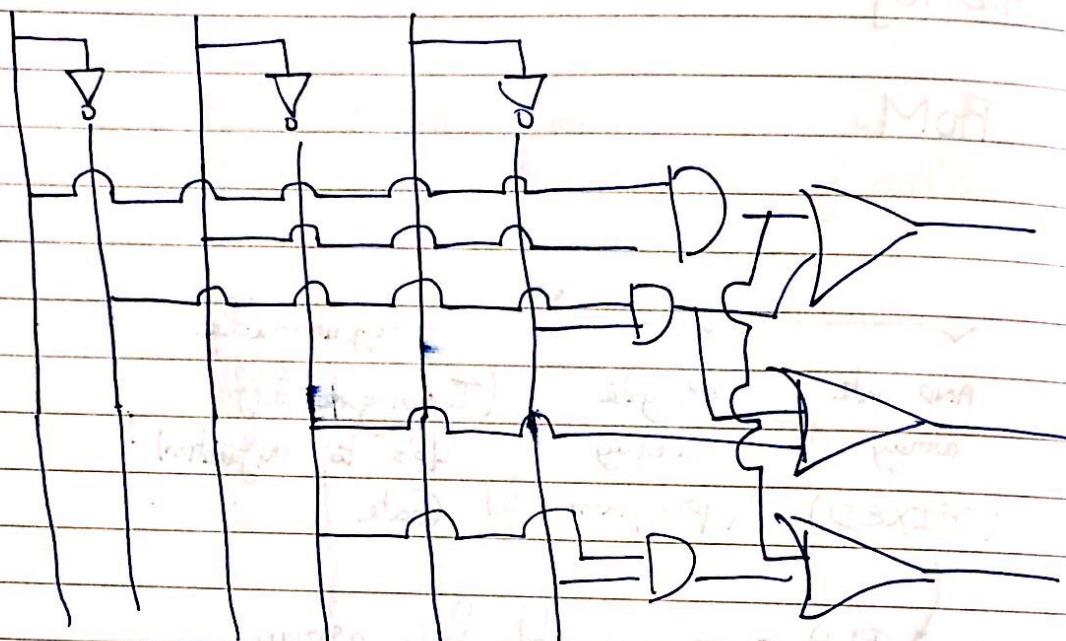
$$F_3 = xy + yz$$

construct PLA



$$\bar{a} + \bar{c}$$

$$(b+c)$$

 $x$  $y$  $z$ 

Q

$$f_1(a, b, c) = \sum m(0, 1, 3, 4)$$

$$f_2(a, b, c) = \sum m(1, 2, 3, 4, 5)$$

construct  $3 \times 4 \times 2$  PLA

↓  
i/p and o/p  
gates

	00	01	10	11
0	0	1	3	2
1	4	5	7	6

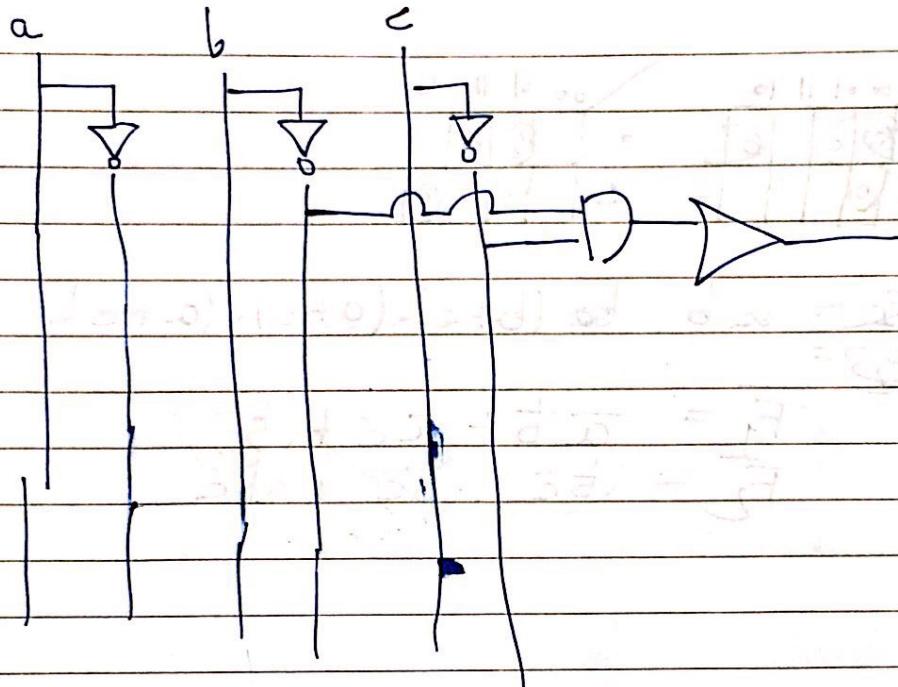
	00	01	11	10
$\bar{a}$	0	X	X	X
a	X	0	X	X

	$\bar{b}\bar{c}$	$b\bar{c}$	$b\bar{c}$	$\bar{b}\bar{c}$
$\bar{a}$	X	X	X	X
a	X	X	X	X

$$F_1 = \bar{b}\bar{c} + \bar{a}c$$

$$F_2 = ab + \bar{a}c + \bar{a}b$$

$$a(b+c) + b\bar{c} = ab + ac + b\bar{c}$$



Q  $f_1(a, b, c) = \sum m(3, 5, 6, 7)$

$$f_2(a, b, c) = \sum m(0, 2, 4, 7)$$

<input checked="" type="checkbox"/>							
<input checked="" type="checkbox"/>							
<input checked="" type="checkbox"/>							
<input checked="" type="checkbox"/>							

$F_1 = \overline{ab}c + ab + bc$   
 $F_2 = \overline{b}\overline{c} + abc + a\overline{c}$

$\overline{F_1} = \overline{bc} + a$   
 $\overline{F_2} = \overline{b} + \overline{a}c + \overline{abc}$

$$a(b+c) + b\bar{c}$$

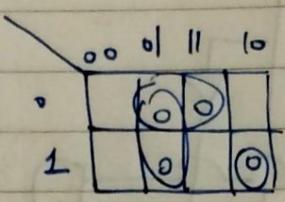
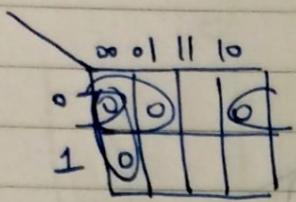
$$\overline{F_1} = (\bar{a} + \bar{c}) \cdot (\bar{b} + \bar{c}) \cdot (\bar{b} + \bar{c})$$

$$\overline{F_2} = (b+c) \cdot (\bar{a} + \bar{b} + \bar{c}) + (\bar{a} + c)$$

$$\overline{abc} \leftrightarrow \bar{a}$$

$$\overline{F_1} = (b+c) \cdot a$$

$$\overline{F_2} = (b + \bar{c}) \cdot (a + \bar{c}) \cdot (\bar{a} + \bar{b} + c)$$



$$F_1 = \cancel{abc} + (b+c) \cdot (a+b) \cdot (a+c)$$

~~(12)~~ =

$$\overline{F_1} = \overline{a} \overline{b} + \overline{a} \overline{c} + (\overline{b} \overline{c})$$

$$\overline{F_2} = (\overline{b} \overline{c}) + \overline{a} \overline{c} + abc$$

$$(F_1 \cdot \overline{F_2}) \cdot \overline{abc} = (b+c)(a+b)(a+c) \cdot \overline{abc}$$

$$(F_1 + \overline{F_2}) \cdot \overline{abc} = (b+c)(a+b)(a+c) \cdot \overline{abc}$$

(30.8.18)

PAL

$$W(A, B, C, D) = \Sigma(2, 12, 13)$$

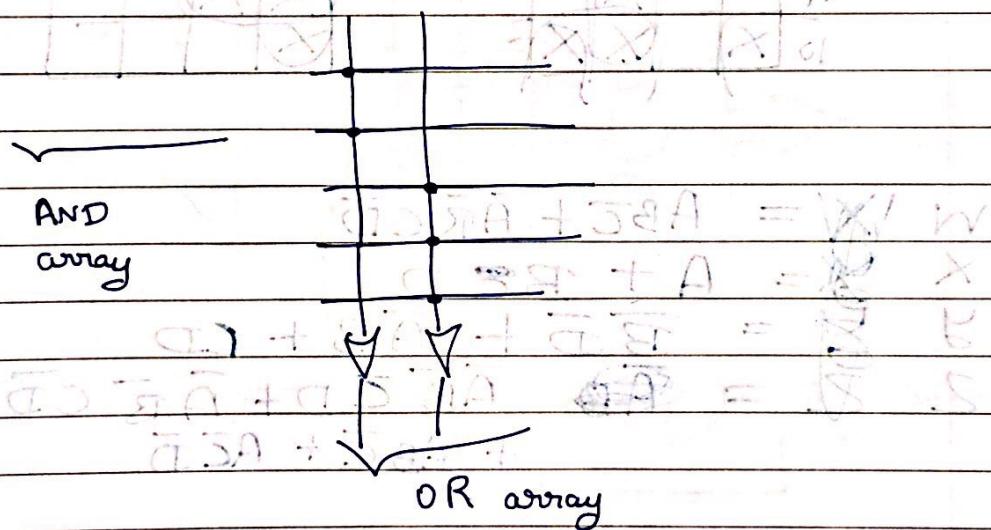
$$X(A, B, C, D) = \Sigma(7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$Y(A, B, C, D) = \Sigma(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$$

$$Z(A, B, C, D) = \Sigma(1, 2, 8, 12, 13)$$

design a combinational circuit using PAL

- here the connections to the OR gate array are fixed
- the product term cannot be shared among two or more OR gates



$$\bar{B} \bar{C} \bar{D} A + \bar{B} \bar{C} A = W$$

$$\bar{B} \bar{C} \bar{D} + \bar{B} \bar{C} = X$$

$$\bar{B} \bar{C} \bar{D} + \bar{B} \bar{C} D + \bar{B} C \bar{D} = Y$$

$$\bar{B} \bar{C} A + \bar{B} C \bar{D} + \bar{B} \bar{C} D + \bar{B} C \bar{D} = Z$$

1	2	3	2
4	5	7	6
12	13	15	17
8	9	11	10

 $Z = R_0, 8, A) W$ 
 $Y = (4, 6, 8, A) X$ 
 $X = (0, 2, 5, D) Y$ 

W	X	Y	Z
00			(X)
01			
11	(X)(X)		
10			


W	X	Y	Z
00	(X)	(X)(X)	(X)
01	(X)(X)(X)		(X)
11		X	
10	X	(X)(X)	


$W = ABC + \bar{A}\bar{B}CD$

$X = A + BCD$

$Y = \bar{B}\bar{D} + \bar{A}B + CD$

$Z = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C} + A\bar{C}\bar{D}$

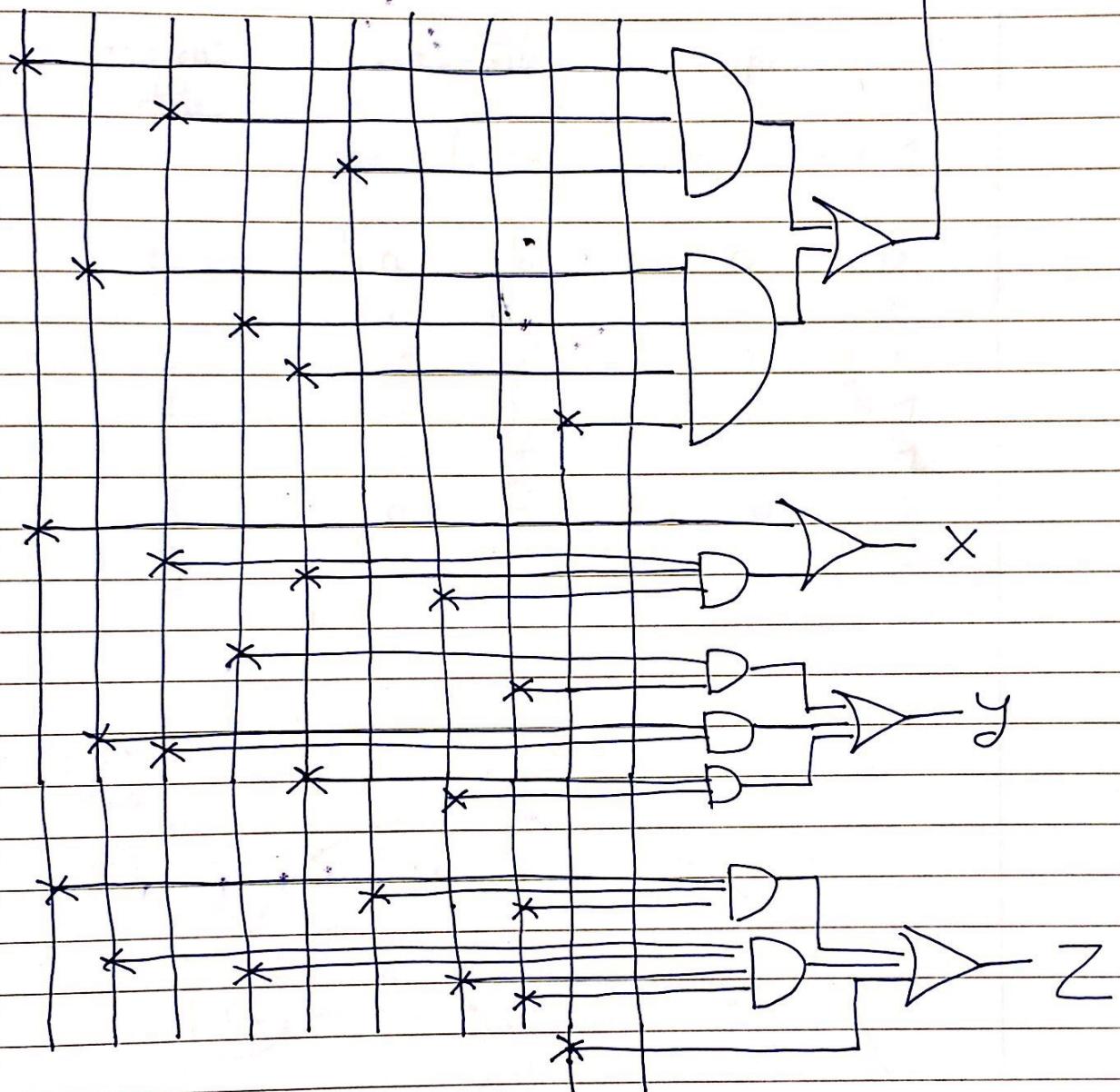
$W = ABC + \bar{A}\bar{B}CD$

$X = A + BCD$

$Y = \bar{B}\bar{D} + \bar{A}B + CD$

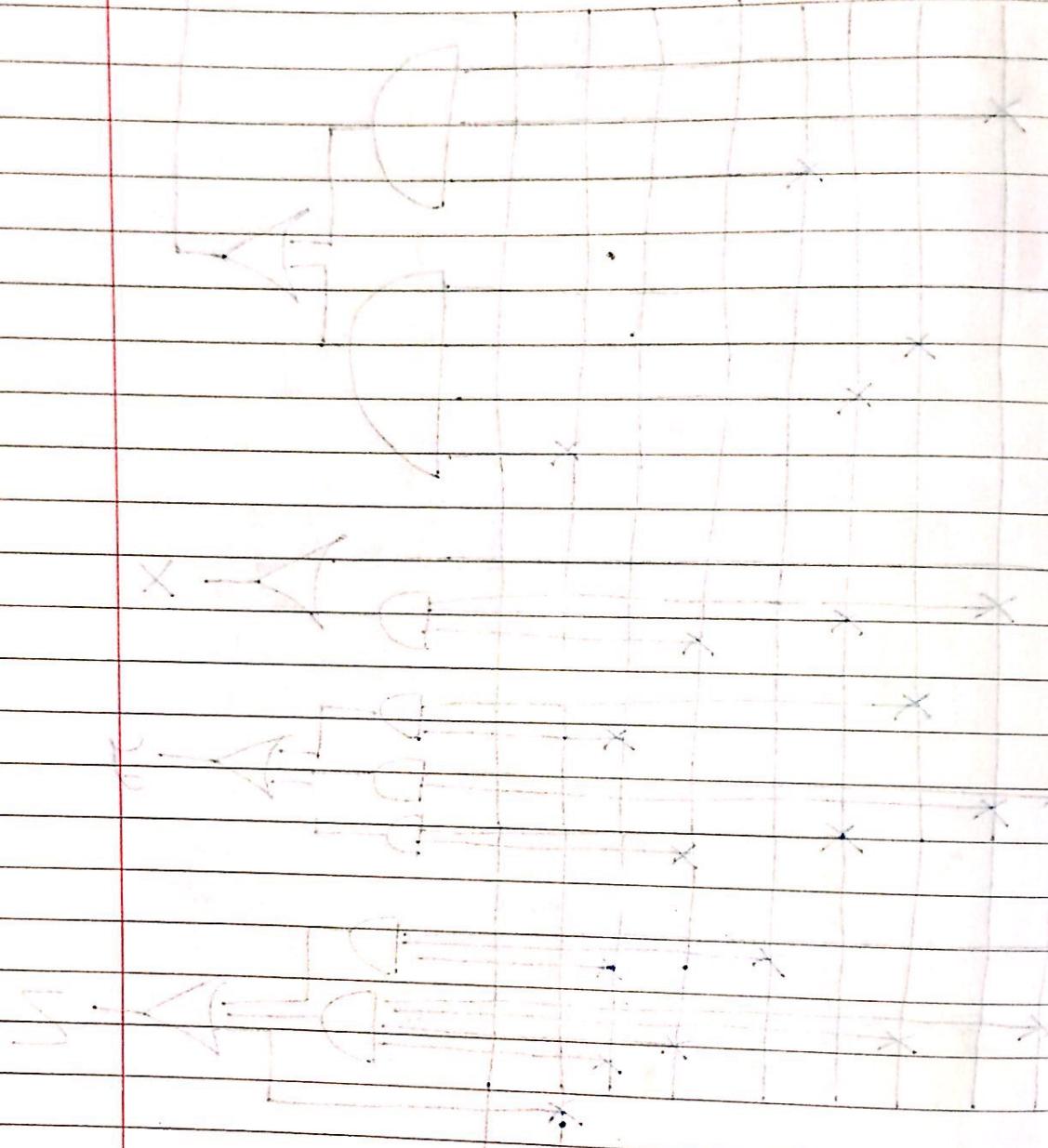
$Z = ABC + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}$

A A' B B' C C' D D' W W'



HOT

WATER BOTTLE



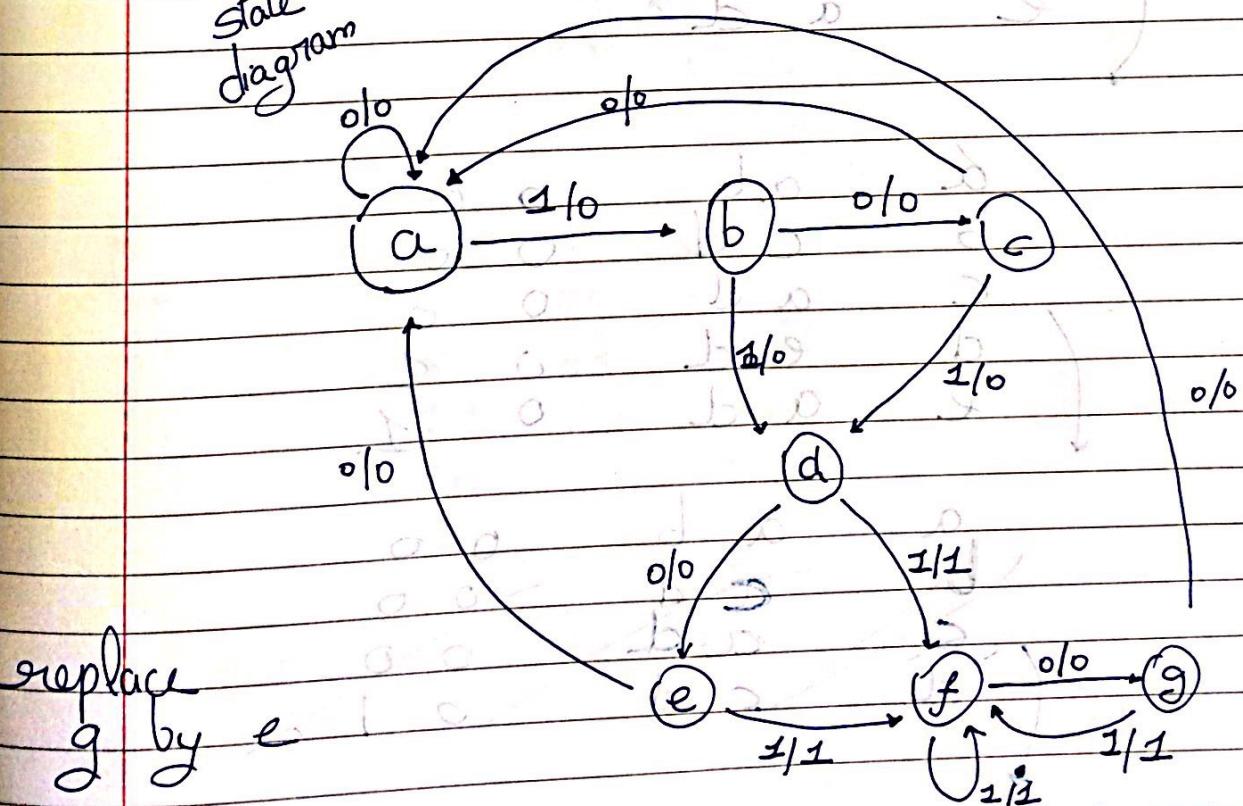
[4.9.18]

present state      next state      output

$x=0 \mid x=1$        $x=0 \mid x=1$

a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

draw  
state  
diagram

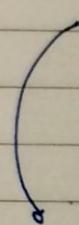


replace  
g by e

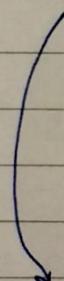
BASIC CHOICE

B.P.N.

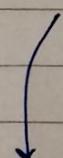
a	b	c	d	e	f	g	h
b	c	d					
c	a	d					
d	e	f					
e	a	f					
f	e	f					
g	a	f					
h							



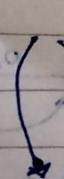
a	b						
b	c	d					
c	a	d					
d	e	d					
e	a	d					
f	e	d					
g	a	d					
h							

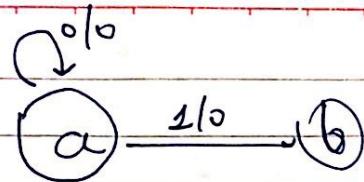


a	ab						
b	c	d					
c	a	d					
d	e	d					
e	a	d					
f	e	d					
g	a	d					
h							



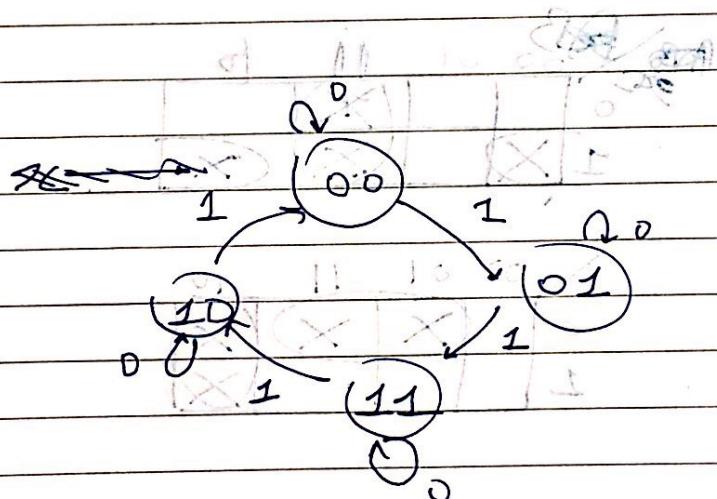
a	a	b					
b	c	d					
c	a	d					
d	c	d					
e	a	d					
f	c	d					
g	a	d					
h							





Q

Give state diag for

when  $x_c = 0$  state of ckt remains the same $x_c = 1$  ckt goes through the state transition from 00 to 01 to 11 to go back to 00.

$$T_2 + T_2 = 0A + 1 \text{ (unclear)}$$

00 00 01

01 01 11

11 11 10

10 10 00

→ using d flip flops

present if next state  
 A B      A B

00	0	0	0
00	1	0	1
01	0	0	1
01	1	1	1
10	0	1	1

11	1	1	0
10	0	1	0
10	1	0	0

00	01	11	10
1	X	X	X
1	X	X	X

00	01	11	10
1	X	X	X
1	X	X	X

$$A \cancel{B} \bar{C} + B \cancel{C} = S_0 I + S_1 \bar{I}$$

$$B \cancel{B} \bar{C} + \bar{A} \cancel{C} + B \bar{C} = S_0 \bar{I} + S_1 I$$

