P-5387

[6186]-513

S.E. (Electronics/Computer Engineering/E&TC) (Insem.)
DIGITAL CIRCUITS
(2019 Pattern) (Semester - III) (204182)

Time : 1 Hour]   *[Max. Marks : 30*

Instructions to the candidates:

1) *Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.*
2) *Figures to the right indicate full marks.*
3) *Neat diagrams must be drawn wherever necessary.*
4) *Use of non-programmable calculator is allowed.*
5) *Assume suitable data, if necessary.*

Q1) a) Explain the following characteristics of digital IC's :   **[6]**

    i) Fan In and Fan Out

    ii) I_{IL} and I_{OH}

    iii) Propagation delay

  b) Draw and explain the operation of CMOS inverter for LOW and HIGH inputs.   **[4]**

OR

Q2) a) Draw and explain the working of 2-input CMOS NAND gate.   **[6]**

  b) Explain the following characteristics of digital IC's :   **[4]**

    i) Noise Margin

    ii) Power Dissipation

Q3) a) Implement and explain the working of full adder using basic gates.

                                                       [5]

  b) Minimize the following expression using K-map and implement using logic gates :   **[5]**

    d( ) indicates don't care conditions

    $Y = \Sigma m(1, 3, 7, 11, 15) + \Sigma d(0, 2, 5)$

P.T.O.

Q4) a) Design 3-bit Gray to Binary code converter. **[6]**

b) Design full subtractor using half subtractors. **[4]**

Q5) a) Design and implement BCD to Excess-3 code converter using logic gates. **[6]**

b) Draw and explain the working of 2-input TTL NAND gate. **[4]**

OR

Q6) a) Explain the difference between current sourcing and current sinking in TTL logic. **[4]**

b) Minimize the following function using Quine Mc Clusky method. **[6]**

$F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

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