Total No. of Questions :8]

SEAT No. : ____

P3329

[Total No. of Pages :2

[5670]-598
B.E. (E &TC)
VLSI DESIGN & TECHNOLOGY
(2015 Pattern) (Semester-I) (End Sem.) (404181)

Time :2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat Diagram must be drawn whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data if necessary.***
5) ***Use of calculator is allowed.***

Q1) a) Explain any two modelling styles in VHDL **[6]**

b) Explain power distribution & power optimization techniques. **[7]**

c) Write features, specifications & applications of CPLD **[7]**

OR

Q2) a) Write VHDL code and test bench for D flip flop. **[6]**

b) Explain clock distribution techniques in detail **[7]**

c) Draw and explain CLB structure of FPGA device **[7]**

Q3) a) Design CMOS combinational logic for y=AB(D+C) and calculate W/L ratio of NMOS & PMOS (pull down & pull up) **[8]**

b) Explain **[8]**

i) Velocity saturation

ii) Hot electron effect

iii) Body effect

iv) channel length modulation

OR

Q4) a) Explain need for Transmission gate. Draw 4:1 mux using TG **[8]**

b) Draw CMOS Inverter & explain VTC in detail **[8]**

P.T.O.

Q5) a) Write spice code for CMOS inverter for AC analysis **[10]**

b) Explain ASIC design flow in detail **[8]**

OR

Q6) a) Explain micros rules for CMOS layout **[10]**

b) Explain design issues like antenna effect & electro migration effect. **[8]**

Q7) a) What are types of foult. Explain observability & controllability **[8]**

b) Write short note on BIST **[8]**

OR

Q8) a) Explain TAP controller with state diagram **[8]**

b) Explain Boundry scan Architecture **[8]**

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