Total No. of Questions : 6] **SEAT No. :**

P494

[Total No. of Pages : 2

TE/Insem/APR - 21
T.E. (E & TC)
EMBEDDED PROCESSORS
(2012 Pattern) (Semester - II)

Time : 1 Hour] ***[Max. Marks : 30***

Instructions to the candidates :

1) ***Answer Q.1 or Q.2, Q.3 or Q.4 and Q.5 or Q.6.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Draw and explain programming model of ARM 7. **[5]**

b) Explain bits and it's function in CPSR? What is need of SPSR. **[5]**

OR

Q2) a) Explain the privileged and non - privileged modes of processor. **[6]**

b) Explain following ARM instructions (any two) **[4]**

i) ANDS r_0, r_1, r_2

ii) RSB R_0, R_1, # 4

iii) STMDA R_0!, {R_1 – R_3}

iv) MLA R_0, R_1, R_2, R_3

Q3) a) Explain the relationship between Fosc, CCLK, Fcco w.r.t. PLLO. Show the frequency calculations to achieve CCLK = 60 MHz. **[6]**

b) Explain in brief system control block in LPC2148 **[4]**

OR

P.T.O.

Q4) a) With an interfacing diagram, explain LCD (16 × 2) interfacing with LPC2148. Write algorithm for the same. **[6]**

b) State the features of LPC2148. **[4]**

Q5) a) Draw and explain interfacing of GPS module with LPC2148. **[5]**

b) What are SFRs associated with ADC in LPC2148. Write algorithm to use on - chip ADC in LPC2148. **[5]**

OR

Q6) a) Compare I2C and SPI protocol. **[5]**

b) What is vectored interrupt controller (VIC) in LDC2148? Explain significance of it. **[5]**

♦♦♦♦