Total No. of Questions : 8]

SEAT No. :

P4603

[Total No. of Pages : 2

[4860]-1259
M.E. (E&TC) VLSI & Embedded System
FAULT TOLERANT SYSTEMS
(2013 Credit Pattern)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of logarithmic tables non programmable electronic pocket calculator allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Construct a binary decision diagram for $f = \bar{a}bc + a\bar{b}c + abc$ considering "a" as root node. **[5]**

b) Compare & contrast parallel, deductive & concurrent simulation techniques. **[5]**

Q2) a) Write a short note on fault sampling. **[5]**

b) Discuss the general aspects of compression techniques. **[5]**

Q3) a) Explain transition - count compression technique in detail. **[5]**

b) Draw & explain state diagram of TAP controller. **[5]**

Q4) a) Describe the various trade-offs which need to be considered for DFT. **[5]**

b) Illustrate in detail flow of event-driven simulation with the help of flowchart. **[5]**

Q5) a) Why simulation is preferred over prototype for verification of new design? **[2]**

b) Determine different levels of modeling. **[3]**

c) Write a short note on self-checking berger code checkers. **[5]**

P.T.O.

Q6) a) What is statistical fault analysis? **[5]**

b) Write a short note on PLA testing. **[5]**

Q7) a) Justify how k/n & Berger codes can be used to detect multiple bit errors. **[5]**

b) Explain in detail with timing diagram different delay models with respect to 2 input AND gate. **[5]**

Q8) a) Briefly explain exhaustive & pseudorandom form of testing. **[5]**

b) Explain following terms: **[5]**

i) Stuck RTL variables

ii) Fault variables