Total No. of Questions: 8]	SEAT No.:
P3653	[Total No. of Pages : 2

[4859]-1036

B.E. (E & T/C)					
VLSI DESIGN & TECHNOLOGY					
	(2012 Pattern) (Semester - I)				
Time: 2½ Hours] [Max. Marks		ks : 70			
Instr	ructio	ons to the candidates:			
	1)	Answer any one question out of Q.No.1 or 2, Q.No.3 or 4, Q.No. 5 or 6, Q or 8.	2.No.7		
	<i>2</i>)	Neat diagrams should be drawn wherever necessary.			
	<i>3</i>)	Use of electronic pocket calculator is allowed.			
	4)	Assume suitable data, if necessary.			
Q1)	a)	Write VHDL code for 8 bit serial in serial out shift register by stru & behavioural modeling methods.	ıctural [7]		
	b)	What is need of FPGA? List typical specifications of FPGA.	[7]		
	c)	Explain I/O architecture in detail. OR	[6]		
Q2)	a)	What are flip flop timings? What is meta-stability? What are solution	ions? [7]		
	b)	Explore the architecture of CPLD in detail.	[7]		
	c)	What are different wire parasitics? How do they play important routing?	role in [6]		
Q3)	a)	Derive the expressions for power dissipations in CMOS. What a techniques to minimize the dissipations?	are the		
	b)	Design CMOS logic for Y = AB + CDEFG+H. Compute area on ch OR	nip.[9]		
Q4)	a)	What is power delay product? Derive the expression for it. What significance?	t is its [9]		
	b)	Explain linear delay model in detail.	[9]		

Q5) a) Compare push-pull, current source & active load inverters with respect to voltage gain, voltage range, output resistance & bandwidth in detail.[8] b) Draw the schematic of CMOS differential amplifier and give the expressions for voltage gain, output resistance. CMRR & ICMR. OR Q6) a) Draw common drain amplifier. Compare with common source & common gate amplifiers with respect to gain, output resistance & bandwidth. [8] b) Draw & explain CMOS operational amplifier. Give the expressions for voltage gain & output resistance. [8] **Q7**) a) What is need of DFT? Explain with suitable example. [8] b) Explain fault models in detail. [8] OR **Q8)** a) With the interface ports involved, explain JTAG in detail. [8] b) What is partial & full scan path? [8]

