Total No. of Questions—**8**] [Total No. of Printed Pages—**4**

Seat No.	

[4857]-1042

S.E. (E & TC/Electronics) (I Sem.) EXAMINATION, 2015

ELECTRONIC DEVICES AND CIRCUITS

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Attempt Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Use of calculator is allowed.

(*v*) Assume suitable data, if necessary.

1. (*a*) State and explain three stability factors. [6]

(*b*) Consider single stage CE amplifier with R_s = 1 kΩ, R_1 = 50 kΩ, R_2 = 2 kΩ, R_C = 2 kΩ, R_L = 2 kΩ, h_{fe} = 50, $h_{re} = 2.5 \times 10^{-4}$, h_{oe} = 25 μ Amp/V, h_{ie} = 1.1 kΩ.

Calculate : A_i, R_i and R_0. [6]

Or

2. (*a*) Explain diode compensation technique against I_{CO}. [6]

(*b*) Calculate A_{VS}, A_{is} & R_0 for the transistor amplifier shown in Fig. (1) having *h*-parameters h_{ie} = 1.1 k, h_{fe} = 50, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = \frac{1}{40\text{ k}}$. [6]

P.T.O.

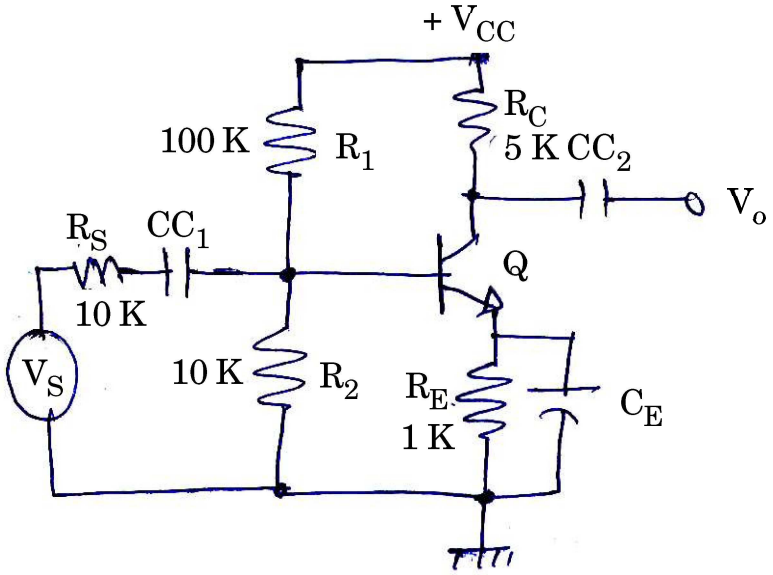

Fig. 1

3. (*a*) Draw and explain low frequency response of single stage RC coupled CE amplifier. [6]

(*b*) Determine the frequency of Oscillation when RC phase shift oscillator has R = 10 k, C = 0.01 μf and R_C = 2.2 k. Also find the minimum current gain needed for this purpose. [6]

Or

4. (*a*) The following measurement were taken while testing an amplifier using square wave input waveform : [6]

(*i*) for frequency of 5 kHz, *tr* = 20 μsec.

(*ii*) for frequency of 100 Hz, there is a sag/tilt of 1 volt in 2.5 volts.

Amplitude as observed on CRO. Determine the bandwidth of the amplifier undertest.

(*b*) Draw and explain Hartley oscillator. [6]

5. (*a*) Draw and explain vertically oriental structure of *n-p-n* power BJT. [6]

(*b*) Class A power amplifier has zero signal collector current of 100 mA. If the collector supply voltage is 5 V, determine :

(*i*) Maximum ac power output

(*ii*) Power rating of transistor

(*iii*) Maximum collector circuit efficiency. [7]

Or

6. (*a*) Draw and explain class B-push pull power amplifier. State its merits and demerits. [7]

(*b*) A power amplifier supplies 3 watt to a load of 6 kΩ. The zero signal dc collector current is 55 mA and the collector current with signal is 60 mA. How much is the percentage second harmonic distortion ? [6]

7. (*a*) Explain the following non-ideal current voltage characteristics of MOSFET :

(*i*) Finite output resistance

(*ii*) Body effect

(*iii*) Subthreshold conduction. [6]

(*b*) Calculate the drain current and drain to source voltage of common source circuit shown in Fig. 2. Given : V_{TN} = 1 V, K_n = 0.1 mA/V^2. [7]

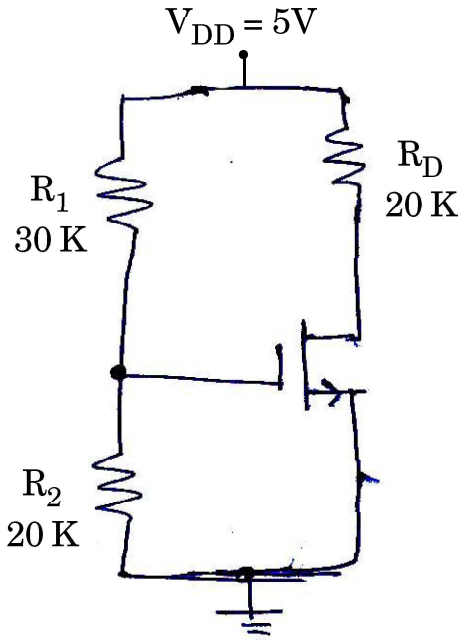

Fig. 2

Or

8. (*a*) Draw and explain constant current source biasing circuit for EMOSFET. [6]

(*b*) For the circuit shown in Fig. 3 determine the small signal voltage gain. Assume parameters V_{GSQ} = 2.12 V, V_{DD} = 5 V, R_D = 2.5 kΩ, V_{TN} = 1 V, K_n = 0.8 mA/V^2, λ = 0.02 V^{-1}. Assume the transistor is biased in the saturation region. [7]

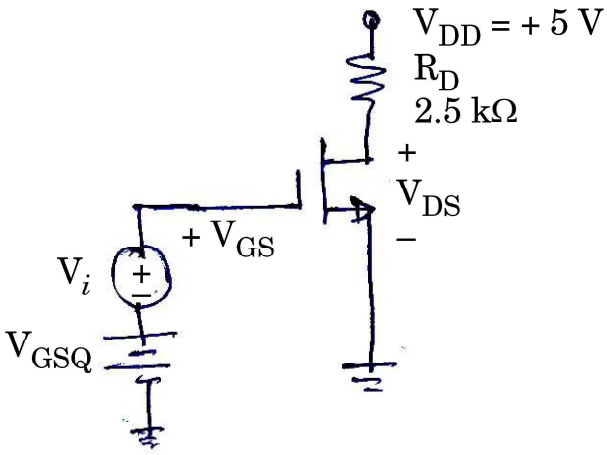

Fig. 3