Total No. of Questions : 8]

SEAT No. :

P3222

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[4660] - 1192
M.E. (E & T/C)(VLSI & Embedded Systems)
DIGITAL CMOS DESIGN
(2013 Credit Pattern) (504201) (Semester - I)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) What is technology scaling? What are types? Explore each in brief. **[5]**

b) Draw ac equivalent circuit for MOSFET and give details of capacitances involved. Compare these capacitances w.r.t. regions of operation of MOSFET. **[5]**

Q2) a) Certain CMOS logic operates at 1 GHz with supply of 1 Volt. The output of logic is connected to load of 100 pF through metal wire of length 10 μm. If the capacitance per unit length of wire is 1 pF/μm, compute power dissipation in the logic. **[5]**

b) Derive the expression for power delay product. How does it help designer? Give an example. **[5]**

Q3) a) What is SPICE? List SPICE model parameters of MOSFET. How are these useful in design? **[4]**

b) Explore any one CMOS fabrication process in brief. **[4]**

c) Draw layout of CMOS inverter. List DRC rules. **[2]**

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Q4) a) What are delay estimation techniques? Along with mathematical analysis, explain two of them in brief. **[4]**

b) Write note on transistor sizing with suitable example. **[4]**

c) What is noise margin? Give expressions. How does it help designer? **[2]**

Q5) a) Design CMOS logic for Y = A + BC + D (E+F+G+H). Compute active area in terms of λ. Comment on area and perimeter of drain/source of any one transistor. **[4]**

b) Design one bit latch using transmission gates. Comment on performance. **[4]**

c) Compare CMOS NAND & NOR in detail. **[2]**

Q6) a) With the help of schematic, explain dynamic hazards in detail. Explore mitigation techniques. **[4]**

b) Draw FSM diagram & write HDL code for overlapped type Mealy 1001 sequence detector. **[4]**

c) Define set up & hold time of a flip flop. How to take care of these timings while designing the system? **[2]**

Q7) a) Draw an example of ratioed circuit & explain in brief. What are merits & application areas of ratioed circuits? **[4]**

b) With the help of suitable schematic, explain cascade voltage switch logic. **[4]**

c) Explain low power design techniques. **[2]**

Q8) a) What is need of dynamic circuits? Draw an example of dynamic circuit & explain. **[4]**

b) Draw & explain sense amplifier circuit. What are its applications? **[4]**

c) Explain high speed design techniques. **[2]**

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