Total No. of Questions : 8]

SEAT No. :

P3183

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[5872]-296
M.E. (E&TC)(VLSI AND EMBEDDED SYSTEMS)
SYSTEM ON CHIP
(2017 Pattern) (Semester - II) (504208)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data if necessary.***

Q1) a) Enlist the various limitations of Dataflow Models? **[4]**

b) How to determine the hardware implementation of an FSMD? **[6]**

Q2) a) Enlist the various limitations of Control flow models? **[4]**

b) What is the Need for Concurrent Models? **[6]**

Q3) a) Which are the Factors Affecting Delay and Slew? **[4]**

b) Write a brief overviwe on CONTROL hazards in association with RISC Pipeline. **[6]**

Q4) a) Explain different Timing Parameters for Digital logic? **[4]**

b) What do you mean by Control Design? Explain in detail the Hierarchical Control design approach? **[6]**

Q5) a) Write a note on Timing parameters for digital logic? **[4]**

b) Write a note on Simulation - Synthesis Mismatch? **[6]**

P.T.O.

Q6) a) Write a note on Memory Optimization and Management? **[4]**

b) Write a note on Bus Synchronization along with the Challenges in it and Enable Synchronization Method? **[6]**

Q7) a) What are the Design Issues and Techniques for image codec? **[4]**

b) Enumerate on Energy Management techniques for SOC? **[6]**

Q8) a) Explain the Important Issues for Embedded Compilers? **[4]**

b) Write a note on "A SOC Controller for Digital still Camera"? **[6]**