S.E. 2012 (Electronics/E&Tc)
COMPUTER ORGANIZATION
(Semester - II)

Time: 2 Hours   *Max. Marks : 50*

Instructions to the candidates:
  1) *Neat diagrams must be drawn wherever necessary.*
  2) *Figures to the right side indicate full marks.*
  3) *Assume Suitable data if necessary*

Q1) a) Draw and explain the Von Neumann architecture   [6]
     b) Represent $(178.1875)_{10}$ in single precision floating point format   [6]
                                OR
Q2) a) Explain pipelining & superscalar operation   [6]
     b) multiply the following numbers using bit pair recoding method   [6]
         Multiplicand   01111 (15)
         Multiplier   10110   (-10)
Q3) a) Write control sequence for execution of instruction ADD (R1), R2 using single   [6]
         bus organization
     b) Draw and explain the interface between printer and processor   [6]
                                OR
Q4) a) Explain different methods to handle multiple interrupt requests   [6]
     b) Explain the steps involved in fetching a word from memory   [6]
Q5) a) Draw and explain the structure of Asynchronous DRAM and hence explain how   [7]
         the data can be read or written in the DRAM
     b) Explain different mapping schemes for cache memory   [6]
                                OR
Q6) a) Explain the concept of virtual memory.Explain how virtual address is translated   [6]
         to physical address.
     b) With the help of a neat diagram, explain the working principle of SRAM   [7]
Q7) a) Explain the following instructions of 8086 with suitable example   [6]
         i) XLAT   ii)DAA   iii) PUSH   iv) IN   v) TEST   vi) LEA
     b) Explain interrupt structure of 8086   [7]
                                OR
Q8) a) Explain the following addressing modes of 8086 with examples   [6]
             i)   String addressing
             ii) Based Indexed addressing
             iii) Direct addressing
     b) Draw the bit pattern for flag register of 8086 and explain significance of each bit   [7]