Total No. of Questions : 8]

SEAT No. :

P5240

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M.E. (E & TC) (VLSI & Embedded Systems)

TESTING AND VERIFICATION OF VLSI CIRCUITS

(2017 Course) (604201)

Time : 3 Hours] *[Max. Marks :50*

Instructions to the candidates:

1) ***Attempt any 5 questions.***
2) ***Figures to the right in bold indicate full marks.***
3) ***Assume suitable data.***

Q1) a) Briefly discuss how VLSI technology trends have affected the domain of testing. **[4]**

b) Explain role of testing in VLSI realization process. **[4]**

c) Briefly explain Test Programming. **[2]**

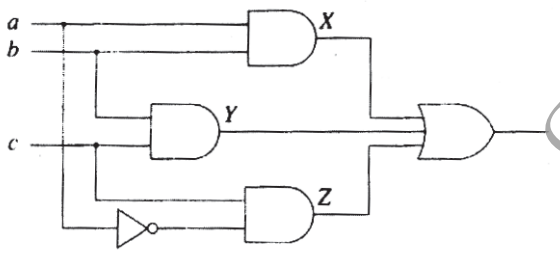
Q2) a) Differentiate between Defect, Fault and Error with suitable example. **[4]**

b) Define Fault Dominance and explain it with respect to all two input logical gates. **[4]**

c) Explain Benefit-Cost Analysis for IC Fabrication. **[2]**

Q3) a) Compare and contrast between simulation for design verification and simulation for Test Evaluation. **[5]**

b) Find min test set for following circuit to cover all single stuck at faults. **[5]**



P.T.O.

Q4) a) Explain briefly various delay models of digital simulators. **[4]**

b) Write Short Note on "Observability and Controllability". **[4]**

c) Give Controllability calculations for a two-input OR gate. **[2]**

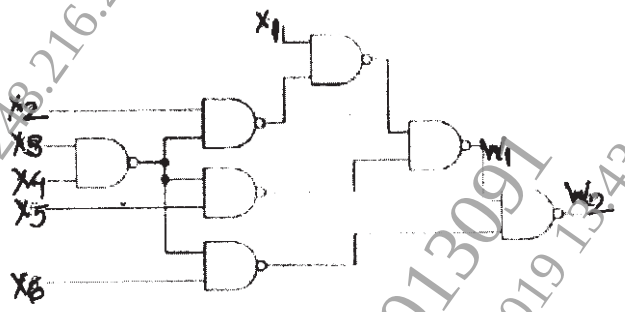
Q5) a) Explain principle and operation for Linear Feedback Shift Register. **[5]**

b) Explain Boundary scan Testing in IEEE 1149.1 architecture. **[5]**

Q6) a) Write Short Note on "Time Frame Expansion Method of ATPG". **[5]**

b) Explain Memory Testing. **[5]**

Q7) a) Compute the combinational SCOAP testability measures for following circuit. **[5]**



b) Explain any five fault models with suitable examples. **[5]**

Q8) a) Explain challenges and special need for embedded core testing. **[4]**

b) Compare and Contrast between formal and functional verification. **[4]**

c) State Importance of avoiding errors in test generation. **[2]**

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