Total No. of Questions : 8]

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SEAT No. :

[Total No. of Pages : 2

[5060]-744
M.E. (E&TC) (VLSI and Embedded Systems)
ASIC DESIGN
(2013 Pattern) (Semester - III)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates :

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Draw the design flow for an ASIC design process and explain each step. **[4]**

b) What do you mean by ASIC cell library? And what should it contain? **[3]**

c) Compare different ASIC technologies **[3]**

Q2) a) Explain in detail Gate array based ASICs. **[4]**

b) Differentiate static and dynamic timing analysis. Which is better? and why? **[3]**

c) Write a VHDL code for sequence detector, which detects the sequence '1101' using moore machine. **[3]**

Q3) a) What is cross talk delay and cross talk noise in context to ASIC design? Which parameter it will severely affect? **[4]**

b) Explain Gate level mixed mode simulation and testing of ASIC. **[4]**

c) Explain the synthesis process in detail. **[2]**

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Q4) a) Explain noise coupling and element matching with respect to practical aspects of mixed signal analog digital design. **[5]**

b) Explain signal integrity effects in ASIC design. **[5]**

Q5) a) What are objectives of system partitioning and explain different algorithms used for the same. **[4]**

b) What are the factors contributes to best floor planning? Explain in detail. **[3]**

c) What is parameter extraction pertaining to ASIC design? **[3]**

Q6) a) Differentiate pre layout and post layout simulation with respect to ASIC. **[4]**

b) What are the approaches to global routing? Explain in detail any one algorithm to find shortest path. **[4]**

c) Define channel density and Elmore's delay. **[2]**

Q7) a) Explain in detail about ATPG algorithm using test vectors with neat diagram. **[4]**

b) Briefly explain Boundary scan test. **[4]**

c) Define the term controllability and observability. **[2]**

Q8) a) Explain the Built In Self Test (BIST) with example. **[5]**

b) Write short notes on Any two: **[5]**

i) Design Rule check (DRC)

ii) Features of EDA tools

iii) Fault simulation