Total No. of Questions : 8]

SEAT No. :

P2147

[Total No. of Pages : 2

[4460]-737

M.E. (E & TC) (VLSI and Embedded Systems)

RECONFIGURABLE COMPUTING

(2013 Pattern) (Semester - I)

Time :3 Hours] *[Max. Marks :50*

Instructions to the candidates :

1) ***Attempt any five questions out of 8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of logarithmic tables slide rule, Mollier charts and electronic pocket calculator and steam tables are allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) With help of suitable example explain difference between reconfigurable machines and conventional processor. **[4]**

b) Explain delta delay, intrinsic delay, interconnect delay pertaining to RD. **[3]**

c) Compare FPGA, GPP, ASIC with respect to functional capacity, data density and functional diversity. **[3]**

Q2) a) How would you modify the present multicontext FPGA to convert into RFPGA? Explain in brief. **[4]**

b) How to calculate instruction bandwidth of LUT based structure? How does that BW make a decision of on/off chip memory? **[3]**

c) How to compute area on chip per bit PE? Give the expression and Explain. **[3]**

Q3) a) What is partially reconfigurable? Is it supported in any present device? How do you decide that the task needs fully reconfigurable device? **[4]**

b) Give the issues in Reconfigurable Network Design. **[3]**

c) Write short note on Configurable, Programmable, and fixed-Function devices. **[3]**

P.T.O.

Q4) a) Draw and explain architecture of DPGA? **[4]**

b) What are the research challenges in the design and development of Reconfigurable devices? **[3]**

c) What are the problems with simple networks? Explain in details with example. **[3]**

Q5) a) State and explain reconfigurable device characteristics. **[4]**

b) Explain the terms functional density, functional diversity and data density with reference to reconfigurable devices. **[3]**

c) What is need of instruction compression? What are its techniques? Which is best suitable for RD? **[3]**

Q6) a) Explain hierarchical interconnects in detail. What are its effects on the performance of the reconfigurable device? **[4]**

b) What is Rent Rule? Explain its importance. **[3]**

c) Find area required for interconnect a 2500 4-LUT device. Assume minimum wire pitch is 8λ and the crossbar is implemented with two layers of dense metal routed at this minimum wire-pitch. **[3]**

Q7) a) Give the first order comparison of area occupied by different blocks on chip of FPGA.What is conclusion? **[5]**

b) Give mathematical analysis of switch, channel and wire growth. **[5]**

Q8) a) What are the advantages of MATRIX architecture over general purpose architecture? Draw the block diagram and briefly explain the function of each block. **[5]**

b) Write short note on Network utilisation efficiency. **[5]**