Total No. of Questions : 8]

SEAT No. :

P5404

[Total No. of Pages : 2

[5562]-265

M.E. (E &TC) (VLSI & Embedded Systems) (Semester - II)

SYSTEM ON CHIP

(2017 Pattern)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates :

1) ***Answers any five questions. Each question carry 10 marks and each bit carries 5 marks.***
2) ***Draw the neat diagram whenever necessary.***
3) ***Figures to the write indicate full marks.***
4) ***Assume suitable data whenever necessary.***

Q1) a) Explain RTL Based Chip Design Flow.

b) What is Metastability? Explain the Problems Due to Metastability?

Q2) a) Control Flow Modeling and the Limitations of Data Flow Models?

b) How to determine the hardware implementation of an FSMD?

Q3) a) Explain the difference between the following terms:

i) Control hazard and data hazard

ii) Delayed branch and conditional branch

b) Explain time multiplexing of two hardware-Module ports over a single control shell.

Q4) a) Explain different Timing Parameters for Digital Logic?

b) Explain various synchronization schemes adopted by Hardware and Software interface.

P.T.O.

Q5) a) Which are the Factors Affecting Delay and Slew?

b) What are Causes of Power Dissipation?

Q6) a) What is the need of memory optimization and management in SoC?

b) Write a note on Bus Synchronization along with the Challenges in it and Enable Synchronization Method?

Q7) a) What is Hybrid Power Management Technique?

b) Write a note on 'A SOC Controller for Digital Still Camera".

Q8) a) What are the Design Issues and Techniques for image codec?

b) Explain energy management techniques for SoC design.

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