Total No. of Questions : 8]

SEAT No. :

PA-743

[Total No. of Pages : 2

[5928]-210
M.E. (E & TC) (VLSI & Embedded System)
TESTING AND VERIFICATION OF VLSI CIRCUITS
(2017 Pattern) (Semester - III) (604201)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:

1) ***Answer any 5 questions from the following.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) Briefly discuss how VLSI technology trends have affected the domain of testing. **[5]**

b) Differentiate between Defect, Fault and Error. **[5]**

Q2) a) List different types of testing VLSI. Explain any two in brief. **[6]**

b) Differentiate between verification and testing with respect to VLSI process. **[4]**

Q3) a) What is the need of fault simulation. Explain in details serial fault simulation algorithm. **[5]**

b) Explain fault equivalence of combinational circuits with suitable examples. **[5]**

Q4) a) Explain briefly observability and controllability. **[5]**

b) Differentiate between combinational circuit test generation and sequencial circuit test generation. **[5]**

P.T.O.

Q5) a) With the help of neat diagram explain LFSR and signature compaction of BIST. **[5]**

b) How Analog testing is different than digital testing. **[5]**

Q6) a) Explain need of DFT. Also explain scan architecture briefly. **[5]**

b) Explain different test pattern generation methods for BIST. **[5]**

Q7) a) Write a short note on "SOC Testing". **[5]**

b) Write short note on ATPG. **[5]**

Q8) a) Write a short note on "Embedded core testing". **[5]**

b) State importance of avoiding design errors in hardware design. **[5]**