Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5252]-136

S.E. (Electronics/Electronics & Telecommunication)

(Second Semester) EXAMINATION, 2017

INTEGRATED CIRCUITS

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. **1** *or* Q. **2**, Q. **3** *or* Q. **4**, Q. **5** *or* Q. **6** and Q. **7** *or* Q. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Use of electronic pocket calculator is allowed.

(*v*) Assume suitable data, if necessary.

1. (*a*) Derive the expression for A_d, R_i and R_o for dual input balanced output difference amplifier using *r*-parameters. [6]

(*b*) Define and explain the following terms with respect to Op-Amp : PSRR, CMRR, Gain bandwidth product. [6]

Or

2. (*a*) What is the need of frequency compensation ? Explain pole zero method of external frequency compensation. [6]

(*b*) With neat diagram explain the necessity and working of current mirror circuit. [6]

P.T.O.

3. (*a*) What are problems associated with the ideal integrator ? Draw neat circuit diagram of practical integrator. Explain its operation with its frequency response. [6]

(*b*) Draw and explain difference amplifier using Op-amp. Derive the expression for its output voltage. [6]

Or

4. (*a*) Explain the necessity of Precision rectifier and explain the operation of Full wave Precision rectifier with neat circuit diagram. [6]

(*b*) Draw and explain Sample and Hold circuit using Op-amp. Explain the necessity of Sample and Hold circuit. [6]

5. (*a*) With the help of neat diagram explain the operation of R-2R ladder type of DAC. [7]

(*b*) Draw neat diagram and V to I convertor with grounded load and explain its operation. [6]

Or

6. (*a*) Calculate output voltage of 6-bit DAC for digital input 100000, 111111 and 111100 with reference voltage of 5V. [6]

(*b*) With the help of neat diagram explain the operation of Dual Slope ADC. [7]

7. (*a*) Explain operation of PLL with the help of neat block diagram. Define the terms Lock range and Capture range. [7]

(*b*) Draw neat diagram and explain three-terminal adjustable voltage regulator with expression for output voltage. [6]

Or

8. (*a*) Draw and explain circuit of FM demodulator using PLL. [7]

(*b*) Explain low drop out voltage regulator. [6]