Total No. of Questions :8]

SEAT No. :

P5241

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[5671]-268
M.E. (E&TC)
ASIC DESIGN
VLSI & Embedded Systems
(2017 Pattern) (604202)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any 5 questions.***
2) ***Neat diagrams must be drawn whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) What is the need of ASIC Library? **[3]**

b) Explain Gate Array based ASICS, state types of Masked Gate Array (MGA) ASICs. **[4]**

c) What are optimization targets of logic synthesis? **[3]**

Q2) a) Compare different ASIC technologies. **[5]**

b) Write a VHDL code for a sequence detector, which detects the sequence '1011' using Mealy machine. **[5]**

Q3) a) Explain the final routing steps in ASIC design? **[4]**

b) Which source makes power dissipation in CMOS ASIC design? Why? **[4]**

c) What are objectives of partioning for ASIC design? **[2]**

Q4) a) How delay is minimize in contest to time driven placement method? **[3]**

b) What is parameter extraction pertaining to ASIC design? **[3]**

c) What is the CAD design tool? Explain in brief. **[4]**

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Q5) a) Explain the different timing parameters for Static Timing Analysis. **[3]**

b) Define channel density and Elmore's delay. **[3]**

c) What do you mean by the false path detection in ASIC. **[4]**

Q6) a) Explain the concept mixed mode design. **[4]**

b) How delay calculation in done in static timing analysis? **[3]**

c) Which design tool is more preferable to solve the SI Problem? **[3]**

Q7) a) Explain Partial scan and Full scan. **[3]**

b) Explain mixed signal ASIC Design. **[4]**

c) What is the need of DFT? **[3]**

Q8) a) Explain the signal integrity effect in ASIC design. **[4]**

b) Explain basic ATPG algorithm with an example. **[4]**

c) What are Fault models? **[2]**