Total No. of Questions : 8]

SEAT No. :

**P4016**

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# M.E. (E&TC) (VLSI & Embedded Systems)
# FAULT TOLERANT SYSTEMS
# (2013 Credit Pattern)

*Time : 3 Hours]* *[Max. Marks : 50*

***Instructions to candidate :***

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Assume suitable data, if necessary.***
3) ***Solve any five questions.***

***Q1)*** a) Define

i) Cube

ii) Primitive cube.

What is the procedure of constructing a cube? **[5]**

b) Construct a binary decision diagram for a JK flip-flop with asynchronous set (S) & reset (R) inputs. **[5]**

***Q2)*** a) Briefly explain following types of cross point faults. **[8]**

i) Shrinkage fault

ii) Growth fault

iii) Appearance fault

iv) Disappearance fault.

b) Discuss the term pin-fault model. **[2]**

***Q3)*** a) Explain following terms : **[4]**

i) Stuck RTL variables

ii) Fault variables

b) Describe the working of self checking checkers. **[6]**

***P.T.O.***

***Q4)*** a) Define bridging fault. Find test vector that determine the OR bridging fault between input A & B in the following figure (Figure 1). **[4]**

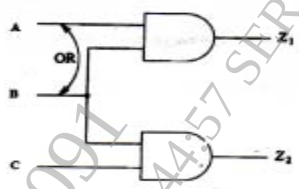


Figure 1

b) Explain how testing is performed using test-response compression technique. Draw a suitable diagram. **[6]**

***Q5)*** a) How to detect hazards present in asynchronous circuits? **[6]**

b) List any four benefits of on-line testing. **[4]**

***Q6)*** a) With the help of suitable diagram explain the triple modular redundancy (TMR) technique used in fault tolerant design. **[5]**

b) Discuss the functional & structural forms of off-line BIST techniques. **[5]**

***Q7)*** a) Draw & explain chip architecture for IEEE 1149.1. **[8]**

b) Briefly explain exhaustive form of testing. **[2]**

***Q8)*** a) Write a short note on syndrome testing. **[6]**

b) Define following terms : **[4]**

i) Structural faults

ii) Functional faults

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