Total No. of Questions : 8]

SEAT No. :

P4807

[Total No. of Pages :2

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M.E. (E & TC) (VLSI & Embedded Systems)

SYSTEM ON CHIP

(2017 Pattern) (Semester - II)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions. Each question carry 10 marks and each bit carries 5 marks.***
2) ***Draw the neat diagram whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data if necessary.***

Q1) a) Explain the Dualism of Hardware Design and Software Design.

b) What are the limitations of Data flow models?

Q2) a) What are pipeline hazards? How pipeline hazards can be handled.

b) Discuss why it is a bad idea to model data-path expressions as FSM, while it can still be useful to model FSM as data-path expression.

Q3) a) Explain the Hardware schematic for a counter with Timing Diagram.

b) Explain RTL Based Chip Design Flow.

Q4) Explain the difference between the following terms:

a) Control hazard and data hazard

b) Delayed branch and conditional branch

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Q5) a) Explain different architectural techniques that can be used to optimize the performance of the Co-processor.

b) Explain time multiplexing of two hardware-Module ports over a single control shell.

Q6) a) What is Metastability? Explain the Problems Due to Metastability?

b) What is bus synchronization in RTL?

Q7) a) What is Motion Estimation (ME)?

b) Explain the Important Issues for Embedded Compilers.

Q8) a) What are the Design Issues and Techniques for image codec?

b) How Dynamic Power Management is useful in memories.