Total No. of Questions :8]

SEAT No. :

P3059

[Total No. of Pages :3

[4660]-1201

M.E. (E & TC) (VLSI & Embedded Systems)

FAULT TOLERANT SYSTEMS

(2013 Credit Pattern) (Semester - III) (604201)

Time : 3 Hours] *[Max. Marks :50*

Instructions to the candidates:

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Assume suitable data if necessary.***
3) ***Solve any five questions.***

Q1) a) What is binary decision diagram? Explain step by step process to draw the binary decision diagram for function $F = \bar{a}\ b\ \bar{c} + a\,c$. **[3]**

b) Define unknown logic value. Explain how to construct a truth table for 2 input XOR gate. **[3]**

c) Classify and define circuit simulation. Explain with neat diagram the event driven logic simulation method. **[4]**

Q2) a) Construct a primitive cube table for function: **[3]**

$$F = \bar{x}_1\,\bar{x}_2 + x_1\,\bar{x}_2 + \bar{x}_1\,x_2\,x_3$$

b) Define and explain in detail with the timing diagram, different delay models w.r.to 2 input AND gate. **[4]**

c) Write short note on static and dynamic hazard detection. **[3]**

Q3) a) State Fault Equivalence and Fault Dominance Theorem. For figure 1 determine collapse ratio by applying fault equivalence and fault dominance theorem in detail. **[5]**

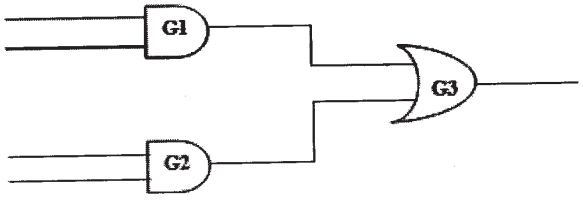

Figure 1

P.T.O.

b) State Masking Theorem. Prove that fault 'a' s-a-1 masks fault 'c' s-a-0 for the circuit as shown in figure 2. Determine the test vector for the same. **[5]**

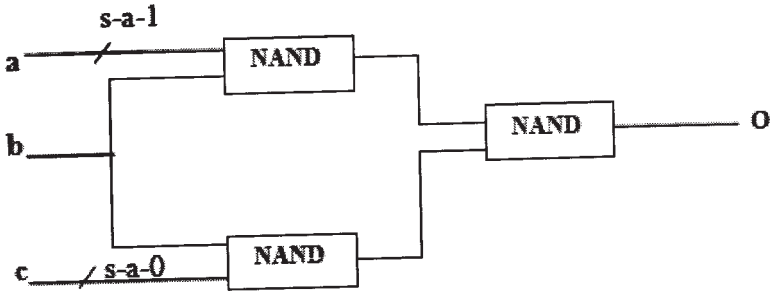

Figure 2

Q4) a) Explain in detail the Deductive fault simulation algorithm. **[4]**

b) Define Detectability. Find test vectors that determine the OR bridging fault between input B & C in fig. 3. shown below. **[4]**

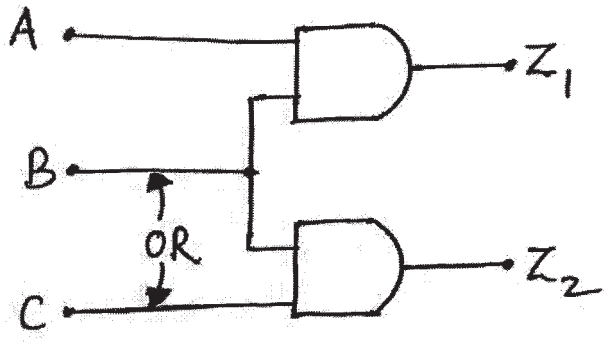

Figure 3

c) Write short note on Wired logic and Bidirectionality. **[2]**

Q5) a) Explain single input signature analyzer to generate the output stream whose reciprocal characteristics polynomial is given by

$P(X) = 1 + X^2 + X^4 + X^5$. Assume input sequence as 11110101. **[5]**

b) What are the drawbacks of conventional testing approach. Classify different compression techniques. Explain One's count compression technique. **[5]**

Q6) a) What is Boundary Scan? Show a design for the boundary-Scan cell circuitry for a Bidirectional I/O pin in the IEEE 1149.1 methodology. **[5]**

b) List and explain the different factors for the selection of BIST architecture. **[5]**

Q7) a) Explain any two techniques of DFT to increase controllability, observability & predictability. **[4]**

b) List out the various functions carried out by BIST controller. Draw and explain with neat diagram the Generic Off-line BIST architecture. **[4]**

c) Write a short note on PLA testing. **[2]**

Q8) a) Explain fault propagation using D-algorithm for the circuit shown in figure 4. **[4]**

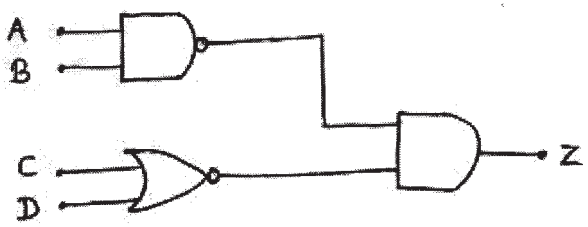

Figure 4

b) Explain in detail the random testing technique and suppose that the tests W1, W2, W3, W4=0100, 1010, 0011,1111 and 0110 are chosen randomly to test the figure 5. Derive and calculate percentage of single faults detected. **4]**

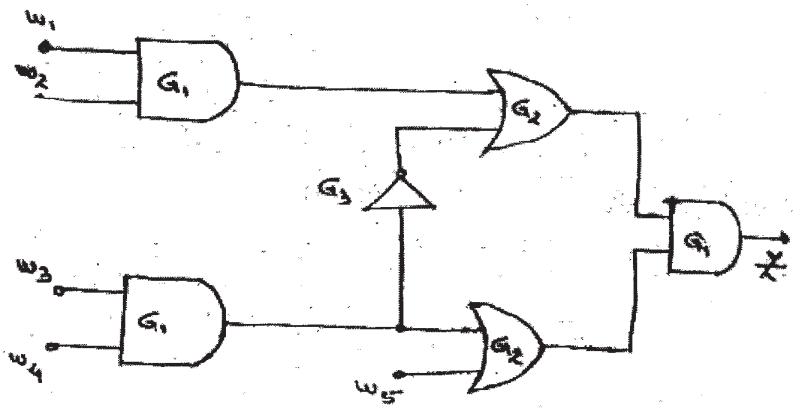

Figure 5

c) Write short note on ATG systems. **[2]**

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