Total No	o. of Questions : 8] SEAT No. :	
P620	[Total No. of Pages	::2
	[5869]-242	
	S.E. (Electronics & Telecommunication)	
	ELECTRONIC CIRCUITS	
	(2019 Pattern) (Semester - III)	
Time . 2	[Max. Marks :	. 70
	tions to the candidates:	. 70
1)	Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.	
2)	Figures to the right indicate full marks.	
3)	Neat diagrams must be drawn whenever necessary.	
4)	Make suitable assumptions whenever necesary.	
Q1) a)		the
		[6]
b)		[6]
c)	Design an adjustable voltage regulator using LM317 for output volta	_
	1.25V to 15V and draw necessary connection diagrams. Assur	
		[6]
00)	OR	
Q2) a)		
1. \		[6]
b)		[6]
c)	Explain the concept of current boosting with necessary diagram.	[6]
Q3) a)	An emitter biased Dual input balanced output differential amplifie	has
~ /	the following specifications:	
	$V_{CC} = \pm 12 \text{ V}, R_{CC} = 3.7 \text{k}\Omega \text{ and } R_{E} = 4.2 \text{k}\Omega,$	
	the following specifications: $V_{CC} = \pm 12 \text{ V}, R_{CC} = R_{C2} = 3.7 \text{k}\Omega \text{ and } R_{E} = 4.2 \text{k}\Omega, \\ \beta = 100 \& V_{BE} = 0.7 \text{ V}. \text{ Calculate:} \\ \text{i)} \text{Voltage Gain (Ad)} \\ \text{ii)} \text{Input Resistance (Ri)} \\ \text{iii)} \text{Output Resistance (Ro)} \\ \text{Define the following characteristics of OP AMP}$	
	i) Voltage Gain (Ad)	
	ii) Input Resistance (Ri)	
	iii) Output Resistance (Ro)	[6]
b)	Define the following characteristics of OP AMP	
	i) input bias current	
	ii) Slew rate	
	iii) CMRR	[6]
c)	Explain Current mirror circuit with neat diagram.	[5]
	OR OR	

P.T.O.

Q4)	a)	Draw a block diagram of the op-amp and explain in detail.
	b)	Find the Q point for a Dual input Balanced output differential amplified with RC=RE=65Kohm. Supply voltage used is ±15V, VBE=0.7V. [6]
	c)	Compare ideal & practical parameters of an Op-amp. [5]
Q 5)	a)	Draw and inverting summing amplifier with three inputs and derive expression for its output voltage $V_0 = -(V_a + V_b + V_c)$. [6]
	b)	Draw a circuit diagram of three op-amp Instrumentation amplifiers and write its output equation. [6]
	c)	Design and inverting Schmitt Trigger circuit whose V_{UT} and V_{LT} are $\pm 5V$ Draw input and output waveforms. Assume op-amp saturates at $\pm 13.5V$
		OR
Q6)	a)	Design a practical integrator with input signal of 2Vpp and cut of frequency of 2.5KHz for DC voltage gain of 10. [6]
	b)	Explain in detail the working of square wave generators with a neat circuid diagram. draw waveform of output voltage and capacitor voltage. [6]
	c)	Explain the operation of a precision full wave rectifier with necessary waveforms. [6]
Q 7)	a)	Draw block diagram and explain any one application of IC PLL 565 in detail.
	b)	Draw circuit diagram and explain D/A converter with binary weighted resistors and give output voltage equation $V_o=?$
	c)	With neat circuit diagram explain V to I converter. OR
Q 8)	a)	For PLL IC 565 define and give expression of free running frequency lock range and capture range. [6]
	b)	Design a PLL circuit using 565 IC to get free running frequency 4.5KHz lock range 2 KHz and capture range 100 Hz. Assume supply voltage of ± 10V.
	c)	With neat circuit diagram explain I to V converter. [5]