Total No of Questions: [08] *SEAT NO. :* [ ]

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S.E. 2012 (E&TC Engineering)

Integrated Circuits (204187)

(Semester - II)

Time: 2 Hours ***Max. Marks : 50***

Instructions to the candidates:

1) ***Neat diagrams and waveforms must be drawn wherever necessary.***
2) ***Figures to the right side indicate full marks.***
3) ***Use of Calculator is allowed.***
4) ***Assume Suitable data if necessary.***

Q1) a) State any four characteristics of an ideal OPAMP? **[02]**

b) A dual input, balanced-output (DIBO) differential amplifier has following specifications: $R_{C1} = R_{C2} = 2.2\ K\Omega$, $R_E = 4.7\ K\Omega$, $R_{in\ 1} = R_{in\ 2} = 50\ \Omega$, $+V_{CC} = 10V$, $-V_{EE} = -10\ V$, $\beta_{dc} = \beta_{ac} = 100$ and $V_{BE} = 0.715V$. Calculate **[04]**

i) I_{CQ}

ii) V_{CEQ}

iii) Voltage gain: A_d

c) Why frequency compensation is required in OPAMP? Explain dominant pole compensation with circuit & frequency response. **[06]**

OR

Q2) a) Give the classification of ICs according to number of components per chip? **[02]**

b) An inverting amplifier using IC741 OPAMP has flat frequency response up to 40 KHz, voltage gain of 10. Find maximum peak – to peak input voltage to get maximum distortion less output? **[04]**

c) Why level shifter / translator is needed in an OPAMP? What are its different types? Explain level shifter with constant current bias using diodes. **[06]**

Q3) a) Draw an inverting summing amplifier with three inputs? Derive an expression for its output voltage $V_O = -(Va + Vb + Vc)$. **[06]**

b) Draw half wave precision rectifier & explain its operation in brief ? **[03]**

c) Draw an inverting comparator using OPAMP with +ve reference & explain its operation in brief with waveforms? **[03]**

OR

Q4) a) For an inverting Schmitt trigger $R1 = 100\Omega$, $R2 = 56K\ \Omega$ (where R2 is connected in feedback path) . If $Vin = 1V_{(P-P)}$ sine wave and $Vs = \pm 15V$, calculate: **[02]**

i) V_{UT} & V_{LT}

b) Draw & explain in brief an instrumentation amplifier interfaced with RTD bridge for temperature measurement. **[06]**

c) Draw & explain in brief a sample &hold circuit with waveforms? **[04]**

Q5) a) In a V-I converter with grounded load, Vin = 5V, R = 10KΩ and voltage at noninverting terminal is 1V. Assuming that OPAMP is initially nulled, Calculate: **[04]**

i) Load current

ii) The output voltage Vo

b) Draw a 2-bit D/A converter with R-2R resistors & explain its operation? State its advantages? **[05]**

c) Explain various specifications of A/D converter. **[04]**

OR

Q6) a) Draw an I-V converter and derive an expression for its output voltage (Vo)? **[04]**

b) Draw & explain 2-bit flash type analog to digital converter (ADC) **[05]**

c) An 8-bit D / A converter has a resolution of 10 mV / bit. Find the analog output voltage for the following digital inputs: **[04]**

i) 10001010

ii) 00010000

Q7) a) Draw the block schematic of PLL and explain each block in detail. **[07]**

b) Design an adjustable voltage regulator using LM317 for following specifications: **[04]**

Output voltage, Vo = 5V to 12V

Output current, Io = 1A and R1 = 240Ω (R1 is connected between o/p terminal & adj terminal).

c) Explain the following terms: **[02]**

i) Load regulation

ii) Line regulation

OR

Q8) a) For a PLL 565, the free running frequency is 2.5KHz, +Vcc = +10V, $-V_{EE}$ = -10V. If demodulation capacitor (C2) is 10μF, find lock range & capture range. **[04]**

b) State applications of PLL? Also draw block diagram of FSK demodulator. **[05]**

c) Draw & explain a three terminal voltage regulator with current boosting. **[04]**