Total No. of Questions : 8]

SEAT No. :

P4393

[Total No. of Pages : 2

[4960]-1259
M.E. (E&TC) (VLSI & Embedded Systems)
FAULT TOLERANT SYSTEMS
(2013 Pattern)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Solve any five questions.***
2) ***Draw neat diagrams wherever necessary.***
3) ***Assume suitable data if necessary.***

Q1) a) Define wired logic mechanism. Explain in detail with diagram wired AND logic and bidirectionality. **[6]**

b) Write a short note on Truth table and Primitive cubes. **[4]**

Q2) a) Define unknown logic value. Construct AND truth table of 6-valued logic for static hazard analysis. **[6]**

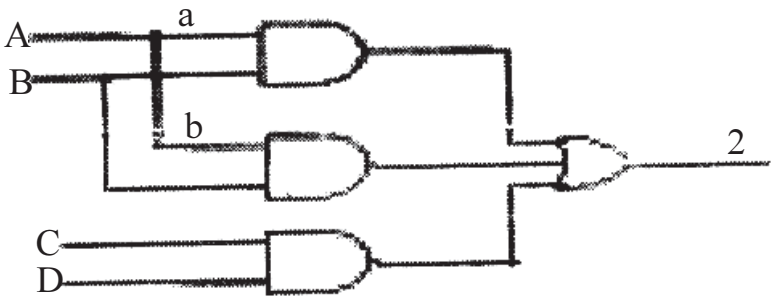
b) Write a short note on Fault simulation techniques. **[4]**

Q3) a) For circuit shown. **[8]**

i) Find the set of all tests that detect the faults a s-a-0.

ii) Find the set of all tests that detect the faults b s-a-0.

iii) Find the set of all tests that detect the multiple faults.



b) Write Short Note On : Delay models **[2]**

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Q4) a) Classify in detail different faults models. Specify their advantages. &disadvantages. **[6]**

b) Explain Parallel fault simulation in detail with appropriate example. **[4]**

Q5) a) Explain the necessity of compression techniques. List out different compression techniques and write the features of each technique. **[6]**

b) What are the drawbacks of conventional testing approach. List out general aspects of compression techniques. **[4]**

Q6) a) What is mean by error masking? List out the techniques to measure masking characteristics in compression techniques. **[6]**

b) With neat diagram explain in detail the compression techniques which provides excellent fault and error coverage. **[4]**

Q7) a) Classify and explain less memory storage testing approach in detail with neat diagram. **[5]**

b) Define the following terms. **[5]**

i) Fault location

ii) Fault propagation

iii) Fault justification

iv) Fault Efficiency

Q8) a) Differentiate between on line and offline BIST. Explain in detail the off line BIST architecture at the board level. **[5]**

b) List and define important factors that determine the complexity of deriving a test for a circuit. **[5]**