Total No. of Questions : 8]

SEAT No. : ____

PA-938

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B.E. (Electronics & Telecommunication Engineering)

VLSI DESIGN & TECHNOLOGY

(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates :

1) ***Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume sitable data, if necessary.***

Q1) a) Draw and explain the architecture of CPLD. Explain Macrocell in detail. **[10]**

b) What are the technologies supported by FPGA? Explain any two of it detail. **[8]**

OR

Q2) a) List and Explain in brief various Simulation and Synthesis Tool. **[6]**

b) Draw and Explain the following for FPGA : **[12]**

i) Logic Cell

ii) Programmable Switch Matrix

iii) I/O Block

Q3) a) Design CMOS logic for F = AB + C(D+E). **[5]**

b) Draw 2:1 Mux using CMOS as well as TG. Comment on the savings of transistors using TG and CMOS method. **[12]**

OR

Q4) a) Define Scaling and Explain any one type of scaling and its effect on at least 4 parameters. **[9]**

b) Explain the following terms : **[8]**

i) Velocity Saturation

ii) Hot Electron Effect

P.T.O.

Q5) a) Which Lambda rules are used for CMOS Layout? Give its significance. **[6]**

b) Explain the steps involved in fabrication of CMOS transistor with suitable diagram. **[12]**

OR

Q6) Draw the block diagram of half adder and its truth table. Draw it CMOS transistor level circuit. Draw Euler's Path for both networks. Draw the stick diagram for sum and Carry (outputs) of HALF ADDER. **[18]**

Q7) a) Explain different types of faults existing in VLSI chips. **[8]**

b) Explain Controllability. Observability and Predictability in testability. **[9]**

OR

Q8) a) Explain Path sensitization method. **[8]**

b) Explain JTAG boundary Scan, Explain all the pins involved. **[9]**

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