Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5252]-139

S.E. (Elect/E&TC) (Second Semester) EXAMINATION, 2017

COMPUTER ORGANIZATION

(2012 Pattern)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Draw the block diagram of basic structure of computer and explain function of each block. [6]

(*b*) Give the IEEE standard for floating point numbers for :

(*i*) Single precision number

(*ii*) Double precision number [6]

Or

2. (*a*) Draw and explain single bus organization. [6]

(*b*) Multiply (7) and (3) using Booths algorithm. Register size 5 bits. [6]

3. (*a*) Compare RISC and CISC processor. [6]

(*b*) Write a short note on PCI BUS. [6]

P.T.O.

Or

4. (*a*) Write control sequence for instruction MOVE (R1), (R2) using single bus organization. [6]

(*b*) What is BUS arbitration ? Explain Daisy chain and polling method. [6]

5. (*a*) Explain cache memory. Why is it used ? [6]

(*b*) Explain the connection of memory to processor. [7]

Or

6. (*a*) Explain the memory hierarchy of computer system. [6]

(*b*) Explain the concept of virtual memory ? How virtual memory addresses is translated to physical memory address ? [7]

7. (*a*) List out addressing modes of 8086. [6]

(*b*) Explain interrupt structure of 8086. [7]

Or

8. (*a*) Explain the following addressing modes of 8086 with suitable example : [6]

(*i*) Direct addressing

(*ii*) Register addressing

(*iii*) Immediate addressing

(*b*) Draw flag structure of 8086 and explain operation of each flag. [7]