Total No. of Questions : 8]

SEAT No. :

**P4013**

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## M.E. (E&Tc) (VLSI & Embedded System Design)

## ANALOG CMOS DESIGN

## (2013 Pattern) (Semester - II)

*Time : 3 Hour]* *[Max. Marks : 50*

***Instructions to the candidates :***

1) ***Answer any Five questions.***
2) ***Figures to the right indicate full marks.***
3) ***Use of electronic pocket calculators is allowed.***
4) ***Assume suitable data, if necessary.***

***Q1)*** a) Discuss the effect of channel length modulation and body effect on MOSFET and show how these are taken care of in small signal equivalent model. **[5]**

b) For the circuit of CS amplifier with diode connected load as shown in Fig. 1, calculate small signal voltage gain if $(W/L)_1 = 50/0.5$. $(W/L)_2 = 10/0.5$ and $I_{D1} = 0.5$ mA. Assume $\mu_n C_{ox}$ $2\mu_p C_{ox} = 60$ $\mu A/V^2$. Also find voltage gain if $M_2$ is PMOS. Neglect second order effects. **[5]**

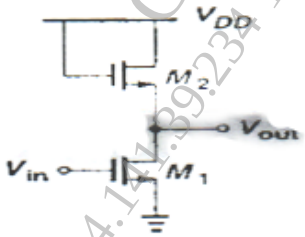


Figure 1

***Q2)*** a) With the help of suitable schematic and expressions, explain MOSFET as a switch, diode and active resistor. **[5]**

b) What is band gap reference circuit, draw any one band gap voltage or current reference circuit and explain the same. **[5]**

***P.T.O.***

***Q3)*** a) List and elaborate the important performance parameters of CMOS operational amplifier. **[5]**

b) Draw cascode amplifier with current source load and list its advantages and limitations over single stage CS and CG amplifier. **[5]**

***Q4)*** a) Determine the differential and common mode voltage gain of the circuit shown in Fig 2. Assume $\lambda \neq 0$, also $M_1$ and $M_2$ are identical and $M_3$ and $M_4$ also. Also find CMRR. assume non ideal tail current source with internal resistance $R_{ss}$. **[5]**

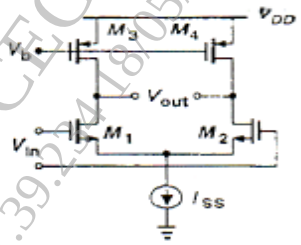


Figure 2

b) Draw circuit diagram of two stage CMOS op amp and explain its working. **[5]**

***Q5)*** a) List and elaborate static characteristics of Digital-to-Analog converter. **[4]**

b) How zeros work as bandwidth enhancers, give expression of bandwidth of such circuit. **[4]**

c) What is effect of source degeneration resistance on the voltage gain of CS amplifier? **[2]**

***Q6)*** a) Write short notes on **[6]**

i) Tuned amplifiers

ii) DAC topologies in CMOS monolithic circuits

iii) High speed op amps

b) Explain in detail open and short circuit techniques for bandwidth estimation. **[4]**

***Q7)*** a) What is difference between active and passive mixers. Draw' and explain their architectures. **[5]**

b) List and elaborate the design considerations for RF chip. **[5]**

***Q8)*** a) Draw circuit diagram of differential LNA and explain how it overcomes drawbacks of single ended LNA. **[5]**

b) With the help of different Low Noise Amplifier (LNA) topologies explain how noise and power trade off is achieved. **[5]**

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