Total No. of Questions : 8]

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M.E. (E & TC) (VLSI and Embedded Systems)

SYSTEM ON CHIP

(2017 Pattern) (Semester-II)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:

1) ***Answers any five questions. Each questions carry 10 marks and each bit carries 5 marks.***
2) ***Draw the neat diagram whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data whenever necessary.***

Q1) a) What is the Need for Concurrent Models?

b) Explain the limitations of Control flow models?

Q2) a) What are pipeline hazards? How pipeline hazards can be handled.

b) How to determine the hardware implementation of an FSMD?

Q3) a) Explain the Hardware schematic for a counter with Timing Diagram.

b) Write ASIP Design flow & How ASIP design flow show better performance that SOC design based on hardware.

Q4) a) What is Simulation - Synthesis Mismatch?

b) Which are the Factors Affecting Delay and Slew?

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Q5) Explain the difference between the following terms:

a) Control hazard and data hazard

b) One-Way and Two-Way Handshake

Q6) a) What are Causes of Power Dissipation?

b) What is the need of memory optimization and management in SoC?

Q7) a) Explain different Timing Parameters for Digital Logic?

b) Explain the Important Issues for Embedded Compilers.

Q8) a) What are the Design Issues and Techniques for image codec?

b) Explain energy management techniques for SoC design.

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