Total No. of Questions : 8]

SEAT No. :

P4142

[Total No. of Pages : 3

[5255]-640

M.E. (E & TC) (VLSI and Embedded Systems)

ASIC DESIGN

(2013 Pattern) (Semester-III) (604202)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Explain in brief the combinational and sequential modelling with an example. **[4]**

b) What is ASIC library? What is need of library? **[3]**

c) Discuss the economics of using ASICs in a product. **[3]**

Q2) a) Explain the various steps in ASIC design. **[4]**

b) Write a VHDL code for a sequence detector, which detects the sequence '10101' using Mealy Machine. **[4]**

c) Differentiate between channelled and channel less Gate Array. **[2]**

Q3) a) What is mean by Gate Level Simulation? **[4]**

b) What is cross talk noise in context of ASIC design? How it can be avoided? **[4]**

c) Explain the different timing parameters used for Static Timing Analysis. **[2]**

P.T.O.

Q4) a) What is mean by signal integrity problem? How to overcome it? **[4]**

b) What are the different testing approaches for mixed signal Analogue and Digital circuits? **[3]**

c) Explain signal integrity effects in ASIC design. **[3]**

Q5) a) What are different objectives of system partitioning and explain different algorithms used for the same. **[4]**

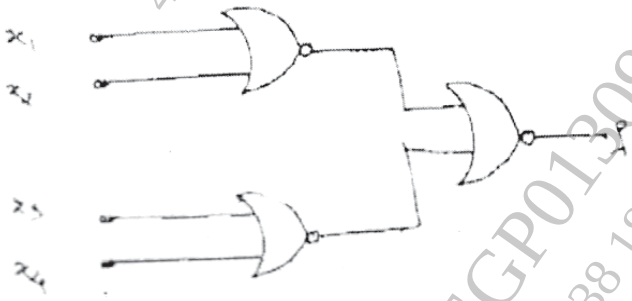
b) What is force directed placement algorithm? Explain different force directed placement algorithms. **[3]**

c) What are the different approaches for global routing? **[3]**

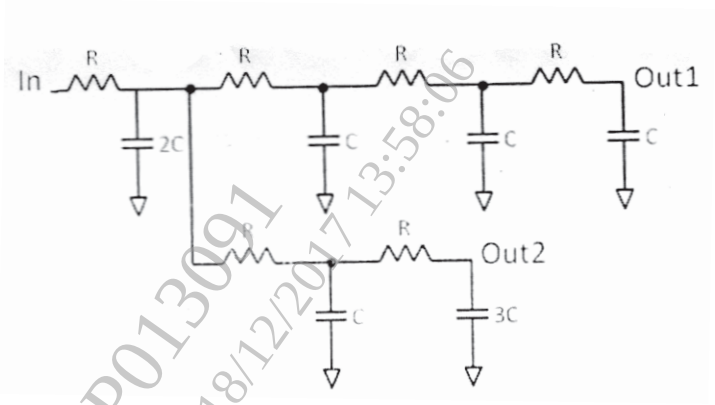
Q6) a) What is system partitioning? Explain any one algorithm used for system partitioning? **[4]**

b) Differentiate pre layout and post layout simulation with respect to ASIC. **[3]**

c) Classify fault Model. Find the Test Set for the Circuit Shown in Fig. 1. to find the maximum fault coverage. **[3]**



Q7) a) Consider the RC network given below: **[5]**



i) Calculate the Elmore's delay from In to Out 1 and from In to Out 2. Which one is critical path?

ii) Assume R = 100Ω and C = 10fF, Calculate the Elmore's delay of the critical path you find in part 1.

b) Explain the ASIC verification and its issues. Write the features of any four EDA tools. **[5]**

Q8) a) Write short notes on (any two): **[5]**

i) Design Reuse

ii) Simulation

iii) Controllability and Observability

b) Explain the Boundary Scan Test. **[5]**