Total No. of Questions : 8]

SEAT No. :

P1105

[Total No. of Pages : 3

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S.E. (E & TC/Electronics) (Semester - I)

ELECTRONIC DEVICES AND CIRCUITS

(2012 Course)

Time : 2 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of logarithmic tables slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) For the circuit shown in the Figure No.1, with transistor $\beta = 55$, find the Q point and stability factor S. **[6]**

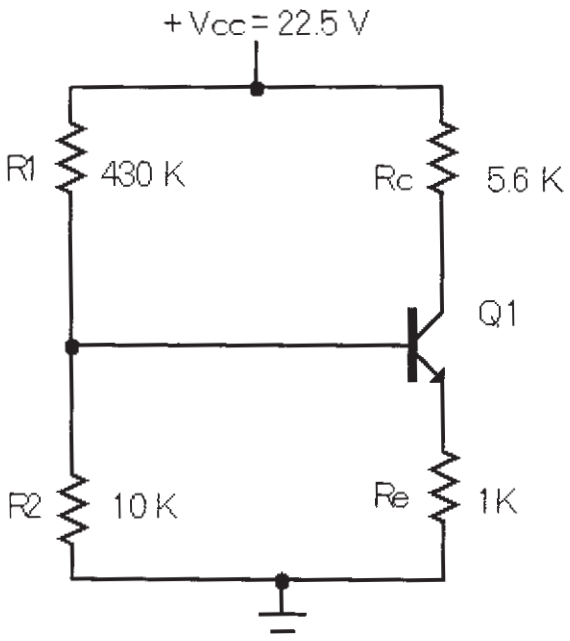


Figure No. 1

b) Draw circuit diagram of a Darlington emitter follower. Explain why it's input impedance is higher than that of a single-stage emitter follower. How to improve input impedance of Darlington emitter follower further high. **[6]**

OR

P.T.O.

Q2) a) Define Bias Stabilization and Compensation Techniques. Draw circuits which uses diode to compensate for changes in V_{BE} and Ico. **[6]**

b) Determine Ai, Ais, Ri, Av, Avs, Ro for a Common Emitter BJT Amplifier having Rs = 1 $K\Omega$ and RL = 10 $K\Omega$. The h-parameters for the BJT are, hie = 1.1 $K\Omega$, hre = 2.5 x 10-4, hfe = 50, hoe = 25 μA/Volts. (Ignore effect of biasing resisters and Re is bypassed with high value capacitor). **[6]**

Q3) a) For a BJT, at room temperature and Ic = 1.3 mA, determine f_β and f_T. Consider hfe = 50, Ce = 1 pF and Cc = 0.2 pF. **[6]**

b) State effect of negative feedback on Input Impedance, Output Impedance, Gain, Bandwidth for Voltage Amplifier, Trans-conductance Amplifier, Trans-resistance Amplifier & Current Amplifier. **[6]**

OR

Q4) a) Explain, how Step Response of an Amplifier can be used to determine its Bandwidth. **[6]**

b) Draw circuit diagram of transistorized Hartley Oscillator. Explain, how this circuit satisfies the minimum criteria to generate sustained oscillations. Calculate frequency of oscillations for the circuit if

$C = 100\,nF, L_1 = 100\,\mu H \& L_2 = 150\,\mu H$. **[6]**

Q5) a) What is large signal amplifier? How it is different from small signal amplifier? Classify them on the basis of operating point position and compare their performance in terms of maximum conversion efficiency. **[7]**

b) A transistor amplifier supplies 5mW to a 100Ω load. Its dc collector current is 12rnA. If the second-harmonic distortion must stay within 10%, determine the peak collector current (with signal) allowed in the transistor. **[6]**

OR

Q6) a) Draw circuit diagram of Class-B Push-Pull power amplifier using power BJTs. If BJTs in it are not perfectly matched, show output waveforms with sine wave input. Suggest changes in the circuit to eliminate any distortions that may occur in the output. **[7]**

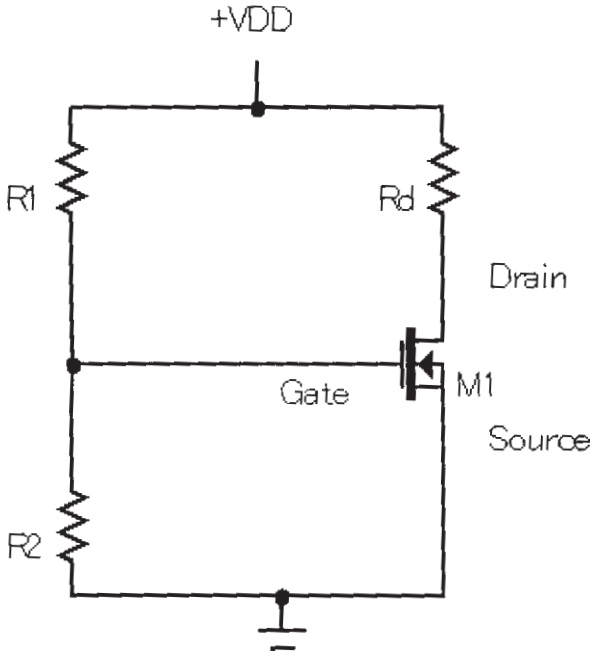
b) A complementary - symmetry power amplifier has capacitive coupled load $R_L = 8\Omega$ supply voltage $\pm$ 12V calculate, **[6]**

i) P_{ac} max.

ii) P_D of each transistor.

iii) Efficiency.

Q7) a) The transistor in Figure 3 has parameters V_{TN} = +2V and Kn = 0.25 mA/V^2. The circuit parameters are V_{DD} = 10V, R_1 = 280 kΩ, R_2 = 160 kΩ, and R_D = 10 kΩ. Find I_D, V_{DS}. **[6]**



b) Explain the following non-ideal characteristics of MOSFET: **[7]**

i) Breakdown effect,

ii) Body Effect,

iii) Subthreshold conduction,

iv) Temperature effect.

OR

Q8) a) Determine the small-signal voltage gain of a E-MOSFET Common Source circuit Assume circuit parameters : V_{GSQ} = 2.12 V, V_{DD} = 5V, and R_D = 2.5 kΩ. Assume transistor parameters: V_{TN} = 1V. K; = 0.80 mA/V^2, and $\lambda = 0.02V^{-1}$. Assume the transistor is biased in the saturation region. **[6]**

b) Draw diagrams and state need of

i) Constant Current Source Biasing Circuit for E-MOSFET. **[4]**

ii) Bi-MOS Transistor. **[3]**