Total No. of Questions : 8]

SEAT No. :

P4305

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[4860]-1254

M.E. (E & TC) (VLSI & Embedded Systems)

RECONFIGURABLE COMPUTING

(2013 Credit Pattern) (Semester-I)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data if necessary.***

Q1) a) Give the key differences between reconfigurable machines and conventional processors. **[4]**

b) Explain the distinguishing features of Configurable, Programmable, and fixed-Function devices. **[4]**

c) Draw 2 context 4-LUT and explain its working for combinational and sequential configuration. **[2]**

Q2) a) Explain with suitable the metrics Functional Capacity, Data Density and Functional Diversity. **[5]**

b) Compare ASIC, GPP, FPGA, Memory, RALU, PDSP, CPLD and RD with respect to power consumption, design efforts, throughput and NRE, speed and time to market. **[5]**

Q3) a) Explain in detail the issues in Reconfigurable network design. **[4]**

b) State Rent rule and explain Rent rule based hierarchical interconnect model. **[4]**

c) State the effects of interconnect granularity. **[2]**

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Q4) a) Find the number of bits required to specify each LUT's interconnect for a 1000 4-LUT device with 200 inputs compare it with bits required by 9000 4-LUT device with 600 inputs and comment on it. **[4]**

b) Elaborate the term "Multi Context Device", with proper diagram. **[4]**

c) Define the term instruction distribution bandwidth. **[2]**

Q5) a) State and explain various methods for instruction stream compression. **[4]**

b) Explain the RP space area model. **[4]**

c) Elaborate the term "coarse grain" and "fine grain". **[2]**

Q6) a) Give the basic architecture of DPGA and explain multicontext 4-LUT from it. **[5]**

b) Explain with suitable diagram the Array element of DPGA. **[5]**

Q7) a) Draw and explain in brief the architecture of Matrix. **[4]**

b) What are the advantages of MATRIX architecture over general purpose architecture. **[4]**

c) Explain the term partial reconfigurability. **[2]**

Q8) a) Explain the application Rapid prototyping using reconfigurable platform. **[4]**

b) What are Promises of RC to DSP. **[4]**

c) Explain the relation between Design W and Architecture W. **[2]**

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