

Total No. of Questions : 6]

SEAT No. :

PC393

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[Total No. of Pages : 2

S.E. (ELECTRONICS / E&TC/Electronics & Computer (Electronics

Eng.(VLSI Design & Tech.)/Electronics & Comm.-Adv. Comm. Tech.)

DIGITAL CIRCUITS

(Insem)(2019 Pattern) (Semester-III) (204182)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.
- 2) Figures to the right indicates full marks.
- 3) Neat diagram must be drawn wherever necessary.
- 4) Use of non-programmable calculator is allowed.
- 5) Assume suitable data, if necessary.

Q1) a) Explain the following characteristics of digital IC's: [6]

- i) Figure of Merit
- ii) Propagation delay.
- iii) V_{IH} and V_{OH}

b) Draw and explain the working of CMOS Inverter. [4]

OR

Q2) a) Draw and explain the working of 2- input TTL NAND gate. [6]

List advantages of Totem Pole.

b) Explain the following characteristics of digital IC's: [4]

- i) Noise Margin
- ii) Fan out and Fan in

Q3) a) Design full adder using logic gates. [4]

b) Minimize the following expression using K-map and implement using logic gates : $Y = \sum m(1, 3, 5, 9, 11, 13)$ [6]

OR

P.T.O.

- Q4)** a) Design 3-bit Gray code to Binary converter. [6]
b) Design full subtractor using logic gates. [4]

- Q5)** a) Minimize the following function using K-map and implement it using only NAND gates. [6]

$$F(P,Q,R,S) = \sum m(4,5,6,7,8,12) + d(1,2,3,9,11,14)$$

- b) Compare TTL and CMOS logic families. [4]

OR

- Q6)** a) Explain the current parameters in TTL logic. [4]

- b) Minimize the following function using Quine Mc Clusky method. [6]

$$F(A, B, C, D) = \sum \pi(0, 3, 5, 7, 12, 15) + d(2, 9).$$

