Total No. of Questions : 8]

SEAT No. : [ ]

P3102

[Total No. of Pages : 2

[5670]-201
B.E. (E & TC)
VLSI Design and Technology
(2012 Pattern)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Figures to the right indicate full marks.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Assume suitable data, if necessary.***

Q1) a) Explain Data Objects in VHDL. **[6]**

b) Write the features, specifications and applications of CPLD. **[7]**

c) Write VHDL code and test bench for D FlipFlop. **[7]**

OR

Q2) a) Explore any four attributes in VHDL with suitable example codes. **[6]**

b) Draw and explain the CLB structure of FPGA device. **[7]**

c) Explain clock distribution techniques in detail. **[7]**

Q3) a) Explain static and dynamic power dissipation with suitable mathematical expressions. **[8]**

b) Draw NAND, NOR, EX-OR gates and 2:1 MUX using CMOS. **[10]**

OR

Q4) a) Draw CMOS inverter and explain VTC in detail. **[10]**

b) Explain need for transmission gate. Draw 4:1 MUX using TG. **[8]**

Q5) a) With the help of equivalent circuit explain MOS as diode and resistor. **[8]**

b) Write short note on "Cascade Amplifier". **[8]**

OR

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Q6) a) Draw and explain current mirror circuits. **[8]**

b) Draw and explain current source and sink circuits. **[8]**

Q7) a) Explain TAP controller with state diagram. **[8]**

b) Explain IEEE 1149.1 architecture. **[8]**

OR

Q8) a) Explain different fault models. **[8]**

b) Explain boundary scan architecture. **[8]**