

Total No. of Questions :8]

SEAT No. :

**P3057**

**[4660]-1197**

[Total No. of Pages :2

**M.E. (E&TC) (VLSI & Embedded Systems)**  
**ANALOG CMOS DESIGN**  
**(2013 Credit Pattern) (Semester - II) (504207)**

*Time : 3 Hours]*

*[Max. Marks :50*

*Instructions to the candidates:*

- 1) Answer any FIVE questions.*
- 2) Neat diagrams must be drawn wherever necessary.*
- 3) Assume suitable data if necessary.*

- Q1)** a) Explain in detail MOS as a active diode and resistor. [4]  
b) Write short note on CMOS inverter as an amplifier. [3]  
c) Draw and explain single MOSFET current sink. [3]
- Q2)** a) Draw cascade current sink. What are the techniques to improve  $v_{min}$ . [4]  
b) Justify the necessity of band gap reference. Give the schematic and principle of BGR & conventional BGR. Give the necessary expression. [3]  
c) Explain in detail common source amplifier. [3]
- Q3)** a) Draw and explain CMOS OPAMP. [5]  
b) Explain the concept of low noise OPAMP. [3]  
c) Explain in brief the output amplifier of CMOS OPAMP. [2]
- Q4)** a) Write short note on micro power OPAMP. [5]  
b) Write short note on weak inversion, MOS small signal models & short channel regime. [3]  
c) Draw and explain differential amplifier. [2]

**P.T.O.**

- Q5)** a) Explain in detail switched capacitor. [4]  
b) Write short note on trends in RF chip design. [4]  
c) What are the techniques to improve the bandwidth. [2]
- Q6)** a) Explain the concept of Zero as bandwidth enhancers. [4]  
b) Explain in detail open circuit and short circuit method. [4]  
c) Write short note on Tuned amplifier. [2]
- Q7)** a) Explain the concept of power constrained noise optimization. [5]  
b) Derive the expression for intrinsic MOSFET of two port noise parameter. [5]
- Q8)** a) Explain in detail Low noise amplifier. [5]  
b) Explain in detail the LNA topologies. [5]

*EEE*