Total No. of Questions: 8]	26	SEAT No:
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## B.E.(Electronics & Telecommunication) VLSI DESIGN & TECHNOLOGY (2012 Pattern) (End Semester) (404181)

		[Max. Marks	: 70
Instr	ucti	ions to the candidates:	
	<i>1)</i>	Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.	
	<i>2)</i>	Neat diagrams must be drawn wherever necessary.	
	<i>3)</i>	Assume suitable data, if necessary.	
<b>Q</b> 1)	a)	Explain the following:	[10]
		i) Constants ii) Variables	
		iii) Signals iv) Functions	
		v) Procedures	
	b)	Write VHDL code for half adder by structural and behavioral model	ling
		technique.	[10]
		OR	
<b>Q</b> 2)	a)	Describe the PLD design flow.	[10]
	b)	Write the VHDL programming for D flip-flop and its test bench.	[10]
			7
Q3)	a)	Derive the static and dynamic power dissipations in CMOS.	[7]
	b)	Explain the following terms.	[4]
		i) Clock jitter ii) Clock skew	
	c)	Draw and explain CMOS transfer characteristics.	[7]
		OR OF	
Q4)	a)	Define Scaling and explain any one type of scaling.	[6]
	b)	Explain the following:	[4]
		i) Channel Length Modulation ii) Body effect	
	c)	Explain the working of a transmission gate and Implement a circuit of	f2:1
	•	multiplexer using transmission gate.	[8]

$Q_{3}$	a)	Dra	w and explain active load	Inverter in detail.	[8]	
	b)	-	lain current sink and current sink and current.	rent source and their	characterization with [8]	
				OR		
<b>Q</b> 6)	a)		w and explain CMOS of out resistance.	perational amplifier v	with voltage gain and [8]	
	b)		w the schematic of Cl ressions for output resis		_	
<b>Q7</b> )	a)	Exp	lain the fault models with	n examples.	[8]	
~	b)		lain the need of DFT wit	-	[8]	
	,	1		OR		
Q8)	a)	Dra	w the TAP controller stat	e diagram and explaii	n. [10]	
	b) \	Exp	lain the following terms:	9, 000	[6]	
	7	i)	Partial scan	3		
		ii)	Full scan	5		
		iii)	JTAG			
		,		30.		
			40		B	)
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			7.			
					0,3	
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[515	<b>[4]-6</b> ]	11				
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