Total No. of Questions : 8] **SEAT No. :**

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[6182]-973
M.E.(E & TC) (VLSI and Embedded Systems)
ASIC DESIGN
(2017 Credit Pattern) (Semester - III) (604202)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:

1) ***Attempt any 5 questions out of 8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicates full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) Draw design flow of ASIC Design process and explain each step in detail. **[5]**

b) What is test bench explain with one example. **[5]**

Q2) a) What are different types of ASIC? Classify and explain in details. **[5]**

b) Write VHDL code and test bench code for 8 bit counter. **[5]**

Q3) a) Differentiate floor-planning and placement in ASIC Design. **[4]**

b) Write short note on gate level mixed mode testing. **[4]**

c) List various CAD tools used in ASIC Design process. **[2]**

Q4) a) With neat labeled diagram explain clock distribution technique in ASIC. **[4]**

b) Compare global routing and detailed routing. **[4]**

c) What is placement in ASIC Design? Write its goals and objectives. **[2]**

Q5) a) How false path detection is carried out in application specific intergrated circuits. **[4]**

b) What is the need of time optimization? Give one example which describes time optimization in ASIC. **[4]**

c) Differentiate pre layout simulation and post layout simulation techniques. **[2]**

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Q6) a) What are different signal integrity issues? How it occurred in ASIC design. **[4]**

b) What is functional simulation? Where it is required? Give one example. **[4]**

c) What are the time related constraints? Explain with one example. **[2]**

Q7) a) Describe with one example static timing analysis. **[4]**

b) Describe how memory testing is carried out in ASIC design. **[4]**

c) What are different physical faults occurred in ASIC . **[2]**

Q8) a) Describe in brief Automatic Test Pattern Generator. **[4]**

b) Write short note on Joint Test Action Group. **[4]**

c) Write types and features of existing EDA tools. **[2]**