Total No. of Questions : 8]

SEAT No. :

PA-744

[Total No. of Pages : 2

[5928]-211
M.E. (E & TC) (VLSI and Embedded Systems)
ASIC DESIGN
(2017 Pattern) (Semester - III) (604202)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Attempt any 5 questions out of 8.***
2) ***Neat diagrams must be drawn whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) With neat flow chart explain in detail ASIC Design Flow. **[5]**

b) With neat labeled diagram describe different types of ASIC. **[5]**

Q2) a) Explain VHDL code and test-bench code for D-flip-flop. **[5]**

b) Write short note on logic synthesis and simulation. **[5]**

Q3) a) Differentiate floorplanning and placement in ASIC design. **[4]**

b) How to reuse any ASIC design? Give one example. **[4]**

c) List different CAD tools used in ASIC Design. **[2]**

Q4) a) With neat labeled diagram explain clock distribution technique in ASIC. **[4]**

b) Differentiate global routing and detailed routing. **[4]**

c) Give example of Left-edge algorithm and comment on it. **[2]**

Q5) a) How false path detection is carried out in application specific integrated circuits. **[4]**

b) Write short note on static timing analysis. **[4]**

c) How to estimate logic delays in sequential logic design. **[2]**

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Q6) a) Write short note on mixed mode design in ASIC. **[4]**

b) Describe in brief signal integrity issues in ASIC Design. **[4]**

c) What are the time related constraints? Explain with one example. **[2]**

Q7) a) Draw and explain linear feedback shift register in detail. **[4]**

b) Write short note on Joint Test Action Group. **[4]**

c) Explain basic automatic test pattern generator (ATPG) algorithm for $A'B + BC$ **[2]**

Q8) a) Explain in detail physical faults occured in ASIC. **[4]**

b) Write short note on memory testing. **[4]**

c) Differentiate Scan test Vs Partial test. **[2]**

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