Total No. of Questions : 8]

SEAT No. :

**P4307**

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# [4860]-1257

## M.E. (ETC) (VLSI & Embedded System)

## SYSTEM ON CHIP

## (2013 Credit Pattern) (Semester-II) (504208)

*Time : 3 Hours]* *[Max. Marks : 50*

***Instructions to the candidates:***

1) ***Answer any 5 questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***All questions carry equal marks.***
4) ***Your are advised to attempt not more than 5 questions.***
5) ***Your answers will be valued as a whole.***
6) ***Assume suitable data, if necessary.***

***Q1)*** a) Explain control flow modeling.

b) Describe software implementation of data flow.

***Q2)*** a) How to determine the H/W implementation of an FSMD?

b) What is One-way and two-way Handshake?

***Q3)*** a) Discuss why it is a bad idea to model datapath expressions as FSM.

b) Explain time multiplexing of two hardware module ports over a single control shell.

***Q4)*** a) What are the limitations of FSM?

b) Write ASIP Design flow and how ASIP design flow show better performance than SOC design based on hardware.

***Q5)*** a) What is motion compensation (MC)?

b) Explain combinational Read-write Race.

***P.T.O.***

***Q6)*** a) What is Simulation-Synthesis Mismatch?

b) Explain causes of power dissipation.

***Q7)*** a) Which are the Factors Affecting Delay and Slew?

b) What is the need of memory optimization and management in SOC?

***Q8)*** a) Explain any one Real time dynamic voltage scaling scheduling algorithm.

b) Explain Energy Management Techniques for SOC Design.

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