Total No. of Questions : 8]

SEAT No. :

P3060

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[4660]-1202
M.E. (E&TC -VLSI and Embedded Systems)
ASIC DESIGN
(Semester-III) (2013 Credit Pattern) (604202)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Attempt any five questions out of 8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Draw the design flow for an ASIC design process and explain each step. **[4]**

b) Classify and explain in detail gate array based ASIC. **[3]**

c) What is test bench? Explain with example. **[3]**

Q2) a) Explain the terms: **[3]**

i) Constants

ii) Attributes

iii) Variables

b) Explain in brief the combinational and sequential modelling with respect to 4 bit multiplexer and 4bit SISO shift register. **[5]**

c) Write a short note on static Timing Analysis. **[2]**

Q3) a) Explain the terms: **[4]**

i) Gate level simulation

ii) Switch level simulation

iii) Transistor level simulation

b) Explain mixed mode synthesis of ASIC. **[3]**

c) Write a note on gate level mixed mode testing. **[3]**

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Q4) a) Explain the practical aspects of mixed signal analog digital design. **[5]**

b) Write in brief about signal integrity effects in ASIC design. **[5]**

Q5) a) Explain with step by step process K-L algorithm for system partitioning. **[5]**

b) Differentiate between Global routing and detailed routing. Calculate Elmore constants for node 4 and node 2 for the circuit shown in fig.1. **[5]**

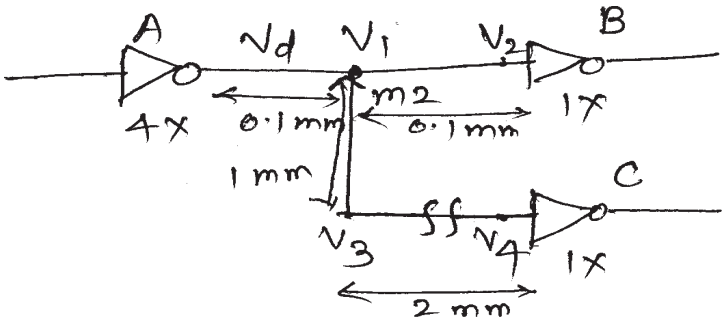

fig. (1)

Given Parameters

- m_2 resistance 50 m Ω/square
- m_2 capacitance 0.2 PF/mm
- 4x inverter delay is 0.02 ns+0.5 C_L n_S
  (C_L is in PF)
- Delay is measured using 0.35/0.65 output trip points
- m_2 minimum width is 3 λ=0.9μm
- 1x inverter input capacitance is 0.02 PF

Q6) a) List the goals and objectives for ASIC physical design steps. **[4]**

b) Explain wrt floorplanning: **[3]**

i) Channel capacity

ii) Channel density

iii) Channel allocation and ordering

c) What are the different approaches to global routing? **[3]**

Q7) a) Write short note on any two: **[4]**

i) Features of EDA tools

ii) Issues in verification

iii) Testing techniques used in ASIC design.

b) Briefly describe about boundary scan testing. **[4]**

c) Define the terms, controllability and observability. **[2]**

Q8) a) Explain in detail about ATPG algorithm using test vectors with neat diagram. **[5]**

b) What is the need of testing and explain with neat diagram the SCAN Path arrangement. **[5]**

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