Total No. of Questions : 8]

SEAT No. :

P2729

[Total No. of Pages : 3

M.E. (E & TC) (VLSI and Embedded Systems) (Semester - II)
SYSTEM ON CHIP
(2013 Pattern)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates :

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data if necessary***

Q1) a) What is the need of concurrent model? Explain dataflow model with suitable example. **[4]**

b) Draw CFG and DFG for following C program **[3]**

```
Unsigned char mysqrt(unsigned int N){
Unsigned int x, j;
x=0;
for(j=1<<7;j!=0;j>>=1){
x=x+j;
if(x*x>N)
x=x-j
}
return x;
}
```

c) Design a Mealy type FSM that recognizes pattern of 1l01.The pattern should be read from left to right and they are to be matched into stream of single bits. **[3]**

Q2) a) What is the significance of multirate expansion? Convert the multirate shown in Fig.l into a single rate SDF. **[4]**

Fig. 1

P.T.O.

b) How the control shell maps a custom -hardware module to a hardware-software interface? **[3]**

c) Explain microprogram pipelining and what is the role of pipelined register in microprogram Pipelining. **[3]**

Q3) a) Explain various synchronization schemes adopted by hardware/software interfaces. **[4]**

b) Write a C program calculating mean of five numbers, Design datapath and controller. **[3]**

c) Using the microprogrammed machine, create a program that reads in a number from the input and that counts the number of nonzero bits in that number. The resulting bitcount must be stored in register R7. **[3]**

Q4) a) Fig.2 shows microprogrammed datapath architecture, Develop a horizontal and vertical microinstruction encoding for the list of microinstructions given below : **[5]**

Micro-Instruction:

1) SWAP Rl,R2 ; Exchange R1 and R2
2) ADD Rx, R1,R2; Rx=Rl+R2
3) COPY R1,R2; Rl=R2
4) NOP ; Do nothing

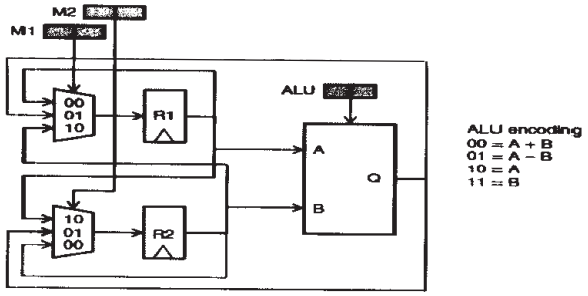

Fig. 2

b) How pipeline stall occurs in RISC architecture? What are the pipeline hazards? How pipeline hazards can be handled. **[5]**

Q5) a) Explain the discrete factors affecting Delay and skew in digital design. **[4]**

b) Explain Baseline JPEG Codec with proper block diagram. **[3]**

c) Explain SoC design flow and verification environment. **[3]**

Q6) a) How metastability is observed due to CDC? What are the ways to solve the problem of metastability. **[4]**

b) Explain the features and architecture of multilayered, quality aware memory controller. **[3]**

c) Explain the factors affecting power in SoC architecture. **[3]**

Q7) a) Explain HW/SW co-design flow of an embedded device and its driver. **[4]**

b) What are the effective timing parameters in RTL Design Explain in brief. **[3]**

c) Explain the methods of reducing the switching power in SoC architecture. **[3]**

Q8) a) What is the need of RTL simulation? How to avoid simulation race in RTL design. **[5]**

b) Explain A simplified architecture of a two-bank SDRAM in detail. **[5]**