Total No. of Questions : 8]

SEAT No. :

P3764

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M.E. (E & TC) (VLSI & Embedded System)

System On Chip

(2013Pattern) (Semester - II)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***All questions carry equal marks.***
4) ***Your are advised to attempt not more than 5 questions.***
5) ***Your answers will be valued as a whole.***
6) ***Assume suitable data, if necessary.***

Q1) a) Draw and explain Hardware Schematic for a counter, timing diagram also.

b) Explain the need for concurrent models.

Q2) a) Explain the limitations of data flow models.

b) Explain the difference between control hazard and data hazard.

Q3) a) Derive and draw CFG and the DFG.

b) Explain the limitations of F.S.M.

Q4) a) Explain the difference between delayed and conditional branch.

b) Which are the different dimensions of the synchronization problem. Explain.

P.T.O.

Q5) a) Explain RTL based chip design flow.

b) Describe the sequential Read-Write Race.

Q6) a) Which are the factors affecting power.

b) Explain the problems due to Metastability.

Q7) a) What is Motion Estimation (ME)?

b) What are the design issues and techniques for image codec.

Q8) a) How dynamic power management is useful in memories system?

b) Explain the important issues for Embedded Compilers.