

Total No. of Questions : 8]

SEAT No. :

[Total No. of Pages : 2

P3159

[5461]-201

B. E. (E & TC)

VLSI DESIGN & TECHNOLOGY

(2012 Pattern) (Semester - I) (End Sem.) (404181)

Time : 2½ Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) *Answer any one question out of Q. No.1 or Q. No.2, Q. No.3 or Q. No.4, Q. No.5 or Q. No.6, Q. No.7 or Q. No.8.*
- 2) *Neat diagrams should be drawn wherever necessary.*
- 3) *Use of electronic pocket calculator is allowed.*
- 4) *Assume suitable data, if necessary.*

- Q1)** a) What do you mean by operator overloading? Explain? [4]
- b) State the Different Data Types used in VHDL with example. [4]
- c) Which and why the structural hierarchy is used in FPGA. Explain? [6]
- d) What do you mean by Supply and Ground Bounce. [6]

OR

- Q2)** a) Write VHDL code for 1100 Mealy sequence detector with test bench. [8]
- b) Draw and explain PAL and PLA. Give example of each. [6]
- c) Define Clock Skew, and Clock Jitter. Explain its effect? [6]

- Q3)** a) What is technology scaling? What are its effects? [4]
- b) Which lambda rules are used for CMOS layout? Give its significance. [4]
- c) Design CMOS logic for $Y = \overline{A(D+E) + BC}$. Calculate W/L ratio for N_{mos} and P_{mos} area needed on chip. [10]

OR

- Q4)** a) Explain transmission gate. States its advantages. Implement a circuit of 2:1 multiplexer using transmission gate. Comment on the number of transistor required using transmission gates and conventional method. [10]

P.T.O.

- b) Explain the following [8]
- i) Velocity saturation
 - ii) Body effect
 - iii) Hot electron effect
 - iv) Channel Length Modulation

Q5) a) Explain with diagram small signal low frequency and small signal high frequency model of MOS transistor. [8]

b) Draw and explain Current sink and source circuits. [8]

OR

Q6) a) Explain Device parasitic and their limitation on the performance of CMOS circuits. [8]

b) Draw and explain current mirror circuits. [8]

Q7) a) Draw and Explain TAP Controller with state diagram. [8]

b) What are the types of faults? Explain with schematic. [8]

OR

Q8) a) What is scan path? Give advantages and disadvantages of scan path. [8]

b) Explain the faults caused by manufacturing defects. [8]

