Total No. of Questions : 8] **SEAT No. :**

P4836 **[Total No. of Pages : 3**

[5060]-743
M.E. (E & TC) (VLSI & Embedded Systems)
FAULT TOLERANT SYSTEMS
(2013 Pattern) (Credit System) (Semester - III)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:-

1) ***Neat diagrams must be drawn wherever necessary.***

2) ***Assume suitable data, if necessary.***

3) ***Solve any five questions.***

Q1) a) Construct a primitive cube table for the following equation. **[3]**

$$F = \overline{X1}\,\overline{X2} + X1\overline{X2} + \overline{X1}X2X3$$

b) What do you mean by Static and Dynamic Hazards? Explain? **[4]**

c) Define unknown logic value and construct truth tables of 3 - valued logic for OR & AND gate. **[3]**

Q2) a) Write short note on Delay Modeling with timing diagrams for different delay models. **[4]**

b) Define and explain Event driven simulation in detail. **[3]**

c) Construct a binary decision diagram for a given function. **[3]**

$$F = A\,\overline{B}\,C + \overline{A}C + BC$$

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Q3) a) For the circuit of figure. 1 **[5]**

i) Find the set of all tests that detects the fault *c s-a-*1.

ii) Find the set of all tests that detects the fault *a s-a-*0.

iii) Find the set of all tests that detects the multiple faults {*c s-a-*1, *a s-a-*0}.

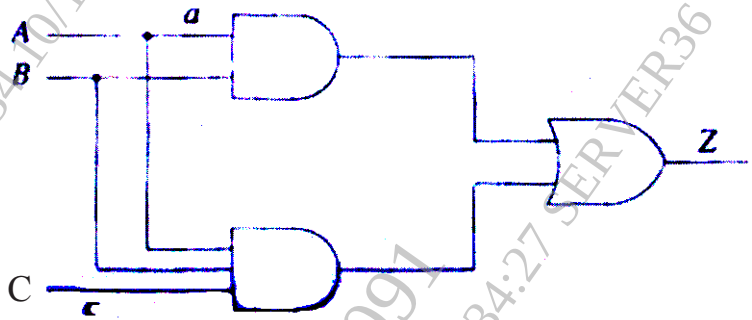

Figure .1

b) Explain in brief **[5]**

i) Fault dominance

ii) Equivalent fault collapsing

iii) Dominance fault collapsing

Q4) a) Explain in detail different fault models. Give their advantages and disadvantages. **[6]**

b) Explain any two techniques of DFT to increase controllability and predictability? **[4]**

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Q5) a) Explain in brief parity check function with self checking 3-bit parity checker and general self-checking parity checker. **[5]**

b) Give classification of different compression techniques. Explain parity check compression. **[5]**

Q6) a) Explain signature analyzer in compression techniques. Also give one Example. **[5]**

b) Write a brief note explaining the working of self checking Berger code. **[5]**

Q7) a) Write short note on built in self test. **[5]**

b) Explain in detail: PLA testing. **[5]**

Q8) a) What is error masking? Give the techniques to measure masking techniques to measure masking characteristics in compression techniques? **[5]**

b) Explain in detail logical fault model. **[5]**

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