

[5255] - 639

M.E. (E & TC) (VLSI & Embedded Systems)

FAULT TOLERANT SYSTEMS

(Semester - III) (2013 Pattern) (604201) (Credit System)

Time : 3 Hours]

[Max. Marks :50

Instructions to the candidates:

- 1) Neat diagrams must be drawn wherever necessary.
- 2) Assume suitable data, if necessary.
- 3) Solve any five questions.

- Q1)** a) Define unknown logic value. Construct the truth table for 2 input NAND gate. Prove that there is a loss of information associated with the use of 3-valued logic. [5]
- b) Explain main flow of Event driven simulation. [5]

- Q2)** a) Explain following delay models for 2 input AND gate with timing diagrams,
i) Rise and Fall delay
ii) Transport delay
iii) Inertial delay [5]
- b) Explain 8 valued logic for static and dynamic hazard analysis. Calculate AND (R, 1*). [5]

- Q3)** a) Calculate equivalent collapse ratio and dominance collapse ratio for the circuit shown in Fig. 1. [5]

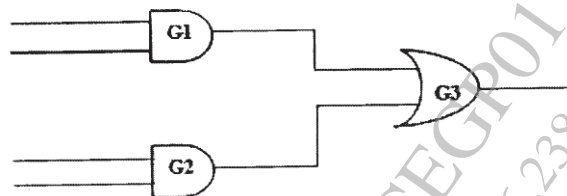
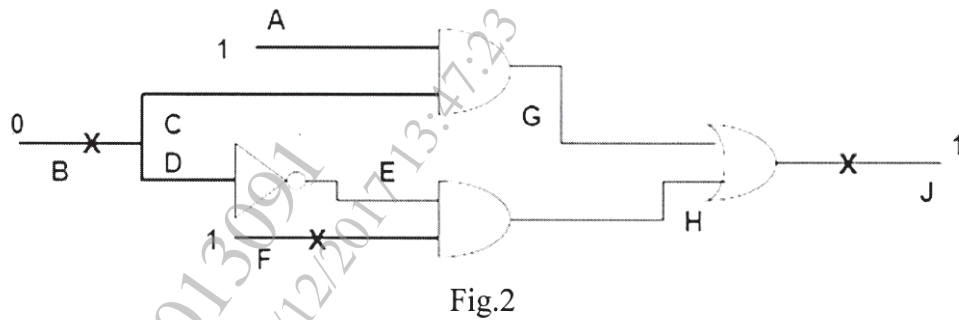


Fig.1

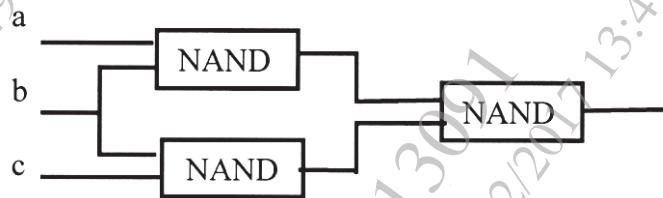
- b) Construct the truth table of an XOR function of two inputs using five composite logic values. [5]

P.T.O.

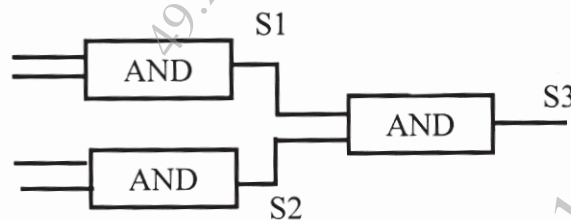
- Q4) a)** Find fault list at J by considering faults B/1, F/0, J/0 for inputs shown in Fig.2 using deductive fault simulation. [5]



- b) For the circuit shown in Fig. 3, [5]
- find the set of all tests that detect the fault c s-a-1
 - find the set of all tests that detect the fault {c s – a – 1, a s – a – 1}



- Q5) a)** Obtain the Berger code for three information bits (I). [5]
- b) Prove that for the following circuit, Syndrome $S3 = S1 * S2$. [5]



- Q6) a)** Prove that residue m must be odd for the Residue code to detect single bit error. [5]
- b) What are the properties of LFSRs that make them suitable for generation of pseudorandom code in signature analysis. [5]

- Q7)** a) Explain different test pattern generation methods for BIST. [5]
- b) Explain following Ad Hoc design for testability techniques. [5]
- Initialization.
 - Monostable Multivibrators.
- Q8)** a) Give classification of BIST techniques. [5]
- b) What is crosspoint fault? Explain different types of crosspoint faults occurred in PLA. [5]

