Total No. of Questions : 8]

SEAT No. :

P2075

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M.E. (E&T/C) (VLSI & Embedded Systems) (Semester - I)

DIGITAL CMOS DESIGN

(2013 Pattern)

Time : 3 Hours] *[Max. Marks :50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) Draw ac equivalent ckt of MOSFET & explain parasitics in detail. **[5]**

b) What is λ parameter? List layout design rules. Draw layout of CMOS Inverter. **[5]**

Q2) a) Explore CMOS fabrication steps in detail. **[5]**

b) What is technology scaling? Explain in brief. **[5]**

Q3) a) Derive the expression for dynamic power dissipation. **[4]**

b) Pertaining to CMOS logic, explain Fan in and Fan out. Explain dependencies analytically. **[4]**

c) Why is MOSFET sizing necessary? What are the effects if sizing is not followed? **[2]**

Q4) a) What is significance of Power Delay Product? Derive the expression. **[4]**

b) Explore delay model in brief. **[4]**

c) Give the expression for static dissipation of certain logic. Compare it with dynamic dissipation. **[2]**

Q5) a) Design CMOS logic for X = ABCD + EF + G. Calculate area on chip. **[4]**

b) What are the types of hazard? Explore any one with suitable example along with solutions. **[4]**

c) Explain limitations of Transmission Gate? What are the solutions? **[2]**

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Q6) a) Design 8:1 Mux using Transmission Gates. Compare with the conventional method. **[4]**

b) What is metastability? Explain the solution in detail. **[4]**

c) What is importance of tristate logic? Draw CMOS tristate logic. **[2]**

Q7) a) Explain the techniques for low power design. **[4]**

b) What is ratioed ckt? Explain with example. **[4]**

c) Compare logic ckt families. **[2]**

Q8) a) With the help of schematic example, explain sense amplifier ckt. **[4]**

b) What is need of BiCMOS ckt? Explore with appropriate logic ckt. **[4]**

c) Write note on static CMOS. **[2]**