Total No. of Questions : 8] **SEAT No. :**

PB3622 **[Total No. of Pages : 2**

[6261]-27
S.E. (E & TC/Electronics/Computer Engineering)
DIGITAL CIRCUITS
(2019 Pattern) (Semester - III) (204182)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q. No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6 and Q.No.7 or Q.No.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume Suitable data, if necessary.***

Q1) a) Explain implementation of full adder using 8 : 1 MUX. **[6]**

b) Explain 3-bit parity checker circuit. **[6]**

c) Implement 1 : 16 demux using 1 : 4 demux. **[6]**

OR

Q2) a) Implement the given logic function using a 4 : 1 multiplexer. **[6]**

f (A, B, C) = $\sum m(0, 1, 2, 4, 7)$

b) Implement 3-bit parity generator circuit. **[6]**

c) Explain the working of a half-subtractor? Draw its logic diagram. **[6]**

Q3) a) Design a circuit to generate the following sequence using D FFs 1011. **[8]**

b) Explain with neat diagram the types of shift register. **[9]**

OR

Q4) a) Design a 3- Bit asynchronous counter using JK FF. **[9]**

b) Convert SR flip - flop into JK flip flop. **[8]**

Q5) a) Write short note on state diagram and state table with suitable example. **[6]**

b) Write short note on Principal Component of an ASM Chart. **[6]**

c) Draw the state diagram of SR flip flop and JK flip flop. **[6]**

OR

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Q6) a) Draw ASM chart for 2 bit binary counter having enable line E Such that : E = 1, Count Enable and E = 0, Count Disable. **[9]**

b) Compare Mealy and Moore machine. **[9]**

Q7) a) Classify and explain the characteristics of memories. **[9]**

b) Implement 3-bit binary to Gray code converter using PROM. **[8]**

OR

Q8) a) Design and implement 2-bit comparator using PAL? **[9]**

b) Explain CPLD architecture. **[8]**

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