Total No. of Questions : 8]

SEAT No. :

P3603

[Total No. of Pages : 2

[4959] - 1081
BE (E & TC)
VLSI Design & Technology (End - Sem)
(2012 Pattern)

Time :2½ Hours] ***[Max. Marks :70***

Instructions to the candidates:-

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Use of electronic pocket calculator is allowed.***
3) ***Assume suitable data, if necessary.***
4) ***Answer any one questions out of Q.1 or Q.2, Q.3 or Q.4, Q5 or Q6, Q.7 or Q.8.***

Q1) a) What is meant by concurrent & sequential statements in VHDL? Explore in detail with two examples of each. **[7]**

b) With the help of suitable schematics, compare PROM, PLA & PAL architectures. What is need of CPLD? **[7]**

c) What is clock skew? Explain the solutions to it. **[6]**

OR

Q2) a) Write VHDL code for Mod - N counter. Write suitable test bench for it. **[7]**

b) Explain PLD targeted design flow in detail. **[7]**

c) What is supply & ground bounce? What are remedies to it? **[6]**

Q3) a) Draw ac equivalent ckt of MOSFET & explain various capacitances involved. **[9]**

b) What is technology scaling? What are types? Explain each in detail. **[9]**

OR

Q4) a) With the help of mathematical analysis & suitable schematic, explain DC transfer characteristics of CMOS Inverter. **[9]**

b) What are merits of transmission gate? Design 4 : 1 mux using transmission gates. **[9]**

P.T.O.

Q5) a) Draw the ckt diagram for push pull CMOS inverter as an amplifier & explain. Give the expressions for output voltage range, output resistance & bandwidth. **[8]**

b) With the help of suitable schematic, explain cascode amplifier. What are its merits? Give the expressions for voltage gain and output resistance. **[8]**

OR

Q6) a) Explain current mirror in detail. Why is it needed? **[8]**

b) Explain current sink & current source in detail. Give expressions for output voltage range & output resistance. **[8]**

Q7) a) What are the types of fault? Explain each in brief. **[8]**

b) What is need of BIST? Explain typical BIST in detail. **[8]**

OR

Q8) a) With the help of block diagram, explain TAP controller in detail. **[8]**

b) Explain boundary scan technique. **[8]**

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