

Total No. of Questions : 8]

SEAT No. :

P3766

[Total No. of Pages : 2

[4960] - 1260

M.E. (E & TC) (VLSI and Embedded Systems)

ASIC Design

(2013 Credit Pattern) (Semester - III)

Time : 3 Hours]

[Max. Marks : 50

Instructions to the candidates:

- 1) *Answer any five questions out of 8.*
- 2) *Neat diagrams must be drawn wherever necessary.*
- 3) *Figures to the right indicate full marks.*
- 4) *Use of electronic pocket calculators is allowed.*
- 5) *Assume suitable data, if necessary.*

Q1) a) What are different types of ASIC? Explain in brief. [5]

b) Draw and explain the flow chart relating to ASIC design flow. [5]

Q2) a) What are different types of simulation? Explain in brief. [4]

b) Explain different modelling techniques used in VHDL. [3]

c) Write a short note on ASIC cell libraries. [3]

Q3) a) Write a note on signal integrity effects in ASIC design. [5]

b) Write a VHDL code for full adder using structural architecture. Also write test bench for it. [5]

Q4) a) Write an explanatory note on practical aspects of mix analog digital design. [4]

b) What is boundary scan testing? Explain in brief. [3]

c) Define logic synthesis and logic simulation. [3]

P.T.O.

- Q5)** a) What are the factors contributing to best floor planning? Explain in detail. [3]
b) What is force directed placement algorithm? Explain different force directed placement algorithms. [3]
c) Explain in detail group migration algorithm for system partitioning. [4]
- Q6)** a) List the goals and objectives for system partitioning and routing. [4]
b) Define channel density and Eimore's delay. [2]
c) Write a short note on Design Rule Check (DRC) and LVS. [4]
- Q7)** a) Explain in detail Automatic Test Vector Generation. [5]
b) Write a short note on features of EDA tools. [3]
c) Define the terms LFSR and BIST. [2]
- Q8)** a) Write a short note on stack at fault model. [4]
b) What is fault simulation? What are different types of fault simulation. [4]
c) Explain in detail formal verification. [2]

