Total No. of Questions : 8]

SEAT No. : ____

P4832

[Total No. of Pages : 2

[5060] - 737
M.E. (E & TC) (VLSI & Embedded Systems)
RECONFIGURABLE COMPUTING
(2013 Pattern) (Semester - I)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates :-

1) ***Answer any five questions.***
2) ***Neat diagram must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume Suitable data if necessary.***

Q1) a) Explain key differences between Configurable, Programmable, and fixed- Function devices. **[4]**

b) What are Research challenges in RC? What is state of Art? **[4]**

c) What is key relation between interconnect, configuration memory and active logic. **[2]**

Q2) a) Discuss general purpose computing issues. **[5]**

b) Explain the Metric: Density and Diversity. **[5]**

Q3) a) Compare ASIC, GPP, FPGA, Memory, RALU, PDSP with respect to power consumption, design efforts, throughput and NRE. **[4]**

b) Explain VLIW processor, discuss its failure from performing at peak. **[4]**

c) Explain the term Multi-Context. **[2]**

Q4) a) Explain the hierarchical interconnect scheme. **[4]**

b) What are issues in Reconfigurable Network Design. **[4]**

c) Brief on channel and wire growth. **[2]**

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Q5) a) What are different instruction compression techniques? Explain any one. **[4]**

b) Find the number of interconnect bits required for a 1000 4-LUT device with 200 inputs. **[4]**

c) Explain the terms Architecture W & Design W. **[2]**

Q6) a) Draw and explain the architecture of DPGA. **[5]**

b) Explain with suitable diagram the time switched input register. **[5]**

Q7) a) What are working RC examples? What tasks are being performed by them? **[5]**

b) Explain MATRIX as reconfigurable architecture. **[5]**

Q8) a) Explain Rapid prototyping as the application of RC. **[4]**

b) Explain Multicontext FPGA as platform for RC. **[4]**

c) Brief on the term partial reconfigurability. **[2]**

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