Total No. of Questions : 8]

SEAT No. : [ ]

P-9598

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M.E. (E & TC) (VLSI & Embedded Systems)

TESTING AND VERIFICATION OF VLSI CIRCUITS

(2017 Pattern) (Semester - III) (604201)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:

1) ***Answer any five Questions.***
2) ***Figures to the right indicate full marks.***
3) ***Assume suitable data, if necessary.***

Q1) a) Explain Principles of testing? Explain Production testing in brief. **[4]**

b) Explain how cost and difficulty of chip testing have greatly affected by recent n VLSI technology trends. **[4]**

c) Differentiate between verification and testing in VLSI process. **[2]**

Q2) a) State any foult fault models and explain any two in brief. **[4]**

b) Compare Functional Vs. structural Testing. **[4]**

c) State the "Rule of 10". **[2]**

Q3) a) Explain Fault Equivalence of combinational circuits with suitable examples. **[5]**

b) What is need of Fault Simulation? Explain parallel fault simulation algorithm. **[5]**

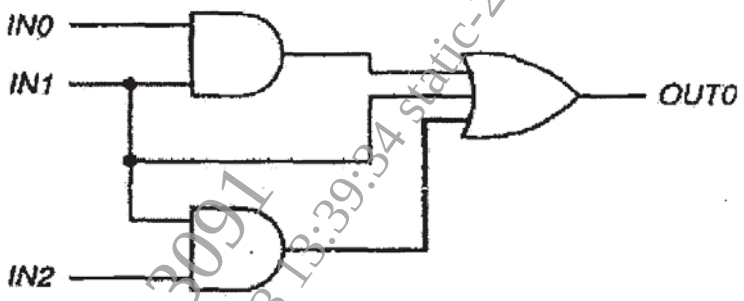
Q4) a) Write Short Note on techniques of Memory testing. **[4]**

b) Explain briefly Observability and Controllability. **[4]**

c) Find min. tests that together test all single stuck-at faults in a two-input AND gate. **[2]**

P.T.O.

Q5) a) Calculate SCOAP Measure for following circuit. **[5]**



b) With the help of suitable diagram explain LFSR and Signature Compaction of BIST. **[5]**

Q6) a) Write Short Note on "Analog Fault Models". **[5]**

b) How Analog Testing is different than Digital Testing. **[5]**

Q7) a) Explain different test pattern generation methods for BIST. **[5]**

b) Explain IDDQ Current testing. **[5]**

Q8) a) Write a short note on "SoC Testing". **[4]**

b) State need and limitation of Formal verification Techniques. **[4]**

c) State Importance of Hardware emulators in Hardware design. **[2]**

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