Total No. of Questions : 8]

SEAT No. :

P4806

[Total No. of Pages :3

[5355] - 665

M.E. (E & TC) (VLSI & Embedded Systems)

ANALOG CMOS DESIGN

(2017 Pattern)

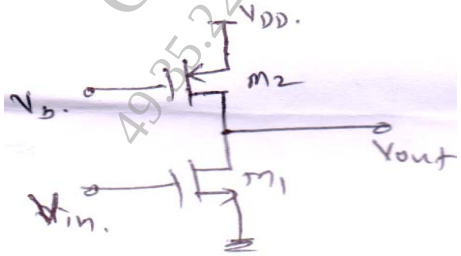
Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Figures to the right indicate full marks.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) What is need of voltage / current reference. Draw a circuit of supply independent current source and explain its working. **[5]**

b) For common source amplifier with current source load shown in figure 1, find small signal voltage gain if $\left(\frac{W}{L}\right)_1 = \frac{50}{0.5}, \left(\frac{W}{L}\right)_2 = \frac{50}{2}$ and $I_{D1}=I_{D2}=0.5$ mA. Assume $\mu_n C_{ox} = 2\mu_p C_{ox} = 60\ \mu A/V^2$ and $T_n=0.1$ and $T_p=0.2\ V^{-1}$ at L=0.5. **[5]**



Q2) a) Using suitable schematic and expressions, explain how MOSFET can work as a switch, diode and active resistor. **[5]**

b) Draw a circuit diagram of cascode current mirror source and derive expression for its output resistance. **[5]**

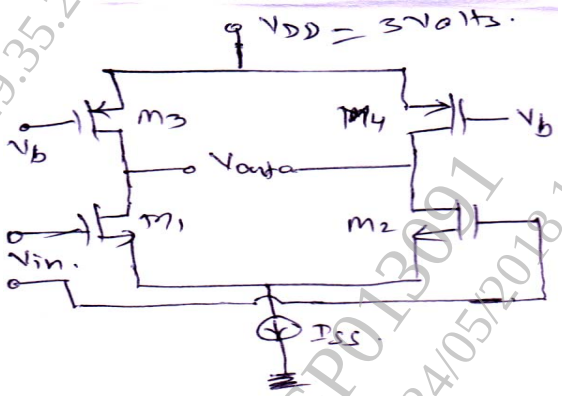
P.T.O.

Q3) a) Compare various types of inverting CMOS amplifiers on the basis of voltage gain and output resistance. **[5]**

b) What is need of cascode amplifier. Draw a circuit diagram of CS-CG cascode amplifier and compare with single stage inverting amplifier. **[5]**

Q4) a) In the circuit of figure 2, calculate differential voltage gain if I_{ss}= 1mA, $\left(\frac{W}{L}\right)_{1,2} = \frac{50}{0.5}$ and $\left(\frac{W}{L}\right)_{3,4} = \frac{50}{1}$. Assume $\mu_n C_{ox} = 2\mu_p C_{ox} = 60 \frac{\mu A}{V^2}$ and T_n=0.1 V^{-1}, T_p=0.2V^{-1} at L=0.5

Also find minimum allowable input common mode level if I_{ss} requires at least 0.4 volts across it. **[6]**



b) What is need of a folded cascode amplifier, draw its schematic and discuss its advantages / disadvantages over cascode amplifier. **[4]**

Q5) a) Draw a comparator and discuss its static and dynamic characteristics. What is typical application of comparator. **[5]**

b) Explain the neutralisation and unilaterisation with suitable circuit diagram. **[3]**

c) Find propagation delay of a comparator that has slew rate 1 volt/μ_s. and output voltage swing is 10 volts. **[2]**

Q6) a) What is need of compensation, explain with the help of gain and phase response of multistage amplifier. **[5]**

b) What are different methods to improve slew rates in CMOS operational amplifiers. **[5]**

Q7) a) Draw a schematic of single ended low noise amplifier (LNA). What are its draw backs and how these are over come in differential LNA. **[5]**

b) Explain in brief the design considerations for RF chip design. **[5]**

Q8) a) Explain in detail open and short circuit techniques for bandwidth estimation. **[5]**

b) What is difference between active and passive mixers. Draw and explain their architectures. **[5]**

●●●