Total No. of Questions : 8]

SEAT No. :

P4309

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[4860]-1260

M.E. (E & TC) (VLSI & Embedded Systems)

ASIC DESIGN

(2013-Credit Pattern) (Semester-III) (604202)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Attempt any five out of eight.***
2) ***Figures to the right indicates full marks.***
3) ***Assume suitable data, if necessary.***

Q1) a) With the help of flow-chart explain the sequence of steps for ASIC design. **[5]**

b) Explain the various types of ASIC. What is importance of ASIC cell library? **[5]**

Q2) a) Write a VHDL code for sequence detector, which detects the sequence '1101' using moore machine. **[4]**

b) Explain the dataflow modeling style with the help of example. **[3]**

c) What is delta delay in VHDL? What is its significance? **[3]**

Q3) a) Explain the various parameters used for the static timing analysis. **[3]**

b) Draw & explain the H/W that will generate after synthesizing the following piece of code. **[4]**

```
Proc1: Process (x, y, z, sel)

variable v1, v2: std_logic;

begin
```

P.T.O.

```
if (sel = '1') then
    v1: = v2 AND y;
    v2: = v1 XOR z;
    Res: = v1 AND v2;
end if;
end process;
```

c) What are the different simulation modes in simulator. **[3]**

Q4) a) Explain mixed signal ASIC Design. **[4]**

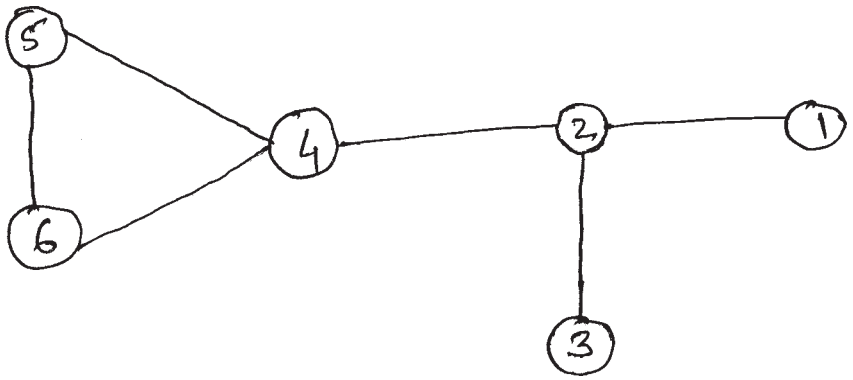
b) Explain the signal integrity effect in ASIC design. **[4]**

c) Explain the synthesis process in detail. **[2]**

Q5) a) Apply the K-L algorithm on the following system to improve the partitioning. Consider initial partition as: **[5]**

Partition A: Nodes 4, 2 and 3.

Partition B: Nodes 1, 5 and 6.



b) Classify the placement algorithms. Explain the min-cut algorithm with the help of example. **[5]**

Q6) a) Explain the constructive partitioning algorithm. **[4]**

b) What is detailed routing? Explain the left edge algorithm with the help of example. **[4]**

c) Explain the different global routing methods. **[2]**

Q7) a) Write short note on Any Two: **[4]**

i) Design Rule Check (DRC).

ii) Features of EDA tools.

iii) Fault simulation.

b) Explain the Built-in Self Test (BIST) with example. **[4]**

c) Define the terms: controllability and observability. **[2]**

Q8) a) Explain the ATPG algorithm in detail. **[4]**

b) Explain the different types of stuck-at fault models with the help of example. **[3]**

c) Briefly describe the boundry scan test. **[3]**

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