Total No. of Questions: 8]			29	SEAT No.:	
P3828		[5561] 240	[Total No. of P	ages: 2	
			[5561]-249		
		VI CII	B.E. (E&TC)	NOI OCV	
			DESIGN & TECHI		
		(2012 Pa	ittern) (Semester -	1) (404181)	
Time: 2	½ Hour	rs/	2.	[Max. Max. Max. Max. Max. Max. Max. Max.	arks : 70
		the candidates:	9	•	
1)	Answ	er Q.1 or Q.2, Q	.3 or Q.4, Q.5 or Q.6, Q.	7 or Q.8.	
2)	Assun	ne suitable data	if necessary.		
<b>Q1)</b> a)	Exp	olain the behav	ioral, data flow, structi	ural VHDL modeling tech	nniques
~ /	_	(	nat are the relevant adv	A STATE OF THE STA	[8]
<b>1</b> <sub>6</sub> )	D	Ty and avalain	the block diagram CD	I D and hitaatuma	[7]
b)	Dra	w and explain	the block diagram CP	LD arcmitecture.	[6]
c)	Exp	olain power dis	tribution and power o	ptimization techniques.	[6]
	,		OR	S	
			OK )		
<b>Q2)</b> a)	Dra	w the state dia	agram of lift controlle	r for two floors. Write op	otimum
	VH	DL code for it			[8]
b)	Fyr	olain the follow	ving terms		[6]
0)	LAL	ram the follow	ing terms.		(
	i)	CLB			; (
	ii)	UCF			NO.
	11)		Sp.		
	iii)	GRM	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	2 6.	
	iv)	EDIF			
c)			s parasitic? How it eff	ect the performance in the	
	chip	Design?			[6]

Q3) a) Explain in detail static and Dynamic power dissipation. [8]

b) With the help of mathematical analysis & suitable schematic, explain DC transfer Characteristics of CMOS Inverter. [10]

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<b>Q</b> 4)	a)	Design CMOS logic for $Y = AB + CDEFG + H$ . [1]	0]
	b)	Explain the following terms:	[8]
		i) Body effect	
		ii) Hot Electron effect	
		iii) Velocity saturation	
		iv) Power delay product	
Q5)	a)	Compare push-pull, current source & active load inverters with respet to voltage gain, voltage range, output resistance & bandwidth in detail.	
	b)	With the help of suitable schematic, explain cascode amplifier. What a its merits? Give the expressions for voltage gain and output resistance.	
		OR OR	
Q6)	a)	Draw schematic diagram and I-V characteristics, explain current sin and current source.	nk [ <b>8]</b>
	b)		
<b>Q</b> 7)	a)	Draw and explain JTAG in detail.	8]
	b)	Draw and explain JTAG in detail.  Explain in detail boundary scan technique.  OR  Explain:  i) Partial scan and full scan  ii) Stuck at '1' and '0' faults  Write short note on BIST.	[8]
Q8)	a)	Explain:	[8]
		<ul><li>i) Partial scan and full scan</li><li>ii) Stuck at '1' and '0' faults</li></ul>	
	b)	Write short note on BIST.	[8]
[556	51]-2	2	