**Total No. of Questions : 8]** **SEAT No. :**

**P4175** **[Total No. of Pages : 2**

# [4760] - 1143
# M.E. (ETC) (VLSI and Embedded System)
# SYSTEM ON CHIP
# (2013 Pattern) (Semester - II)

***Time : 3 Hours]*** ***[Max. Marks : 50***

***Instructions to the candidates:***

1) ***Answer any 05 questions.***

2) ***Neat diagrams must be drawn wherever necessary.***

3) ***All questions carry equal marks.***

4) ***Your answers will be valued as a whole***

5) ***Assume suitable data, if necessary.***

***Q1)*** a) Explain simulation and RTL synthesis of FSMD.

b) What are the limitations of Data flow models?

***Q2)*** a) How pipeline stall occur in RISC Architecture?

b) Explain the need of concurrent models.

***Q3)*** a) What are pipeline hazards? How pipeline hazards can be handled.

b) Explain various synchronization schemes adopted by Hardware/Software interface.

***Q4)*** a) Explain in detail SoC modeling in GEZEL.

b) What is Clock - Domain - Crossing (CDC)? Explain CDC friendly RTL.

***Q5)*** a) Explain different architectural techniques that can be used to optimize the performance of the coprocessor.

b) Explain the Limitations of Simulation?

***P.T.O.***

***Q6)*** a) What are the limitations of static timing Analysis?

b) Explain the Implication on synthesis.

***Q7)*** a) Draw and explain RTL to GDS II design flow.

b) Draw and Explain Generic three - stage pipelined context - based adaptive arithmetic coder architecture?

***Q8)*** a) What is Hybrid Power Management Technique?

b) What are the Factors Affecting delay and slew?

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