Total No. of Questions : 8]

SEAT No. :

P2560

[Total No. of Pages : 2

M. E. (VLSI and Embedded Systems) (Semester - I)
Digital CMOS Design
(2013 Pattern)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume Suitable data if necessary.***

Q1) a) Draw cross section of CMOS Inverter layout. Also draw metal, poly silicon connection diagram as top view. Show all the dimensions in terms of λ. **[5]**

b) With the help of model of MOSFET, explore different capacitors. Give the expressions for capacitors in various regions. Which are the dominant capacitors and in which region are they developed? **[5]**

Q2) a) What are the types of technology scaling? What are merits and constraints? Explain in brief. **[5]**

b) What are wiring parasitics? Explore each in detail. How to minimize these? **[5]**

Q3) a) Certain logic has 40 MOSFETs and each has leakage of 1 pA. If the logic operates at 2.5V, 1 GHz with load of 10 pF; compute total power dissipation. **[4]**

b) With the help of suitable schematic, explain RC delay model. **[4]**

c) What is short circuit dissipation? How to minimize it? **[2]**

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Q4) a) Derive the expression for Power delay product. What is the significance of PDP? **[4]**

b) What is need of logical efforts? Explain with suitable example. **[4]**

c) Explain in brief delay in multistage logic networks. **[2]**

Q5) a) Explore voltage transfer characteristics of CMOS inverter. Give the expression for propagation delay. **[4]**

b) Design CMOS logic for Y = ABC + DE + FGHI. Compute active area on chip. **[4]**

c) What are the merits and demerits of transmission gate? **[2]**

Q6) a) With suitable schematic, explain D-latch using transmission gate. **[4]**

b) Draw FSM diagram and write HDL code for 4 bit ring counter. **[4]**

c) Why is CMOS NAND preferred over NOR gate? **[2]**

Q7) a) Explain NORA logic with suitable example. **[4]**

b) What is ratioed logic circuit? Why is it needed? **[4]**

c) Draw and explain sense amplifier circuit. **[2]**

Q8) a) Explore domino logic with appropriate example. **[4]**

b) Write note on high speed designs. **[4]**

c) List the materials used for performance improvement. **[2]**

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