Total No. of Questions : 8]

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M.E. (E&TC - VLSI & Embedded Systems)

FAULT TOLERANT SYSTEMS

(2013 Course) (Semester-III) (604201)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:

1) ***Attempt any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Assume suitable data if necessary.***

Q1) a) Write short notes on : External & internal models. **[4]**

b) What is statistical fault analysis? **[6]**

Q2) a) Describe the various trade-offs which need to be considered for DFT. **[6]**

b) Discuss the concept of hardcore. **[4]**

Q3) a) Explain the significance of an intersection operator with its table. **[5]**

b) Construct a binary decision diagram for $f = \bar{a}bc + a\bar{b}c + abc$ considering "a" as root node. **[5]**

Q4) a) Explain the following concepts with respect to the design for testability (DFT) technique : **[6]**

i) Monostable multivibrators.

ii) Oscillators & clocks.

b) Write a short note on fault sampling. **[4]**

Q5) a) List and explain various levels of modeling. **[3]**

b) Draw and explain state diagram of TAP controller. **[7]**

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Q6) a) With the help of suitable schematic explain the simulation process. **[5]**

b) Find the test vector to detect stuck-at-0 fault at the output of G2 gate in following figure. (Figure 1). **[5]**

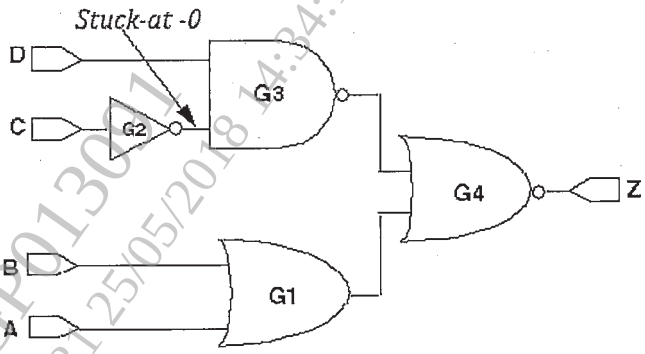

Figure 1

Q7) a) Define the following terms : **[4]**

i) Explicit fault model.

ii) Implicit fault model.

b) With the help of neat diagram explain the working of IEEE 1149.1 test bus circuitry. **[6]**

Q8) a) Write a short note on redundant circuit. **[5]**

b) Describe the following terms : **[5]**

i) Input inertial delay model.

ii) Output inertial delay model.