

Total No. of Questions : 8]

SEAT No. :

P4178

[4760] - 1146

[Total No. of Pages :2

M.E. (E & TC - VLSI and Embedded Systems)

ASIC Design

(2013 Credit Pattern) (Semester - III) (604202)

Time : 3 Hours]

[Max. Marks : 50

Instructions to the candidates:

- 1) Attempt any five questions out of 8.*
- 2) Neat diagrams must be drawn wherever necessary.*
- 3) Figures to the right side indicate full marks.*
- 4) Use of electronic pocket calculator is allowed.*
- 5) Assume suitable data, if necessary.*

Q1) a) Draw the design flow for an ASIC design process and explain each step. **[5]**

b) What do you mean by ASIC cell library? What should it contain. **[2]**

c) Compare different ASIC technologies. **[3]**

Q2) a) Explain in detail Gate array based ASICs. **[5]**

b) Differentiate static and dynamic timing analysis. Which is better? and why? **[2]**

c) Explain Logic synthesis with an example. **[3]**

Q3) a) What is crosstalk delay and crosstalk noise in context to ASIC design? Which parameter it will severely affect. **[4]**

b) Explain Gate level mixed mode simulation and synthesis. **[4]**

c) Write a note on testing of mixed mode ASIC. **[2]**

Q4) a) Explain noise coupling and element matching with respect to practical aspects of mixed signal analog digital design. **[5]**

b) Explain signal integrity effects in ASIC design. **[5]**

P.T.O.

- Q5)** a) What are the different objectives of system partitioning and explain algorithm for the same. [4]
b) What are the factors contributes to test floor planning? Explain in detail. [3]
c) What is parameter extraction pertaining to ASIC design? [3]
- Q6)** a) Differentiate pre layout and post layout simulation with respect to ASIC. [4]
b) What are the approaches to global routing? Explain in detail one algorithm to find shortest path. [4]
c) Define channel density and Elmore's delay. [2]
- Q7)** a) Explain in detail about ATPG algorithm using test vectors with neat diagram. [4]
b) Explain types features of any two EDA tools. [4]
c) Define the term controllability and observability. [2]
- Q8)** a) Briefly describe about Boundary Scan Test with suitable example. [5]
b) Explain LFSR and BIST. [5]

