**Total No. of Questions : 8]**

**SEAT No. :** ____

**P4177**

**[Total No. of Pages : 3**

# [4760]- 1145

## M.E. (E & TC) (VLSI & Embedded System)

## FAULT TOLERANT SYSTEMS

## (2013 Pattern)

***Time : 3 Hours]*** ***[Max Marks :50***

***Instructions to the candidates:***

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Assume suitable data, if necessary.***
3) ***Solve any five questions.***

***Q1)*** a) Construct binary decision diagram for a given function: **[4]**

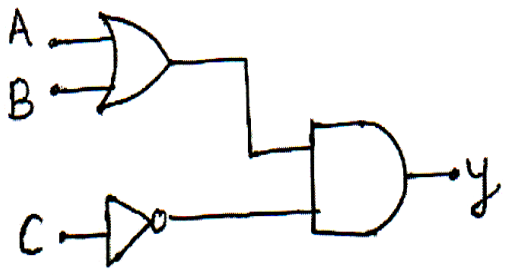
i) $Y=A\bar{B}C+AC$

ii) $Y=\bar{A}\bar{B}+AB$

b) Explain Structural model of RTL. Write on RTL model for a positive edge triggered D-Flip-Flop. **[4]**

c) Write a short note on errors and faults. **[2]**

***Q2)*** a) Construct a primitive cube table for the circuit shown in Fig.1. **[4]**

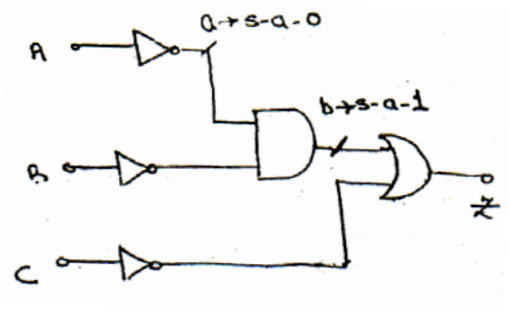



b) Define unknown logic value. Construct AND truth table of 6-valued logic for static hazard analysis. **[4]**

c) Write a short note on Delay Models. **[2]**

***P.T.O.***

***Q3)*** a) Find the set of all tests that detects the multiple stuck fault for fault 'a's-a-0 and fault 'b's-a-1 for the circuit shown in fig.2. **[4]**

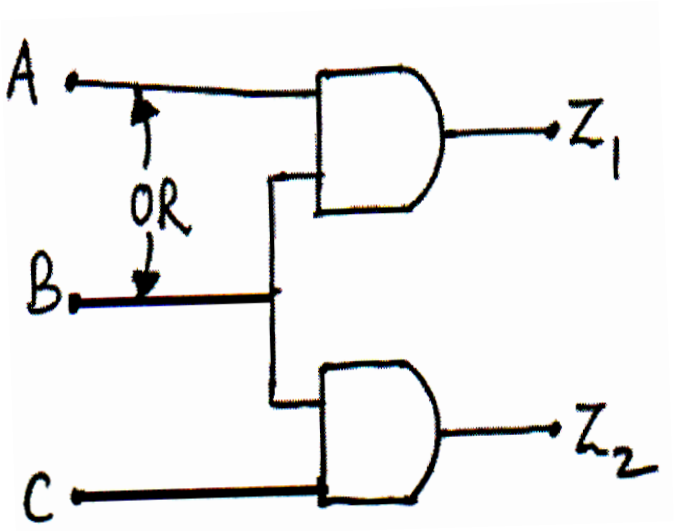



b) Explain event driven logic simulation method with an example. **[4]**

c) Explain the Fault Sampling theorem. **[2]**

***Q4)*** a) Explain Parallel Fault simulation in detail with appropriate example. **[5]**

b) Define Detectability. Find test vectors that determine the OR bridging fault between input A&B in fig.3 shown below. **[5]**




***Q5)*** a) Explain single input signature analyzer with suitable example. **[5]**

b) Classify different compression techniques. Explain Transition count compression technique. **[5]**

***Q6)*** a) What is Boundary Scan? Show a design for the boundary-scan cell circuitry for a Bidirectional I/O pin in the IEEE 1149.1 methodology. **[5]**

b) Explain self-checking Berger code checkers. **[5]**

***Q7)*** a) Explain with block diagram the self-checking system for fault detection. **[5]**

b) Differentiate between On-line and OFF-line BIST. Explain in detail the generic. Off-line BIST architecture at the board level. **[5]**

***Q8)*** a) Explain following test pattern generation methods for BIST: **[5]**

i) Exhaustive Testing.

ii) Pseudorandom Testing.

b) Explain in brief the concepts with respect to DFT (Any2): **[5]**

i) Test points

ii) Partitioning large combinational circuits

iii) Initialization

iv) Partitioning counters and Shift Registers.