Total No. of Questions: 8]		SEAT No. :
P4306	[40(0] 135([Total No. of Pages : 1

[4860]-1256 M.E. (E & TC) (VLSI & Embedded Systems)

(2013 Credit Pattern) (Semester-II)

Time: 3 Hours] [Max. Marks: 50

ANALOG CMOS DESIGN

Instructions to the candidates:

- 1) Answer any 5 questions.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Use of electronic pocket calculator is allowed.
- 5) Assume suitable data, if necessary.
- Q1) a) Explain the effect of channel length modulation and body effect on MOSFET & show how these are accounted in basic small signal model.

 [5]
 - b) With the help of suitable schematic and necessary expressions, explain MOSFET as switch, diode and active resistor. [5]
- Q2) a) For subthreshold MOS model, explain weak inversion using its transconductance characteristics and equations involved. Also explain significance of weak inversion.[5]
 - b) Explain in detail, short channel effects: threshold voltage variation, velocity saturation and output impedance on overdrive voltage. [5]
- **Q3)** a) Explain the performance parameters of CMOS operational amplifier.[5]
 - b) Design cascode current mirror for i_{OUT} 100 μA . Assume suitable data. [5]
- Q4) a) Explain significance of micropower Op amp with examples of two stage miller Op and push-pull output Op amp.[5]
 - b) Design CS-CG cascode amplifier for $A_v = 60$ dB and bandwidth 10 MHz. [5]

- **Q5)** a) Explain static characteristics of Digital-to-Analog converter used for signal processing applications. Also explain offset error and gain error with respect to static characteristics. [5]
 - b) Draw circuit diagram of switched capacitor inverting amplifier and derive expression for its transfer function. [5]
- **Q6)** a) Write short notes on:

[6]

- i) Switched capacitor.
- ii) Bandwidth estimation.
- iii) Zeros as bandwidth enhancer.
- b) If the sampled analog input applied to an 8-bit SAR converter is 0.7 V_{ref}. Find output digital word. [4]
- **Q7)** a) Explain design considerations for RF chip design. [4]
 - b) Draw schematic of any one type of CMOS mixer and explain its design with analysis. [6]
- **Q8)** a) Draw differential LNA, and explain how it overcomes drawbacks of single ended LNA. [5]
 - b) In Low Noise Amplifier (LNA) design, explain how noise and power tradeoff is achieved with respect to different LNA topologies. [5]

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