Total No. of Questions : 8]

SEAT No. :

P4834

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[5060] - 740
M.E. (E & TC) (VLSI & Embedded Systems)
SYSTEM ON CHIP DESIGN
(2013 Pattern) (Semester - II)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates :-

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicater full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume Suitable data if necessary.***

Q1) a) Draw and explain hierarchy of abstraction levels. **[4]**

b) Differentiate Concurrency Vs parallelism. **[4]**

c) Explain the term deep-submicron effect. What is current CMOS design feature Size'? **[2]**

Q2) a) What are the limitations of' data flow models'? In which model these are rectified? **[4]**

b) Explain with an example sequential targets for static schedule design. **[4]**

c) What is advantage of pipelining of SDF graphs'? **[2]**

Q3) a) Explain hardware implementation of Euclid's algorithm through SDF. **[4]**

b) Draw and explain CFG of the CGD program. **[4]**

c) Differentiate : CFD Vs DFG? **[2]**

Q4) a) What are limitations of FSMs? **[4]**

b) Draw and explain design flow to convert software source code into instructions for a processor. **[4]**

c) Why increased instruction latency of a RISC processor is usually not a problem? **[2]**

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Q5) a) When sequential read - write race occurs? Explain it with an example? **[4]**

b) Explain the scope of STA. What is its main limitation? **[4]**

c) Which factors affecting delay and slew? **[2]**

Q6) a) Explain the challenge with bus synchronization design'? **[4]**

b) Explain thc factors which affect power. **[4]**

c) How noise margin is maintained in 0.8 V domains using level shifter? **[2]**

Q7) a) Explain memorty hierarchy trade-offs and characteristics. **[4]**

b) What are limitations of DRAM scheduler designs? **[4]**

c) Which techniques are used for lowering operating voltage? **[2]**

Q8) a) Explain energy - ware device scheduling algorithm. **[4]**

b) Explain SoC design flow for verification environment? **[4]**

c) Which IEEE standars is used for SoC test? Draw the IEEE SOC test architecture. **[2]**

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