Total No. of Questions : 8]

SEAT No. : [ ]

P6613

[Total No. of Pages : 2

[6181]-176

B.E. (Electronics & Telecommunication Engineering)
VLSI DESIGN & TECHNOLOGY
(2019 Pattern) (Semester-VII) (404182)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Distinguish between FPGA and CPLD. **[6]**

b) Explain with diagram SRAM and Anti-fuse programming techniques used in FPGA? **[6]**

c) Write short note on VLSI Design flow with respect to PLDs. **[6]**

OR

Q2) a) Write short note on CPLD. **[6]**

b) Explain synthesis and simulation tools in brief. **[6]**

c) Give typical features and specifications of FPGA. **[6]**

Q3) a) Draw and explain CMOS Inverter transfer characteristics with all regions in detail. **[7]**

b) Draw CMOS logic for $Y = \overline{AB + CD + E}$. Calculate W/L ratio for NMOS and PMOS & area needed on the chip. **[10]**

OR

Q4) Write short note on:

a) Body effect. **[4]**

b) Channel length modulation. **[4]**

c) Draw NAND, NOR, AND, OR gates using CMOS. **[9]**

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Q5) a) Explain Antenna effect. **[5]**

b) Explain Electro migration effect in detail. **[5]**

c) Draw stick diagram of CMOS inverter, 2 input NAND and NOR gates. **[8]**

OR

Q6) a) Explain LAMBDA rules used for CMOS layout design. **[6]**

b) Write short note on Drain punch through. **[6]**

c) Write SPICE code for CMOS invertor for AC analysis. **[6]**

Q7) a) Write short note need of design for Testability & Adhoc DFT techniques. **[8]**

b) Explain stuck at fault models with suitable examples. **[9]**

OR

Q8) a) Write short note on BIST with block diagram. **[8]**

b) Explain JTAG boundary scan method for testing. **[9]**