Total No. of Questions : 8]

SEAT No. :

**P4602**

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# [4860]-1252

## M.E. (E&T/C) (VLSI & Embedded Systems)

## DIGITAL CMOS DESIGN

## (2013 Credit Pattern)

*Time : 3 Hours]* *[Max. Marks : 50*

***Instructions to the candidates:***

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of calculator is allowed.***
5) ***Assume suitable data if necessary.***

***Q1)*** a) With the help of structure of MOSFET, explain the sources of parasitic capacitances. Explain capacitances involved in various operating regions of MOSFET. With the help of model, comment on the dominant capacitance. How to minimize it? **[5]**

b) Explore wiring paracitics in detail. What is sheet resistance? What is its significance? How does it play a role during on-chip wiring? **[5]**

***Q2)*** a) What is SPICE? List 5 parameters of MOSFET SPICE model & explain how these parameters are useful in chip design, What are SPICE levels? **[5]**

b) What are different fabrication techniques? With the help of suitable digrams explain any one of them in detail. What are the limitations occur due to technology scaling? **[5]**

***Q3)*** a) Certain logic operates at supply of 1 Volt at load of 1 pF. To what maximum frequency will it operate if permissible power dissipation is 1 mW? Compute Power Delay Product. **[4]**

b) What is cross talk? List sources & mitigation techniques. **[4]**

c) Explain static & short circuit dissipations. **[2]**

***Q4)*** a) What are delay estimation & analysis techniques? Comment on their accuracies. Explore any one of them in detail. **[4]**

b) What is need of transistor sizing & symmetry in logic design? How does mobility ($\mu$) play the role? Explain with an example. **[4]**

c) Write about design margin in brief. **[2]**

***P.T.O.***

***Q5)*** a) With the help of schematic, explore the operating regions & detail analysis of CMOS inverter. Give the expressions for $V_{OUT}$ for each region. Comment on the region where both the MOSFETs are in saturation. **[4]**

b) Design one bit latch using Transmission Gates. Compare with conventional method. **[4]**

c) What is dynamic hazard? With the help of schematic-waveforms, explain sources & solutions to it. **[2]**

***Q6)*** a) Draw FSM diagram & wirte HDL code for N bit resetable counter. **[4]**

b) Explain flip-flip timings & their significance in metastability. **[4]**

c) Draw different techniques to built tri-state logic. **[2]**

***Q7)*** a) Explain cascode voltage switch logic in detail. What are merits & demerits? **[4]**

b) What is need of BiCMOS? Explain with example. **[4]**

c) Write note on sense amplifier circuit. **[2]**

***Q8)*** a) What are different techniques for low power logic design? Explore any one in detail. **[4]**

b) Explain domino logic with waveforms. **[4]**

c) Explain in brief about materials used for performance improvement. Comment on respective improvement. **[2]**