M.E. (E & TC) (VLSI and Embedded Systems)
ANALOG CMOS DESIGN
(2013 pattern) (Semester-II) (504207)

Time : 3 Hours]   *[Max. Marks : 50*

Instructions to the candidates:
  1) *Answer any five questions.*
  2) *Neat diagrams must be drawn wherever necessary.*
  3) *Figures to the right side indicate full marks.*
  4) *Use of Calculator is allowed.*
  5) *Assume Suitable data if necessary.*

Q1) a) With the help of suitable schematic and necessary expressions, explore MOSFET as switch, diode and active resistor. **[5]**

   b) Draw typical circuit diagram for band gap reference and derive the expression for output voltage. **[5]**

Q2) a) Draw current sink/source. How to improve output resistance? Derive the expression. **[5]**

   b) Design cascode current mirror for i_{OUT} of 10 μA. Assume suitable data. **[5]**

Q3) a) For active load inverter, derive the expressions for $V_{OUT\ max}$ $V_{OUT\ min}$ A_v and r_{OUT}. **[4]**

   b) Carry out large signal analysis of CMOS differential amplifier and find out V_{OUTmax} V_{OUTmin} and ICMR. **[4]**

   c) What are limitations/constraints due to output offset voltage of CMOS Opamp? **[2]**

Q4) a) Compare active load, current source and push pull inverters w.r.t. V_{OUT}, A_v, r_{OUT} and bandwidth. **[4]**

   b) Carry out small signal analysis of CMOS differential amplifier and derive A_v, r_{OUT}, CMRR and bandwidth. **[4]**

   c) Which are dominant noise in CMOS Opamp? List the techniques to reduce these noise. **[2]**

Q5) a) Design multistage amplifier for $A_V = 40$ dB and bandwidth $= 100$ MHz. Comment on r_{OUT}. Assume suitable data. **[4]**

b) Explore open circuit time constant method analytically in detail. **[4]**

c) List assumptions and limitations of short circuit time constant method. **[2]**

Q6) a) How to use zeros as bandwidth enhancer? Explain shunt peaking in amplifier. Give the expression for extended bandwidth. **[4]**

b) What are the constraints on input admittance of tuned amplifier? Explore unilateralization and neutralization in short. **[4]**

c) What are techniques to improve bandwidth? **[2]**

Q7) a) What is power constrained noise optimization? Explore with necessary expressions. **[4]**

b) Draw schematic for any one type of CMOS mixer and explain with analysis. **[4]**

c) What are spurs in mixer? **[2]**

Q8) a) Draw single ended LNA. Mention the drawbacks and show how these are overcome in differential LNA? **[4]**

b) Brief advanced trends in RF chip design. **[4]**

c) Define conversion gain and noise figure w.r.t. mixer. **[2]**

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