Total No. of Questions : 8]

SEAT No. :

P3944

[Total No. of Pages : 2

[5462]-667

M.E. (E&T/C) (VLSI & Embedded Systems)
TESTING AND VERIFICATION OF VLSI CIRCUITS
(2017 Course) (Semester-III) (604201)

Time :3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Attempt any 5 questions.***
2) ***Figures to the right indicate full marks.***
3) ***Assume suitable data if necessary.***

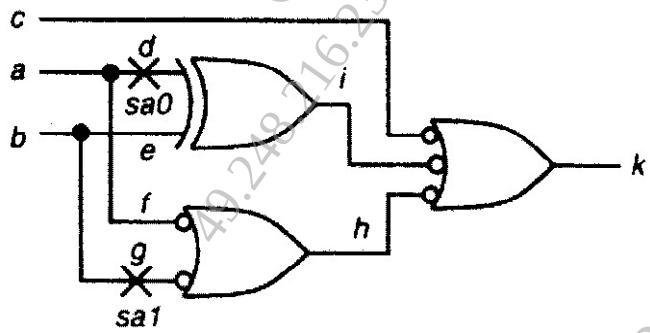
Q1) a) Explain how cost and difficulty of chip testing have greatly affected by recent VLSI technology trends. **[4]**

b) Explain Principles of testing. Discuss briefly production testing. **[4]**

c) Differentiate between verification and testing with respect to VLSI process. **[2]**

Q2) a) Compare Functional Vs. structural Testing. **[4]**

b) Explain Show that the two faults d s-a-0 and g s-a-1 are equivalent. **[4]**



c) State the "Law of diminishing returns". **[2]**

Q3) a) What is the need of fault Simulation? Explain in detail parallel fault simulation algorithm. **[5]**

b) Explain Logic and Switch Level Modeling for Fault simulation. **[5]**

P.T.O.

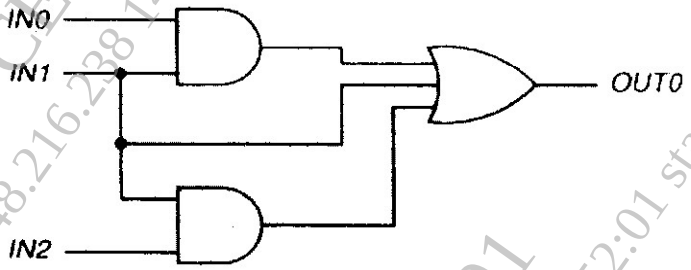
Q4) a) Write a short note on "Testability measures" **[4]**

b) Explain briefly techniques of Memory Testing. **[4]**

c) Find min. tests that together test all single stuck-at faults in a two-input AND gate. **[2]**

Q5) a) With the help of suitable diagram explain LFSR and Signature compaction of BIST. **[5]**

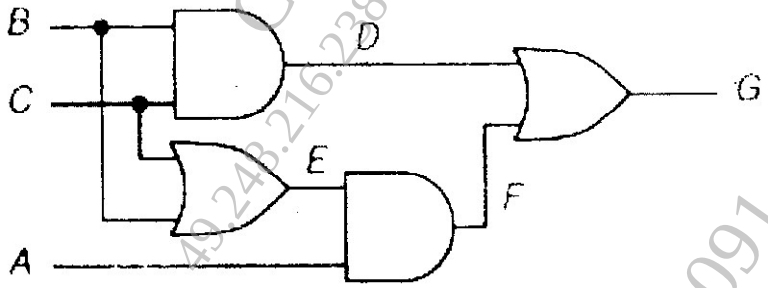
b) Calculate SCOAP Measure for following circuit. **[5]**



Q6) a) With the help of suitable diagram explain Scan Design for DFT. **[5]**

b) How Analog Testing is different than Digital Testing. **[5]**

Q7) a) Find min test set using path sensitization technique for following circuit. **[5]**



b) Explain IDDQ Current testing. **[5]**

Q8) a) Write a short note on "Embedded Core Testing". **[4]**

b) State need and limitations of Formal Verification Techniques. **[4]**

c) State Importance of Hardware emulators in Hardware design. **[2]**