Total No. of Questions : 08]

SEAT No. :

P2018

[Total No. of Pages : 2

[5059] - 621
B.E. (E & TC)
VLSI DESIGN & TECHNOLOGY
(2012 Pattern) (Semester - I)

Time : 2 1/2 Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Neat diagrams should be drawn wherever necessary.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) State the difference between **[6]**

i) Signal and variable

ii) Functions and procedures **[8]**

b) Draw and explain the following for FPGA

i) Logic cell

ii) CLB

iii) Programmable switch matrix

iv) I/O block

c) What is the need of clock distribution? Explain techniques of clock distribution. **[6]**

OR

Q2) a) Write VHDL code and test bench for D FLIP FLOP using function for clock event. **[8]**

b) Explain with diagram SRAM and anti-fuse programming techniques used in FPGA? **[6]**

c) What is floor planning? Explain in detail. **[6]**

P.T.O.

Q3) a) Draw and explain CMOS transfer characteristics in detail showing all regions in the characteristics. **[8]**

b) Design CMOS logic for $Y = \overline{AB+CD+E}$. Calculate W/L ratio for N_{MOS} and P_{MOS} area needed on chip. **[10]**

OR

Q4) a) Explain transmission gate. States its advantages. Implement a circuit of 2:1 multiplexer using transmission gate. Comment on the number of transistor required using transmission gates and conventional method. **[10]**

b) Explain the following. **[8]**

i) Velocity saturation

ii) Body effect

iii) Hot electron effect

iv) Channel length modulation

Q5) a) Explain common source amplifier with the help of circuit diagram. Draw AC equivalent circuit and expression for voltage gain, output resistance. **[8]**

b) Explain device parasitic and their limitation on the performance of CMOS circuits. **[8]**

OR

Q6) a) Draw and explain difference amplifier using MOS transistors. **[8]**

b) Draw and explain current sink and source circuits. **[8]**

Q7) a) Explain the need of design for testability. Explain scan path testing. **[8]**

b) Explain stuck-at-0 and stuck-at-1 faults with example. **[8]**

OR

Q8) Write short note on. **[16]**

a) TAP controller with state diagram.

b) Built In Self Test (BIST)

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