Total No. of Questions : 8]

SEAT No. : [ ]

PB2287

[Total No. of Pages : 2

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B.E. (Electronics and Telecommunication)

VLSI DESIGN AND TECHNOLOGY

(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Solve Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Assume suitable data, if necessary.***

Q1) a) Draw and explain the architecture of CPCD and compare between CPCD and FPGA. **[10]**

b) Write feature of FPGA in detail and write its applications. **[8]**

OR

Q2) a) Draw and explain CLB in detail. **[8]**

b) Draw and explain PLD design flow. **[10]**

Q3) a) Design cmos logic for $y = \bar{a}b + a\bar{b}$. **[8]**

b) What are the merits of transmission gate and design 2:1 multiplexer using transmission gate. **[9]**

OR

Q4) a) Write short note on Hot electron effect. **[6]**

b) Write short note on Power dissipation. **[6]**

c) Write short note on Body effect. **[5]**

Q5) a) Explain in detail lambda design rules in CMOS VLSI. **[9]**

b) Draw stick diagram for invester, NAND and NOR gate. **[9]**

OR

P.T.O.

Q6) a) Write short note on Electrical Rule Check. **[6]**

b) Write short note on Antenna Effect. **[6]**

c) Write short note on Cross talk and drain punch. **[6]**

Q7) a) What is the need of BIST? Explain typical BIST in detail. **[9]**

b) Write short note on **[8]**

i) JTAG

ii) Boundry scan

OR

Q8) a) Explain the need for design for testability? Explain stuck at 0 and stuck at 1 fault with example. **[9]**

b) Draw the TAP controller state diagram and explain. **[8]**

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