Total No. of Questions :8] **SEAT No. :**

P768 **[Total No. of Pages : 2**

[6005]-779
M.E. (E &TC) (VLSI & Embedded Systems)
ASIC DESIGN
(2017 Pattern) (Semester - III) (604202)

Time : 3 Hours] ***[Max. Marks : 50***

Instructions to the candidates:

1) ***Attempt any Five questions out of Eight.***
2) ***Neat diagrams must be drawn whenever necessary.***
3) ***Figures to the right indicates full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) Write short note on logic level optimization. **[5]**

b) Draw and explain ASIC Design Flow. **[5]**

Q2) Explain the terms **[5]**

i) Constants

ii) Variable

iii) Attributes

b) Write VHDL code and test-bench code for 4-bit shift register. **[5]**

Q3) a) Write short note on power Dissipation **[4]**

b) Explain in brief system partitioning technique in ASIC. **[4]**

c) Write CAD tools used in ASIC Design. **[2]**

Q4) a) Explain in detail floor planning in ASIC with one example. **[4]**

b) Write short note on routing techiniques in ASIC. **[4]**

c) What are the goals and objectives of placement. **[2]**

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Q5) a) Explain power optimization techiniques in ASIC. **[4]**

b) With one example describe time optimization technique. **[4]**

c) How to estimate delays in ASIC Design. **[2]**

Q6) a) Explain in detail different time constraints in ASIC Design. **[4]**

b) Write short note on static timing analysis. **[4]**

c) How to design ASIC library. Comment on uses of library. **[2]**

Q7) a) Describe with one example gate level mixed mode simulation. **[4]**

b) Write short note on scan and partial test. **[4]**

c) Explain design challenges in mixed signal ASIC Design. **[2]**

Q8) a) Describe in brief Automatic Test pattern Generator. **[4]**

b) Write short note on memory testing. **[4]**

c) What is the signal integrity issues occured in ASIC Design. **[2]**

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