Total No. of Questions : 8]

SEAT No. :

P5238

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M.E. (E & TC) (VLSI and Embedded Systems)

SYSTEM ON CHIP

(2017 Pattern) (Semester - II)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions. Each question carries 10 marks and each bit carries 5 marks.***
2) ***Draw the neat diagram whenever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data whenever necessary.***

Q1) a) What is the need of Concurrent Models?

b) Explain the Hardware schematic for a counter with Timing Diagram.

Q2) a) How pipeline stall occur in RISC Architecture?

b) Explain the difference between Control hazard and data hazard.

Q3) a) Explain Micro-programmed Architecture.

b) Explain the limitations of FSM.

Q4) a) What is the Implication on Synthesis?

b) Explain in detail the bus synchronization in RTL.

Q5) a) Write a note on Preventing Data Loss through FIFO along with its limitations.

b) What is clock domain crossing?

P.T.O.

Q6) a) What is Simulation-Synthesis Mismatch?

b) Explain importance of low power.

Q7) Explain the Design Issues and Techniques related to Multimedia IP development : Speed, Area, Power, Bandwidth and storage, Perceptual quality.

Q8) a) Write a note on Memory Optimization and Management.

b) What is SoC memory system design?