Total No. of Questions : 4]

SEAT No. :

PC225

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[6361]-91
B.E. (E&TC) (Insem)
VLSI DESIGN & TECHNOLOGY
(2019 Pattern) (Semester -VII) (404182)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4.***
2) ***Figures to the right side indicates full mark.***
3) ***Draw neat diagram wherever necessary.***
4) ***Assume suitable data, if necessary.***

Q1) a) Explain Process Statement in VHDL with suitable examples. **[5]**

b) Explain any 2 Concurrent Statement in VHDL with suitable examples. **[5]**

c) Write VHDL code for full adder using behavioral modeling style. **[5]**

OR

Q2) a) Write VHDL Code for Arithmetic logic Unit and its test bench. **[10]**

b) Explain in brief different WAIT statements supported by VHDL. **[5]**

Q3) a) What is Clock Jitter? What are sources of it? **[5]**

b) Draw state diagram and write VHDL code and its test bench for sequence detector 111. **[10]**

OR

Q4) a) Why should supply and ground bounce be taken care? How are these minimized? **[5]**

b) What is Setup time and Hold Time? Explain Meta-stability in detail. **[5]**

c) Explain Interconnect routing Techniques. **[5]**

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