Total No of Questions: [08] *SEAT NO. :* [ ]

[Total No. of Pages : 02]

M.E. 2013 (E & TC)VLSI & Embedded System

Reconfigurable Computing

(Semester -II)

Time: 3 Hours ***Max. Marks : 50***

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume Suitable data if necessary***

SECTION I

Q1)	a)	With help of suitable example explain difference between reconfigurable machines and conventional processor	[5]
	b)	Define Configurable, Programmable, and fixed-Function devices	[3]
	c)	State the general purpose computing issues	[2]
Q2)	a)	Give the detail mathematical analysis of interconnect growth, what are the various solutions.	[4]
	b)	What are the effects of interconnect granularity.	[2]
	c)	What are the conventional interconnects? What are their limitation?	[4]
Q3)	a)	Compare FPGA, GPP, ASIC w.r.t. functional capacity, data density and functional diversity.	[5]
	b)	State and explain reconfigurable device characteristics	[5]
Q4)	a)	Compare RISC styled processor, VLIW processor, DSP processor and FPGA with respect to limited instruction and data bandwidth, abstraction overhead data movement consume capacity and coarse grained data path network	[5]
	b)	What is pitch of wire? How to compute the area of crossbar? Give design strategy for crossbar.	[5]
Q5)	a)	List the typical characteristics of multicontext FPGA	[2]
	b)	Explain reconfigurable ALU in detail	[4]
	c)	What are the merits and limitations of TSFPGA? Also state its application	[4]
Q6)	a)	Draw and explain architecture of DPGA?	[5]
	b)	Give mathematical analysis along with suitable examples for functional density	[5]
Q7)	a)	What is rent rule? How will you apply it in the design of an RC device	[4]
	b)	Explain the hierarchical interconnect in detail	[4]

	c)	State the Issues in Reconfigurable Network Design	[2]
Q8)	a)	Explain delta delay, intrinsic delay, interconnect delay pertaining to Reconfigurable Device	[4]
	b)	What are the advantages of MATRIX architecture over general purpose architecture	[2]
	c)	How to calculate instruction bandwidth of LUT based structure?	[4]