Total No. of Questions : 6]

SEAT No. : [ ]

P5145

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BE/Insem. - 551

B.E. (E & T/C)

VLSI Design & Technology

(2012 Pattern)

Time : 1 Hour] ***[Max. Marks : 30***

Instructions to the candidates:

1) ***Solve any three questions. (Q.1 or Q.2, Q.3 or Q.4 and Q.5 or Q.6)***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of calculate is allowed.***
5) ***Assume suitable data if necessary.***

Q1) a) Write VHDL code for 2:1 Mux in structural as well as behavioural modeling styles. **[5]**

b) What is meant by metastability? Explain any one solution in detail. **[5]**

OR

Q2) a) What is sub program? Explore with suitable VHDL code. **[5]**

b) What is need of attributes? Explain any three attributes in brief. **[5]**

Q3) a) With the help of suitable diagram of architectural details, explain the typical specifications of FPGA. **[5]**

b) Compare CPLD & FPGA architectures in brief: **[5]**

OR

Q4) a) What is meant by synthesis in design flow? Explain in detail. **[5]**

b) Explore different types of simulations involved in high level design flow. Explore post layout simulation in detail. **[5]**

P.T.O.

Q5) a) Explain signal integrity issues involved in VLSI design. **[5]**

b) Write note on pad design. **[5]**

OR

Q6) a) What is the reason of clock skew? List various clock distribution techniques. Explain any one of them. **[5]**

b) Write note on architectures for low power. **[5]**

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