Total No. of Questions : 8]

SEAT No. :

P4014

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M.E. (E&TC) (VLSI & Embedded Systems)
SYSTEM ON CHIP DESIGN
(2013 Pattern) (Semester - II)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates :

1) ***Answer any Five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculators is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Explain the driving factors in Hardware/Software Co-design. **[4]**

b) Explain dualism of hardware design and software design. **[4]**

c) Explain cycle-accurate abstraction level. **[2]**

Q2) a) Explain with example control flow modelling. **[4]**

b) Explain the concept of multithread dynamic schedules. **[4]**

c) Which steps one need to following to convert a multirate graph to a single-rate graph? **[2]**

Q3) a) Which parameters and methods for FIFO queue requires? **[4]**

b) How to map dataflow into software using sequential schedule? **[4]**

c) Draw and explain Control flow graph of a 'for loop'. **[2]**

Q4) a) Differentiate Microprogrammed controller Vs FSM. **[4]**

b) Explain design trade-offs of the microinstruction format. **[4]**

c) When structural hazards occur? **[2]**

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Q5) a) When write-write race occurs? Explain it with an example? **[4]**

b) How to avoid simulation race? **[4]**

c) What is purpose of IEEE Standard 1364-1995? **[2]**

Q6) a) Which problem arises due to Metastability? **[4]**

b) How FIFO is used to prevent data loss? **[4]**

c) Explain full timing gate level simulation (FTG S) in detail. **[2]**

Q7) a) Draw and explain RTL to GDSII design flow. **[4]**

b) Explain the motion estimation architecture. **[4]**

c) Which good factors one should use for image/video codec design? **[2]**

Q8) a) Explain multilayered, quality-aware memory controller features. **[4]**

b) Explain hard real-time DPM polices. **[4]**

c) Explain the SOC test wrapper operation modes. **[2]**

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