Total No. of Questions : 6]	
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SEAT No. :	

P185

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## APR - 17/TE/Insem. - 21 T.E. (E & TC)

EMBEDDED PROCESSORS (2012 Course) (Semester - II) (304191) Time: 1 Hour] [Max. Marks: 30 Instructions to the candidates: Answer Q1 or Q2, Q3 or Q4, Q5 or Q6. Neat diagrams must be drawn wherever necessary. Figures to the right indicate full marks. 3) 4) Assume suitable data, if necessary. State different processor operating modes & write function of each **Q1)** a) operating mode for ARM 7. [5] What is mean by 7TDMI w.r. to ARM core? [5] b) OR **Q2)** a) List features of ARM7 processor. How it is different then pure RISC processor. [6] Explain following instructions of ARM (any two): [4] b) MVN R<sub>2</sub>, R<sub>3</sub>, ASR # 3 ADDEQ R<sub>0</sub>, R<sub>1</sub>, R<sub>2</sub> ii) TEQ  $R_1$ ,  $R_2$ iii) **BL NEXT** iv) Explain the significance of PLL0 & PLL1 in LPC2148. *Q3*) a) [6] Explain the following Timer registers of LPC 2148. [4] b) i) Prescale Counter Register. ii) Timer Counter Register.

OR

Q4)	a)	Draw interfacing of LEDs to P0.0 to P0.7 of LPC2148. Write the program to blink the LEDs with suitable Delay. [6]			
	b)	Draw	& explain memory map of LPC2148.	[4]	
Q5)	a)		the features of on chip ADC. Explain the function of following DCR register of on chip ADC.	g bits <b>[6]</b>	
		i)	SEL		
		ii)	CLK		
		iii)	CLKDIV		
	b)		the features of UART0 in LPC2148. What is the difference between the UART1?	ween [4]	
			OR		
Q6)	Writ	e shor	rt note on (any two):	[10]	
	a)	I <sub>2</sub> C p	protocol.		
	b)	SD ca	ard interfacing using spl.		
	c)	On c	hip DAC.		
	d)	Vecto	or interrupt controller.		