Total No. of Questions : 8]

SEAT No. :

P4174

[Total No. of Pages : 5

[4760] - 1142

M.E. (E & TC) (VLSI & Embedded Systems) (Semester - II)

ANALOG CMOS DESIGN

(2013 Pattern)

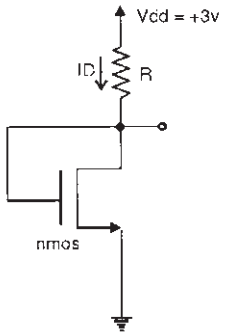
Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***Answer any five questions.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Use of Calculator is allowed.***
5) ***Assume Suitable data if necessary.***

SECTION - I

Q1) a) For the circuit shown in figure, Find 'R' and the d.c. voltage 'V_D' If the drain current I_D is 80μA. The NMOS transistor used have V_t = 0.6V, $\mu_n C_{OX}$ = 200μA/V^2, L = 0.8μm, W = 4μm. **[5]**



b) Draw the transistorized network of Common source amplifier, Common gate amplifier and common drain amplifiers. Differentiate these amplifiers with respect to following terms, **[5]**

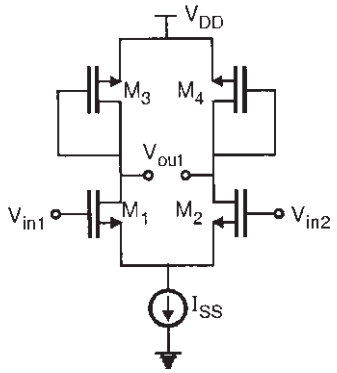
i) Input resistance

ii) Output Resistance

iii) Intrinsic Voltage Gain

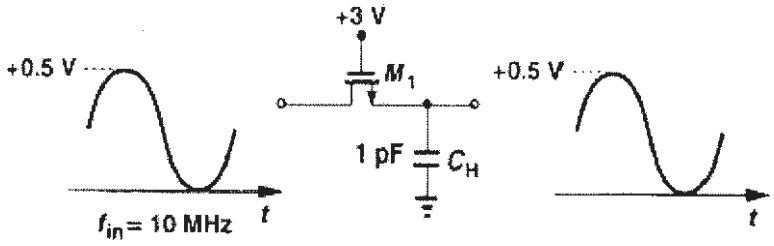
P.T.O.

Q2) a) Determine the voltage gain of the circuit shown in Figure. Assume $\lambda \neq 0$. Assume M_1 is identical to M_2 and M_3 is identical to M_4. **[5]**



b) Explain how CMOS inverter can be used as an amplifier. Draw the neat circuit diagram of two stage CMOS OP-Amp and explain its operation.**[5]**

Q3) a) In the circuit shown in figure calculate the minimum and maximum on-resistance of Ml. Assume $\mu_n C_{ox}$ = 50μA/V², W/L = 10/1, γ = 0, V_{TH} = 0.7 V and V_{DD} = 3V. **[4]**



b) Draw and Explain following analog CMOS circuits **[4]**

i) LNA

ii) Mixer

iii) DAC

iv) Tunned Amplifiers

c) What is source degeneration ? Explain the effect degeneration resistance on the voltage gain of CS amplifier. **[2]**

Q4) a) Design a fully differential telescopic op-amp with the following specifications: **[4]**

V_{DD}= 3 V, differential output swing = 3V, power dissipation= 10mW, voltage gain= 2000. Assume $\mu_n C_{ox}$= 60μA/V^2, $\mu_p C_{ox}$ = 30 μA/V^2 λ_n = 0.1V^{-1}, λ_p = 0.2V^{-1} (for an effective channel length of 0.5 μm) γ = 0, V_{THN} = $|V_{THP}|$ = 0.7 V.

b) What is the necessity of MOS diode/active resistor? Draw the MOS diode/active resistor circuits for NMOS and PMOS transistors. Is there any difference in gain of the following amplifier circuits, **[4]**

i) Common source amplifier with NMOS diode connected load

ii) Common source amplifier with PMOS diode connected load

Justify your answer with the suitable circuit diagrams.

c) With the help of detailed equivalent circuit diagram explain the parasitic capacitances and resistances involved in a MOSFET. **[2]**

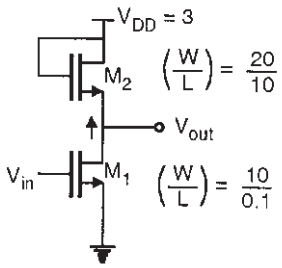
Q5) a) What is the principle of operation of Current mirrors? Explain in short nonideal effects of current mirrors. What is the use of current mirrors?**[4]**

b) What is difference between active mixer and passive mixers. Draw and explain the architectures of both the mixers. **[4]**

c) A 1 V peak-to-peak sinusoidal signal is applied to an 10-bit DAC which has a Vref of 5 V. Find the maximum SNR of the digitized analog output signal. **[2]**

Q6) a) Draw the small signal model MOS transistor including all the parasitic capacitances and derive the equation for its transconductance (g_m) and transition frequency (f_T). **[4]**

b) Determine the voltage gain of the circuit shown in Figure If $I_{D1} = I_{D2} = 1$ mA, $\lambda = 0.1$, $\mu_n C_{ox} = 100\ \mu A/V^2$. Neglect body effect. **[4]**



c) For an ideal n channel MOSFET with parameters L = 1.25 μm, $\mu_n = 650\ cm^2/vs$, $C_{ox} = 6.9 \times 10^{-8}\ F/cm^2$, $V_{THn} = 0.65$ V. Design the channel width W such that $I_{DSSAT} = 4$ mA with $V_{GS} = 5V$. **[2]**

Q7) a) Write Short notes on following(Any Two) : **[4]**

i) DAC Topologies in CMOS ICs

ii) Techniques used in Micro power opamp

iii) Non-Idealities in MOSFET

b) Design an NMOS cascode current source for an output impedance of 500 kΩ and a current of 0.5 mA. Assume M_1 and M_2 are identical

$\mu_n C_{ox} = 100\ \mu A$ and $\lambda = 0.1\ V^{-1}$. **[4]**

c) If the sampled analog input applied to an 8 bit SAR converter is 0.7 Vref. Find the output digital word. **[2]**

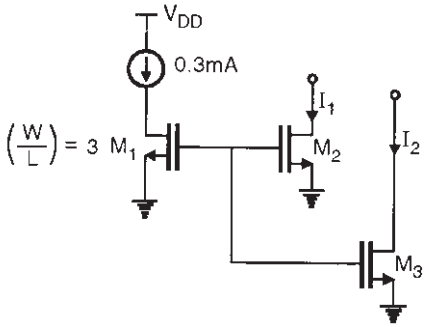
Q8) a) Write Short notes on following(Any Two) : **[4]**

i) High Speed Opamp

ii) Bandgap Reference Source

iii) CMOS Inverter as an amplifier

b) Design a current mirror circuit that produces a currents I_1 = 0.2 mA and I_2 = 0.5 mA from a reference current source of 0.3 mA connected to transistor with aspect ratio 3. **[4]**



c) Define and derive expressions for, **[2]**

i) g_m,

ii) g_{mb}.