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Seat No.	
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[4657]-550

S.E. (Electronics & Telecommunication)

(I Sem.) EXAMINATION, 2014

DIGITAL ELECTRONICS

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :—**
- (i) Figures to the right indicate full marks.
 - (ii) Neat diagrams must be drawn wherever necessary.
 - (iii) Assume suitable data, if necessary.

1. (a) State the following characteristics of Digital IC's (TTL) : [6]
 - (i) Fan in, Fan out
 - (ii) Noise Margin
 - (iii) Figure of Merit.
- (b) Implement the following functions using single 8 : 1 MUX : [6]
 $f(A, B, C, D) = \pi M(0, 3, 5, 7, 12, 15) + d(2, 9).$

Or

2. (a) Draw and explain the working of 2 input CMOS NOR gate. [6]
- (b) Design a 2-Bit magnitude comparator using suitable decoder. [6]

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3. (a) Design a mod-5 ripple counter using a 3-bit ripple counter. [6]
(b) Explain : [6]
(i) State Table
(ii) State Diagram
(iii) State Reduction.

Or

4. (a) Design and explain the following terms : [6]
(i) Melay Machine
(ii) Moore Machine
(iii) State Table.
(b) Design a pulse train generator to generate the following sequence ----10110---- using shift register. [6]
5. (a) Give comparison between PROM, PLA and PAL. [5]
(b) A combinational circuit is defined by the following functions. Implement this circuit with PLA having 3 input, 4 product terms and 2 outputs : [8]
 $F_1(A, B, C) = \Sigma m(0, 1, 3, 4)$
 $F_2(A, B, C) = \Sigma m(1, 2, 3, 4, 5).$

Or

6. (a) Explain in detail the architecture of FPGA. [6]
(b) Design a BCD to excess 3 code converter and implement it using PAL. [7]

7. (a) Write a VHDL code for 2-bit comparator using behavioural modeling style. [7]
- (b) Describe any *two* modeling styles of VHDL with suitable examples. [6]

Or

8. (a) Write a VHDL code for 4-bit ALU using case statement. [7]
- (b) Explain the following statements with examples : [6]
- (i) Process
 - (ii) Case
 - (iii) Wait.