

# CHANKYU LEE

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## WORK SUMMARY

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My research interests lie at the intersection of deep learning and edge computing. I focus on developing energy-efficient and robust deep learning algorithms, with special interests in spiking neural networks (SNNs) and computer vision for event-based cameras. I developed novel unsupervised/supervised/semi-supervised learning methods for deep SNNs. In addition, I developed motion estimation algorithms for event-based camera in challenging scenes such as high speed and wide dynamic range.

## RESEARCH FOCUSES

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◇ Machine learning ◇ Computer Vision ◇ Algorithm-Hardware Co-design

## EDUCATION

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**Purdue University, West Lafayette, IN, USA** *Fall 2015 - present*  
Ph.D., Electrical and Computer Engineering (Advisor: Prof. Kaushik Roy)

**Sungkyunkwan University (SKKU), South Korea** *Spring 2009 - Spring 2015*  
B.S., Electrical and Electronics Engineering

**Hong Kong University of Science and Technology (HKUST), Hong Kong** *Fall 2013*  
Exchange Student Program, Electronic and Computer Engineering

## EXPERIENCE

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**Nanoelectronics Research Laboratory, Purdue University** *Aug. 2016 - present*  
*Graduate Research Assistant (Funded by Center for Brain Inspired Computing, West Lafayette, IN one of six centers in JUMP, a SRC program, Advisor: Prof. Kaushik Roy)*

- Exploratory research on energy-efficient and robust machine learning, overcoming the limitations of current artificial intelligence through algorithm-hardware co-design.
  - Proposed a surrogate derivative method to overcome the discontinuous, non-differentiable nature of the spike generation function in SNNs. This method enables the training of deep convolutional SNNs, such as VGG and ResNet architectures, using backpropagation algorithm. [*Frontiers in Neuroscience, 2020*]
  - Presented a pre-training scheme using a biologically plausible unsupervised learning, namely spike timing dependent plasticity, to better initialize the network parameters in deep SNNs. This semi-supervised approach offers three advantages: faster convergence, enhanced robustness and better generalization. [*Frontiers in Neuroscience, 2018*]
  - Designed novel discretized input representation and hybrid neural architecture for estimating optical flow using event sensors. The proposed network can accurately predict the optical flows from discrete and asynchronous event streams along with substantial benefits in terms of computational efficiency. [*ECCV'20, Realtime Demo Video*]
  - Explored a sensor/architecture fusion framework for motion estimations by leveraging the complementary characteristics of frame- and event-based images as well as deep learning networks and SNNs.

**Access Research Laboratory, Bell Labs, Nokia** *Jun. 2018 - Aug. 2018*  
*Graduate Internship (Supervisor: Hungkei Chow and Joseph Galaro)* *Murray Hill, NJ*

- Developed methodologies of mapping and scheduling convolutional neural network on a specialized MIMD (multi-instruction multi-data) processor for energy-efficient AI computing.

**Graduate School of Convergence Science and Technology, Seoul National University** Jul. 2014 - Sep. 2014, Undergraduate Internship (Advisor: Prof. Yoonkyu Song) Suwon, South Korea

- Research on mid-field wireless powering for simulating neural signals in the brain-machine interface.
  - Designed a full-wave synchronous four-transistor cell rectifier, fed in parallel into each stage through a pump capacitor in implantable bio-chip antenna transmissions.

## ACADEMIC PUBLICATION

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### • International Conference

1. **Chankyu Lee**, Adarsh Kumar Kosta, Alex Zihao Zhu, Kenneth Chaney, Kostas Daniilidis and Kaushik Roy, “Spike-FlowNet: Event-based Optical Flow Estimation with Energy-Efficient Hybrid Neural Networks”, *In Proceedings of the European Conference on Computer Vision (ECCV) 2020, Virtual*.
2. Gopalakrishnan Srinivasan, **Chankyu Lee**, Abhronil Sengupta, Priyadarshini Panda, Syed Shakib Sarwar and Kaushik Roy, “Training Deep Spiking Neural Networks for Energy-Efficient Neuromorphic Computing”, *International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 2020, Virtual, Invited Paper*.
3. Saima Sharmin\*, Priyadarshini Panda\*, Syed Shakib Sarwar, **Chankyu Lee**, Wachirawit Ponghiran and Kaushik Roy, “A Comprehensive Analysis on Adversarial Robustness of Spiking Neural Networks”, *International Joint Conference on Neural Networks (IJCNN) 2019, Budapest, Hungary*.

### • International Journal

1. **Chankyu Lee\***, Syed Shakib Sarwar\*, Priyadarshini Panda, Gopalakrishnan Srinivasan and Kaushik Roy, “Enabling Spike-based Backpropagation for Training Deep Neural Network Architectures” (\*Equally Contributing Authors), *Frontiers in Neuroscience, Neuromorphic Engineering, 2020*.
2. **Chankyu Lee**, Priyadarshini Panda, Gopalakrishnan Srinivasan and Kaushik Roy, “Training Deep Convolutional Spiking Neural Networks with STDP-based Unsupervised Pre-training followed by Supervised Fine-tuning”, *Frontiers in Neuroscience, Neuromorphic Engineering, 2018*.
3. **Chankyu Lee**, Gopalakrishnan Srinivasan, Priyadarshini Panda and Kaushik Roy, “Deep Spiking Convolutional Neural Network Trained with Unsupervised Spike Timing Dependent Plasticity”, *IEEE Transactions on Cognitive and Developmental Systems (TCDS), 2018, Chosen as popular article for May 2018*.
4. Amogh Agrawal\*, Akhilesh Jaiswal\*, **Chankyu Lee** and Kaushik Roy, “X-SRAM: Enabling In-Memory Boolean Computations in CMOS Static Random Access Memories”, *IEEE Transactions on Circuits and Systems I, 2018*.

### • Preprint & Under Review

1. Sayeed Shafayet Chowdhury\*, **Chankyu Lee\*** and Kaushik Roy, “Towards Understanding the Effect of Leak in Spiking Neural Networks” (\*Equally Contributing Authors), *arXiv preprint, 2020*.
2. Amogh Agrawal, **Chankyu Lee** and Kaushik Roy, “X-CHANGR: Changing Memristive Crossbar Mapping for Mitigating Line-Resistance Induced Accuracy Degradation in Deep Neural Networks”, *arXiv preprint, 2019*.

## PRESENTATION

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1. **Chankyu Lee**, Adarsh Kumar Kosta, Alex Zihao Zhu, Kenneth Chaney, Kostas Daniilidis and Kaushik Roy, “Spike-FlowNet: Event-based Optical Flow Estimation with Energy-Efficient Hybrid Neural Networks”, *C-BRIC Industry Meeting, 2020*.
2. **Chankyu Lee**, Priyadarshini Panda, Gopalakrishnan Srinivasan and Kaushik Roy, “Learning Useful Representations in Deep Spiking Neural Network using Unsupervised STDP prior to Supervised Fine-tuning”, *SRC Techcon 2018, Austin, TX*.

## RELEVANT COURSE PROJECTS

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### • Algorithm

- **Artificial Intelligence:** Developed binary weighted SNNs (BSNNs) to reduce the memory storage and remove batchnorm layers. Stochastic input encoding scheme and a spiking neuron model enable BSNNs to achieve competitive accuracy and perform efficient bit-wise computations without the need of the batchnorm layer. [*Language & Software: Python, Pytorch*]
- **Deep Learning:** Presented dynamic iterative synapse pruning for optimizing toward energy-efficient neural networks. Obtained 38-79% pruning efficiency at  $1.5\text{-}2.2\times$  increase in training effort across the layers on MNIST and CIFAR-10 datasets. [*Language & Software: Lua, Torch*]
- **Advanced VLSI Design:** Implemented rank-order temporal spike encoding scheme for rapid and energy-efficient classification tasks. Multi-layer convolutional SNNs are trained using unsupervised spike timing dependent plasticity learning. Obtained  $3.5\times/10\times$  reduction in time-steps/spike-counts during the inference stage compared with a rate-based spike encoding scheme. [*Language: Matlab*]

### • Hardware System

- **System-on-Chip Design:** Demonstrated in-memory computing within STT-MRAMs memory units for Boolean logic operations. Applied the in-memory computing to AES encryption algorithms and evaluated the 172% energy benefit and 8% performance improvement compared with conventional CPU-based computing. Results are published in *IEEE TCAS-I*. [*Language & Platform: C++, Nios-II processor*]
- **MOS VLSI Design:** Implemented 8-bit wallace tree multiplier with scaled-down supply voltage and boost clock frequency by using the principle of pipelining and detecting critical path to lengthen the clock period in the worst case. [*EDA tool: Cadence Virtuoso, Hspice, Nanosim*]

## TECHNICAL STRENGTHS

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<b>Programming Language</b>	Python, Matlab, C++
<b>Machine Learning Tools</b>	Pytorch, TensorFlow, Numpy, OpenCV

## SERVICE ACTIVITIES

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### • Leadership Experience

- President of purdue electrical engineering Korean association (PEEKA) in 2017-2018 academic year
- Student ambassador member of ‘Qualcomm IT Tour’ in summer 2013. Selected as one of top 30 student engineers in Korea and visited Qualcomm’s headquarter in San Diego, CA, USA.

### • Technical Reviewer

- IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
- IEEE Access
- IEEE International Symposium on Circuits and Systems (ISCAS)
- Frontiers in Neuroscience, Neuromorphic Engineering
- Frontiers in Computational Neuroscience
- Journal of Sensors
- International Conference on Computer Science and Application Engineering (CSAE)

## REFERENCE

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Available Upon Request