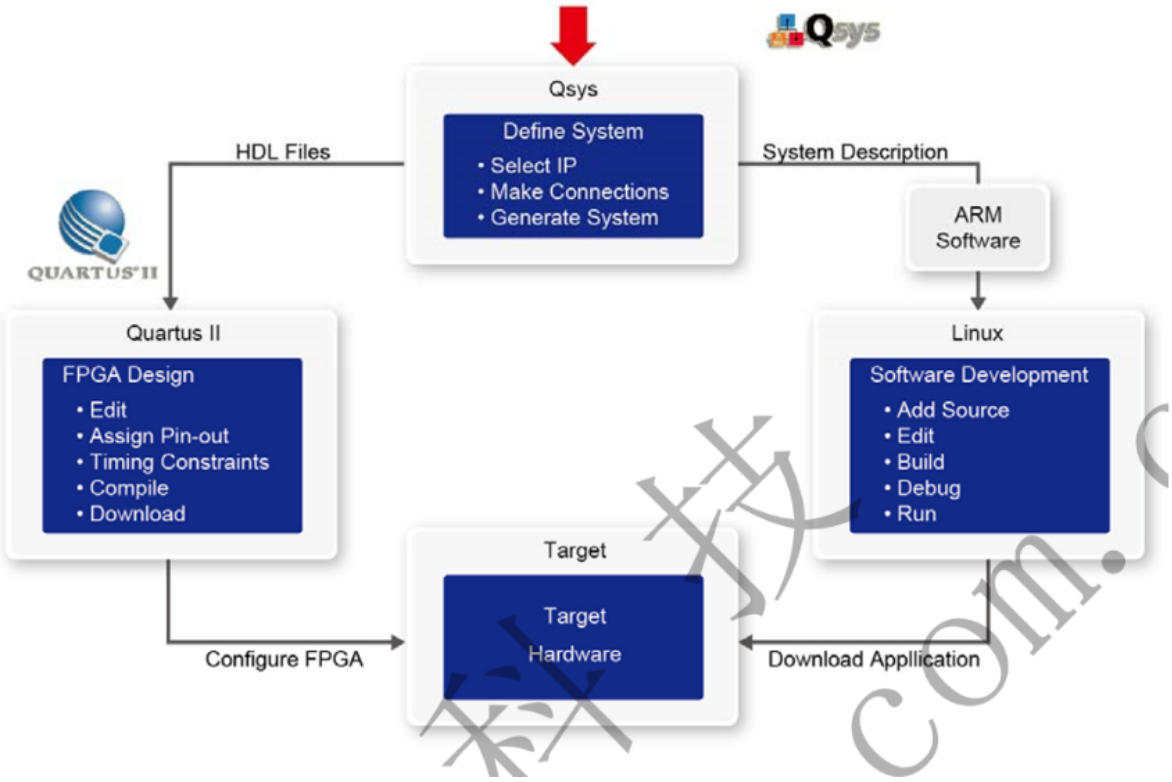
題目：HPS FPGA and Custom QSYS Component

1. 實驗程式碼



system description：解掉註解即可

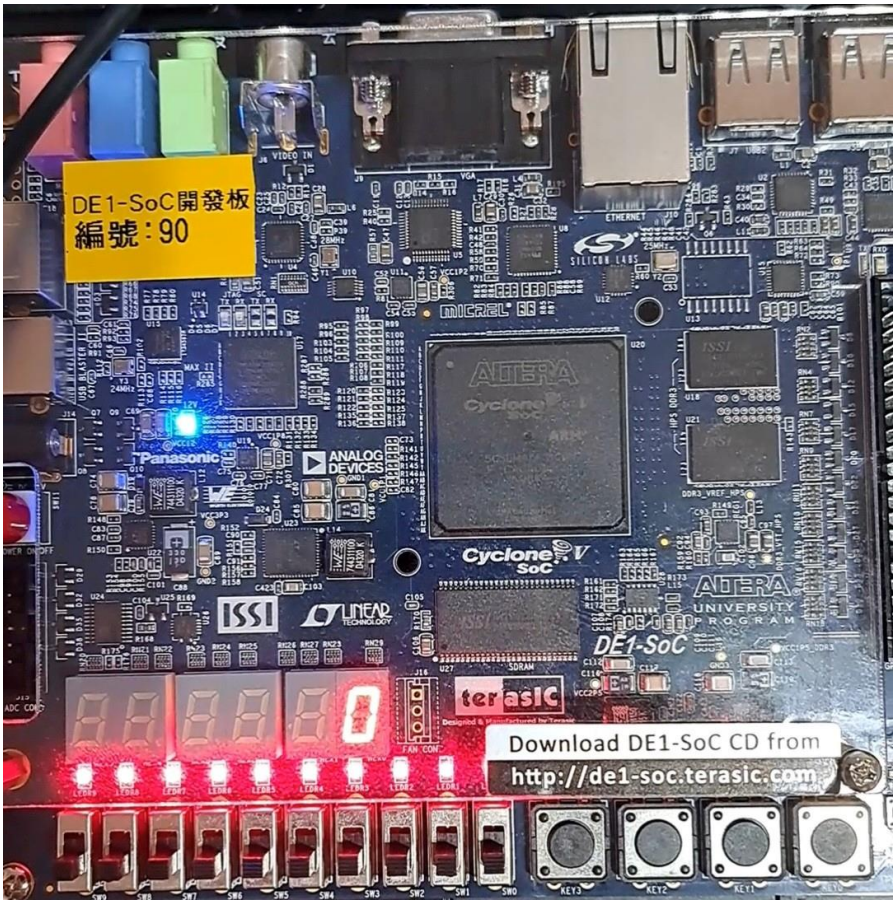
```
h2p_lw_led_addr=virtual_base + ( ( unsigned long  )( ALT_LWFPGASLVS_OFST + PIO_LED_BASE ) & ( unsigned long)( HW_REGS_MASK ) );
h2p_lw_seg_addr = virtual_base + ( ( unsigned long  )( ALT_LWFPGASLVS_OFST + SEG7_LUT_0_BASE ) & ( unsigned long)( HW_REGS_MASK ) );

// toggle the LEDs a bit

loop_count = 0;
led_mask = 0x01;
led_direction = 0; // 0: left to right direction

*(uint32_t *)h2p_lw_led_addr = 0x3FF;
// wait 2s
    usleep( 2000*1000 );
while( loop_count < 60 ) {

    // control led,  add ~ because the led is High-active
    *(uint32_t *)h2p_lw_led_addr = led_mask;
        usleep( 100*1000 );
    *(uint32_t *)h2p_lw_seg_addr = loop_count;


    // wait 1s
    usleep( 1000*1000 );

    // update led mask
    if (led_direction == 0){
        led_mask <<= 1;
        if (led_mask == (0x01 << (PIO_LED_DATA_WIDTH-1)))
            led_direction = 1;
    }else{
        led_mask >>= 1;
        if (led_mask == 0x01){
            led_direction = 0;
            loop_count++;

        }
    }

} // while
```

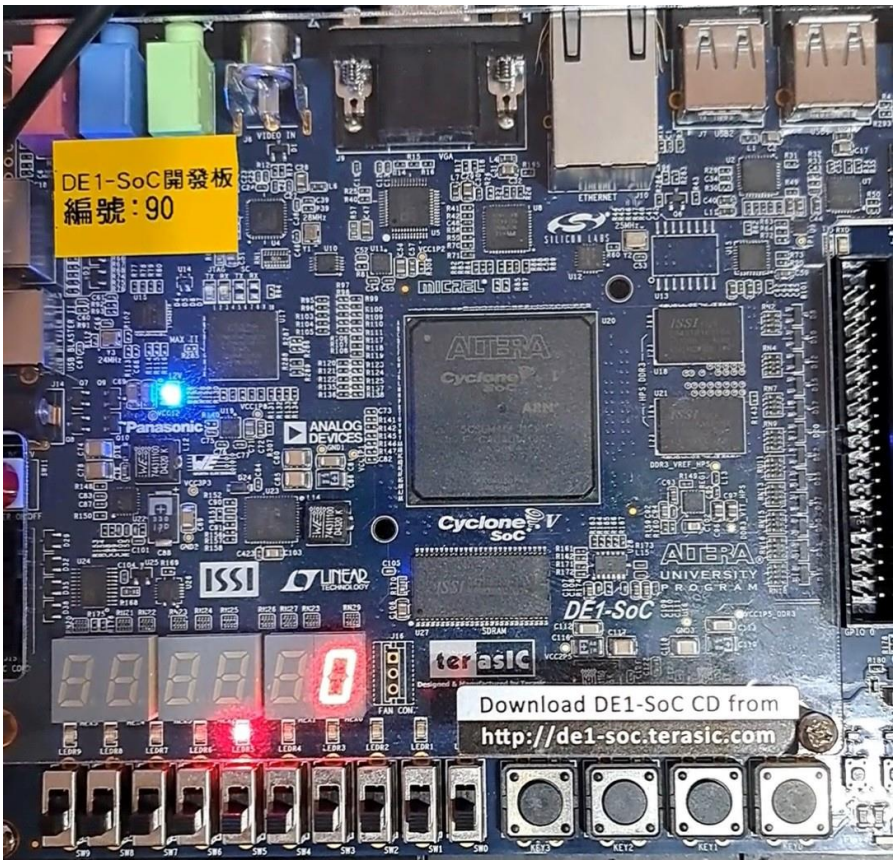
HDL files：將多餘的七段顯示器註解，並在 soc_system 裡面宣告 LED 和七段顯示器的模組

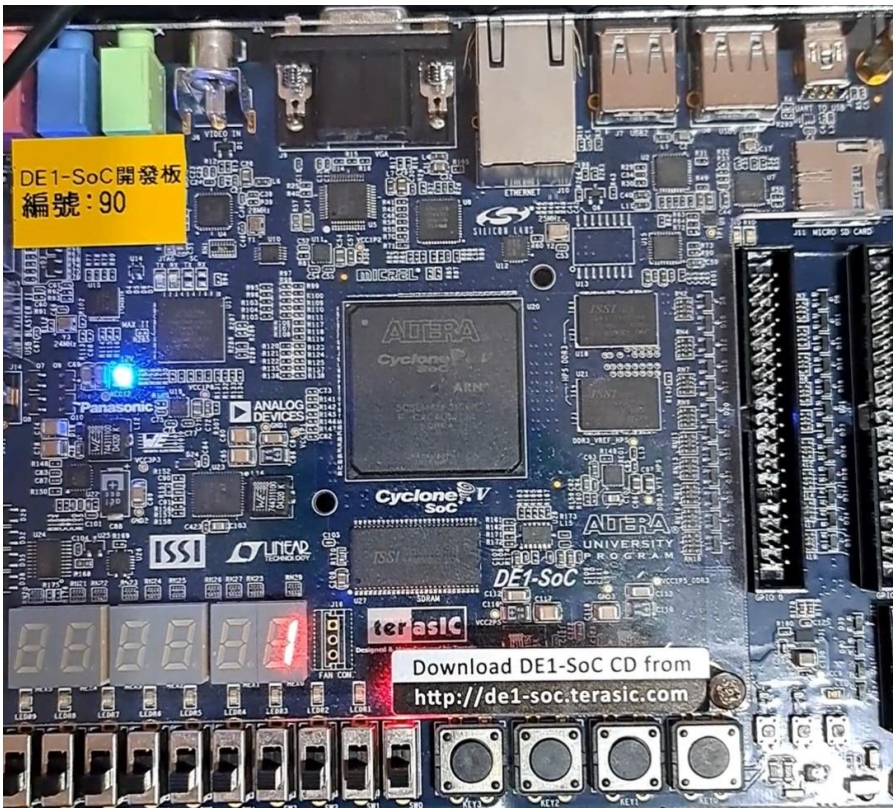
```
//////// HEX0 ////////
output      [6:0]   HEX0,
/*
//////// HEX1 ////////
output      [6:0]   HEX1,

//////// HEX2 ////////
output      [6:0]   HEX2,

//////// HEX3 ////////
output      [6:0]   HEX3,

//////// HEX4 ////////
output      [6:0]   HEX4,

//////// HEX5 ////////
output      [6:0]   HEX5,*/
```

```
.pio_led_external_connection_export     ( LEDR ), //pio_led_external_connection_export
.seg7_lut_0_conduit_end_export          ( HEX0 ), //seg7_lut_0_conduit_end_export
```

2. 實驗結果

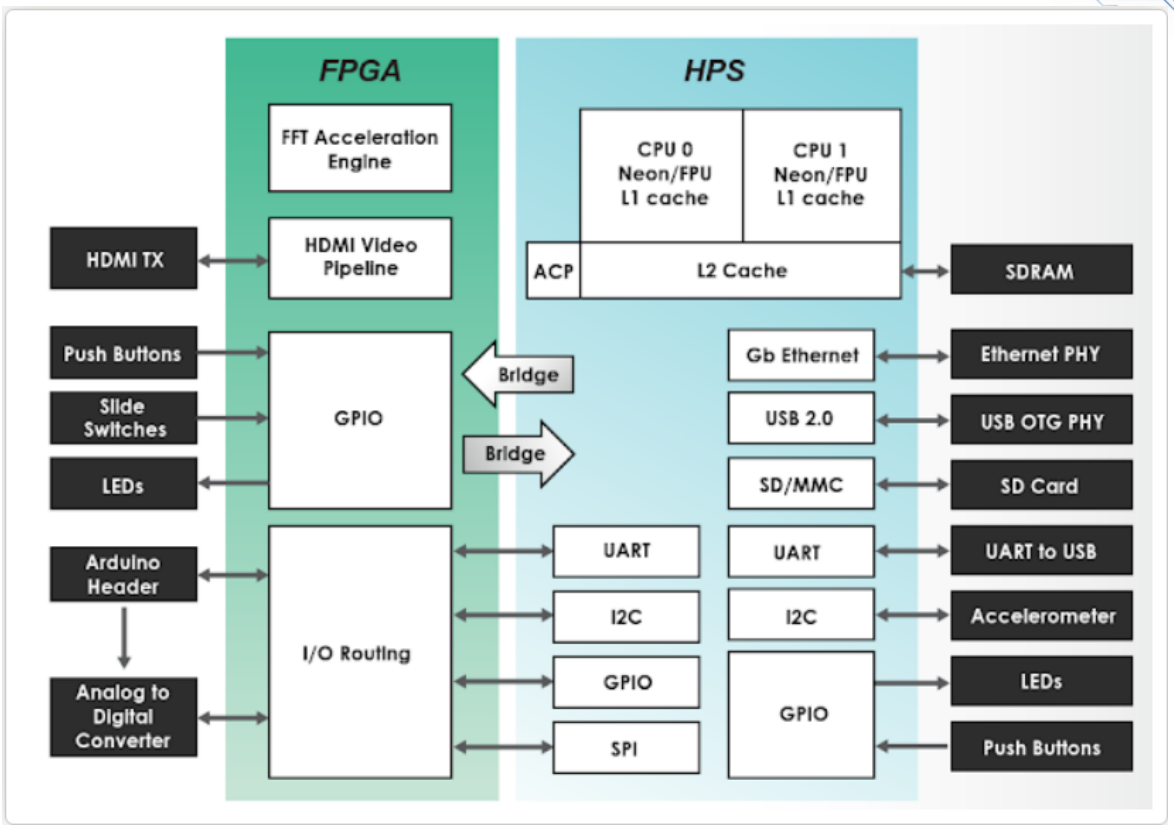


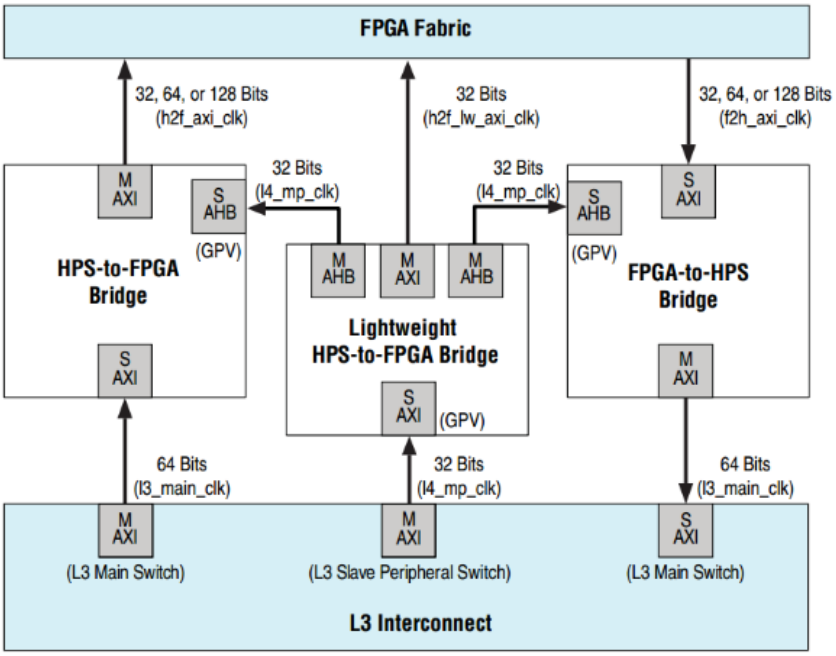




3. 問題與討論

- SOC FPGA 包含 HPS 和 FPGA，可以單獨使用 HPS 或 FPGA，也能兩個一起用，HPS 包含 ARM 處理器、記憶體控制器(AXI-bridge)、I/O 周邊。FPGA 的 BUS 是 Avalon，HPS 和 FPGA 之間要用 AXI-bridge 連接。


FPGA
HPS
FFT Acceleration Engine
HDMI Video Pipeline
GPIO
I/O Routing
CPU 0 Neon/FPU L1 cache
CPU 1 Neon/FPU L1 cache
ACP
L2 Cache
Bridge
Bridge
HDMI TX
Push Buttons
Slide Switches
LEDs
Arduino Header
Analog to Digital Converter
UART
I2C
GPIO
SPI
Gb Ethernet
USB 2.0
SD/MMC
UART
I2C
GPIO
SDRAM
Ethernet PHY
USB OTG PHY
SD Card
UART to USB
Accelerometer
LEDs
Push Buttons


FPGA Fabric
32, 64, or 128 Bits (h2f_axi_clk)
32 Bits (h2f_lw_axi_clk)
32, 64, or 128 Bits (f2h_axi_clk)
M AXI
S AHB
32 Bits (l4_mp_clk)
32 Bits (l4_mp_clk)
S AHB
S AXI
(GPV)
(GPV)
HPS-to-FPGA Bridge
M AHB
M AXI
M AHB
Lightweight HPS-to-FPGA Bridge
FPGA-to-HPS Bridge
S AXI
(GPV)
M AXI
64 Bits (l3_main_clk)
32 Bits (l4_mp_clk)
64 Bits (l3_main_clk)
M AXI
M AXI
S AXI
(L3 Main Switch)
(L3 Slave Peripheral Switch)
(L3 Main Switch)
L3 Interconnect