Graduate Degree Program of Artificial Intelligence,

National Yang Ming Chiao Tung University.

Digital Communication Integrated Circuits - Final Project

Low Latency Scaling-Free Pipeline CORDIC

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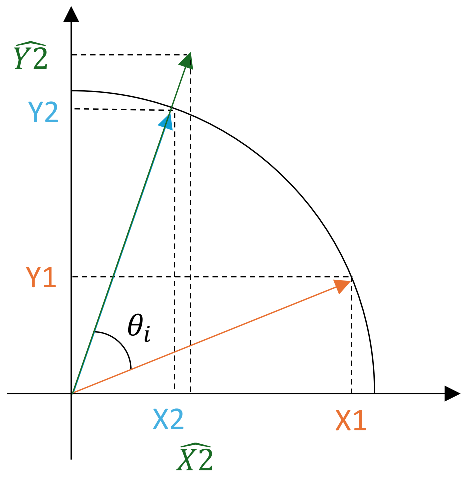
Github of my Project

Table of Contents

1. Introduction

CORDIC 是一種計算三角、雙曲或其他函數的有效方法，基本原理是利用預定義的基本角度(使用 ROM)組成目標角度，因為只需要 adder 和 shifter，所以利於硬體設計。本文將應用此演算法在直角座標轉換極座標。



在理解 CORDIC 前，先來探討旋轉公式。
假設從 X 旋轉到 Y

$$\begin{bmatrix} Y2 \\ X2 \end{bmatrix} = \begin{bmatrix} cos\theta_i & -sin\theta_i \\ sin\theta_i & cos\theta_i \end{bmatrix} \begin{bmatrix} Y1 \\ X1 \end{bmatrix}$$

$$= cos\theta_i \begin{bmatrix} 1 & -tan\theta_i \\ tan\theta_i & 1 \end{bmatrix} \begin{bmatrix} Y1 \\ X1 \end{bmatrix}$$

假設固定旋轉倍率，$tan\theta_i = 2^{-i}$，並忽略$cos\theta_i$，即可得偽長度

$$\begin{bmatrix} \widehat{Y2} \\ \widehat{X2} \end{bmatrix} = \begin{bmatrix} 1 & -2^{-i} \\ 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} Y1 \\ X1 \end{bmatrix}$$

$$\hat{\theta} = \theta_i - \mu_i tan^{-1}(2^{-i})$$

因此，可以利用此法從某一位置逐步旋轉到 X 軸，過程只需除以 2，對應硬體為移位，不需消耗資源，累積的θ_i即為與 X 軸的夾角，最後只需要將長度補償回來即可得到原長和角度。

i	2^i	rotate angle	scaling factor	CORDIC gain
0	1.0	45.000°	1.41421	1.41421
1	0.5	26.565°	1.11803	1.58114
2	0.25	14.036°	1.03078	1.62980
3	0.125	7.125°	1.00778	1.64248
4	0.0625	3.576°	1.00195	1.64569
5	0.03125	1.790°	1.00049	1.64649
6	0.015625	0.895°	1.00012	1.64669

可藉由上述旋轉角度累積轉到任意$-99^{\circ} \sim 99^{\circ}$，誤差可自己來決定轉到多小的角度，所以只要在一開始將所有角度旋轉到第一或第四象限，並將起始角度設定成相對應$\pm 90^{\circ} or\ 0^{\circ}$，即可抵達目的地。最後靠加法和移位即可除以 1.6 補償回原長。

$$\prod_{i=0}^{\infty} \frac{1}{cos\theta_i} = \prod_{i=0}^{\infty} \sqrt{1 + 2^{-2i}} = 1.6468 \ldots$$

2. Proposed Algorithm

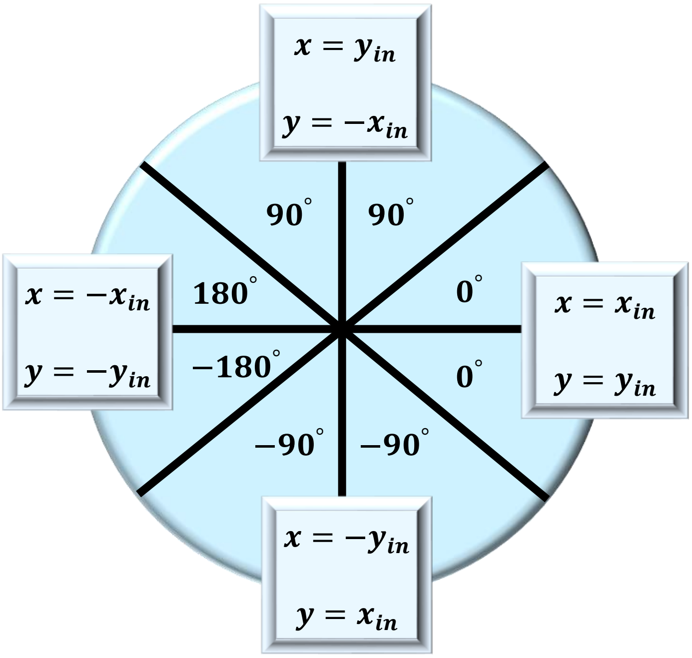
由於 CORDIC 較省計算資源，且需要較大的 latency，假設要不失去太多精度，又會增加不少硬體資源。因此，在本文使用小角度近似的性質減少 latency 的同時又不會失去太多精度，最後的角度藉由判斷是否跨過 X 軸旋轉來微調。

因為小角度近似$sin\theta_i \cong tan\theta_i = 2^{-i}$， $cos\theta_i \cong 1 - 2^{(2i+1)}$

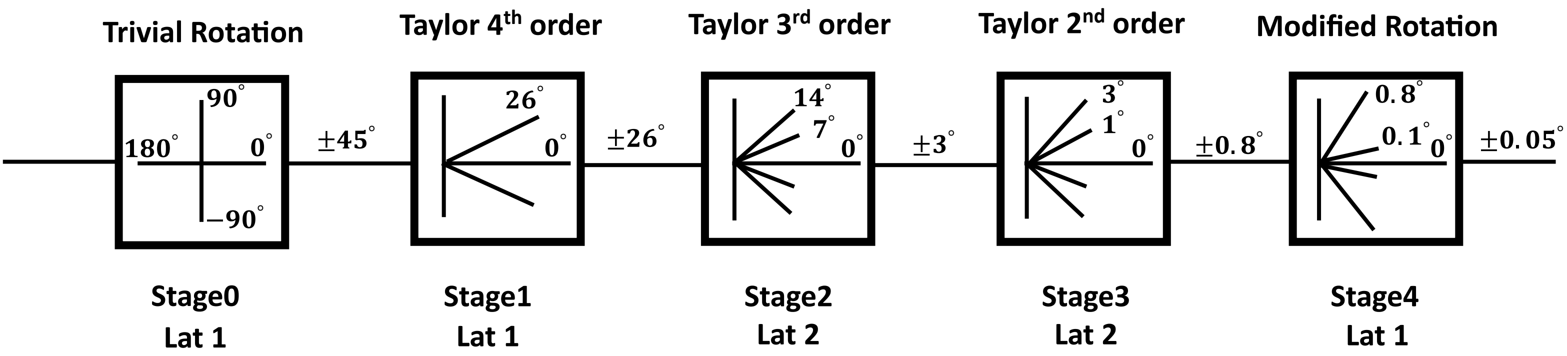
可將旋轉公式以特定階數泰勒展開，以下為 3 階簡略版，係數與原式有差

$$\begin{bmatrix} Y2 \\ X2 \end{bmatrix} = \begin{bmatrix} cos\theta_i & -sin\theta_i \\ sin\theta_i & cos\theta_i \end{bmatrix} \begin{bmatrix} Y1 \\ X1 \end{bmatrix} = \begin{bmatrix} 1 - 2^{(2i+1)} & -(2^{-i} - 2^{-(3i+3)}) \\ 2^{-i} - 2^{-(3i+3)} & 1 - 2^{(2i+1)} \end{bmatrix} \begin{bmatrix} Y1 \\ X1 \end{bmatrix}$$

藉由此法，就不需要補償長度，但是旋轉角度越大，需要越高階數才能近似，會增加不少硬體資源，所以我們不只旋轉到第一或第四象限，直接將範圍限縮至$\pm 45^\circ$，如此一來可忽略45°的旋轉，不只 latency 少一級，還能省去加法器和暫存器等資源。



上圖為指定角度範圍對應的起始角度，這樣便可以將所有角度先旋轉到$\pm 45^\circ$範圍內，查找表的角度從26°開始，之後再配合泰勒展開，便可以極大程度地減少硬體資源並減少 latency。



上圖為該演算法架構:

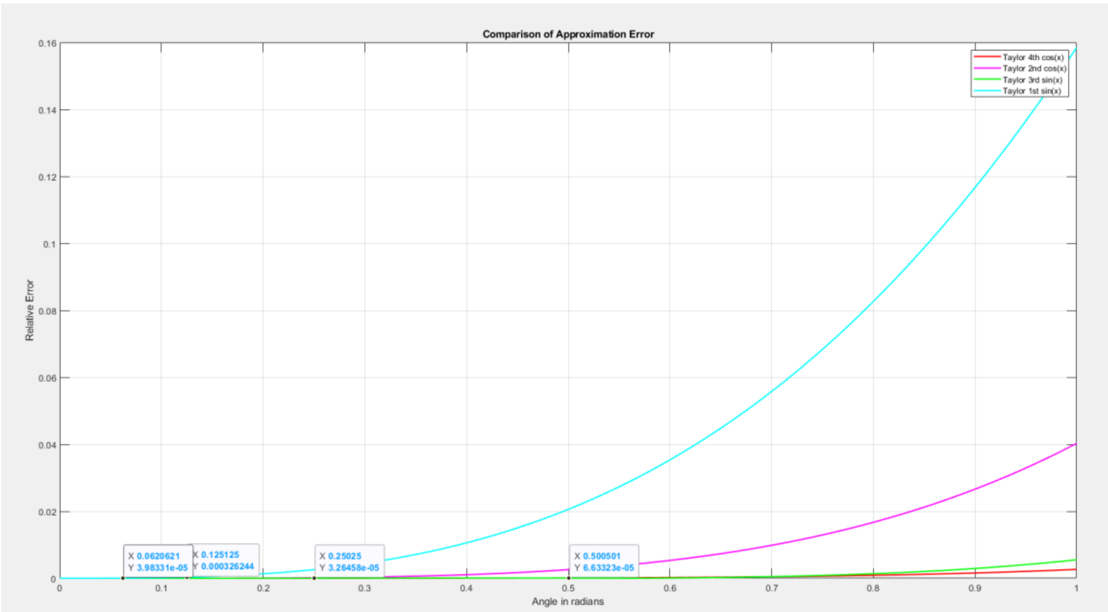
Stage0: 判斷 X,Y 座標以及絕對值大小關係來決定起始角度，轉 1 次。

Stage1: 對$cos\theta, sin\theta$做 4 階泰勒展開，誤差到小數點 **5th** bit 以下，轉 1 次。

Stage2: 對$cos\theta, sin\theta$做 3 階泰勒展開，誤差到小數點 **5th** bit 以下，轉 2 次。

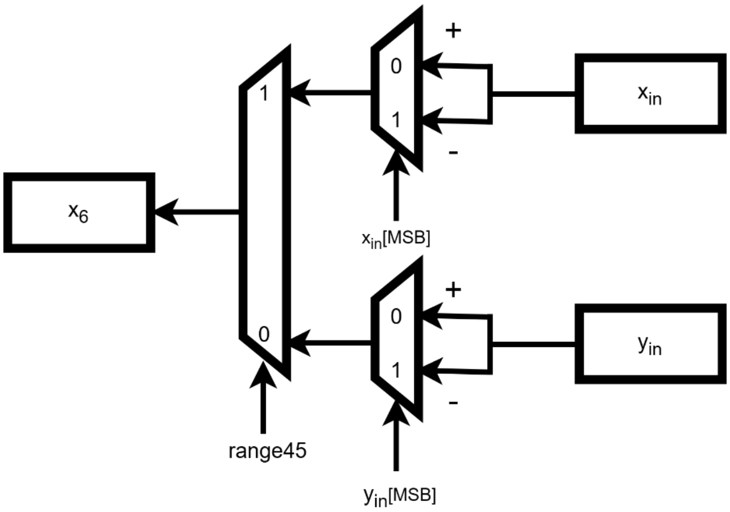
Stage3: 對$cos\theta, sin\theta$做 2 階泰勒展開，誤差到小數點 **5th** bit 以下，轉 2 次。

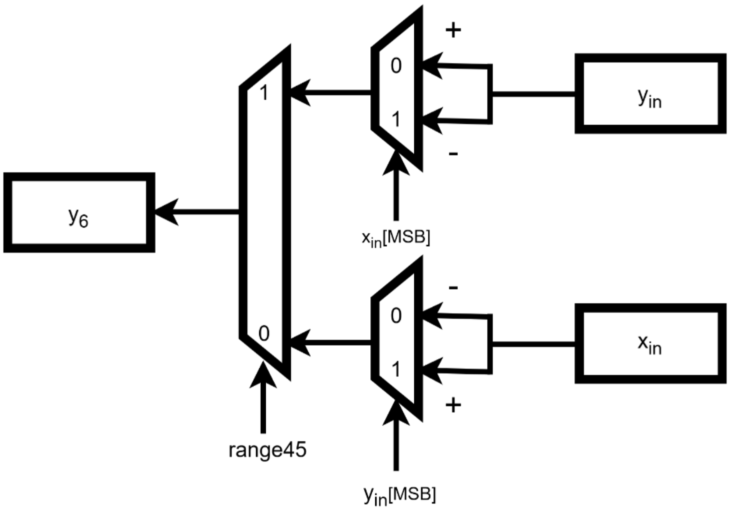
Stage4: 對$cos\theta, sin\theta$做 1 階泰勒展開，誤差到小數點 **10th** bit 以下，藉由 Y 值更新前後的 sign 以及絕對值大小判斷，如果該次旋轉跨過 X 軸且與 X 軸距離較短，大幅旋轉0.8°，否則小幅旋轉0.1°，轉 1 次。此階段優化在長度越小的情況下效果更顯著。

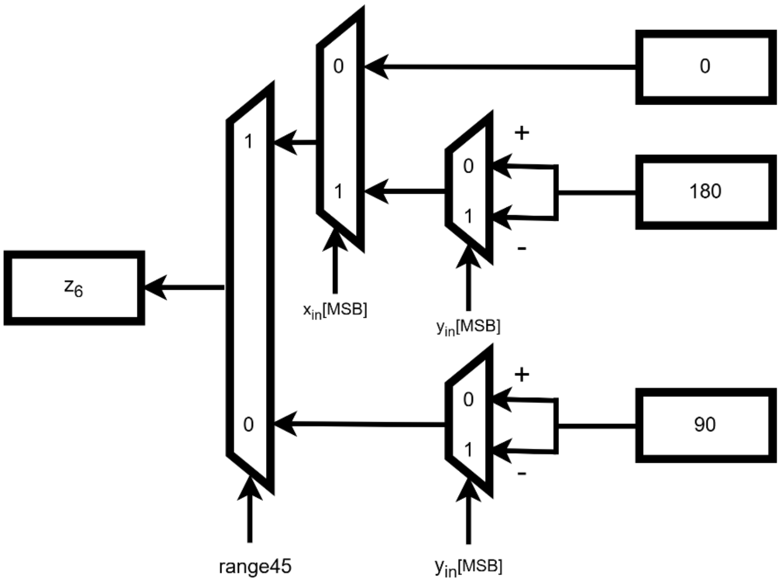


上圖為 MATLAB 模擬小角度近似在不同階數展開的誤差

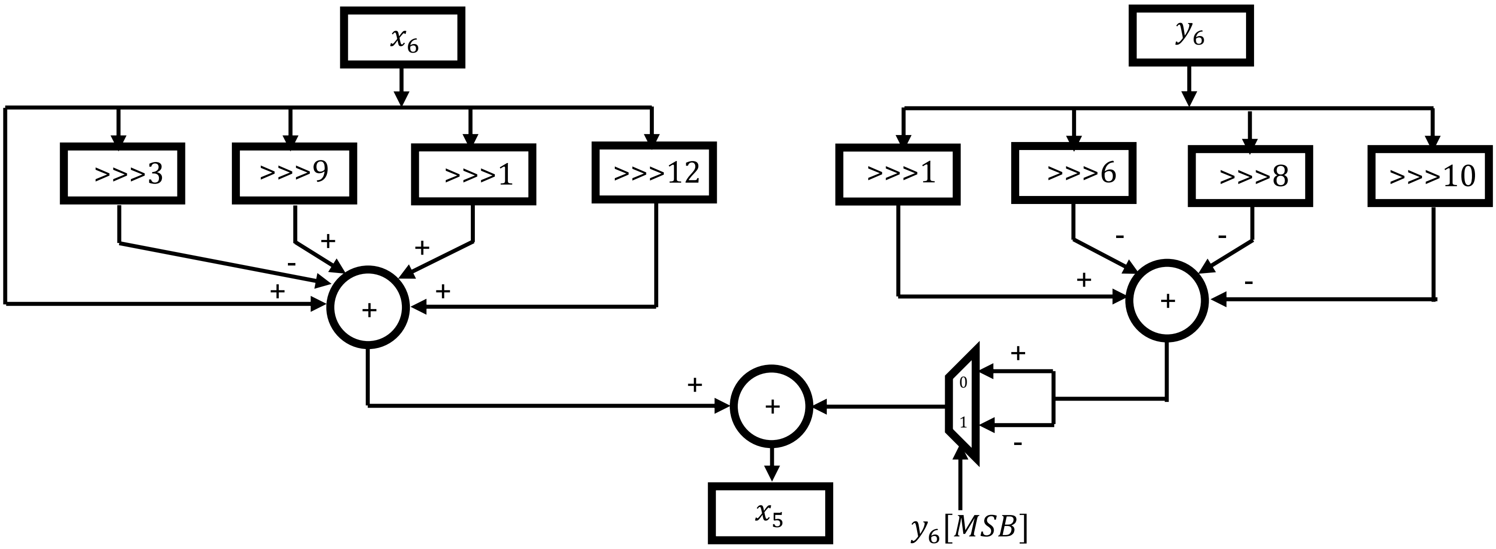
Stage0 Datapath

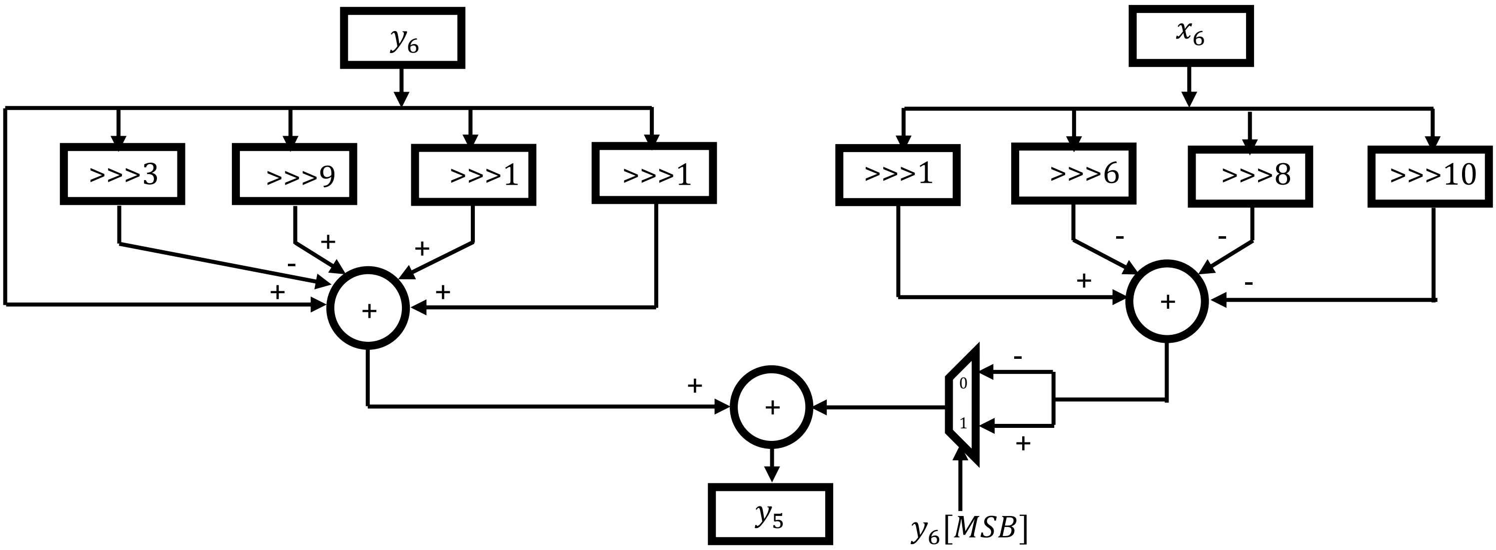


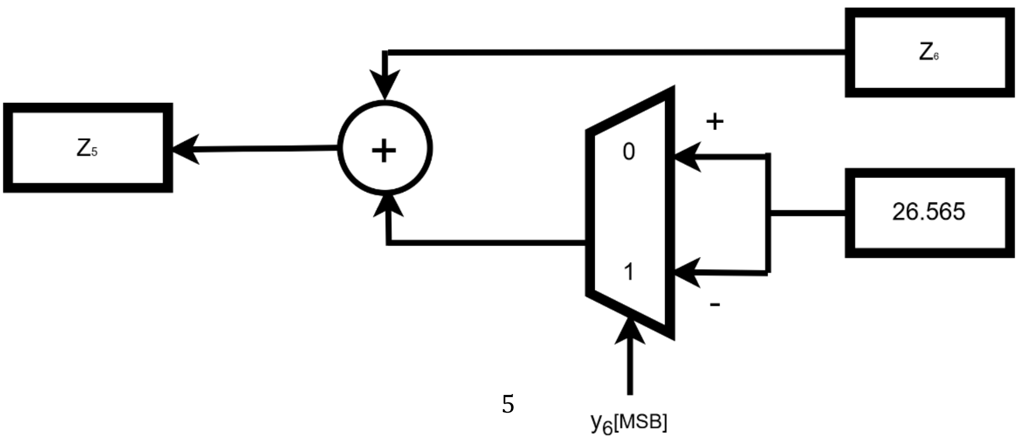




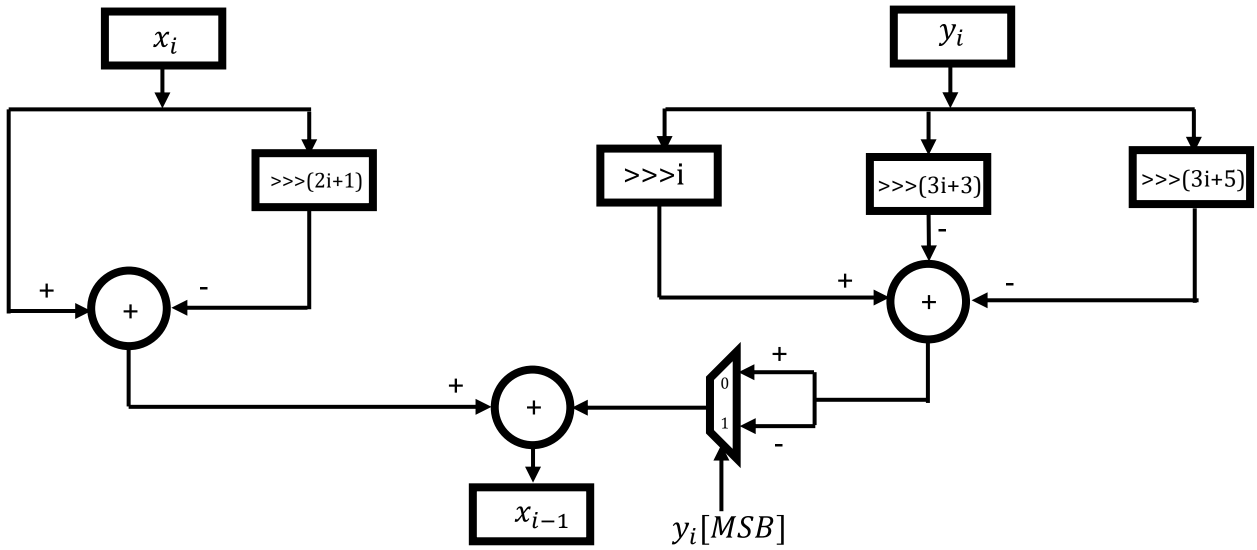
Stage1 Datapath

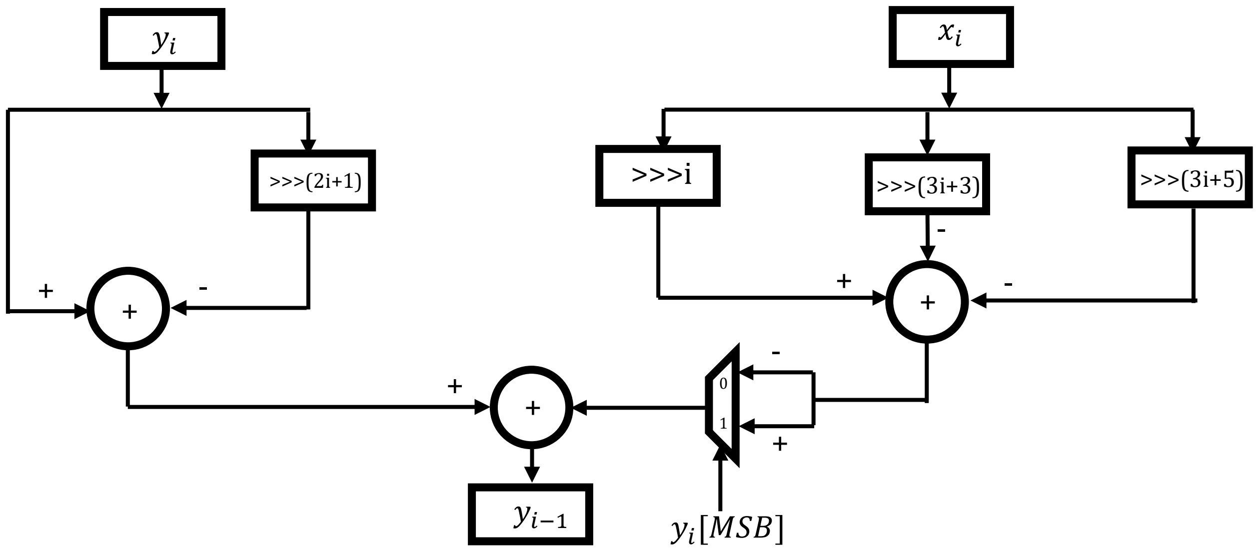


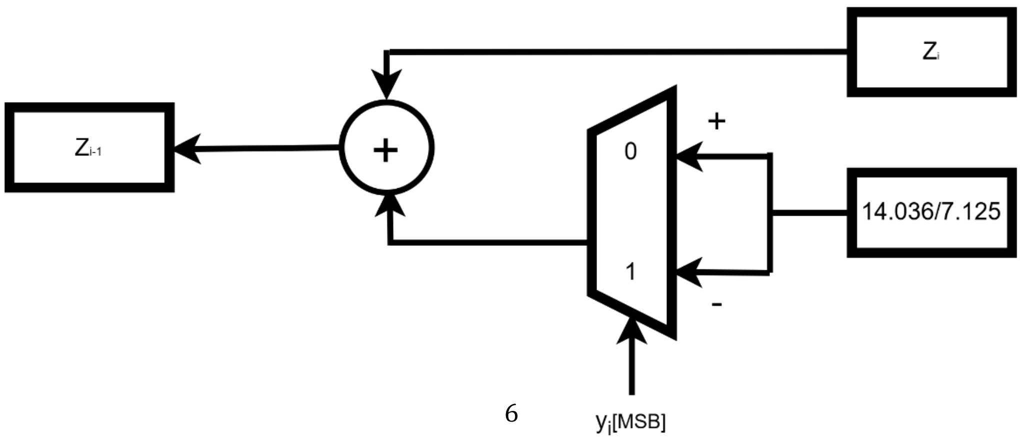




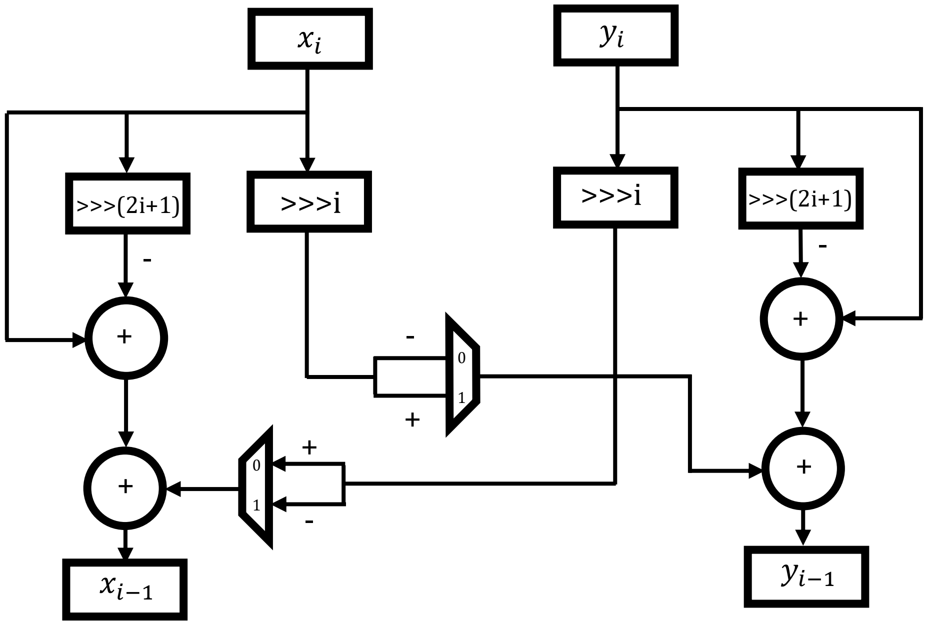
Stage2 Datapath(i=5,4)

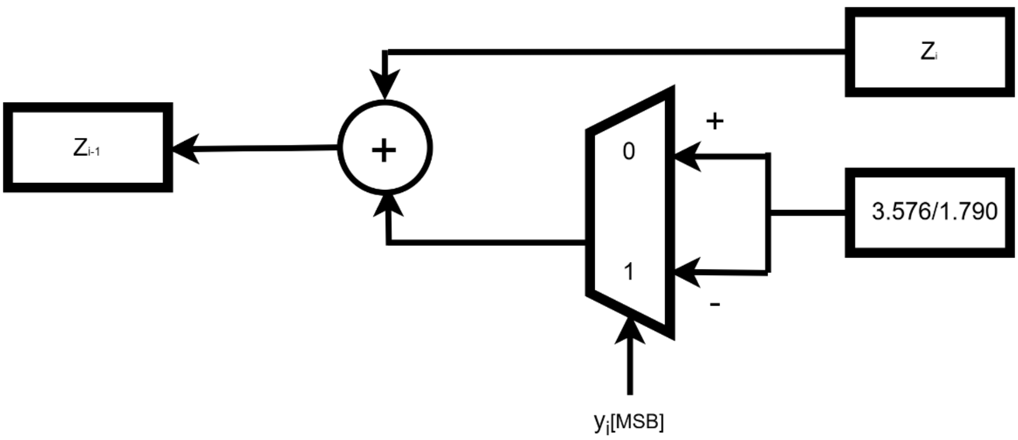




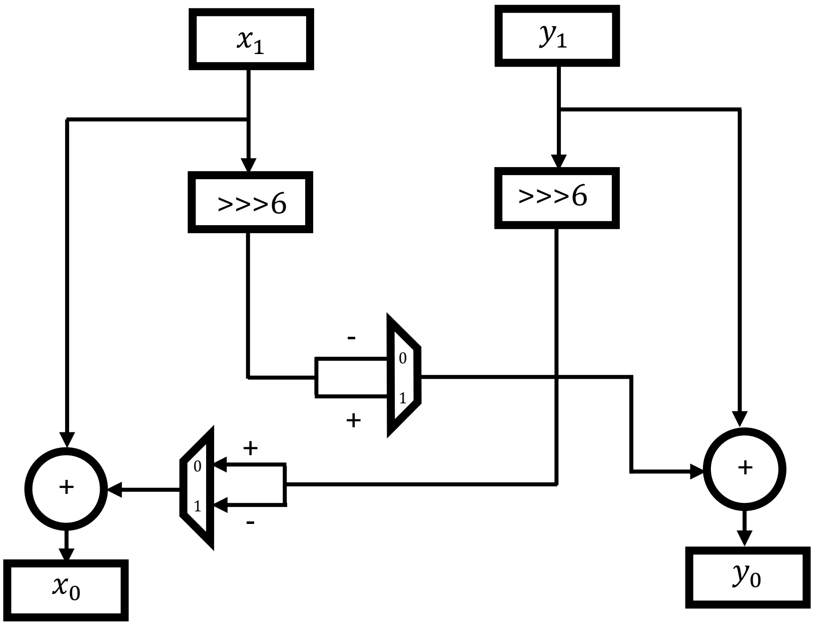


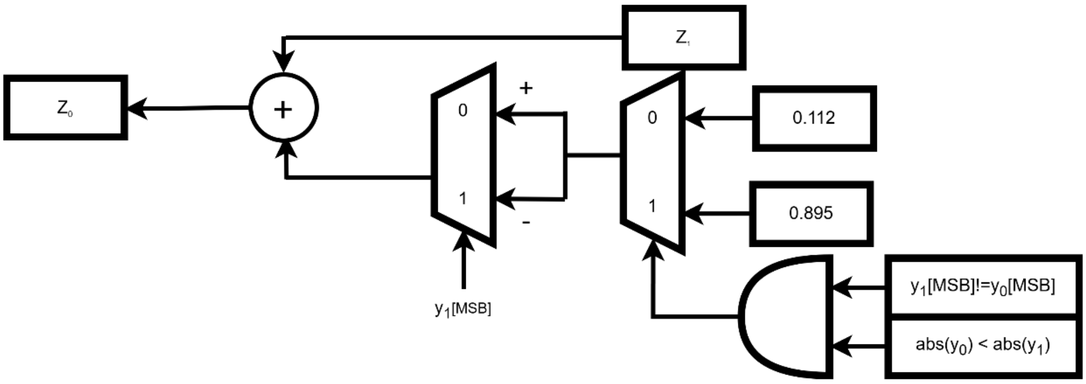
Stage3 Datapath(i=3,2)





Stage4 Datapath

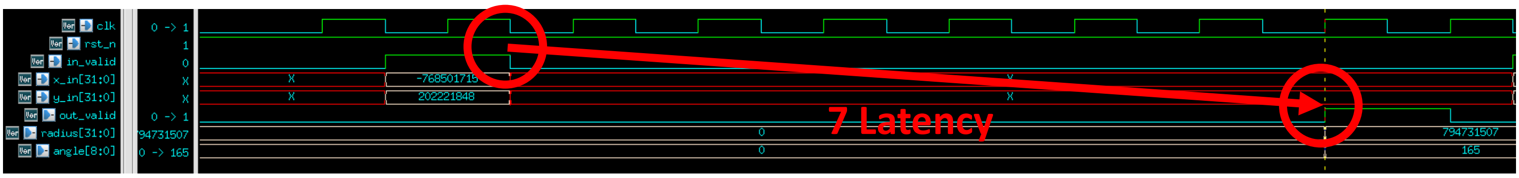




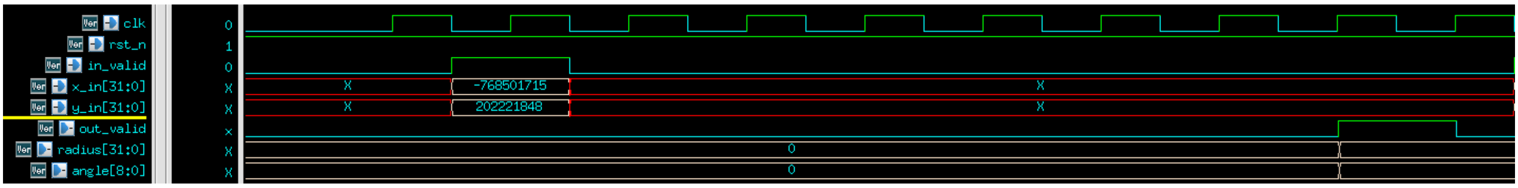
3. ASIC Implementation(UMC 180nm)

Simulation (Taylor CORDIC V.S. CORDIC)

RTL

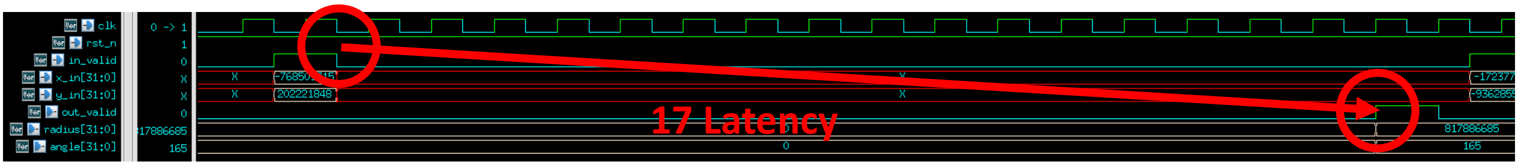


GATE

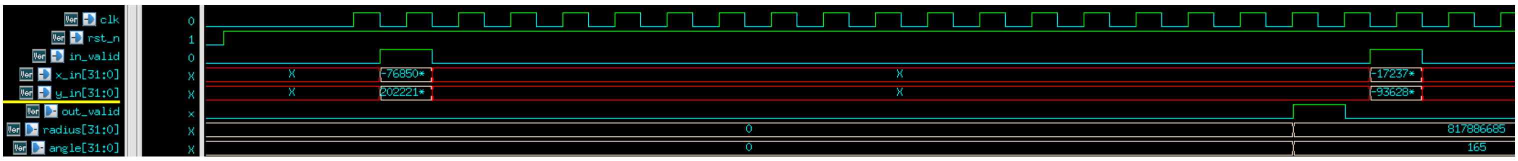



```
Total pat:      1000 Error_rate_radius: 0.000080 Error_rate_angle: 0.048929
```

RTL



GATE



```
Total pat:      1000 Error_rate_radius: 0.017685 Error_rate_angle: 0.017748
```

	Error_rate_radius	Error_rate_angle	Latency
Taylor CORDIC	0.000080	0.048929	7
CORDIC	0.017685	0.017748	17

Timing & Power & Area (Taylor CORDIC V.S. CORDIC)

```
clock clk (rise edge)                     50.00      50.00
clock network delay (ideal)                0.00      50.00
clock uncertainty                         -0.10      49.90
y_reg[6][6]/CK (DFFRHQXL)                  0.00      49.90 r
library setup time                        -0.17      49.73
data required time                                   49.73
-----------------------------------------------------------
data required time                                   49.73
data arrival time                                   -45.49
-----------------------------------------------------------
slack (MET)                                           4.24
```

```
clock clk (rise edge)                     0.00       0.00
clock network delay (ideal)               0.00       0.00
input external delay                     25.00      25.00 f
in_valid (in)                             0.00      25.00 f
U8175/Y (INVXL)                           1.52      26.52 r
U8166/Y (INVXL)                           1.41      27.93 f
U8167/Y (INVXL)                           1.87      29.80 r
U7136/Y (INVXL)                           0.97      30.77 f
U7133/Y (INVXL)                           1.75      32.52 r
U7150/Y (INVXL)                           1.41      33.93 f
U7138/Y (INVXL)                           1.64      35.57 r
U7752/Y (AOI22XL)                         0.19      35.76 f
U13407/Y (OAI2BB1XL)                      0.20      35.97 r
x_reg[16][14]/D (DFFRHQXL)                0.00      35.97 r
data arrival time                                   35.97

clock clk (rise edge)                    50.00      50.00
clock network delay (ideal)               0.00      50.00
clock uncertainty                        -0.10      49.90
x_reg[16][14]/CK (DFFRHQXL)               0.00      49.90 r
library setup time                       -0.16      49.74
data required time                                  49.74
-----------------------------------------------------------
data required time                                  49.74
data arrival time                                  -35.97
-----------------------------------------------------------
slack (MET)                                         13.77
```

```
                 Internal        Switching         Leakage           Total
Power Group      Power           Power             Power             Power    (   %    )  Attrs
---------------------------------------------------------------------------------------------
io_pad              0.0000          0.0000            0.0000          0.0000  (   0.00%)
memory              0.0000          0.0000            0.0000          0.0000  (   0.00%)
black_box           0.0000          0.0000            0.0000          0.0000  (   0.00%)
clock_network       0.6715          0.0000            0.0000          0.0000  (   0.00%)  i
register        3.8657e-02      9.3046e-03        2.1957e+06          0.7217  (  74.58%)
sequential          0.0000          0.0000            0.0000          0.0000  (   0.00%)
combinational       0.1707      6.5612e-02        9.6610e+06          0.2460  (  25.42%)
---------------------------------------------------------------------------------------------
Total               0.8809 mW   7.4917e-02 mW     1.1857e+07 pW       0.9677 mW
```

```
                 Internal        Switching         Leakage           Total
Power Group      Power           Power             Power             Power    (   %    )  Attrs
---------------------------------------------------------------------------------------------
io_pad              0.0000          0.0000            0.0000          0.0000  (   0.00%)
memory              0.0000          0.0000            0.0000          0.0000  (   0.00%)
black_box           0.0000          0.0000            0.0000          0.0000  (   0.00%)
clock_network       2.3263          0.0000            0.0000          0.0000  (   0.00%)  i
register            0.1204      1.4622e-02        7.5930e+06          2.4689  (  86.97%)
sequential          0.0000          0.0000            0.0000          0.0000  (   0.00%)
combinational       0.1788          0.1676        2.3402e+07          0.3698  (  13.03%)
---------------------------------------------------------------------------------------------
Total               2.6254 mW       0.1822 mW     3.0995e+07 pW       2.8386 mW
```

```
Number of ports:                          109
Number of nets:                          5360
Number of cells:                         4564
Number of combinational cells:           4134
Number of sequential cells:               430
Number of macros/black boxes:               0
Number of buf/inv:                        412
Number of references:                      45

Combinational area:             102433.164048
Buf/Inv area:                     4128.062549
Noncombinational area:           30034.065872
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                132467.229920
```

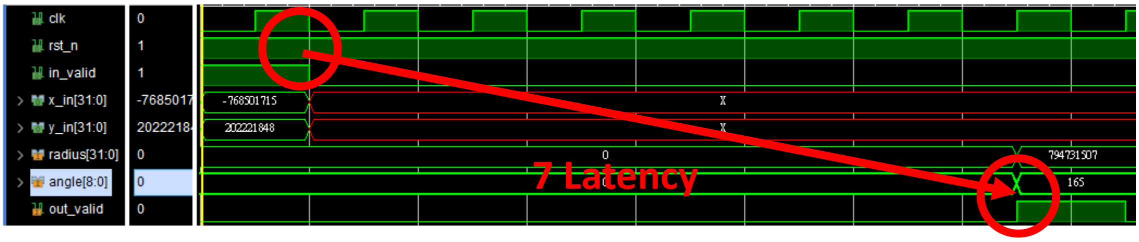
```
Number of ports:                          109
Number of nets:                         15443
Number of cells:                        13158
Number of combinational cells:          11671
Number of sequential cells:              1487
Number of macros/black boxes:               0
Number of buf/inv:                       1384
Number of references:                      38

Combinational area:             291063.333314
Buf/Inv area:                    13814.539702
Noncombinational area:          103873.493744
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                394936.827058
```

	Period(ns)	Power(mW)	Area(μm^2)
Taylor CORDIC	50	0.9677	132467
CORDIC	50	2.8386	394936

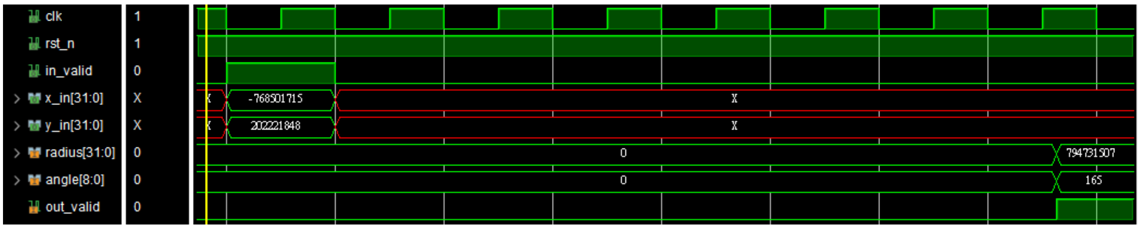
4. FPGA Implementation (Zedboard: Xilinx Zynq-7000)

Simulation (Taylor CORDIC V.S. CORDIC)

RTL

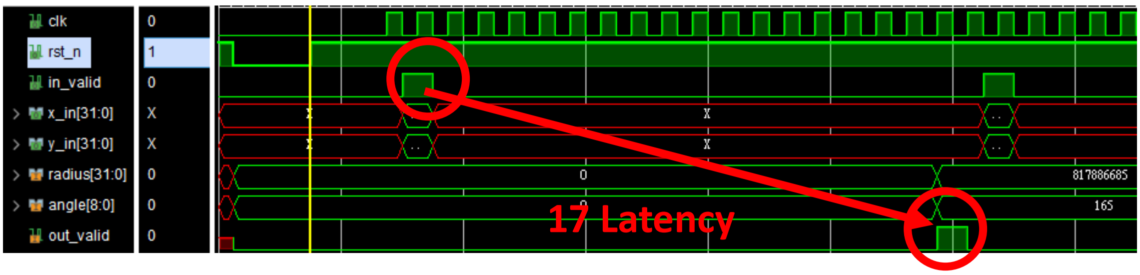


GATE




```
Total pat:     1000 Error_rate_radius: 0.000080 Error_rate_angle: 0.048929
```

RTL



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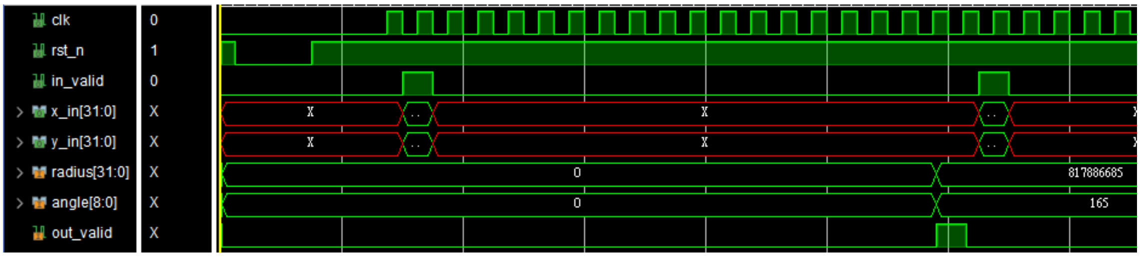



```
Total pat:     1000 Error_rate_radius: 0.017685 Error_rate_angle: 0.017748
```

	Error_rate_radius	Error_rate_angle	Latency
Taylor CORDIC	0.000080	0.048929	7
CORDIC	0.017685	0.017748	17

Timing & Power & Area (Taylor CORDIC V.S. CORDIC)

Setup

Worst Negative Slack (WNS):	18.824 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	900

Hold

Worst Hold Slack (WHS):	0.137 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	900

Pulse Width

Worst Pulse Width Slack (WPWS):	24.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	438

All user specified timing constraints are met.

Setup

Worst Negative Slack (WNS):	22.464 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2994

Hold

Worst Hold Slack (WHS):	0.137 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2994

Pulse Width

Worst Pulse Width Slack (WPWS):	24.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	1503

All user specified timing constraints are met.

derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.117 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.3°C**
Thermal Margin:	58.7°C (4.9 W)

Dynamic:	0.012 W	(10%)
Clocks:	0.001 W	(8%)
Signals:	0.003 W	(27%)
Logic:	0.004 W	(32%)
I/O:	0.004 W	(33%)
Device Static:	0.105 W	(90%)

derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.121 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.4°C**
Thermal Margin:	58.6°C (4.9 W)

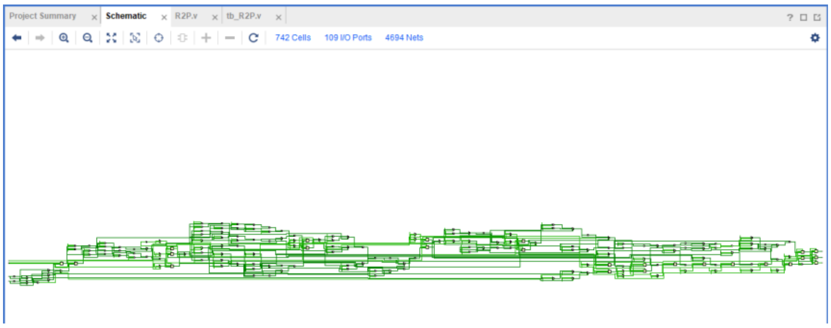
Dynamic:	0.016 W	(14%)
Clocks:	0.003 W	(18%)
Signals:	0.004 W	(26%)
Logic:	0.005 W	(31%)
I/O:	0.004 W	(25%)
Device Static:	0.105 W	(86%)

Name	Slice LUTs (53200)	Slice Registers (106400)	Bonded IOB (200)	BUFGCTRL (32)
R2P	1687	437	109	1

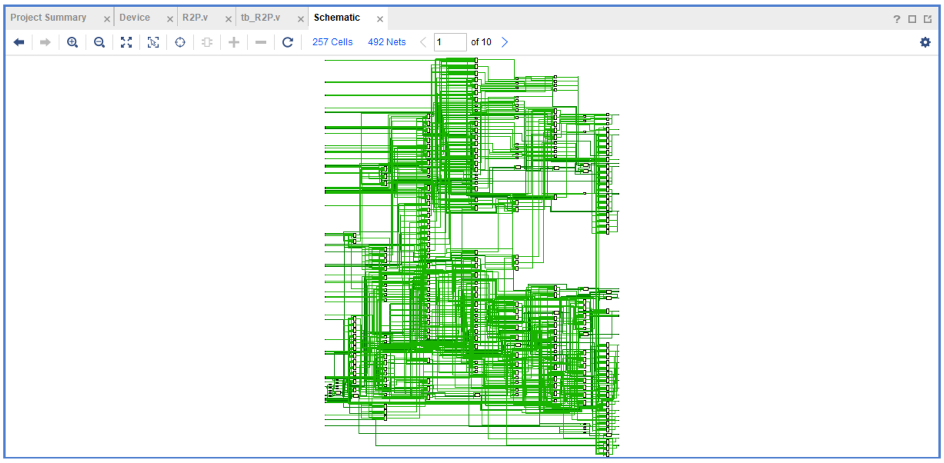
Name	Slice LUTs (53200)	Slice Registers (106400)	Bonded IOB (200)	BUFGCTRL (32)
R2P	2976	1502	109	1

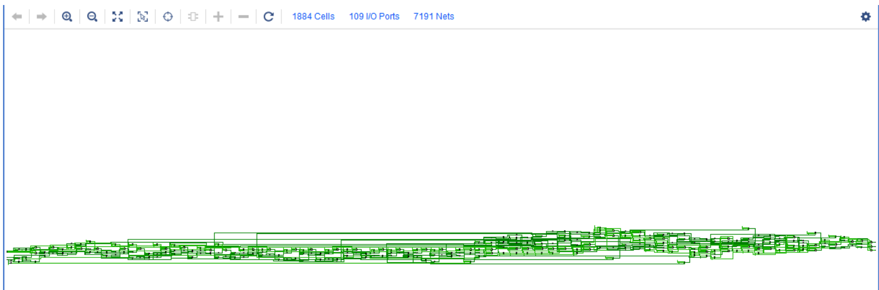
	Period(ns)	Power(W)	Slice LUTs
Taylor CORDIC	50	0.117	1687
CORDIC	50	0.121	2976

RTL elaboration & Logic synthesis (Taylor CORDIC V.S. CORDIC)

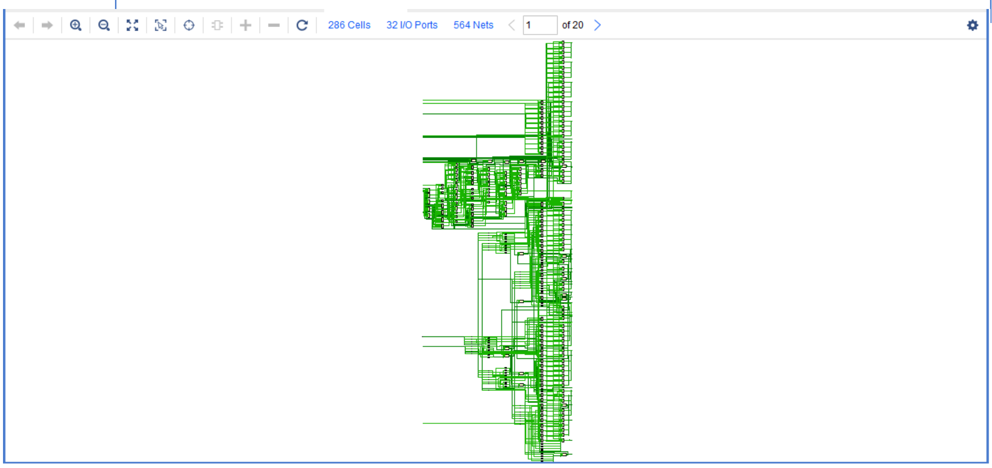


Taylor CORDIC



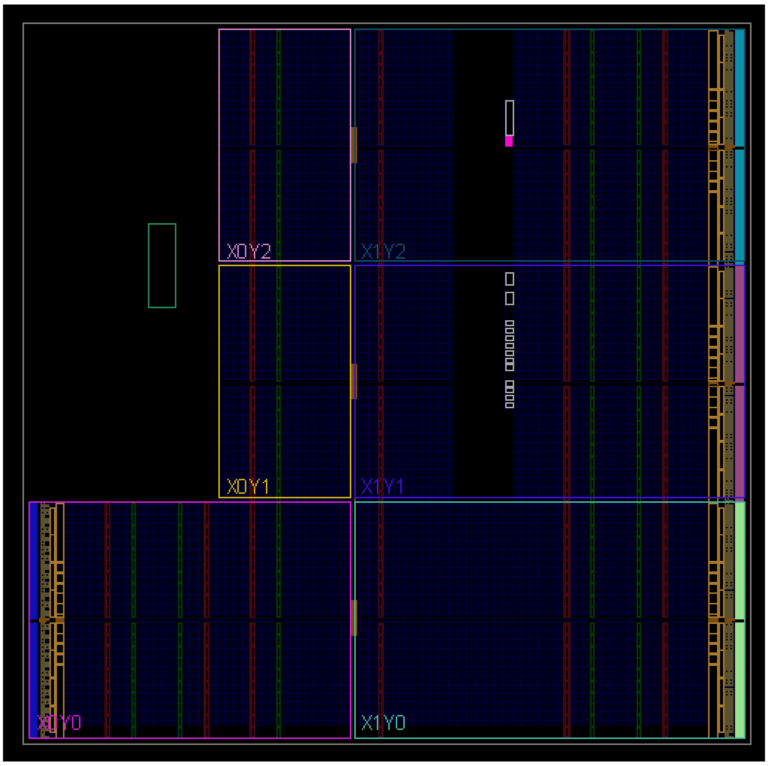


CORDIC

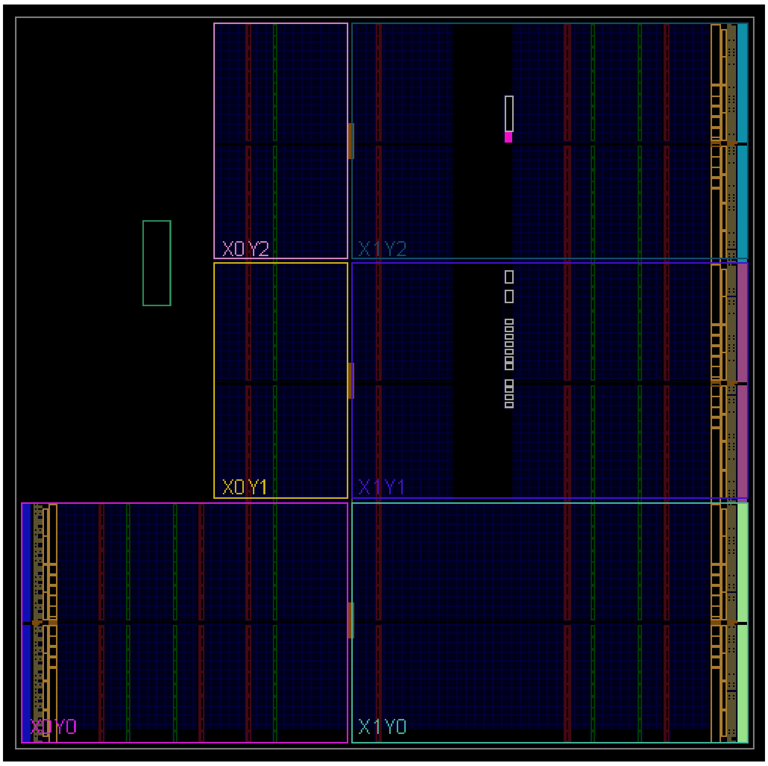


Implementation (Taylor CORDIC V.S. CORDIC)

Taylor CORDIC



CORDIC



5. Conclusion

Taylor CORDIC 在每一級使用泰勒展開，只需要付出額外一些加法器電路便可在 low latency 得到 scaling-free 的長度，在最後一級甚至只加入一階展開即可得到誤差在小數點 **5th** bit 以下，雖然 critical path 相對傳統方法更長，但是可以使用特定加法器去彌補 timing issue，而傳統方法需要更多硬體補償回原長。在角度誤差方面，由於藉由泰勒展開加速收斂，角度相對傳統方法容易失真，所以在最後一級的地方用簡易的邏輯判斷來減少一點誤差。未來會朝角度誤差改善，在泰勒展開時，使用較精準的角度更新判斷，期望能設計出誤差小，latency 更低的電路。

6. Reference

S. S. Wadkar, B. P. Das and P. K. Meher, "Low Latency Scaling-Free Pipeline CORDIC Architecture Using Augmented Taylor Series," *2019 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS)*, Rourkela, India, 2019, pp. 312-315, doi: 10.1109/iSES47678.2019.00077.