University of Global Village (UGV), Barishal

Department of Electrical And Electronics Engineering

EEE 0714-2101
Principle of Electronics
Theory Course Content

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Basic Course Information:

- **Course Title :** Principle of Electronics
- **Course Code:** EEE 0714 – 2101
- **CIE Marks:** 90
- **SEE Marks:** 60
- **Exam Hours:** 2 hours (Mid term Examination)

  3 hours (Semester End Examination)
- **Semester:** 3rd Semester
- **Academic Session:** Winter 2025

Electronics-II

Assessment Pattern:

CIE – Continuous Internal Evaluation (90 Marks)

Bloom's Category Marks (out of 90)	Mid Term (45)	Assignment (15)	Quiz (15)	Attendance & External
Remember	05		05	
Understand	05	05	05	
Apply	10		05	15
Analyze	10			
Evaluate	10			
Create	05	05		

Electronics-II

Assessment Pattern:

SEE – Semester End Examination (60 Marks)

Bloom's Category Marks (out of 90)	Final Examination Term (60)
Remember	15
Understand	10
Apply	10
Analyze	10
Evaluate	10
Create	05

Course Learning Outcome (CLO's):

CLO1	Explain how the basic concepts of solid-state physics relate to the different properties of semiconductors.
CLO2	Determine the energy band diagrams of different semiconductor devices under different operating conditions.
CLO3	Calculate charge, current, voltage and capacitance of different semiconductor devices under different operating conditions.
CLO4	Explain the operation and terminal characteristics of diodes, BJTs, and MOSFETs.
CLO5	Analyze the diode, BJT, and MOSFET circuits with DC only or DC and AC sources
CLO6	Analyze the BJT and MOSFET amplifier circuits to evaluate amplifiers' performance parameters

Course Rationales:

This Course is very essential for learning concepts, principles, and workings of basic electronic circuits. It is targeted to provide a basic foundation for technological areas like electronics devices, communication systems, industrial electronics as well as instrumentation, control systems and various electronic circuit designs.

Course Objectives :

The objective of this course is to give students the basic knowledge of electronic devices like diode, Transistor, MOSFET, Op-Amp, UJT etc. and its applications. Also, to make the students skilled at designing different electronic circuits like rectifiers, amplifiers etc. using electronic devices and to gather basic knowledge about IC fabrication.

Course Contents Summary

Sl. No.	Course Content	Hrs	CLOs
1	Semiconductor, Semiconductor materials, Covalent Bonding, Energy Levels, n-type, p-type, donor atoms, acceptor atoms, majority carriers, minority carriers, No applied bias, Reverse bias, forward bias condition	10	CLO1
2	Shockley's equation and Thermal Voltage, Breakdown Region and Breakdown Potential, Ideal vs Actual Semiconductor characteristics, Difference between Semiconductor diode and mechanical switch,	6	CLO2 CLO3
3	Piecewise-linear equivalent circuit and Simplified vs Ideal vs Piecewise- linear equivalent circuit, Definition, Concept, Implementation and Math Problems related to Reverse recovery time and LED	10	CLO4

Course Contents Summary

SL NO	Course Content	Hrs	CLOs
4	Definition, Concept, Implementation and Math problems related to Load line analysis and Q Point, Half Wave and Full Wave Rectification	8	CLO5
5	Definition, Concept, Implementation and Math problems related to Clippers and Clampers, Zener diode, Zener regulator, Voltage Doubler, Transistor Construction, Common Base Configuration, Output characteristics of Common Base Transmitter	10	CLO6
6	Common Emitter Configuration, Common Collector Configuration, Definition, Basic Concept and Difference between Fixed Bias, Emitter Bias and Voltage Divider Bias, Definition, Basic Concept and Difference between Collector Feedback, Emitter Follower, Common Base	10	CLO5 CLO6
7	MOSFET: Depletion, Enhancement type. (n channel), MESFET: Depletion, Enhancement type. (n channel). Basic Concept of CMOS Inverter	6	CLO2 CLO3 CLO6

COURSE PLAN MAPPED WITH CLO

Week	Content of Course	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
1	Introduction to Semiconductor Diodes: Qualitative and quantitative theory of the p-n junction as a diode; ideal p-n junction, band diagrams, current components.	Lecture, Visual Demonstration	Quiz, Problem Solving	CLO-1
2	Volt-Ampere Characteristics: Transition and diffusion capacitance; dynamic resistance; reverse breakdown (avalanche and Zener breakdown).	Lecture, Problem Solving, Practical Examples	Problem Solving, Quiz	CLO-1
3	Zener Diode and Applications: Zener as a voltage regulator, controlled & uncontrolled rectification.	Lecture, Design Activities	Problem Solving, Assignment	CLO-2

COURSE PLAN MAPPED WITH CLO

Week	Course Content	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
4	Special-Purpose Diodes: Tunnel diode, varactor diode, breakdown diode, optical diode, PIN diode, Schottky diode, and current regulator diode.	Lecture, Demonstration	Quiz, Assignment	CLO-2
5	Rectifier Circuits: Half-wave, full-wave, and bridge rectifiers; performance analysis (ripple factor, efficiency).	Lecture, Circuit Simulation	Quiz, Problem Solving	CLO-2,3
6	Filtering in Rectifiers: Capacitor, inductor, and π filters; design and efficiency improvements.	Lecture, Circuit Design	Assignment, Problem Solving	CLO-2,5
7	Class Test-1: Review and problem solving on diodes and rectifier circuits.	Review, Problem Solving	Class Test	CLO-1, CLO-2
8	Introduction to Transistors: BJT structure, current components, and transistor as an amplifier.	Lecture, Practical Examples	Quiz, Problem Solving	CLO-3,

COURSE PLAN MAPPED WITH CLO

Week	Course Content	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
9	**BJT Configurations: Common Base (CB), Common Emitter (CE), and Common Collector (CC); comparative analysis.**	**Lecture, Demonstration**	**Problem Solving, Quiz**	**CLO-3**
10	Load Line Analysis: DC and AC load lines; operating point selection and stabilization.	Lecture, Practical Examples	Assignment, Problem Solving	CLO-3
11	Transistor Biasing Techniques: Fixed bias, collector feedback bias, voltage divider bias; thermal stabilization.	Lecture, Design Activities	Problem Solving, Written Exam	CLO-3
12	Class Test-2: Review and problem solving on transistors and biasing techniques.	Review, Problem Solving	Class Test	CLO-3
13	Transistor Switching Times: Saturation, cut-off, and active regions; switching time calculations.	Lecture, Circuit Demonstration	Quiz, Problem Solving	CLO-4,5

COURSE PLAN MAPPED WITH CLO

Week	Course Content	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
14	**Small Signal Model of Transistors: Voltage gain, input/output resistance, and frequency response.**	**Lecture, Circuit Design**	**Assignment, Quiz**	**CLO-4,6,7**
15	Special Applications of BJTs: Amplifier design (CE, CB configurations); power amplifiers introduction.	Lecture, Circuit Simulation	Problem Solving, Written Exam	CLO-4,5,6
16	Course Review and Practical Applications: Practical design and analysis of diode and transistor circuits.	Group Problem Solving, Review	Problem Solving, Assignment	CLO-1, CLO-2, CLO-3, CLO-4, CLO-5,CLO-6,CLO-7
17	Viva and Presentation: Comprehensive evaluation of all topics through oral exams and project presentations.	Viva-Voce, Student Presentations	Viva, Presentation	CLO-1, CLO-2, CLO-3, CLO-4, CLO-5,CLO-6,CLO-7

References

- Electronic Devices and Circuit Theory by Robert L. Boylestad
- Principle of Electronic Materials and Devices by S O Kasap
- Electronic Devices and Circuits by Jacob Millman
- Principle of Electronics by V. K. Mehta

Week - 1

Semiconductor Materials

- **Materials commonly used in the development of semiconductor devices**
  - **Silicon (Si)**
  - **Germanium (Ge)**
  - **Gallium Arsenide (GaAs)**

Doping

- The electrical characteristics of silicon and germanium are improved by adding materials in a process called doping.
- There are just two types of doped semiconductor materials
  - n-type
  - p-type
- n-type materials contain an excess of conduction band electrons.
- p-type materials contain an excess of valence band holes.

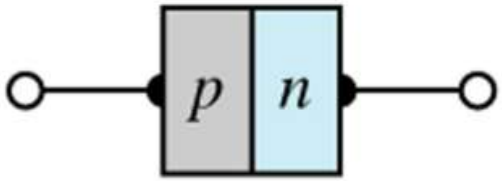
Majority and Minority Carriers

- **Two currents through a diode**
  - **Majority Carriers**
    - **The majority carriers in *n*-type materials are electrons.**
    - **The majority carriers in *p*-type materials are holes.**
  - **Minority Carriers**
    - **The minority carriers in n-type materials are holes.**
    - **The minority carriers in p-type materials are electrons.**

p-n Junctions (1/2)

- **One end of a silicon or germanium crystal can be doped as a *p*-type material and the other end as an *n*-type material.**

- **The result is a *p-n* junction**

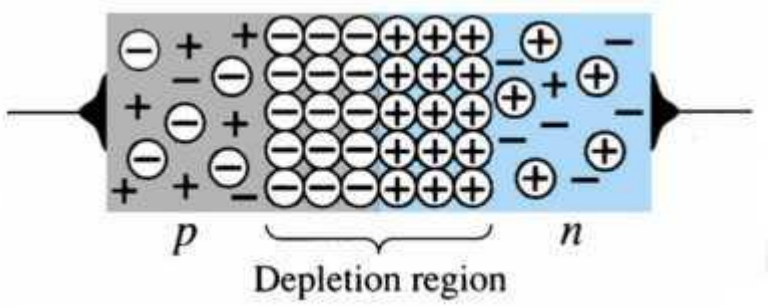


p-n Junctions (2/2)

- **At the *p*-*n* junction, the excess conduction-band electrons on the *n*-type side are attracted to the valence-band holes on the *p*-type side.**

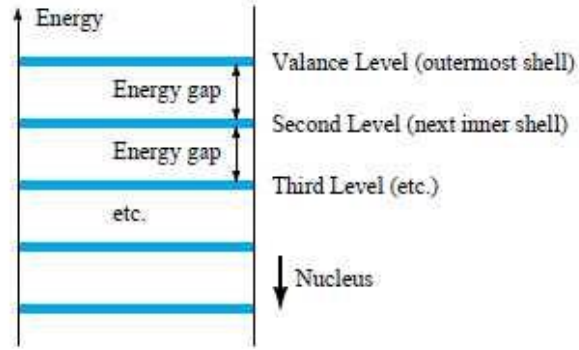
  The electrons in the *n*-type material migrate across the junction to the *p*-type material (electron flow).

- **The electron migration results in a negative charge on the p-type side of the junction and a positive charge on the n-type side of the junction.**

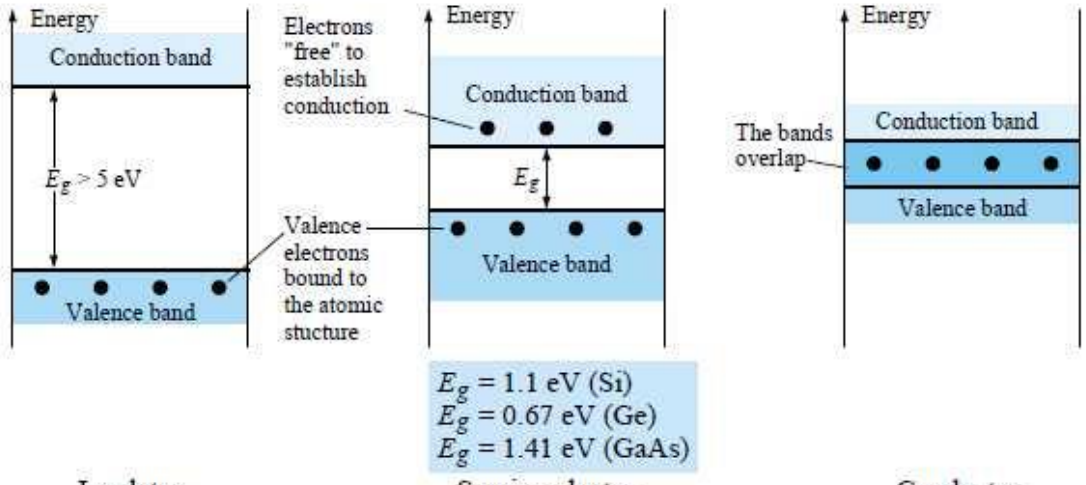


The result is the formation of a depletion region around the junction.

Energy Levels



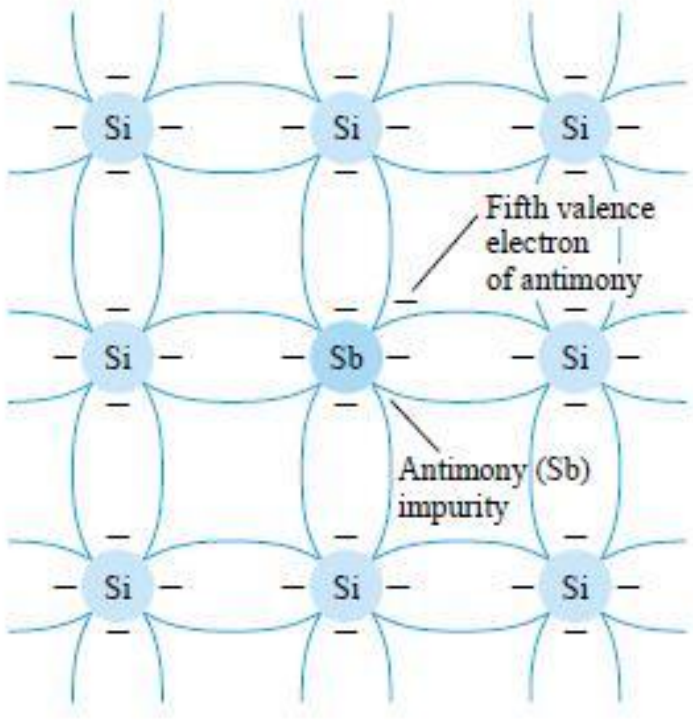
(a)



(b)

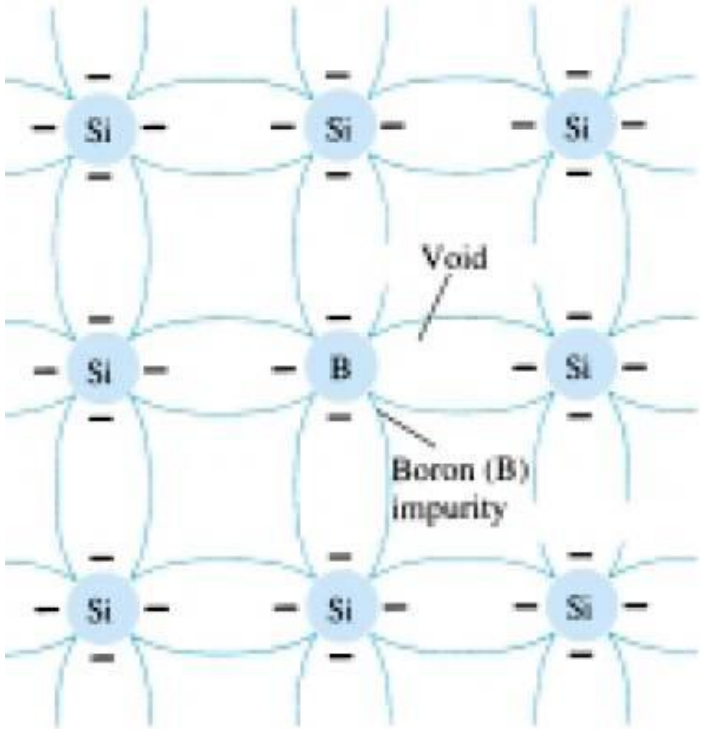
Extrinsic Materials (1/2)

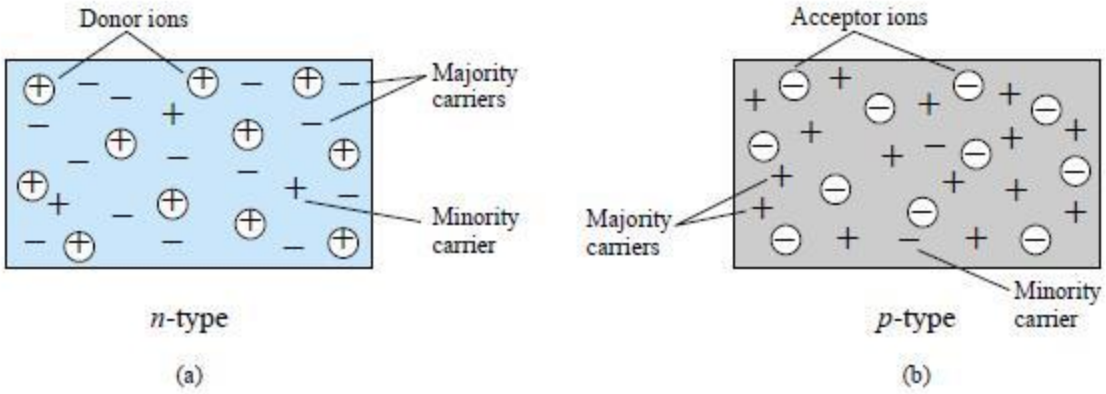
- A semiconductor material that has been subjected to the doping process is called an extrinsic material
- *n*-Type Material
  - **The n-type is created by introducing those impurity elements that have five valence electrons (pentavalent), such as antimony, arsenic, and phosphorus.**



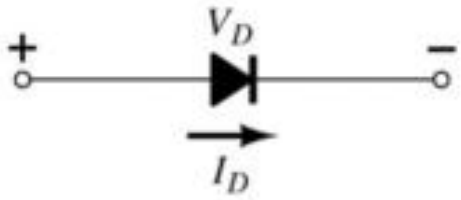
Extrinsic Materials (2/2)

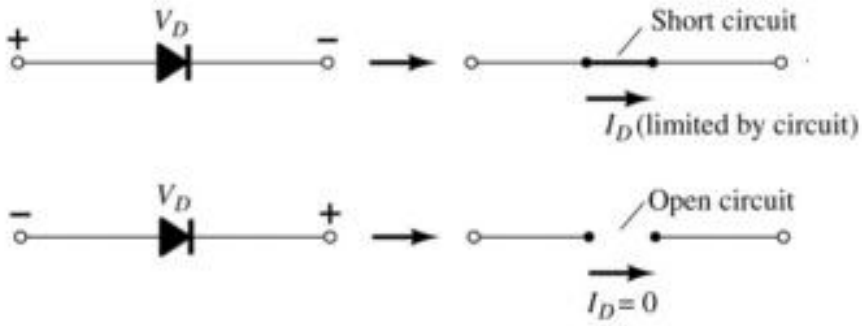
- **p-Type Material**
  - **The p-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having three valence electrons**





Diodes





The diode is a 2-terminal device.

A diode ideally conducts in only one direction.

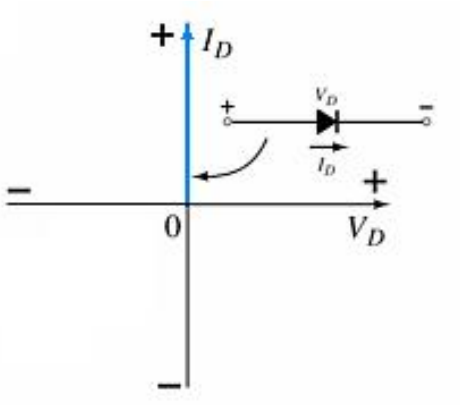
The ideal diode, therefore, is a short circuit for the region of conduction

The ideal diode, therefore, is an open circuit in the region of nonconduction.

Diode Characteristics

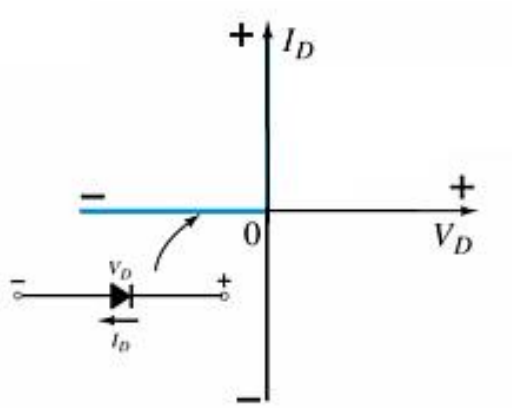
Conduction Region

- The voltage across the diode is 0 V
- The current is infinite
- The forward resistance is defined as $R_F = V_F / I_F$
- The diode acts like a short



Non-conduction Region

- All of the voltage is across the diode
- The current is 0 A
- The reverse resistance is defined as $R_R = V_R / I_R$
- The diode acts like open

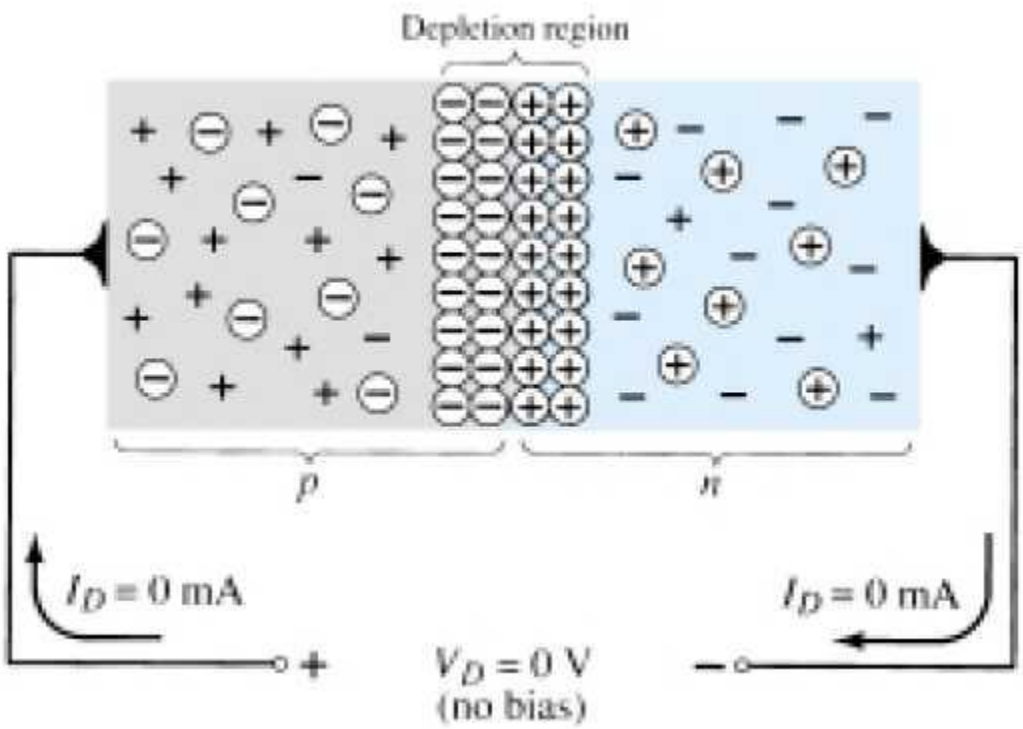


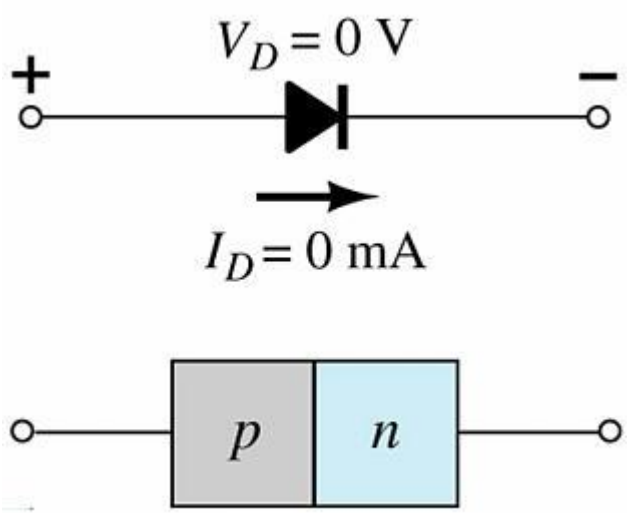
Diode Operating Conditions

- **A diode has three operating conditions**
  - **No bias**
  - **Forward bias**
  - **Reverse bias**

Diode Operating Conditions- No Bias

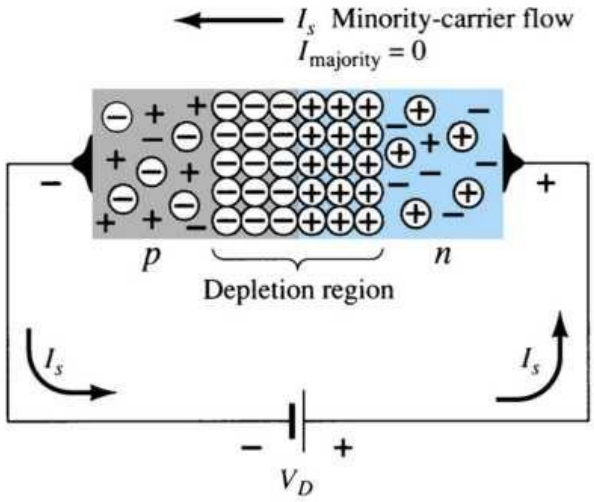
- No external voltage is applied: $V_D = 0$ V
- No current is flowing: $I_D = 0$ A
- Only a modest depletion region exists

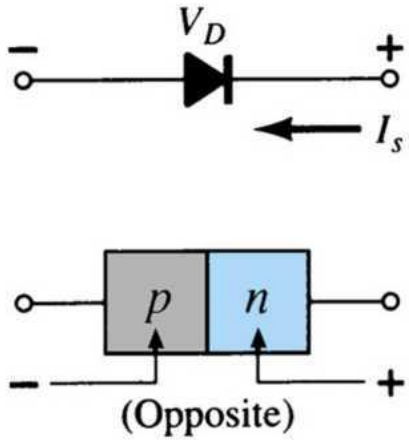




Diode Operating Conditions- Reverse Bias

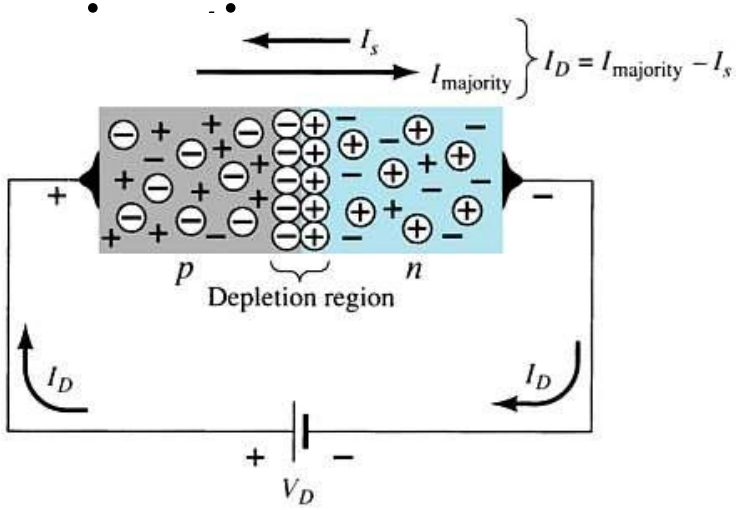
- External voltage is applied across the *p*-*n* junction in the opposite polarity of the *p*- and *n*-type materials.
- The reverse voltage causes the depletion region to widen.
- The electrons in the *n*-type material are attracted toward the positive terminal of the voltage source.
- The holes in the *p*-type material are attracted toward the negative terminal of the voltage source.

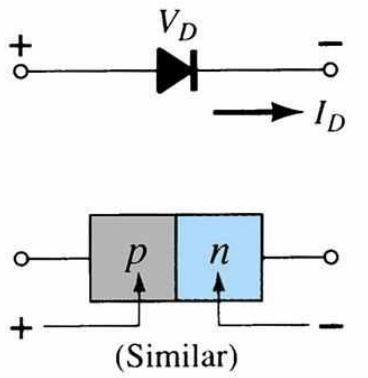




Diode Operating Conditions- Forward Bias

- External voltage is applied across the *p*-*n* junction in the same polarity as the *p*- and *n*-type materials.
- The forward voltage causes the depletion region to narrow
- The electrons and holes are pushed toward the *p*-*n* junction
- The electrons and holes have sufficient energy to cross the *p*-



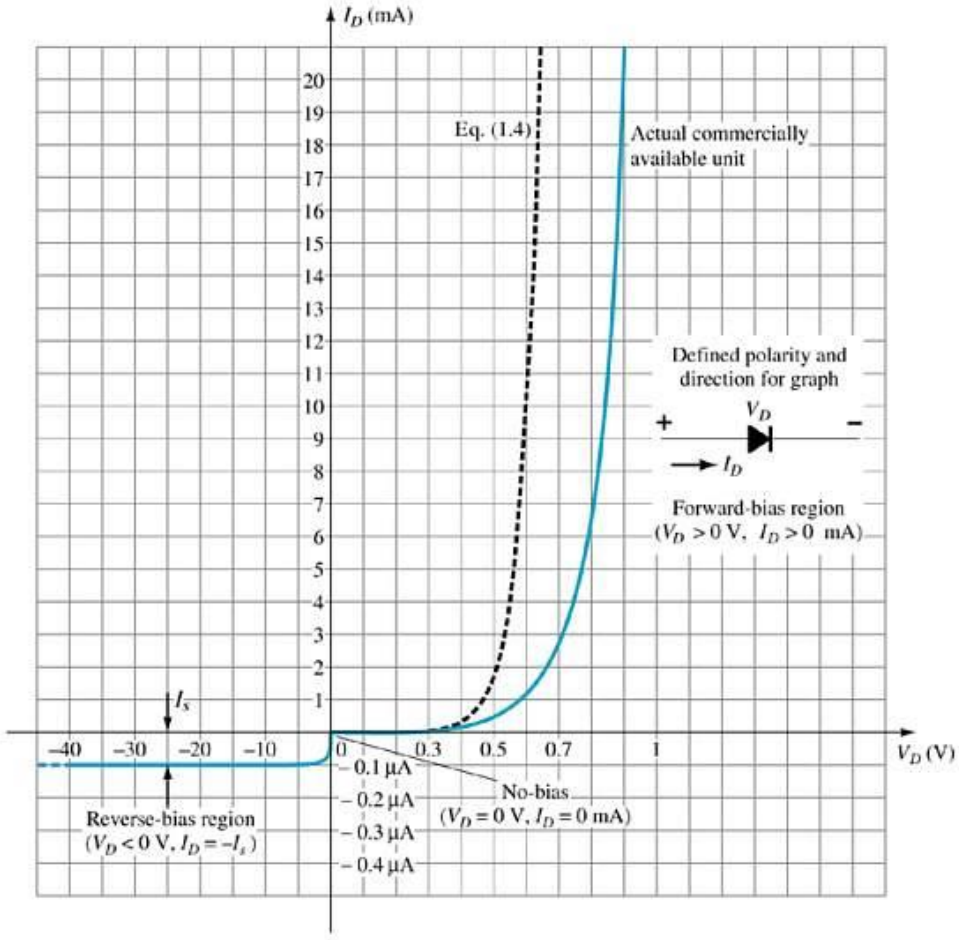


Week - 2

Actual Diode Characteristics

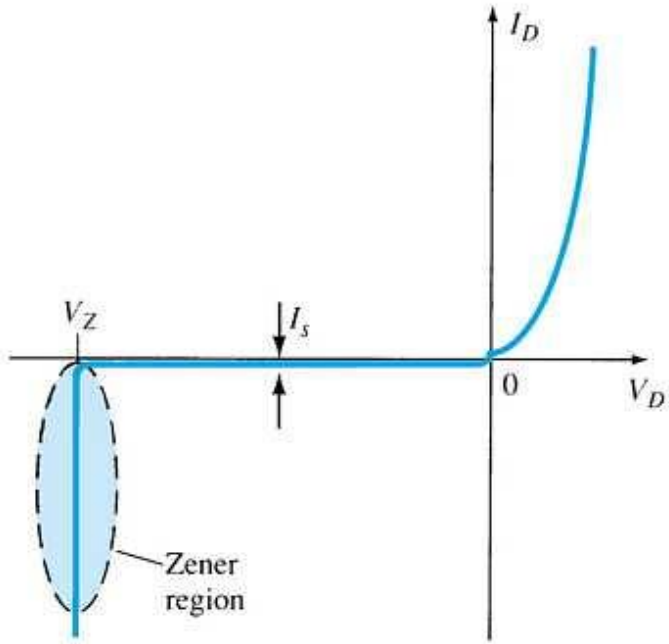
- **Note the regions for no bias, reverse bias, and forward bias conditions.**

- **Carefully note the scale for each of these conditions.**



Zener Region

- **The Zener region is in the diode's reverse-bias region.**
- **At some point the reverse bias voltage is so large the diode breaks down and the reverse current increases dramatically**
- **The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted by PRV rating).**
- **The voltage that causes a diode to enter the zener region of operation is called the zener voltage (V_Z).**



Forward Bias Voltage

- **The point at which the diode changes from no-bias condition to forward-bias condition occurs when the electrons and holes are given sufficient energy to cross the *p-n* junction. This energy comes from the external voltage applied across the diode.**
- **The forward bias voltage required for a**
  - **gallium arsenide diode ≅ 1.2 V**
  - **silicon diode ≅ 0.7 V**
  - **germanium diode ≅ 0.3 V**

Temperature Effects

- **As temperature increases it adds energy to the diode.**
  - **It reduces the required forward bias voltage for forward-bias conduction.**
  - **It increases the amount of reverse current in the reverse-bias condition.**
  - **It increases maximum reverse bias avalanche voltage.**
  - **Germanium diodes are more sensitive to temperature variations than silicon or gallium arsenide diodes.**

Resistance Levels

- **Semiconductors react differently to DC and AC currents.**
- **There are three types of resistance**
  - **DC (static) resistance**
  - **AC (dynamic) resistance**
  - **Average AC resistance**

AC (Dynamic) Resistance

In the forward bias region

$$r'_d = \frac{26\,\text{mV}}{I_D} + r_B$$

- The resistance depends on the amount of current (I_D) in the diode.
- The voltage across the diode is fairly constant (26 mV for 25°C).
- r_B ranges from a typical 0.1 Ω for high power devices to 2 Ω for low power, general purpose diodes. In some cases r_B can be ignored.

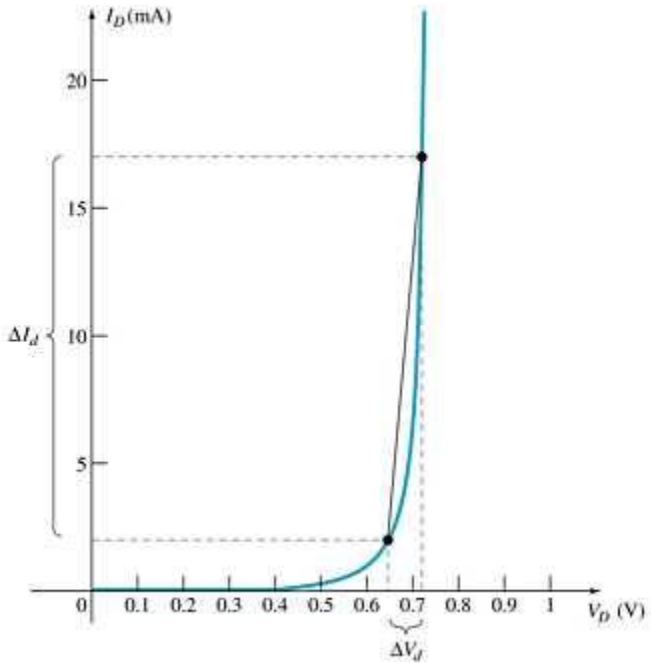
In the reverse bias region

$$r'_d = \infty$$

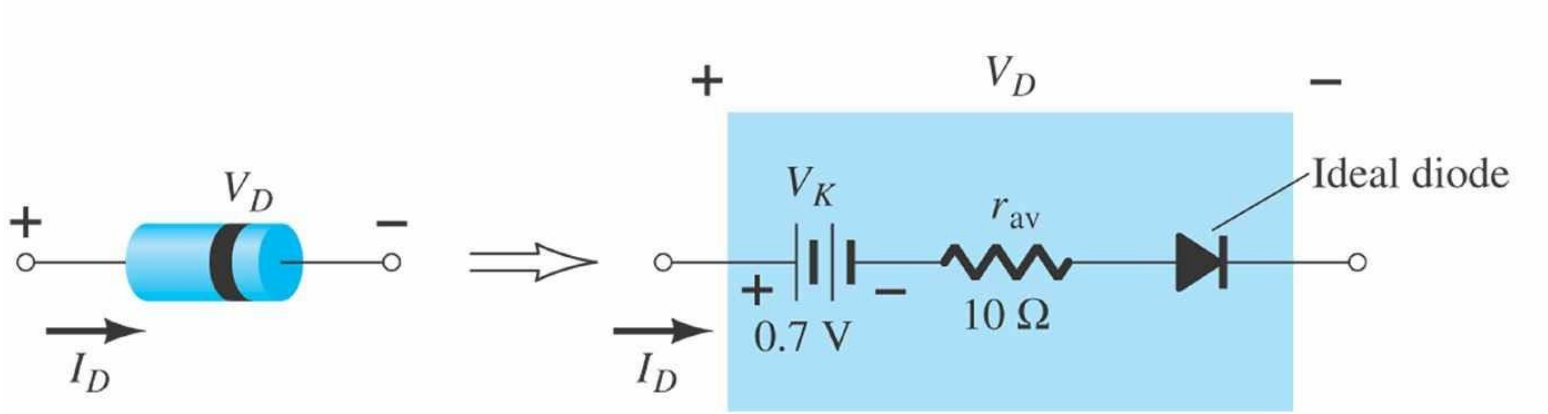
Average AC Resistance

- **AC resistance can be calculated using the current and voltage values for two points on the diode characteristic curve.**

$$r_{av} = \frac{\Delta V_d}{\Delta I_d} \Big| \text{ pt. to pt.}$$



Diode Equivalent Circuit

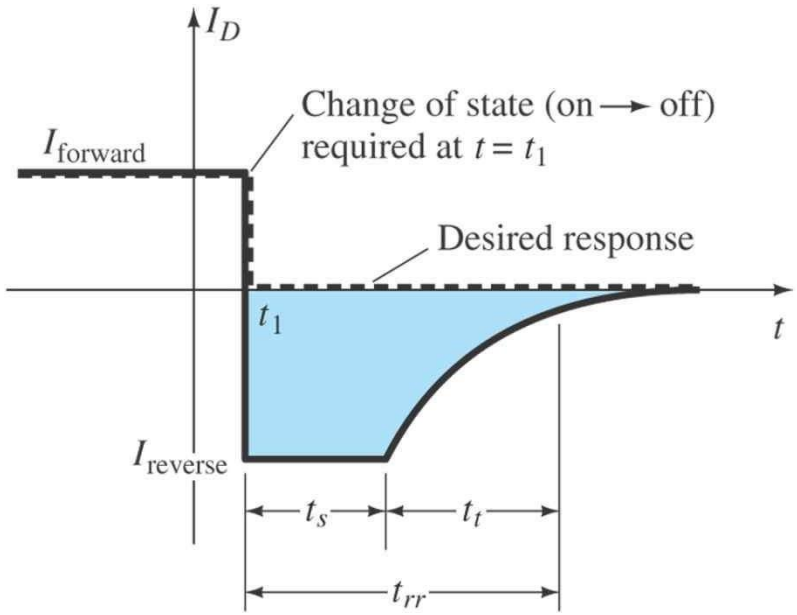


Diode Capacitance

- **In reverse bias, the depletion layer is very large. The diode's strong positive and negative polarities create capacitance, C_T. The amount of capacitance depends on the reverse voltage applied.**
  - **This is transition or depletion region capacitance**
- **In forward bias storage capacitance or diffusion capacitance (C_D) exists as the diode voltage increases.**

Reverse Recovery Time (t_{rr})

- **Reverse recovery time is the time required for a diode to stop conducting once it is switched from forward bias to reverse bias.**



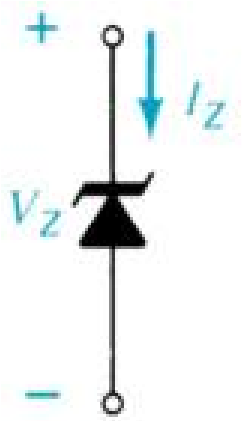
Diode Specification Sheets

1. **Forward Voltage (V_F) at a specified current and temperature**
2. **Maximum forward current (I_F) at a specified temperature**
3. **Reverse saturation current (I_R) at a specified voltage and temperature**
4. **Reverse voltage rating, PIV or PRV or V(BR), at a specified temperature**
5. **Maximum power dissipation at a specified temperature**
6. **Capacitance levels**
7. **Reverse recovery time, t_{rr}**
8. **Operating temperature range**

Week - 3

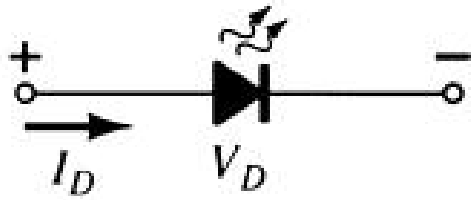
Zener Diode

- **A Zener is a diode operated in reverse bias at the Zener voltage (V_Z).**
- **Common Zener voltages are between 1.8 V and 200 V**



Light-Emitting Diode (LED)

- An LED emits photons when it is forward biased
- These can be in the infrared or visible spectrum
- The forward bias voltage is usually in the range of 2 V to 3 V.



Difference Between Zener Breakdown and Avalanche Breakdown

- The Zener effect is a type of electrical breakdown in a reverse biased p-n diode in which the electric field enables tunneling of electrons from the valence to the conduction band of a semiconductor, leading to a large number of free minority carriers, which suddenly increase the reverse current. Zener breakdown is employed in a Zener diode.
- Under a high reverse-bias voltage, the p-n junction's depletion region widens, leading to a high strength electric field across the junction.[2] A sufficiently strong electric field enables tunneling of electrons across the depletion region of a semiconductor leading to a large number of free charge carriers. This sudden generation of carriers rapidly increases the reverse current and gives rise to the high slope conductance of the Zener diode.

Difference Between Zener Breakdown and Avalanche Breakdown

- Zener breakdown:
  1)heavily doped therefore have narrow depletion layer
  2)strong electric field is developed across this narrow layer.
  3)covalent bonds break due to very strong electric field so even a small amount of reverse voltage is capable of producing large number of current carriers.

  zener breakdown voltage is less than avalanche breakdown.
- Avalanche Breakdown needs collision of minority carriers and covalent bonds to provide electrons and holes. This needs higher potential cos the minority carriers need to be developed in sufficient numbers to get sufficient current resulting in break down
- Avalanche breakdown is a phenomenon that can occur in both insulating and semiconducting materials
- The voltage at which the breakdown occurs is called the breakdown voltage.

Difference Between Zener Breakdown and Avalanche Breakdown

- **Zener Breakdown**
- **This occurs at junctions which being heavily doped have narrow depletion layers**
- **This breakdown voltage sets a very strong electric field across this narrow layer.**

E=V/d

* Do not confused that diode is damaged with any of the breakdowns. Damaged depends on the current rating

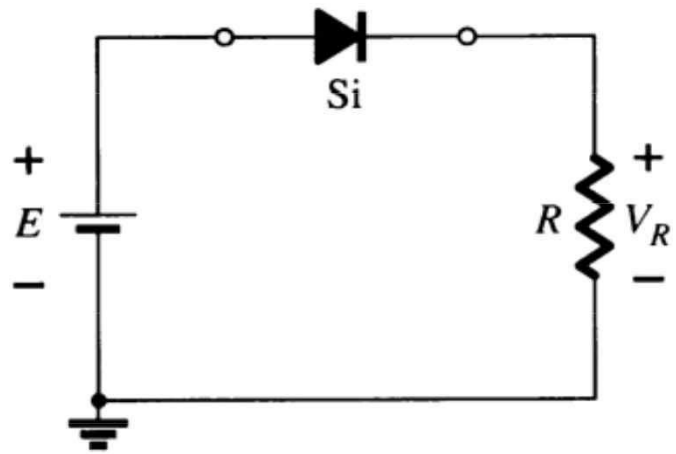
- **Avalanche breakdown**
- **This occurs at junctions which being lightly doped have wide depletion layers.**
- **Here electric field is not strong enough to produce Zener breakdown.**
- **Here minority carriers collide with semi conductor atoms in the depletion region, which breaks the covalent bonds and electron-hole pairs are generated. Newly generated charge carriers are accelerated by the electric field which results in more collision and generates avalanche of charge carriers. This results in avalanche breakdown.**

Series Diode Configurations

Forward Bias

Constants

- **Silicon Diode: $V_D = 0.7$ V**
- **Germanium Diode: $V_D = 0.3$ V**

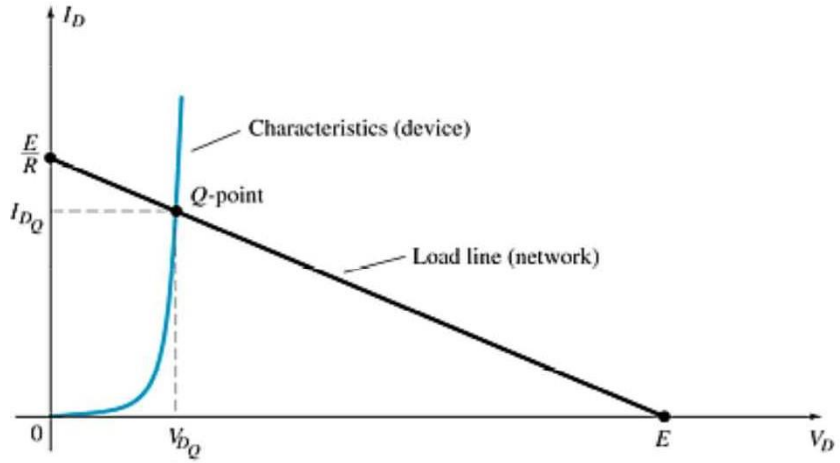


Analysis (for silicon)

- $V_D = 0.7$ V (or $V_D = E$ if $E < 0.7$ V)
- $V_R = E - V_D$, $V_D = E - I_D R$
- $I_D = I_R = I_T = V_R / R$

Load-Line Analysis

The load line plots all possible combinations of diode current (I_D) and voltage (V_D) for a given circuit. The maximum I_D equals E/R, and the maximum V_D equals E.

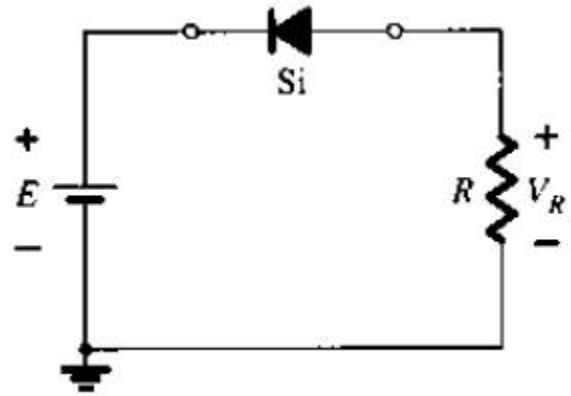


The point where the load line and the characteristic curve intersect is the Q-point, which identifies I_D and V_D for a particular diode in a given circuit.

Series Diode Configurations

Reverse Bias

Diodes ideally behave as open circuits



Analysis

- $V_D = E$
- $V_R = 0$ V
- $I_D = 0$ A

Parallel Configurations

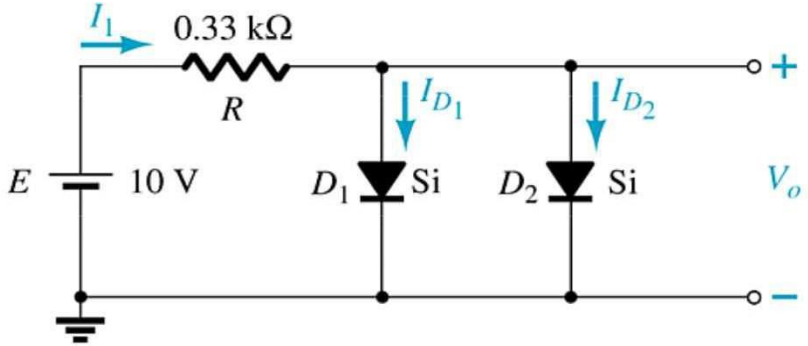
$$V_D = 0.7\,V$$

$$V_{D1} = V_{D2} = V_O = 0.7\,V$$

$$V_R = 9.3\,V$$

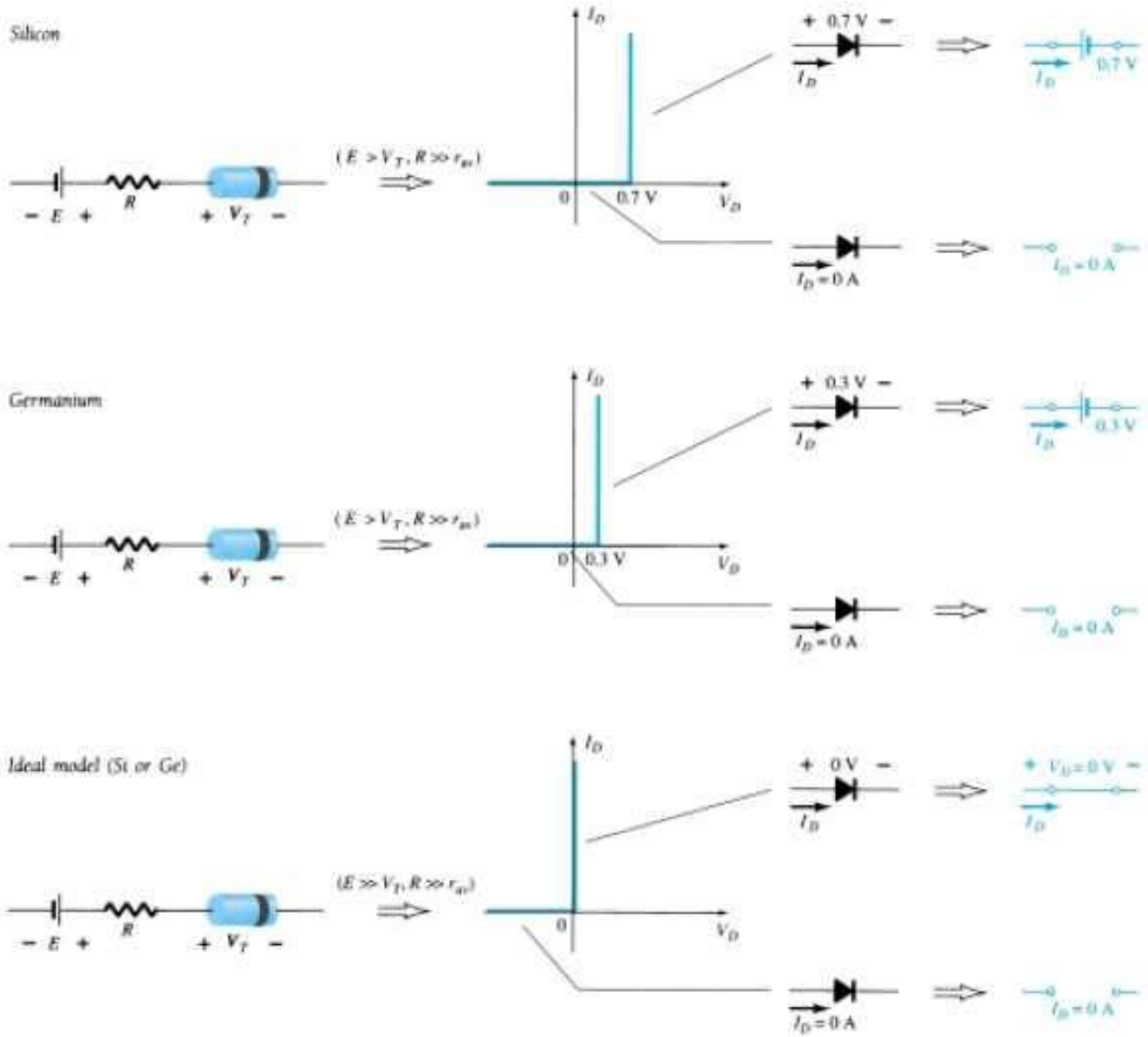
$$I_R = \frac{E - V_D}{R} = \frac{10\,V - .7\,V}{.33k\Omega} = 28\,mA$$

$$I_{D1} = I_{D2} = \frac{28\,mA}{2} = 14\,mA$$



Week - 4

Diode Approximation



Problem

- For the series diode configuration of Fig. 2.3a employing the diode characteristics of Fig. 2.3b determine:
- (a) V_{DQ} and I_{DQ}. (b) V_R.

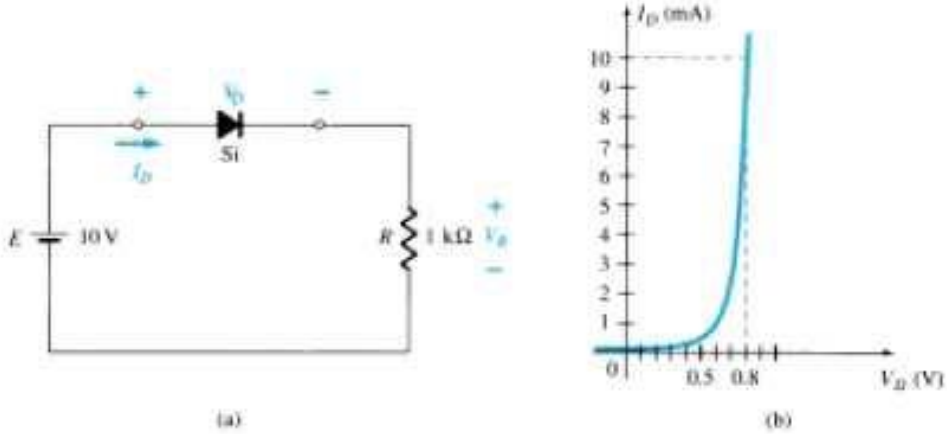
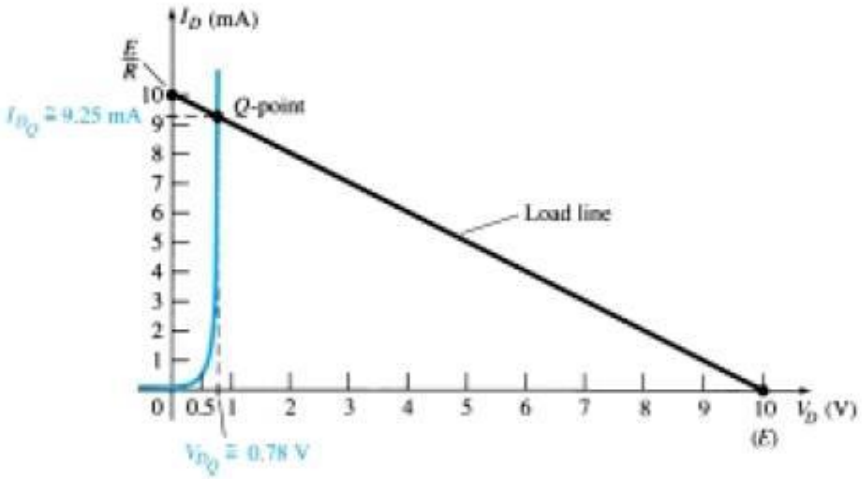


Figure 2.3 (a) Circuit; (b) characteristics.



$V_{D_Q} \cong 0.78$ V

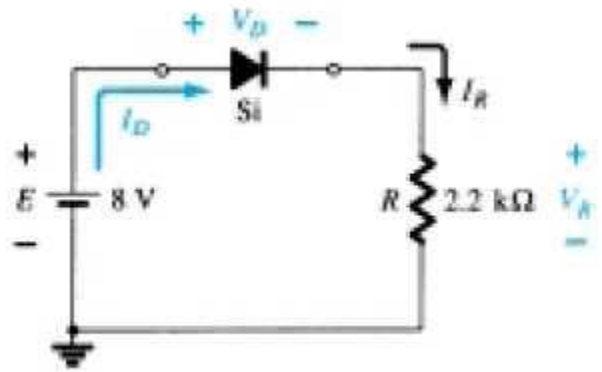
$I_{D_Q} \cong 9.25$ mA

$V_R = I_R R = I_{D_Q} R = (9.25 \text{ mA})(1 \text{ k}\Omega) = 9.25 \text{ V}$

$V_R = E - V_D = 10 \text{ V} - 0.78 \text{ V} = 9.22 \text{ V}$

Problem

- For the series diode configuration, determine V_D, V_R, and I_D.

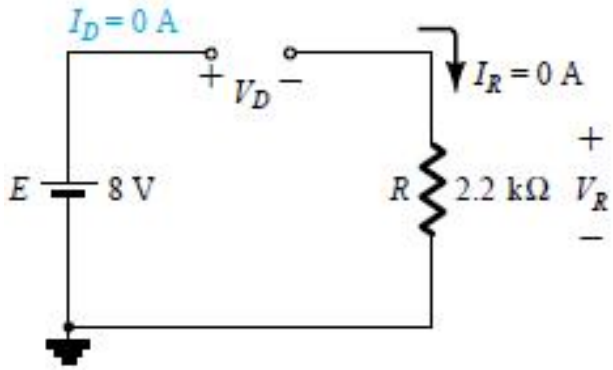


$$V_D = 0.7 \text{ V}$$

$$V_R = E - V_D = 8 \text{ V} - 0.7 \text{ V} = 7.3 \text{ V}$$

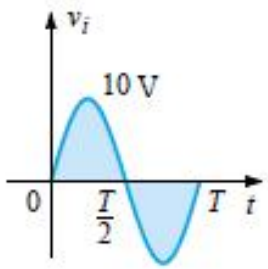
$$I_D = I_R = \frac{V_R}{R} = \frac{7.3 \text{ V}}{2.2 \text{ k}\Omega} \cong 3.32 \text{ mA}$$

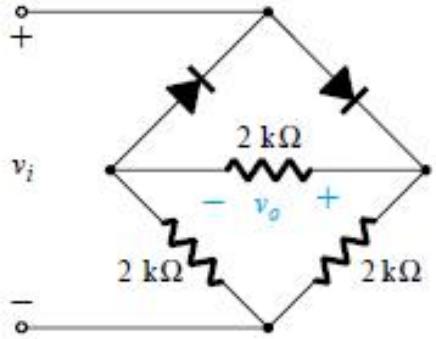
- Repeat the problem with the diode reversed.

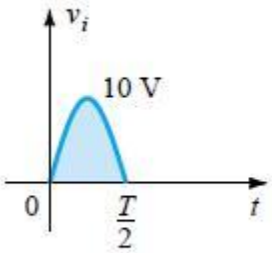


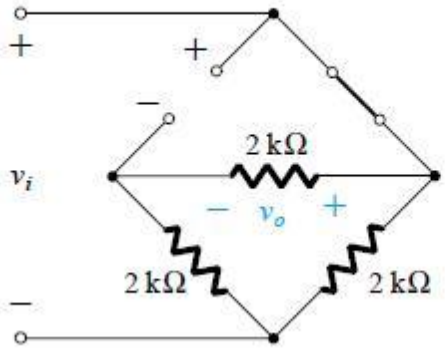
Problem

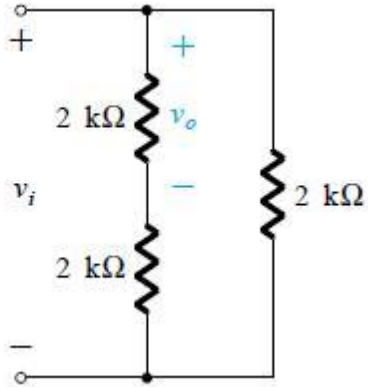
- Determine the output waveform for the network an calculate the output dc level and the required PIV of each diode.

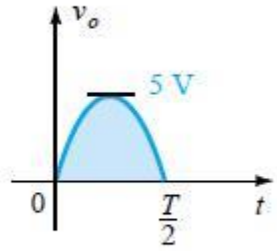


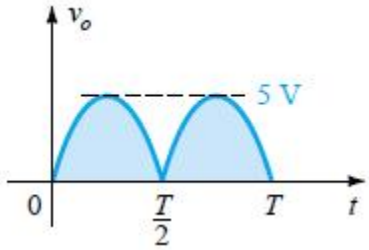








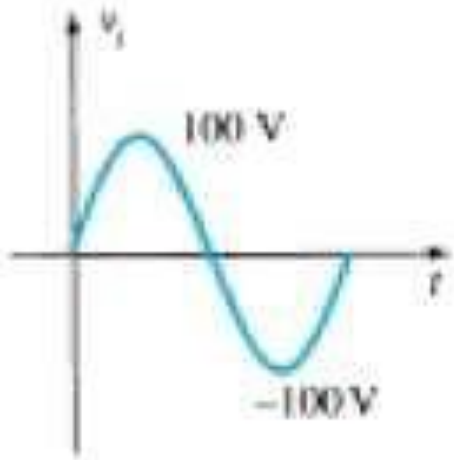


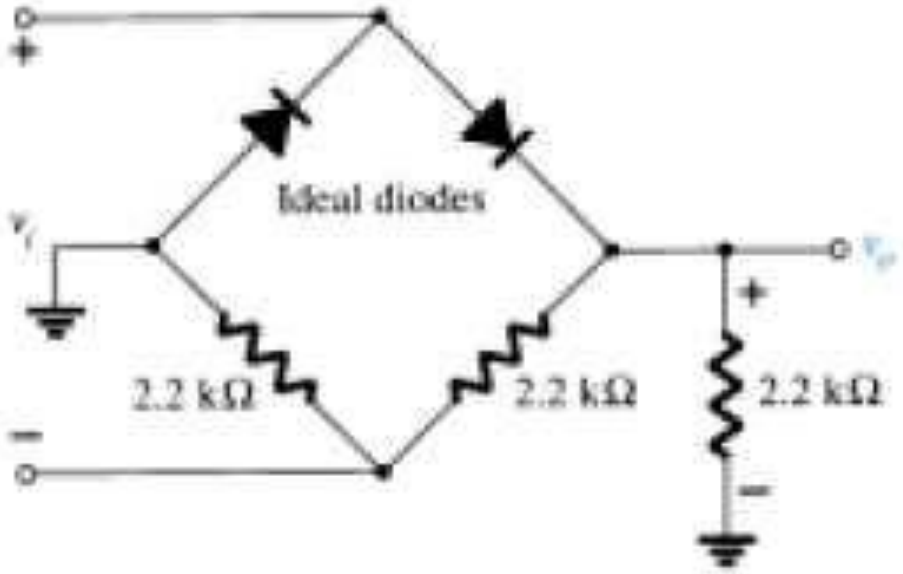


Resulting output

Assignment

- Sketch v_o for the network and determine the dc voltage available

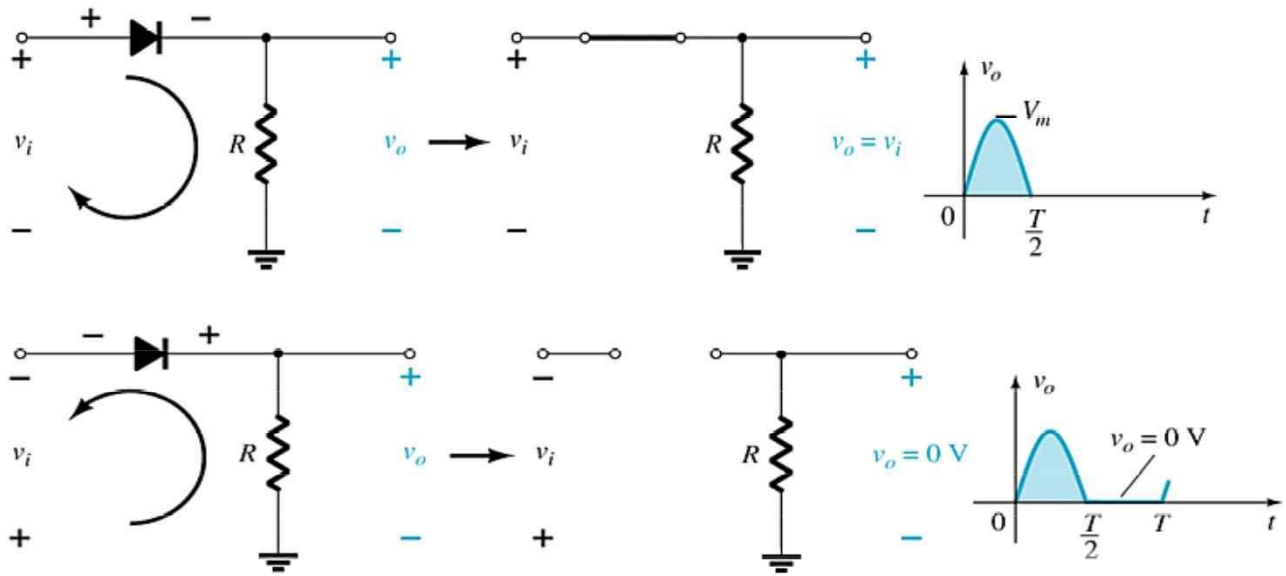




Week - 5

Half-Wave Rectification

The diode only conducts when it is forward biased, therefore only half of the AC cycle passes through the diode to the output.



The DC output voltage is $0.318V_m$, where V_m = the peak AC voltage.

PIV (PRV)

Because the diode is only forward biased for one-half of the AC cycle, it is also reverse biased for one-half cycle.

It is important that the reverse breakdown voltage rating of the diode be high enough to withstand the peak, reverse-biasing AC voltage.

$$\text{PIV (or PRV)} > V_m$$

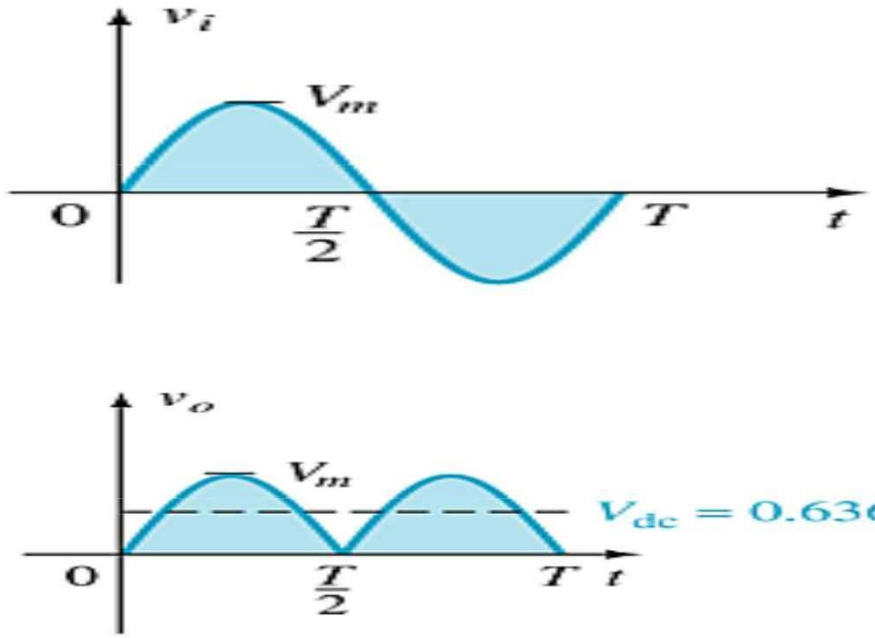
- **PIV = Peak inverse voltage**
- **PRV = Peak reverse voltage**
- V_m **= Peak AC voltage**

Full-Wave Rectification

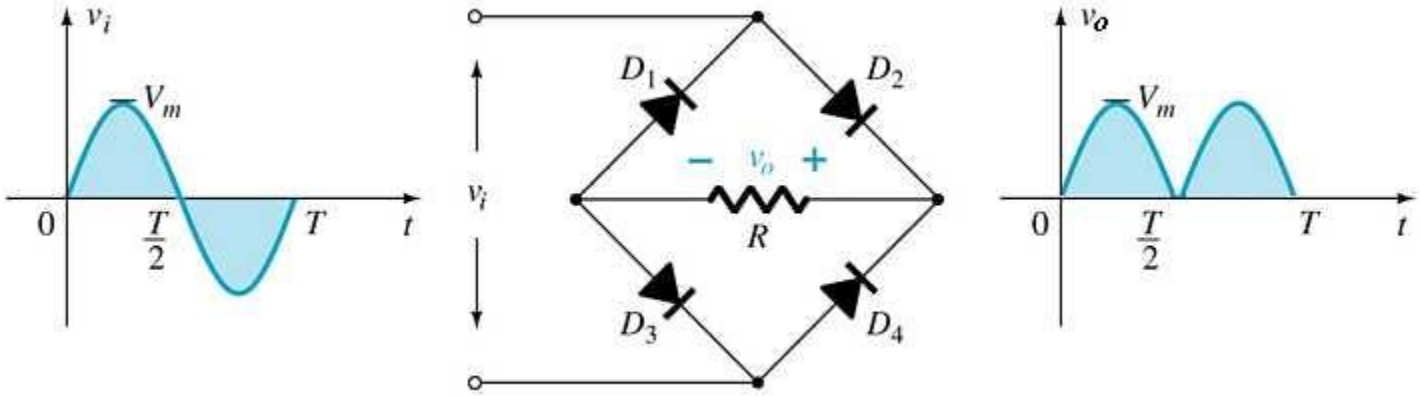
The rectification process can be improved by using a full-wave rectifier circuit.

Full-wave rectification produces a greater DC output:

- **Half-wave:** $V_{dc} = 0.318V_m$
- **Full-wave:** $V_{dc} = 0.636V_m$

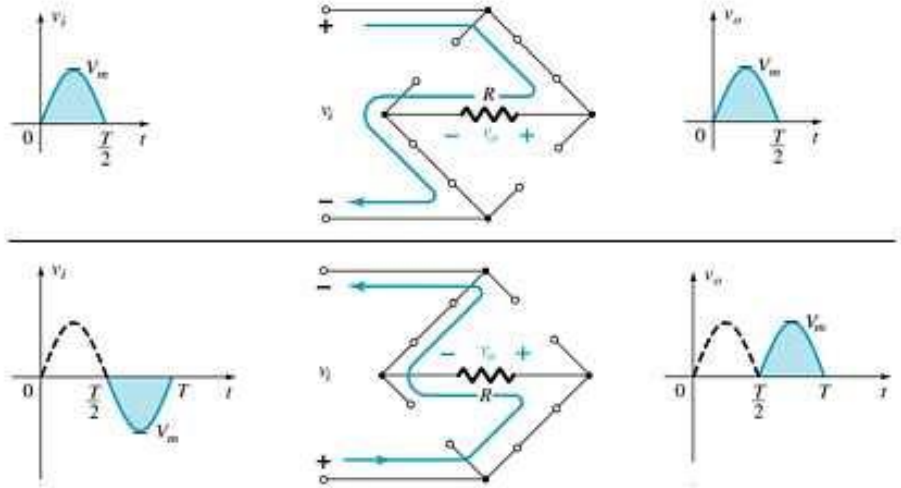


Full-Wave Rectification

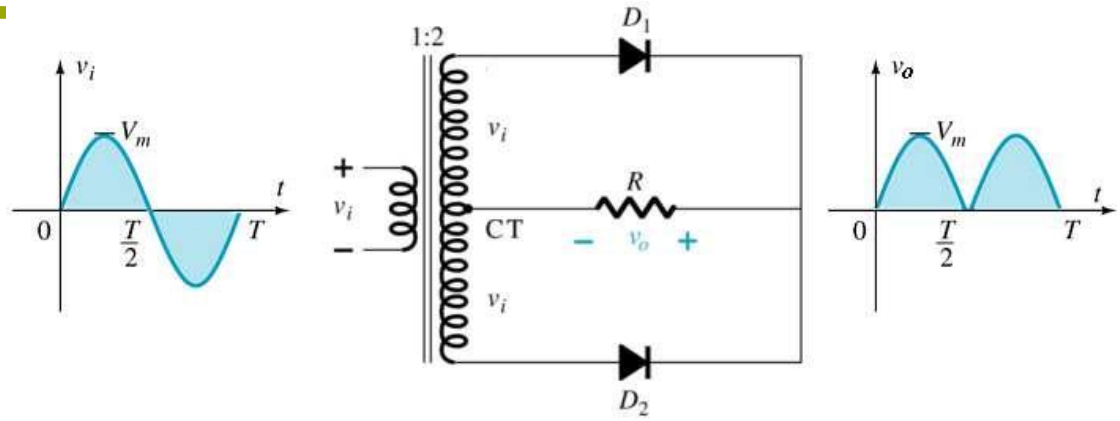


Bridge Rectifier

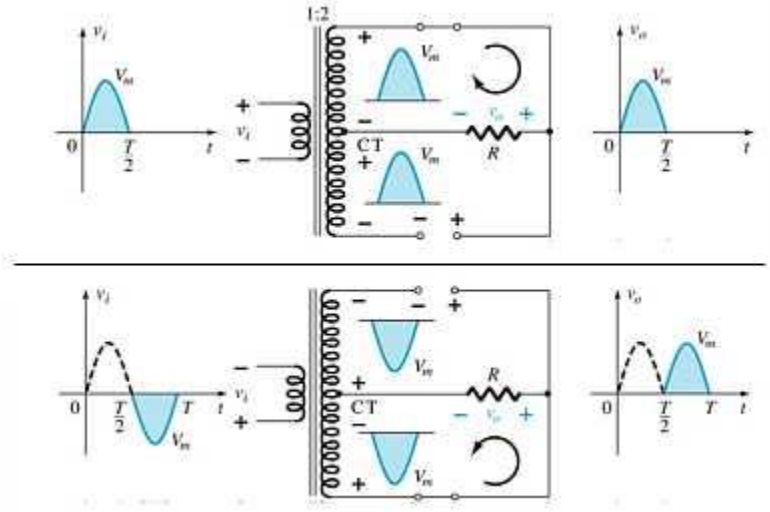
- **Four diodes are connected in a bridge configuration**
- **$V_{DC} = 0.636V_m$**
- **PIV> V_m**



Full-Wave Rectification



Center-Tapped Transformer Rectifier



Requires

- **Two diodes**
- **Center-tapped transformer**
- **PIV>2V_m**
- **V_{DC} = 0.636V_m**

Summary of Rectifier Circuits

Rectifier	Ideal V_{DC}	Realistic V_{DC}
Half Wave Rectifier	$V_{DC} = 0.318V_m$	$V_{DC} = 0.318V_m - 0.7$
Bridge Rectifier	$V_{DC} = 0.636V_m$	$V_{DC} = 0.636V_m - 2(0.7\ V)$
Center-Tapped Transformer Rectifier	$V_{DC} = 0.636V_m$	$V_{DC} = 0.636V_m - 0.7\ V$

V_m = peak of the AC voltage.

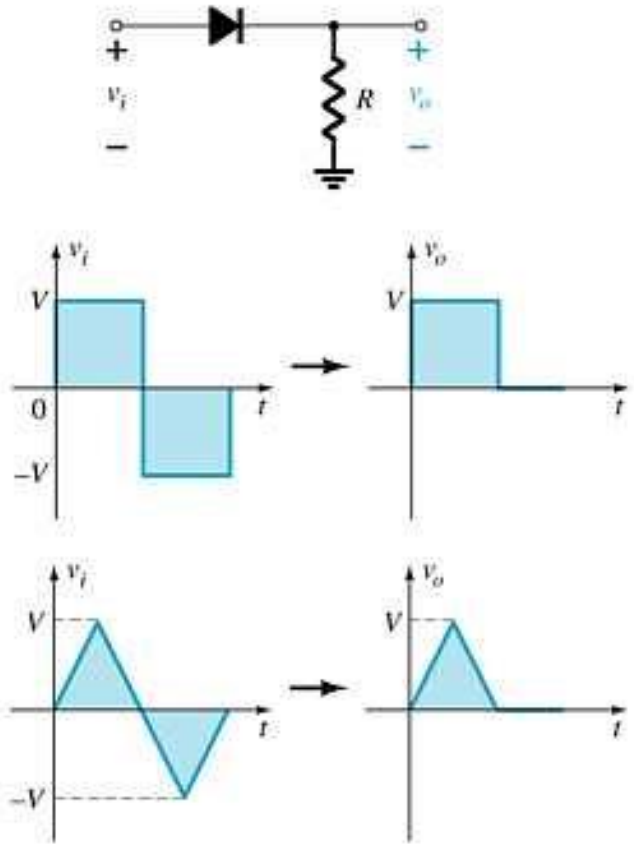
In the center tapped transformer rectifier circuit, the peak AC voltage is the transformer secondary voltage to the tap.

Week - 6

Diode Clippers

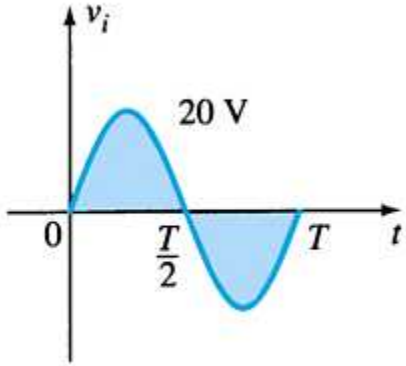
The diode in a series clipper "clips" any voltage that does not forward bias it:

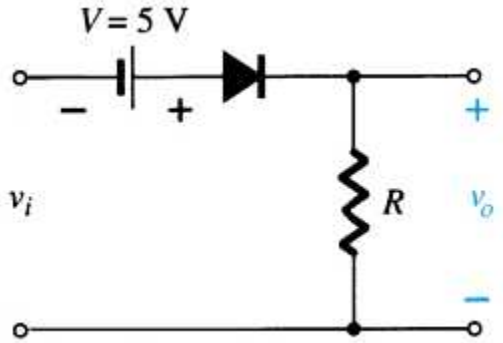
- **A reverse-biasing polarity**
- **A forward-biasing polarity less than 0.7 V (for a silicon diode)**

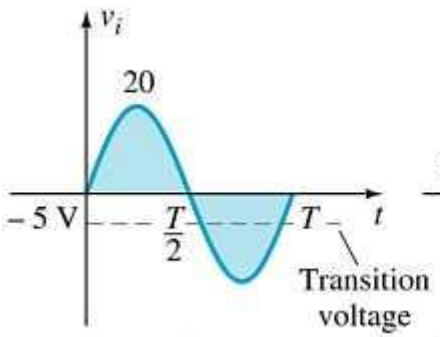


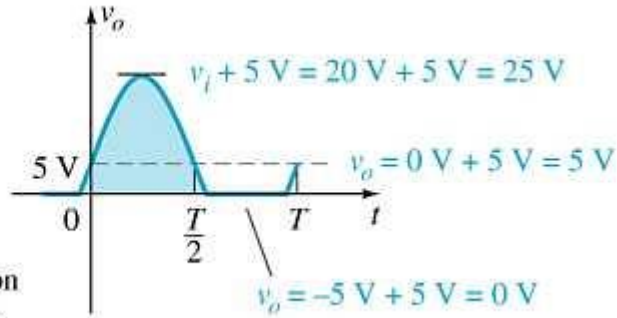
Biased Clippers

Adding a DC source in series with the clipping diode changes the effective forward bias of the diode.









Clampers

A diode and capacitor can be combined to "clamp" an AC signal to a specific DC level.

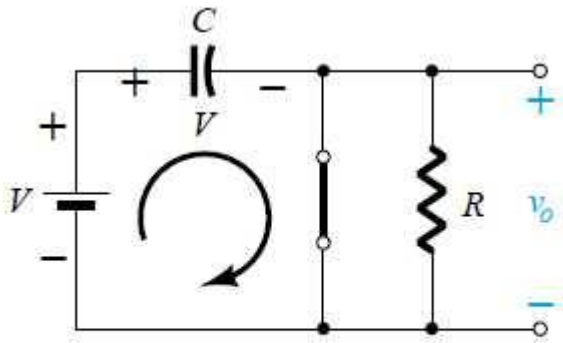
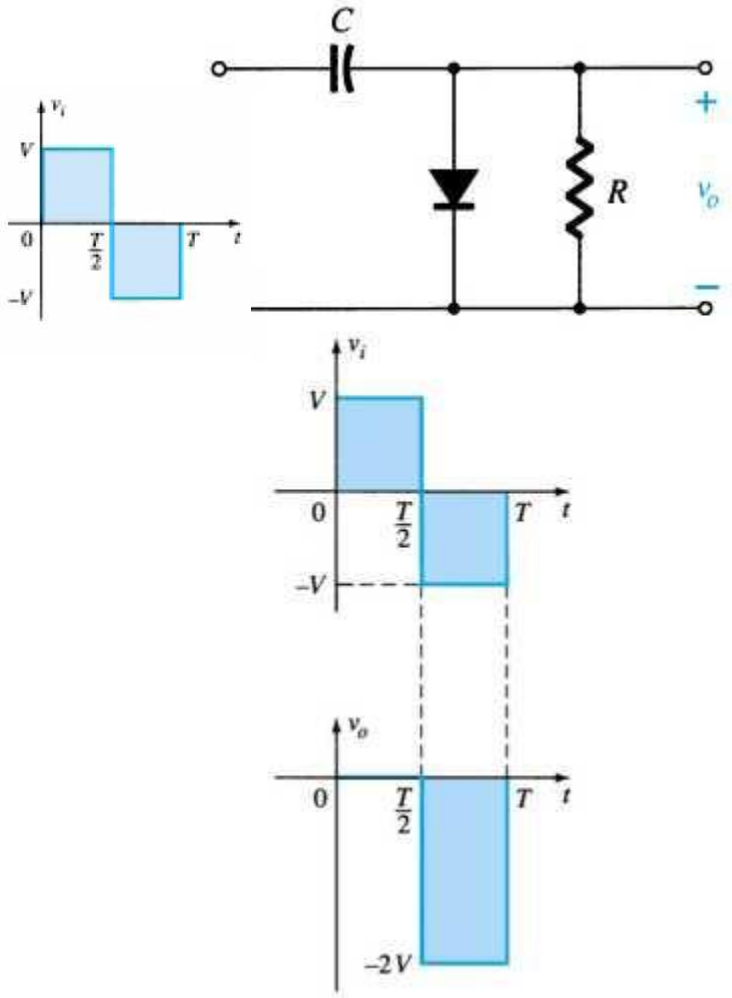
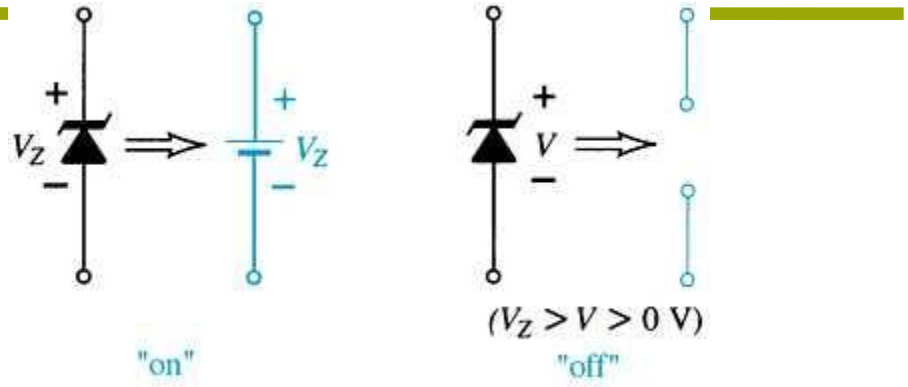


Figure 2.93 Diode "on" and the capacitor charging to V volts.

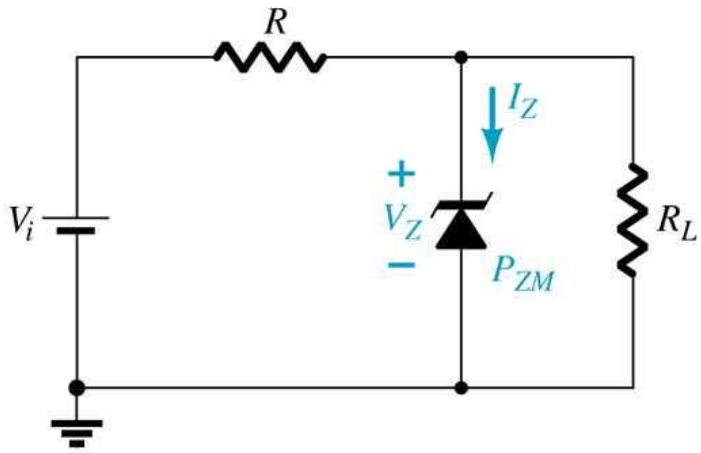


Zener Diodes

The Zener is a diode operated in reverse bias at the Zener Voltage (V_z).



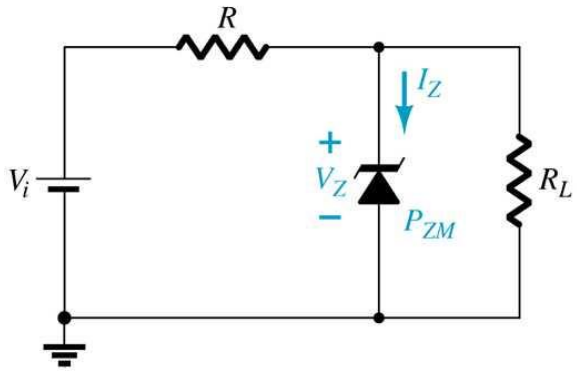
- When $V_i \geq V_Z$
  - The Zener is on
  - Voltage across the Zener is V_Z
  - Zener current: $I_Z = I_R - I_{RL}$
  - The Zener Power: $P_Z = V_Z I_Z$



- When $V_i < V_Z$
  - The Zener is off
  - The Zener acts as an open circuit

Zener Resistor Values

$$V = V_L = \frac{R_L V_i}{R + R_L}$$



$$I_Z = I_R - I_L$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z$$

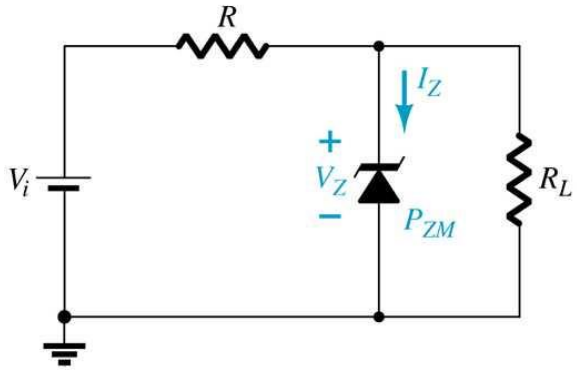
$$I_{L_{max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{min}}}$$

$$R_{L_{min}} = \frac{RV_Z}{V_i - V_Z}$$

Zener Resistor Values

If *R* is too large, the Zener diode cannot conduct because the available amount of current is less than the minimum current rating, I_{ZK}. The minimum current is given by:

$$I_{L\min} = I_R - I_{ZK}$$



The *maximum* value of resistance is:

$$R_{L\max} = \frac{V_Z}{I_{L\min}}$$

If *R* is too small, the Zener current exceeds the maximum current rating, I_{ZM}. The maximum current for the circuit is given by:

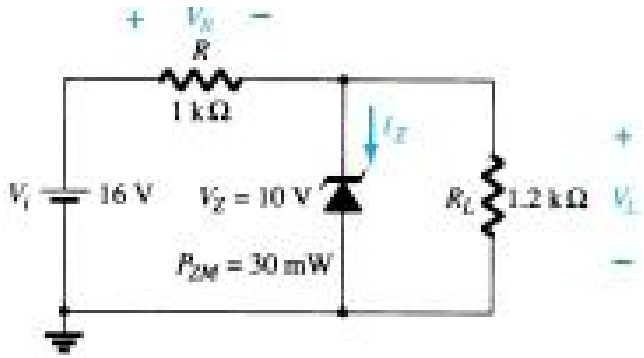
$$I_{L\max} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L\min}}$$

The *minimum* value of resistance is:

$$R_{L\min} = \frac{RV_Z}{V_i - V_Z}$$

EXAMPLE 2.26

- (a) For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
- (b) Repeat part (a) with R_L = 3 k.



$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

Since V 8.73 V is less than V_Z 10 V, the diode is in the "off" state

$$V_L = V = \mathbf{8.73\ V}$$

$$V_R = V_i - V_L = 16\ V - 8.73\ \text{V} = \mathbf{7.27\ V}$$

$$I_Z = \mathbf{0\ A}$$

$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

EXAMPLE 2.26 (cont.)

- **(b)**

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since V 12 V is greater than V_Z 10 V, the diode is in the "on" state

$$V_L = V_Z = 10\ \text{V}$$

$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

$$\text{I}_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

$$I_Z = I_R - I_L\ \text{[Eq. (2.18)]}$$

$$= 6\ \text{mA} - 3.33\ \text{mA}$$

$$= \mathbf{2.67\ mA}$$

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

Practical Applications

- **Rectifier Circuits**
  - **Conversions of AC to DC for DC operated circuits**
  - **Battery Charging Circuits**
- **Simple Diode Circuits**
  - **Protective Circuits against**
  - **Overcurrent**
  - **Polarity Reversal**
  - **Currents caused by an inductive kick in a relay circuit**
- **Zener Circuits**
  - **Overvoltage Protection**
  - **Setting Reference Voltages**

Week - 7

Transistor Construction

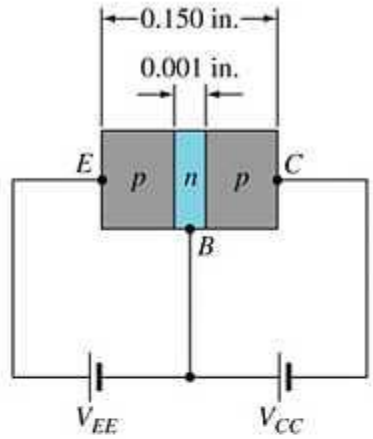
There are two types of transistors:

- *pnp*
- *npn*

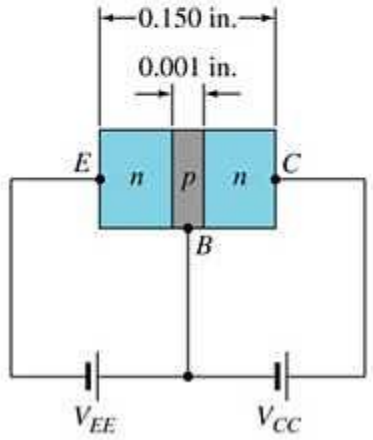
The terminals are labeled:

- **E - Emitter**
- **B - Base**
- **C – Collector**

pnp



npn



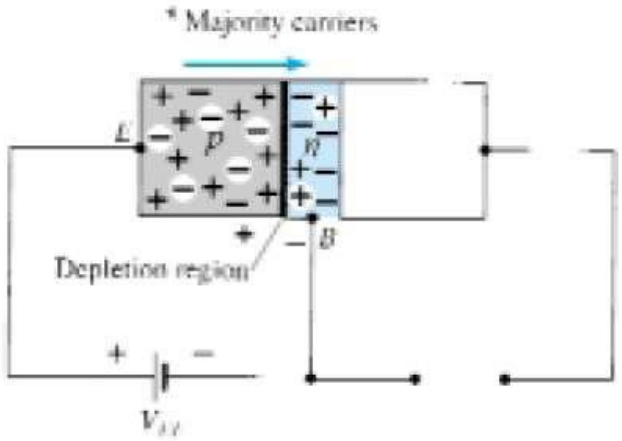
Transistor Construction

- dc biasing is necessary to establish the proper region of operation for ac amplification.
- The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped.
- The outer layers have widths much greater than the sandwiched *p*- or *n*-type material.
- For the transistors shown in Fig. the ratio of the total width to that of the center layer is 0.150/0.001

  15

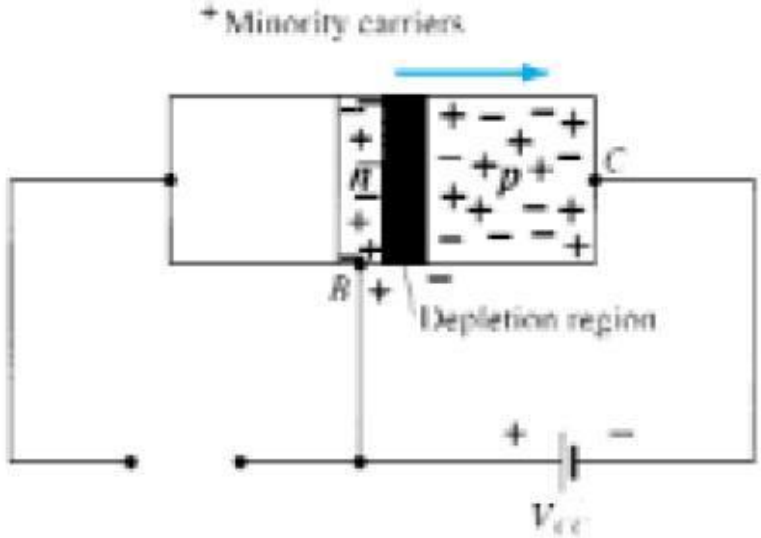
  01.
- The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 101 or less).
- This lower doping level decreases the conductivity of this material by limiting the number of “free” carriers.

Transistor Operation



Forward-biased junction of a *pnp* transistor.

- *forward-biased* diode
- ***heavy flow of majority carriers from the p- to the n-type material***



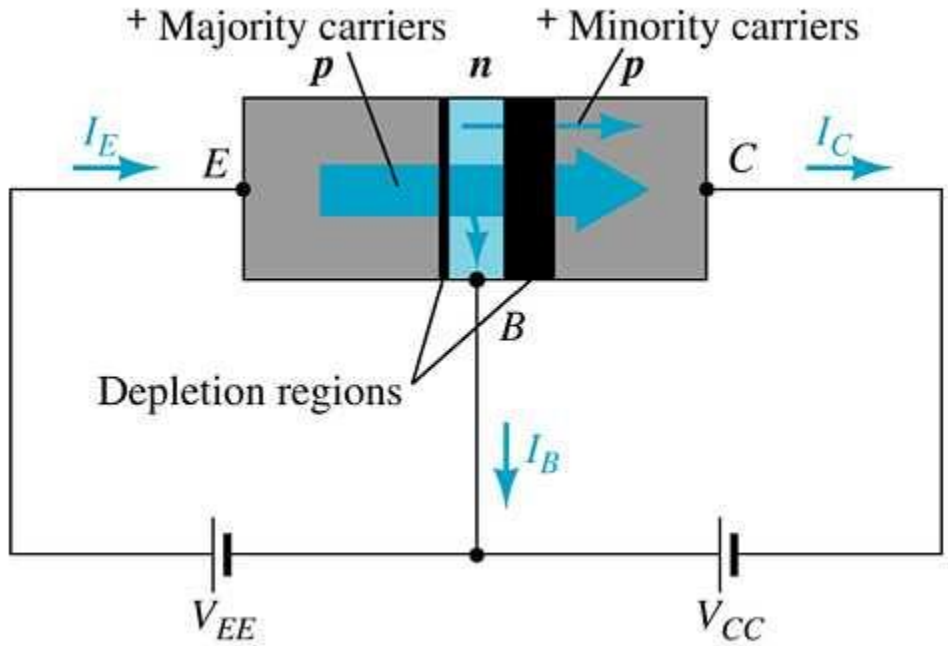
Reverse-biased junction of a *pnp* transistor.

- *forward-biased* diode
- ***flow of minority carriers from the n- to the p-type material***

Transistor Operation

With the external sources, V_{EE} and V_{CC}, connected as shown:

- **The emitter-base junction is forward biased**
- **The base-collector junction is reverse biased**



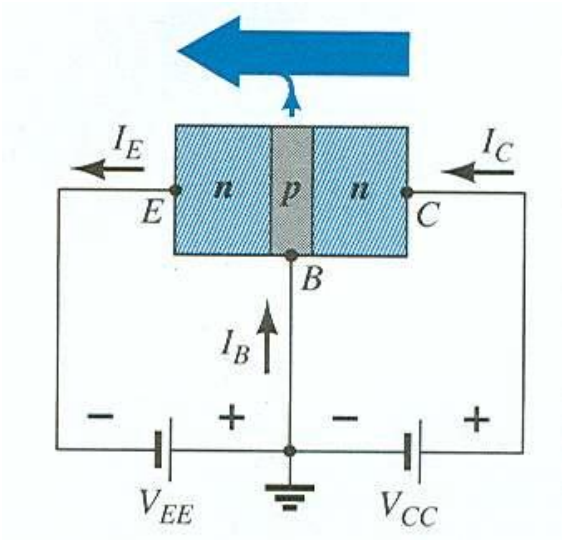
Currents in a Transistor

Emitter current is the sum of the collector and base currents:

$$I_E = I_C + I_B$$

The collector current is comprised of two currents:

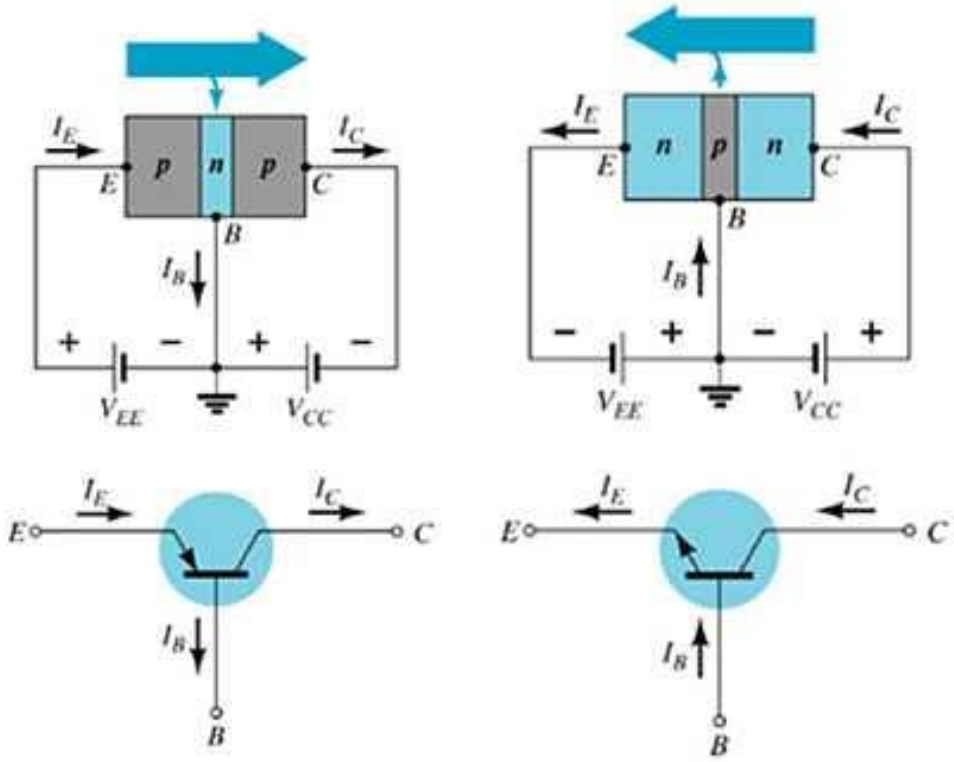
$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$



Transistor Operation

- **Active region**
  - ✓ **In the active region the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased**
- **Cutoff region**
  - ✓ **In the cutoff region the collector-base and base-emitter junctions of a transistor are both reverse-biased.**
- **Saturation region**
  - ✓ **In the saturation region the collector-base and base-emitter junctions are forward-biased**

Common-Base Configuration



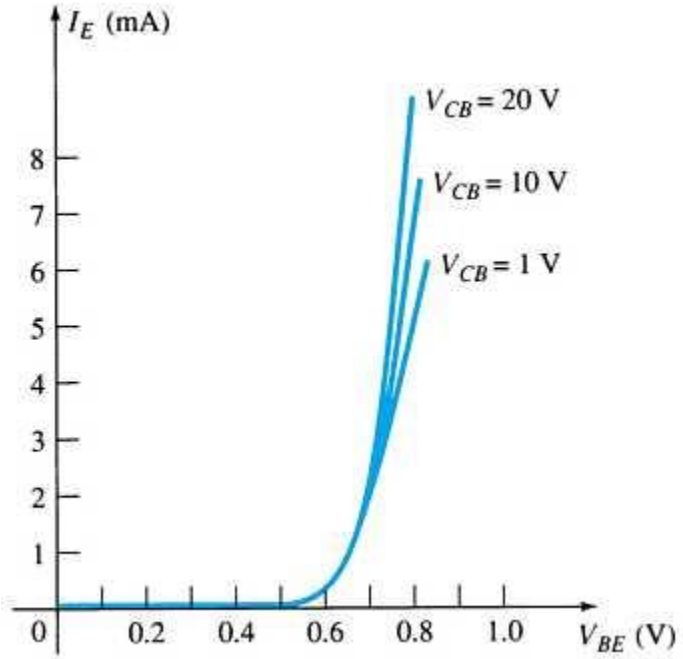
The base is common to both input (emitter–base) and output (collector–base) of the transistor.

Week - 8

Common-Base Amplifier

Input Characteristics

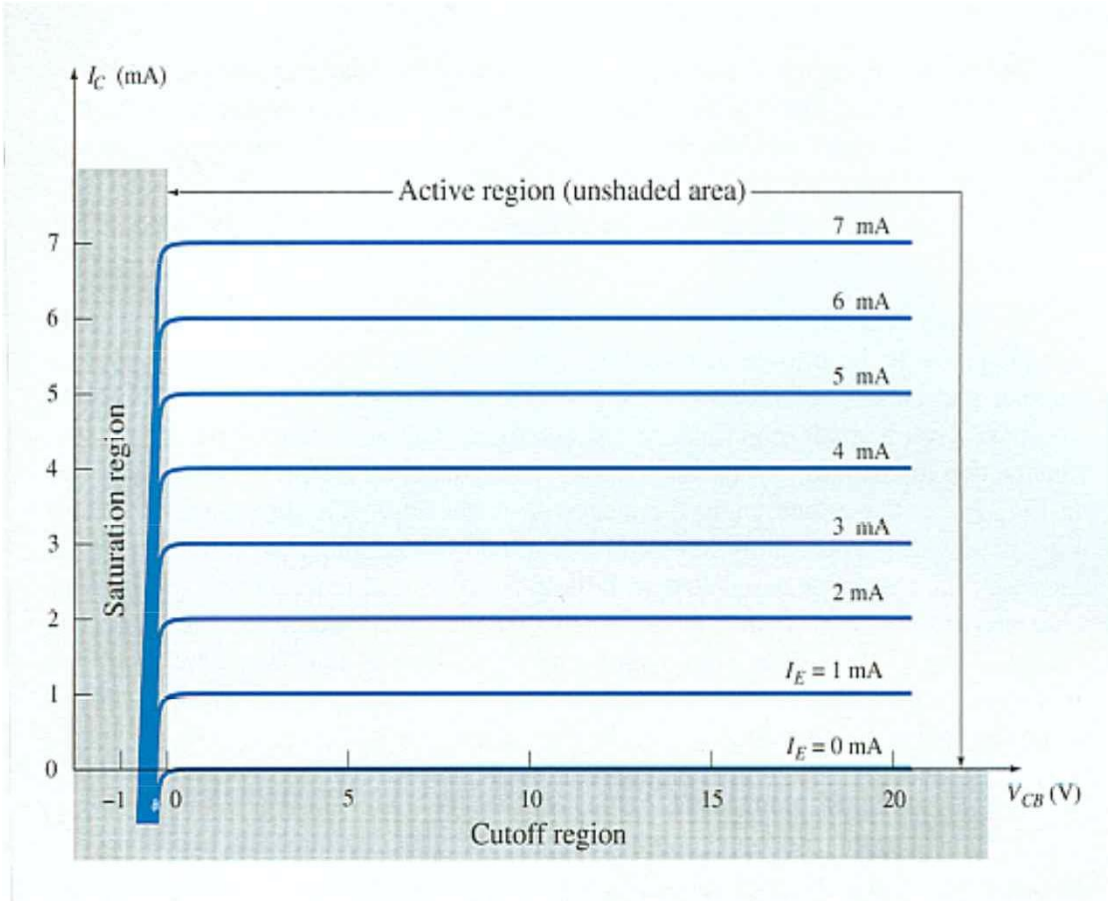
This curve shows the relationship between of input current (I_E) to input voltage (V_{BE}) for three output voltage (V_{CB}) levels.



Common-Base Amplifier

Output Characteristics

This graph demonstrates the output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).



Operating Regions

- **Active – Operating range of the amplifier.**
- **Cutoff – The amplifier is basically off. There is voltage, but little current.**
- **Saturation – The amplifier is full on. There is current, but little voltage.**

Approximations

Emitter and collector currents:

$$I_C \cong I_E$$

Base-emitter voltage:

$$V_{BE} = 0.7\ V \quad \text{(for Silicon)}$$

Alpha (α)

Alpha (α) is the ratio of I_C to I_E :

$$\alpha_{dc} = \frac{I_C}{I_E}$$

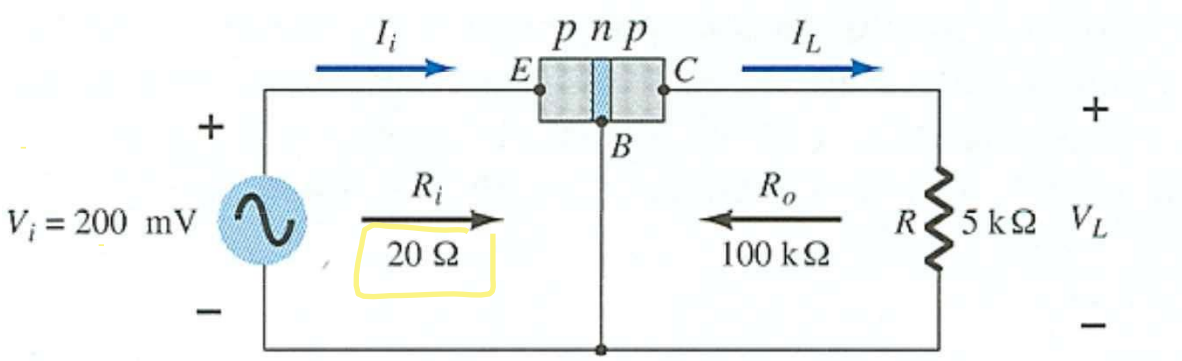
Ideally: α = 1

In reality: α is between 0.9 and 0.998

Alpha (α) in the AC mode:

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$$

Transistor Amplification



Currents and Voltages:

$$I_E = I_i = \frac{V_i}{R_i} = \frac{200\text{mV}}{20\Omega} = 10\text{mA}$$

$$I_C \cong I_E$$

$$I_L \cong I_i = 10\,\text{mA}$$

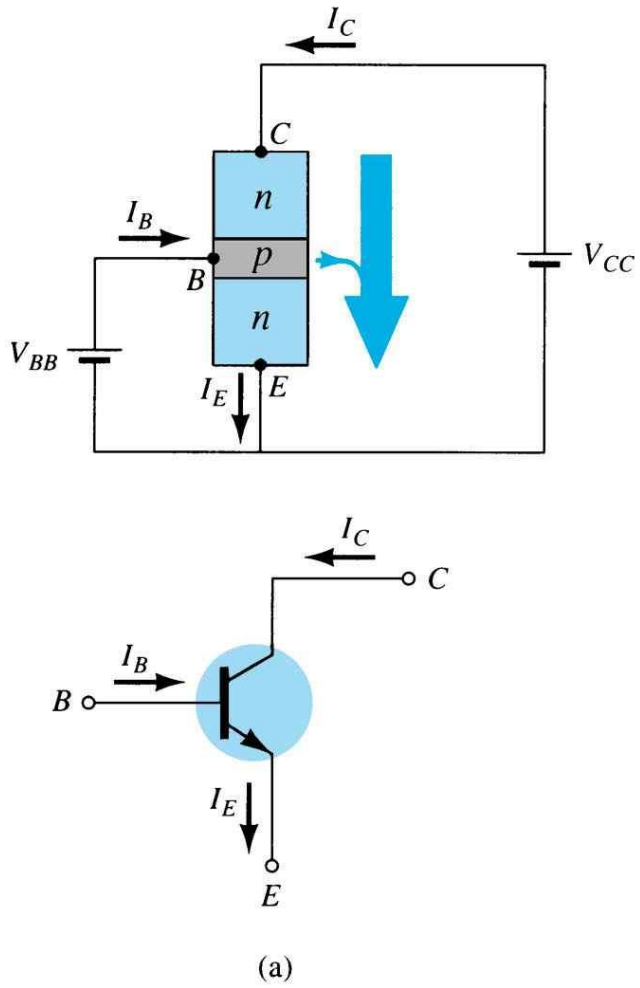
$$V_L = I_L R = (10\,\text{ma})(5\,\text{k}\Omega) = 50\text{ V}$$

Voltage Gain:

$$A_v = \frac{V_L}{V_i} = \frac{50\text{V}}{200\text{mV}} = 250$$

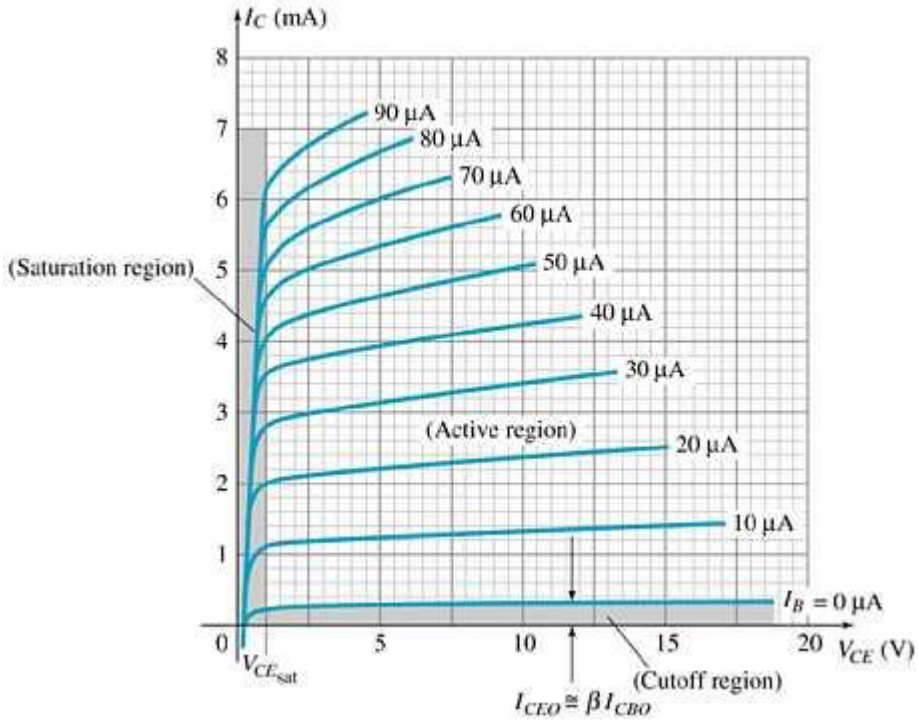
Common–Emitter Configuration

- **The emitter is common to both input (base-emitter) and output (collector-emitter).**
- **The input is on the base and the output is on the collector.**

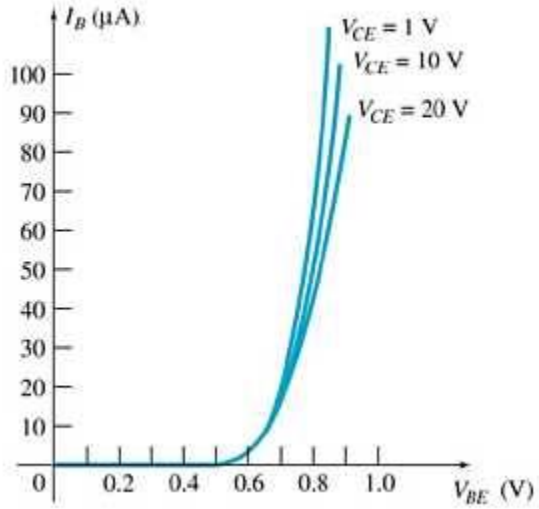


(a)

Common-Emitter Characteristics



Collector Characteristics



Base Characteristics

Common-Emitter Amplifier Currents

Ideal Currents

$$I_E = I_C + I_B \qquad I_C = \alpha I_E$$

Actual Currents

$$I_C = \alpha I_E + I_{CBO}$$

where I_{CBO} = minority collector current

I_{CBO} is usually so small that it can be ignored, except in high power transistors and in high temperature environments.

When I_B = 0 μA the transistor is in cutoff, but there is some minority current flowing called I_{CEO}.

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha}\bigg|_{I_B = 0\,\mu A}$$

Week - 9

Beta (β)

β represents the amplification factor of a transistor. (β is sometimes referred to as h_{fe}, a term used in transistor modeling calculations)

In DC mode:

$$\beta_{dc} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=\text{constant}}$$

Beta (β)

Determining β from a Graph

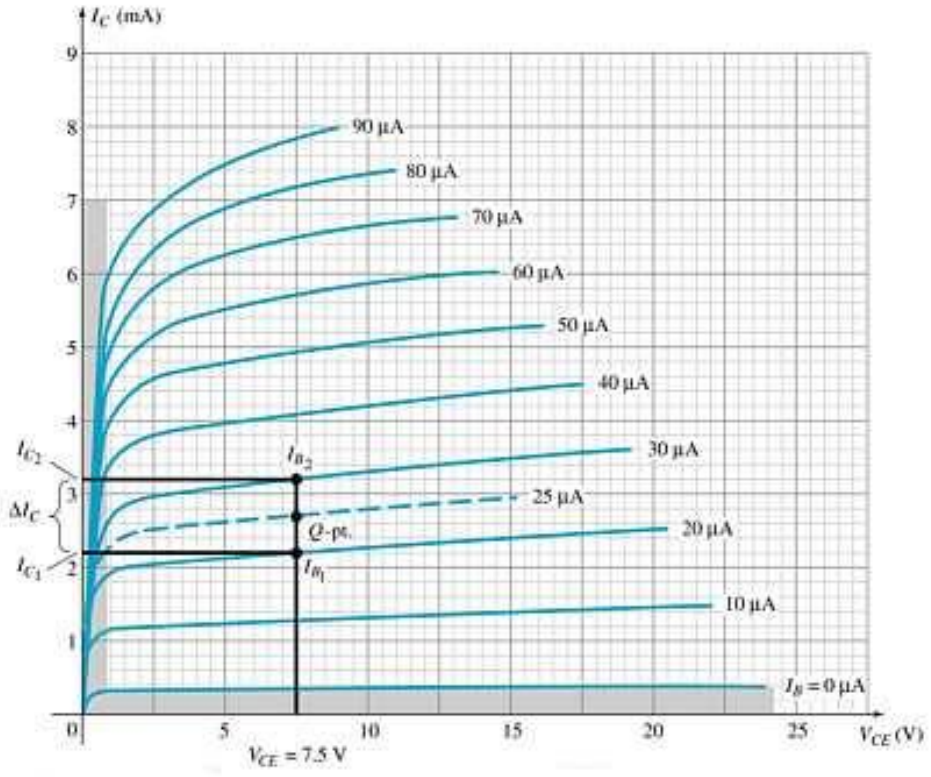
$$\beta_{AC} = \frac{(3.2\,\text{mA} - 2.2\,\text{mA})}{(30\,\mu\text{A} - 20\,\mu\text{A})}$$

$$= \frac{1\,\text{mA}}{10\,\mu\text{A}}\Bigg|_{V_{CE}=7.5}$$

$$= 100$$

$$\beta_{DC} = \frac{2.7\,\text{mA}}{25\,\mu\text{A}}\Bigg|_{V_{CE}=7.5}$$

$$= 108$$



Beta (β)

Relationship between amplification factors β and α

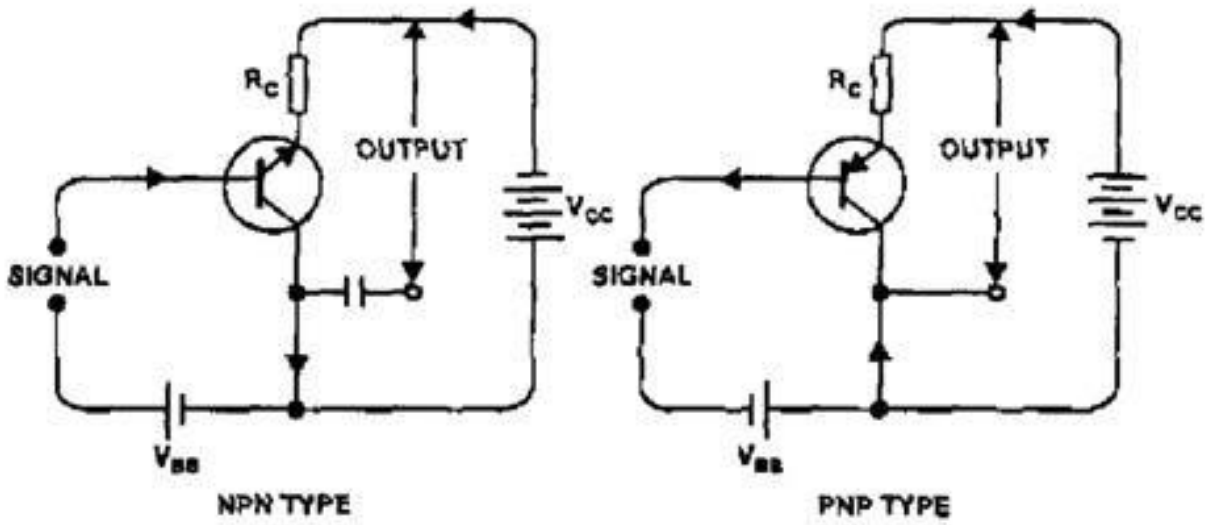
$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

Relationship Between Currents

$$I_C = \beta I_B \qquad I_E = (\beta + 1) I_B$$

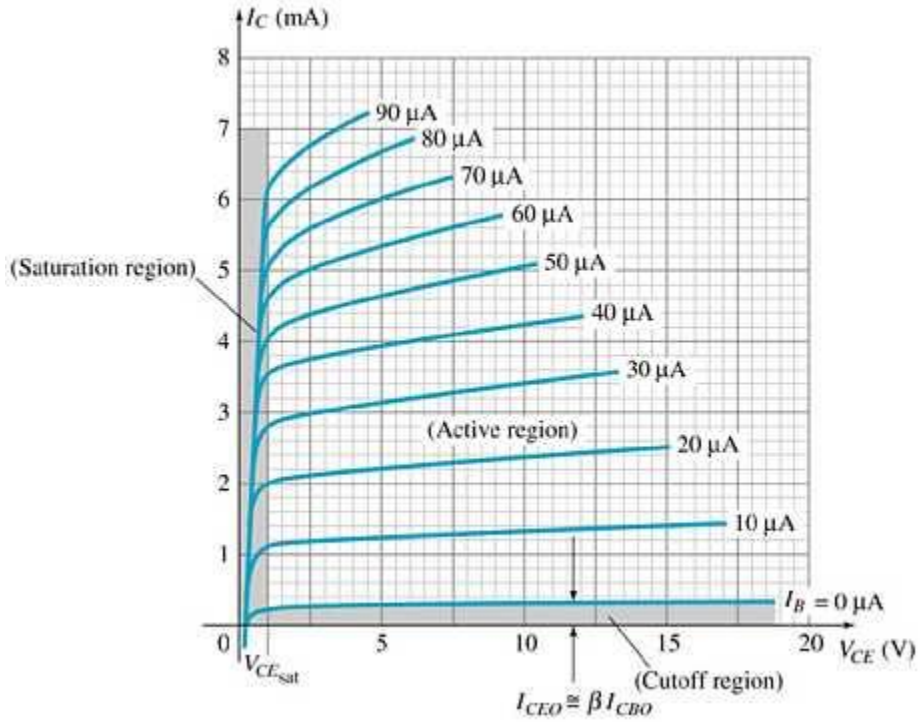
Common–Collector Configuration

The input is on the base and the output is on the emitter.



Common–Collector Configuration

The characteristics are similar to those of the common-emitter configuration, except the vertical axis is I_E.

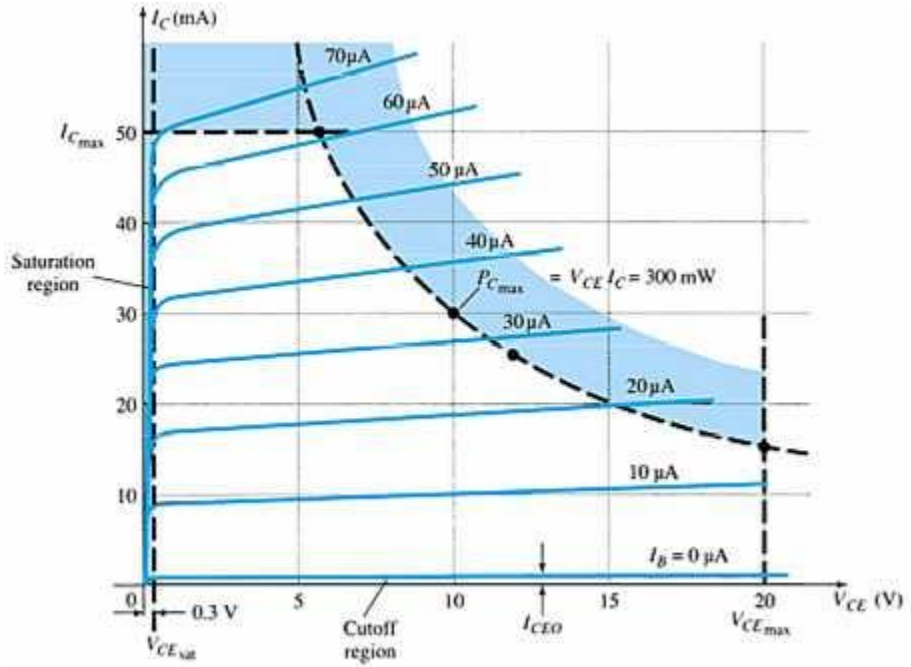


Operating Limits for Each Configuration

V_{CE} is at maximum and I_C is at minimum (I_{Cmax}= I_{CEO}) in the cutoff region.

I_C is at maximum and V_{CE} is at minimum ($V_{CE\ max}$ = V_{CEsat} = V_{CEO}) in the saturation region.

The transistor operates in the active region between saturation and cutoff.



Power Dissipation

Common-base:

$$P_{Cmax} = V_{CB}I_C$$

Common-emitter:

$$P_{Cmax} = V_{CE}I_C$$

Common-collector:

$$P_{Cmax} = V_{CE}I_E$$

Week - 10

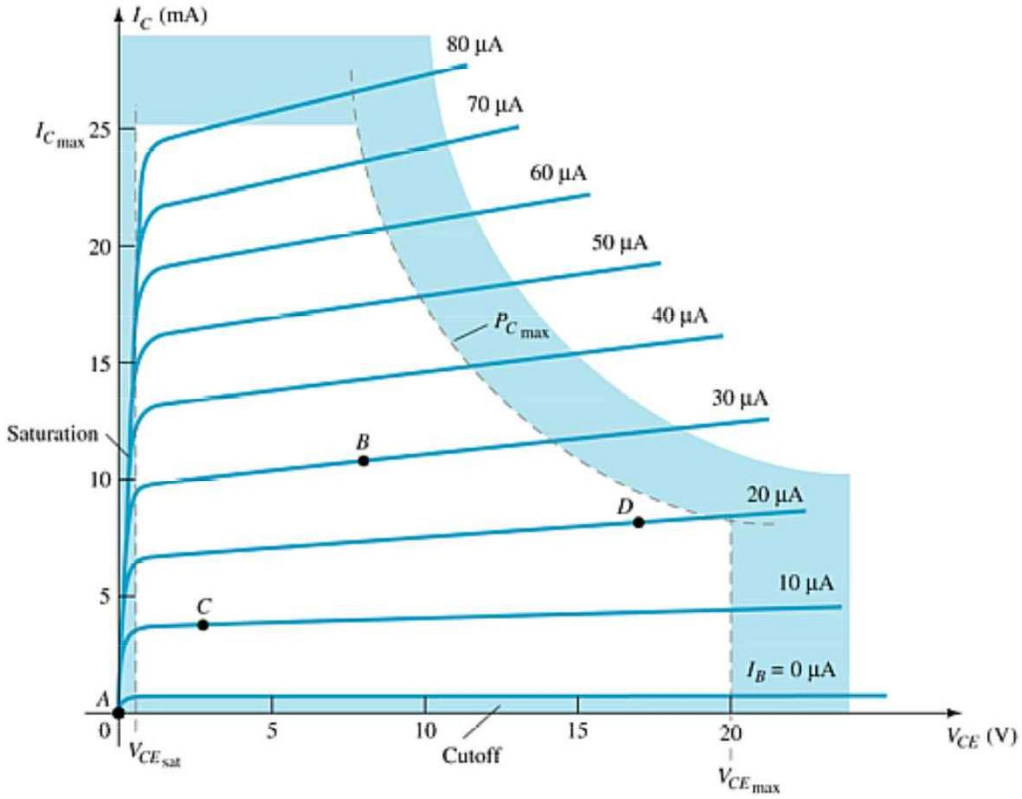
Biasing

Biasing: **The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.**

Operating Point

The DC input establishes an operating or *quiescent point* called the *Q-point*.

Which point is best?



The Three States of Operation

- **Active or Linear Region Operation**
  - **Base–Emitter junction is forward biased**
  - **Base–Collector junction is reverse biased**

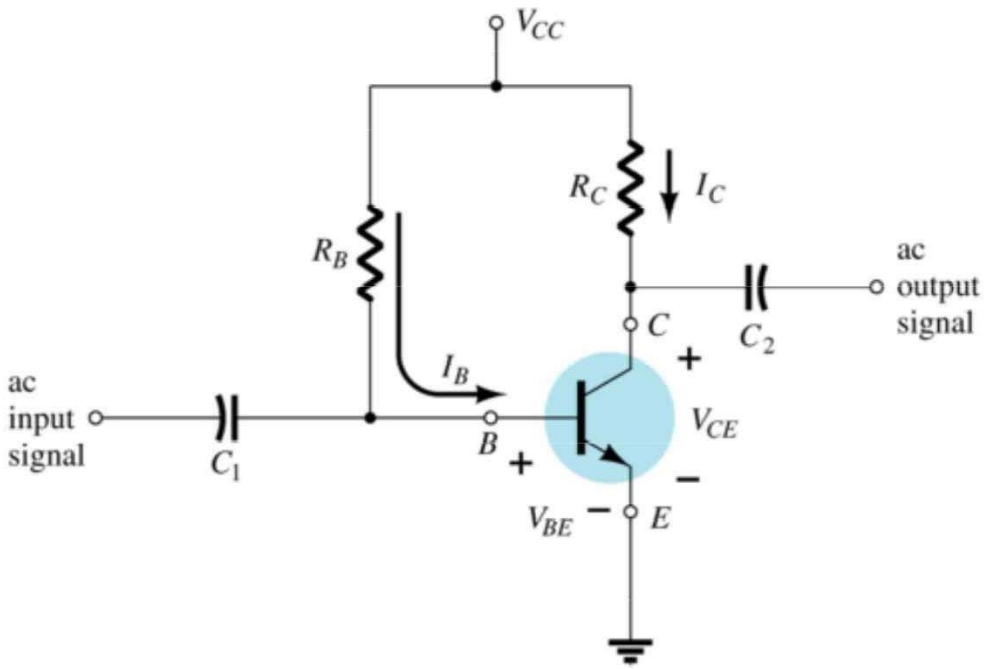
- **Cutoff Region Operation**
  - **Base–Emitter junction is reverse biased**

- **Saturation Region Operation**
  - **Base–Emitter junction is forward biased**
  - **Base–Collector junction is forward biased**

DC Biasing Circuits

- **Fixed-bias circuit**
- **Emitter-stabilized bias circuit**
- **Collector-emitter loop**
- **Voltage divider bias circuit**
- **DC bias with voltage feedback**

Fixed Bias


V_{CC}
R_C
I_C
R_B
ac
output
signal
C_2
C
+
I_B
ac
input
signal
C_1
B
+
V_{CE}
−
V_{BE}
−
E

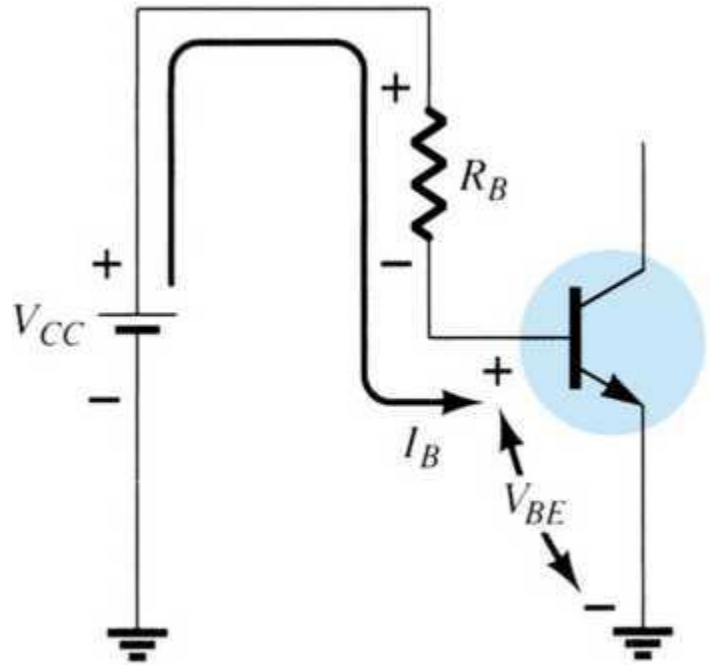
The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



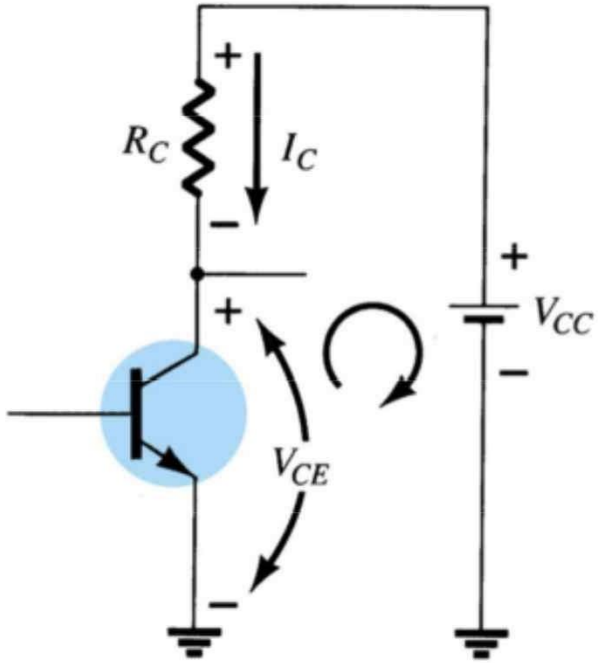
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Week - 11

Saturation

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\,V$$

Load Line Analysis

The end points of the load line are:

I_{Csat}

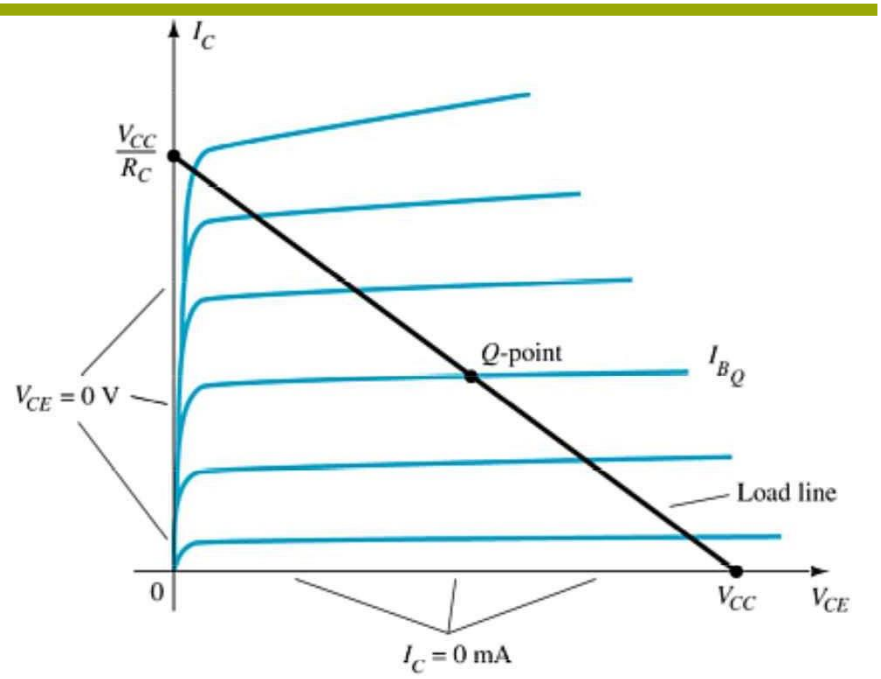
$I_C = V_{CC} / R_C$

$V_{CE} = 0$ V

$V_{CEcutoff}$

$V_{CE} = V_{CC}$

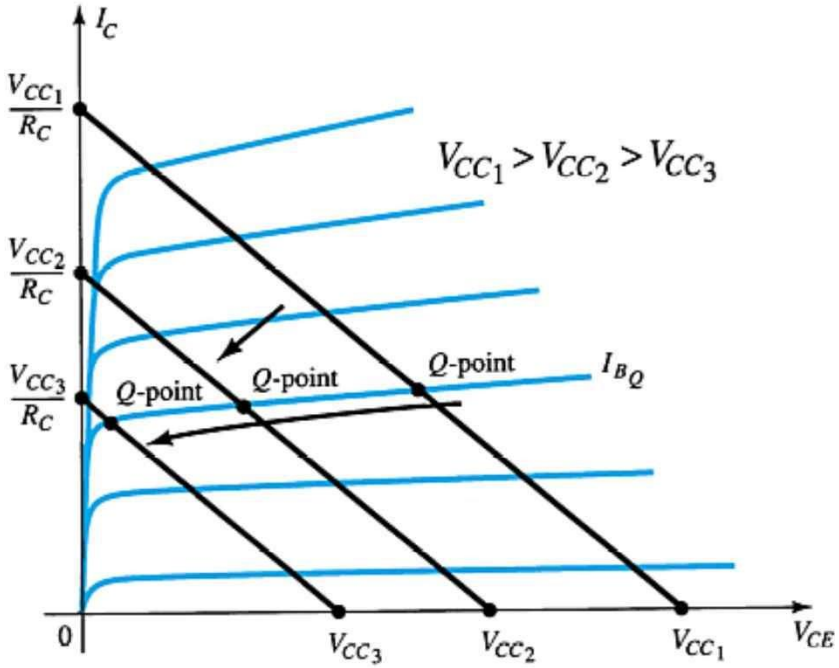
$I_C = 0$ mA



The *Q*-point is the operating point:

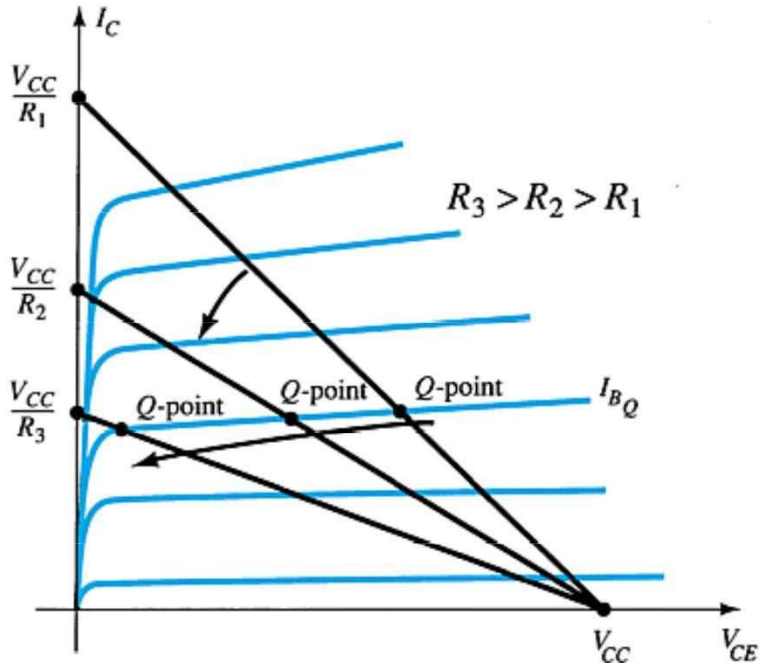
- **where the value of R_B sets the value of I_B**
- **that sets the values of V_{CE} and I_C**

Circuit Values Affect the Q-Point



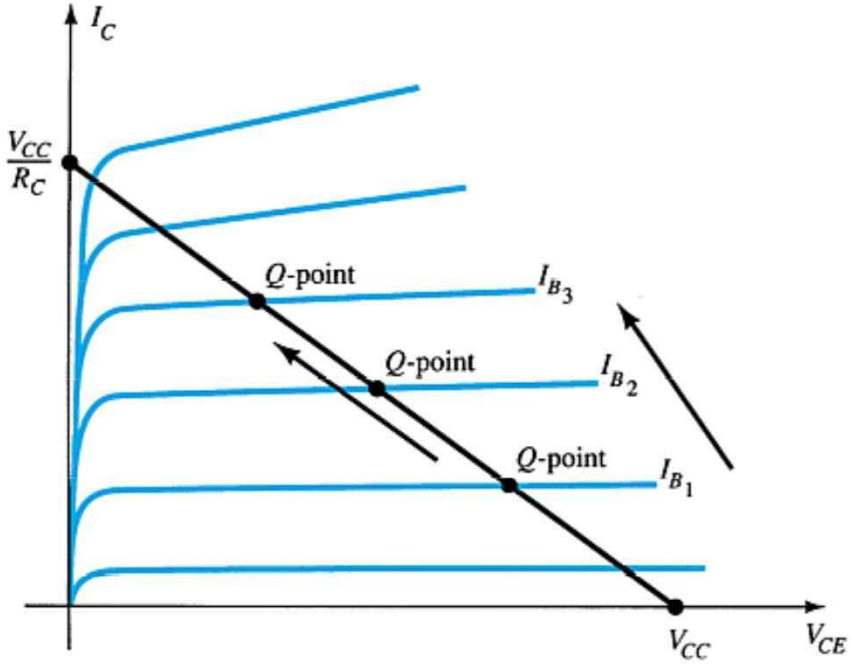
more …

Circuit Values Affect the Q-Point



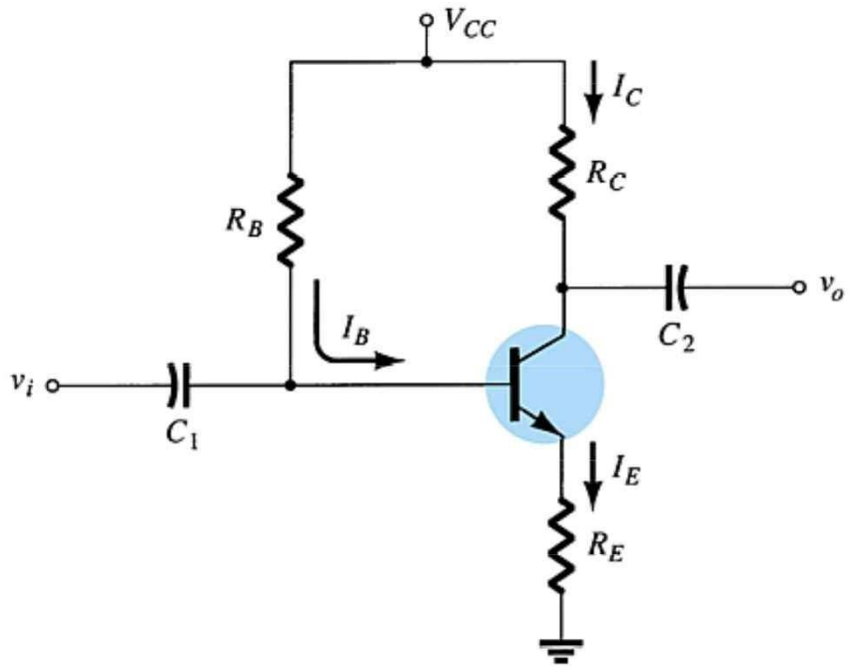
more …

Circuit Values Affect the Q-Point



Emitter-Stabilized Bias Circuit

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Week - 12

Collector-Emitter Loop

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$**:**

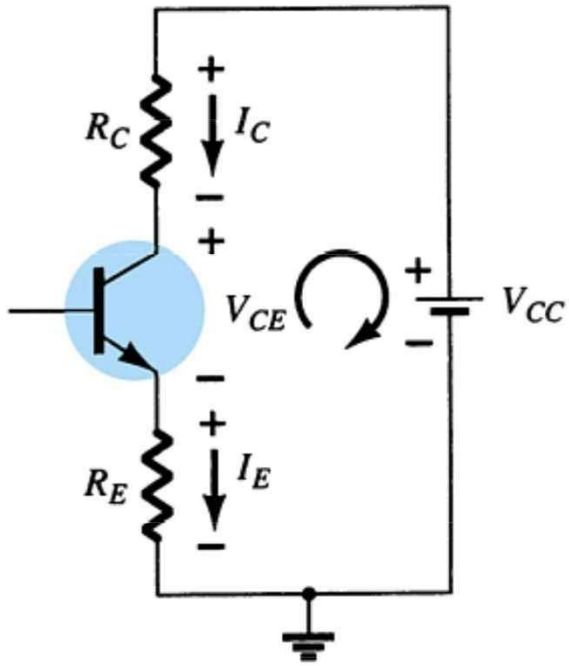
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$

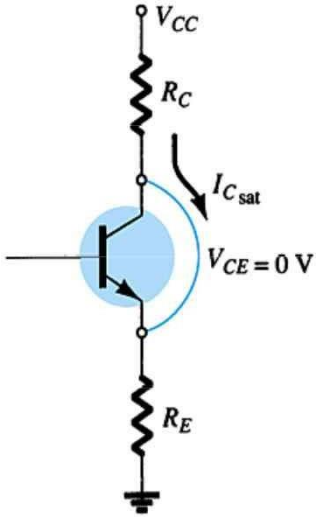


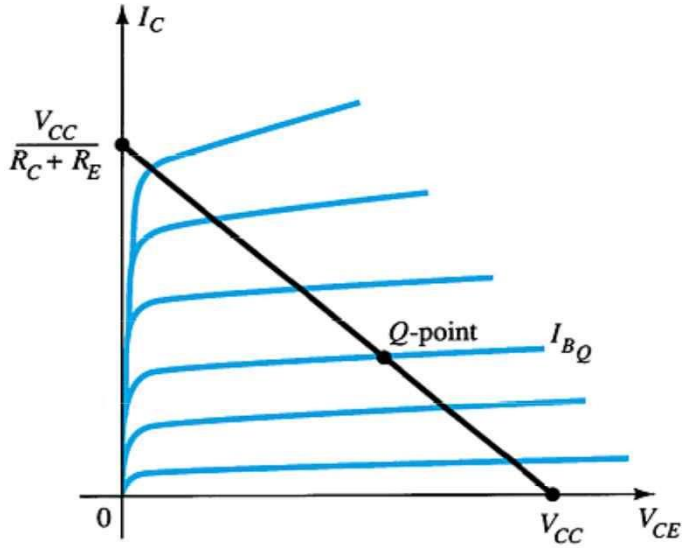
Improved Biased Stability

Stability **refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.**

Adding R_E to the emitter improves the stability of a transistor.

Saturation Level





The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$$V_{CE} = V_{CC}$$

$$I_C = 0\,\text{mA}$$

I_{Csat}:

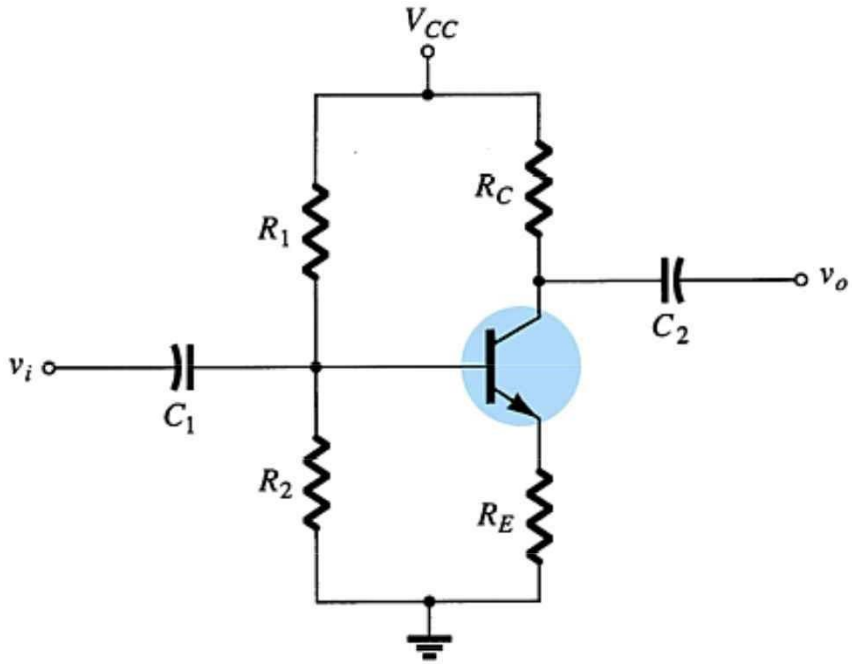
$$V_{CE} = 0\,\text{V}$$

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β.



Week - 13

Approximate Analysis

Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

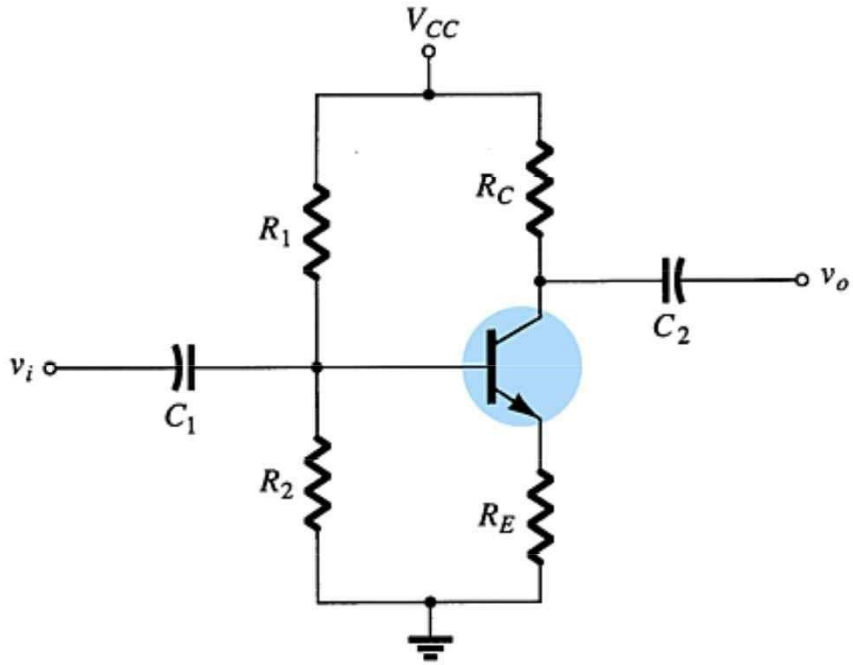
$$V_E = V_B - V_{BE}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$



Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$
$$I_C = 0mA$$

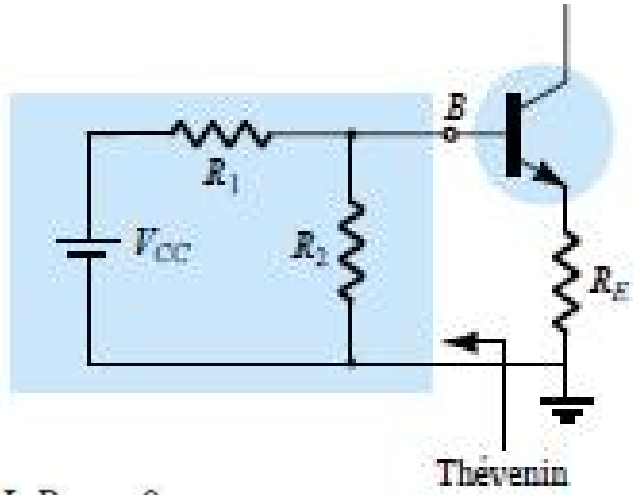
Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$
$$V_{CE} = 0V$$

Exact Analysis

$$R_{Th} = R_1 \| R_2$$

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$



$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1) I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

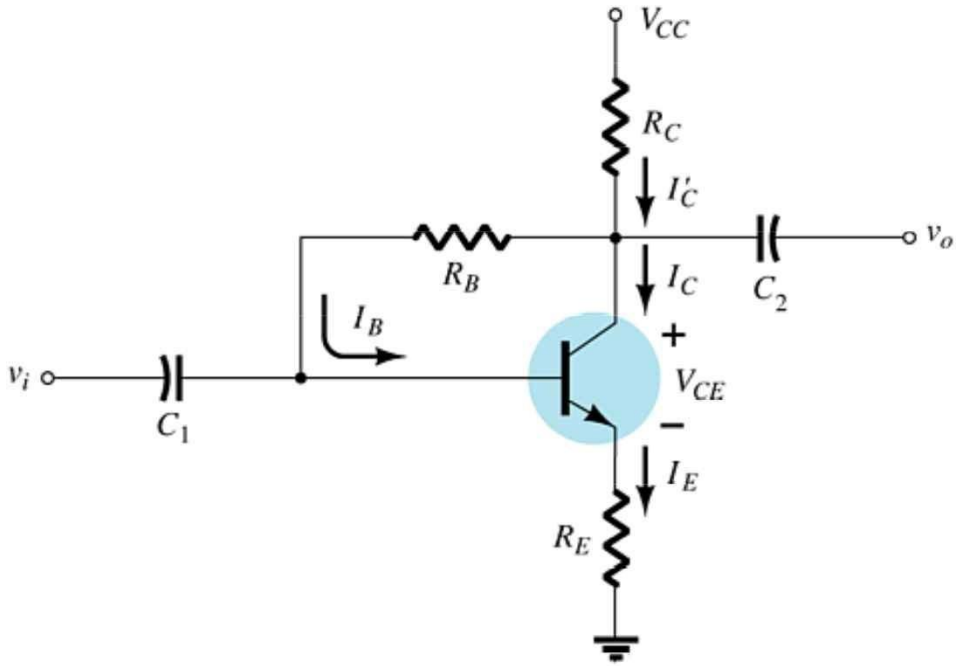
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Week - 14

DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

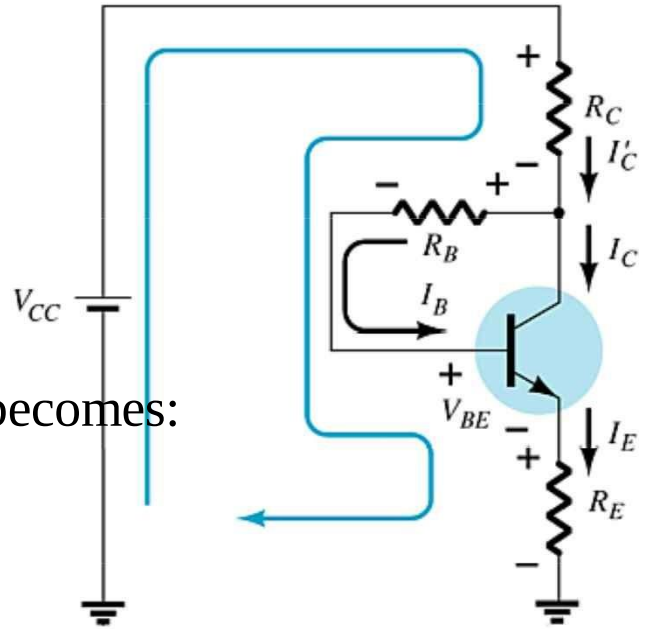
In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Base-Emitter Loop

From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$



Where $I_B << I_C$:

$$I' \cong I \quad \pm I \cong I \quad C \qquad\qquad C$$
B C

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B:

$$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}}$$

Collector-Emitter Loop

Applying Kirchoff's voltage law:

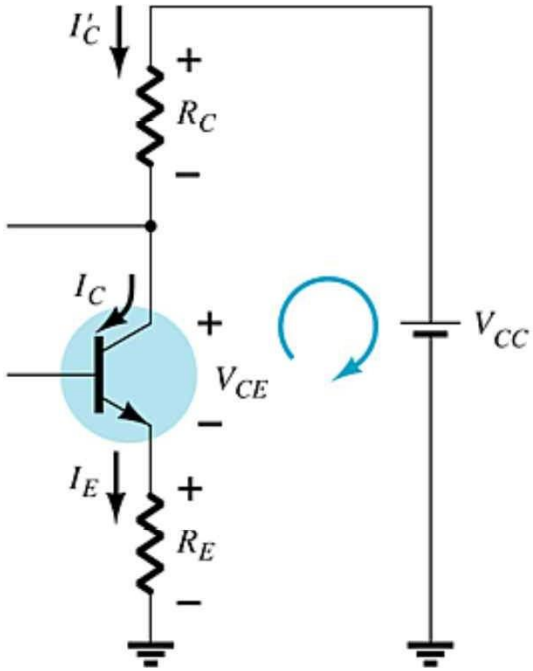
$$R_E I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE}:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Base-Emitter Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0\,mA$$

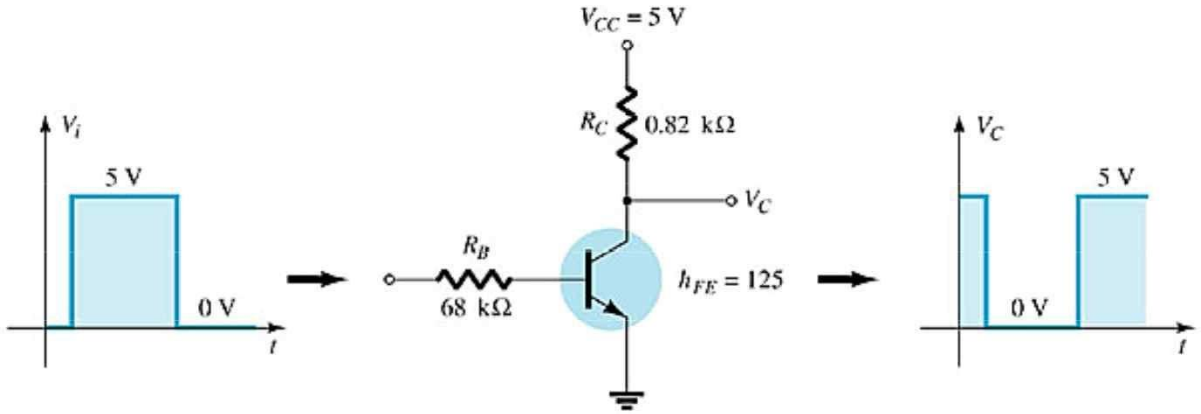
Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\,V$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



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Switching Circuit Calculations

Saturation current:

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

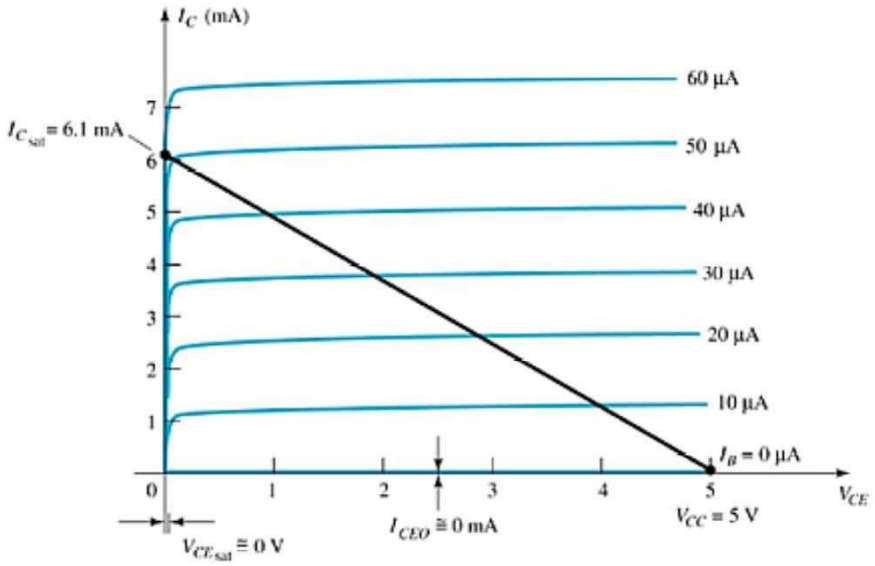
To ensure saturation:

$$I_B > \frac{I_{Csat}}{\beta_{dc}}$$

Emitter-collector resistance at saturation and cutoff:

$$R_{sat} = \frac{V_{CEsat}}{I_{Csat}}$$

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$$

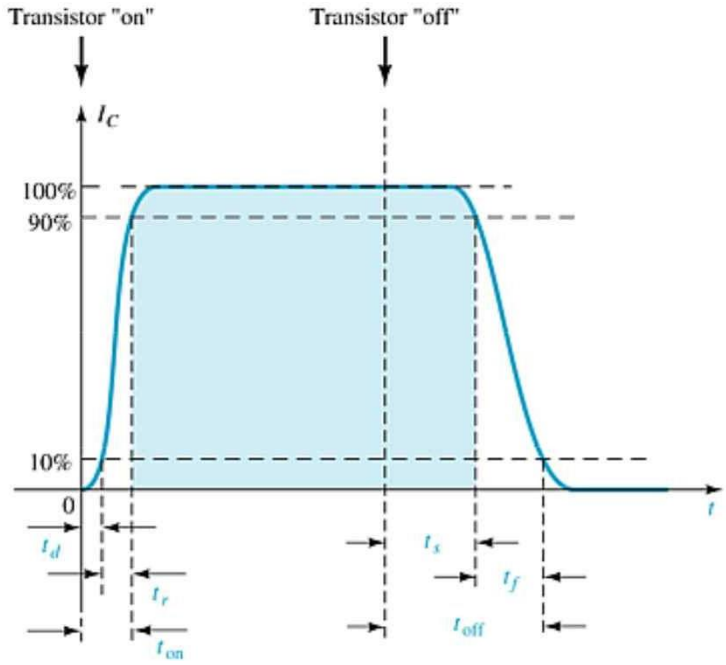


Switching Time

Transistor switching times:

$$t_{on} = t_r + t_d$$

$$t_{off} = t_s + t_f$$



t_r=rise time
t_d=delay time
t_s=storage time
t_f=forward time

PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.

Base-Emitter Loop

From Kirchhoff's voltage law:

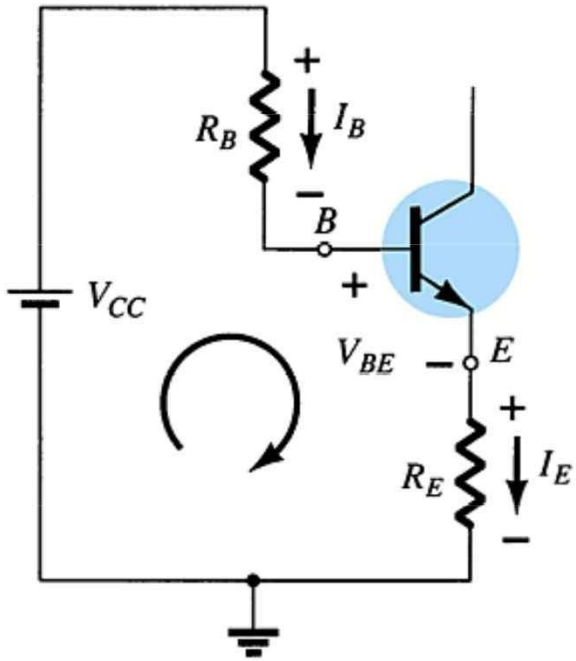
$$+V_{CC} - I_E R_E - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1)I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$




Thank
You!