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RATIOED NAND AND NOR BASED ON-CHIP PROCESS SENSOR

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- What is IC reliability.
- What is process variation, why is it important to monitor.
- Role of Ring Oscillator as sensors.
- Proposed work
- Working principle.
- Simulations and results
- Conclusion.

Introduction

Ever wondered why ICs differ or just vary in their intended performance, despite being manufactured by same fab, sharing same wafer ?

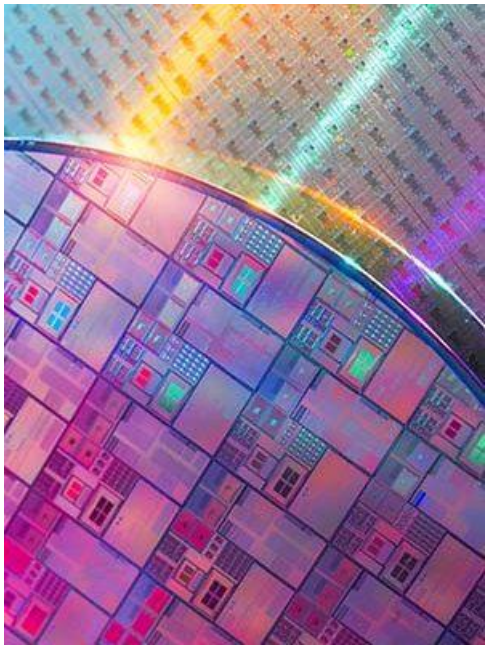


Image source: Ruysdael.nl

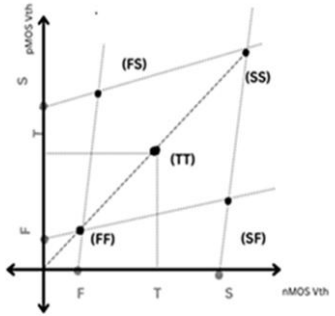
- Yes, **reliability** is of at most concern for yield and quality of ICs.
- Some of them cannot be mitigated !!!
- Process, Voltage, Temperature (PVT) variations.
- Thus, it is very necessary to monitor the environment the IC is experiencing, which would be severe for SoC level IC densities.

Process Variation

- Process variation, is the variation occurring due to **manufacturing processes**. This include non-uniform doping concentration, lateral diffusion, etc. Lithographic issues, such as variability in exposure dose and mask defects that result in microscopic deviations in the edges of patterned lines. [1][2]
- The effect of process variation is **more significant** in deep submicron designs, **due to technology scaling**, which make them more susceptible to variations in process parameters and noise effects like power supply noise, crosstalk reduced supply voltage and threshold voltage operation severely impacting the yield. [3]

Process Variation

- Process variation directly affects threshold voltage (Vth) which plays a crucial role in transistor's switching activity, thus overall performance (frequency).



- Process variations are keyed by process corners, (which helps in binning the IC). Process corners are realized by locus of threshold voltage of nMOS and pMOS.

Ring Oscillators

- Measuring the process variations on the wafer is generally performed by deploying the Ring Oscillator (RO) circuit on the scribe lines. The On-Chip RO-based process sensors are widely used because their frequency can carry information about variation.! [4][1]

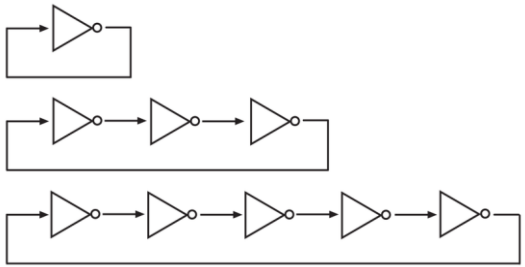


Image source: researchgate.net

Ring Oscillators

- In order to sense the behavior of circuit (MOSFETs to complex circuit), sensing the shift in Vth and thus frequency (1/T) for given temperature is necessary.

$$k_N = \frac{\Delta T/T_0}{\Delta V_n/V_{n0}}$$

$$k_P = \frac{\Delta T/T_0}{\Delta V_p/V_{p0}}$$

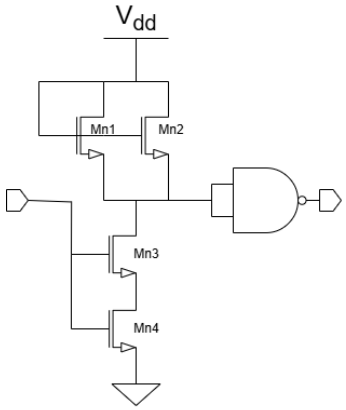
- The coefficients of the process sensitivity in are the change rate of output period according to the threshold voltage variation and can be expressed as above [5] :

Prior works

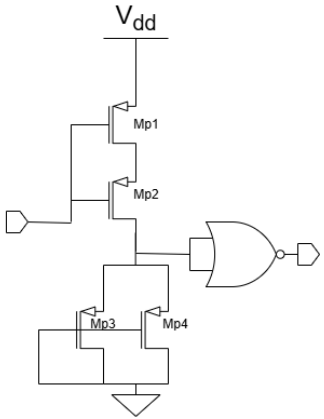
Prior works	Prior work	Sensitivity achieved
Heterogenous Structures [5]	Pass-gate logic (N or P) is introduced in between conventional ring oscillator.	Improved sensitivity than CMOS inverters-based RO, but not as significant in terms of sensitivity.
Ratioed-Inverters [1]	Ratioed logic inverters with CMOS inverters are used as delay-cells and hence ring oscillator is made.	Measures better sensitivity than any other RO based Sensors.
Ratioed-Inverters with Reshaper [6]	Only ratioed logic inverter is used for even number of stage and wave reshaper is used as inverting stage in RO.	Measure higher sensitivity than [1] and fails for higher number of stages

Proposed Work

- We propose two delay cell structures to be used in RO circuit to be used as process sensors.
- **N-Ratioed-NAND** delay cell captures variation in nMOS and **P-Ratioed-NOR** delay cell captures in pMOS.



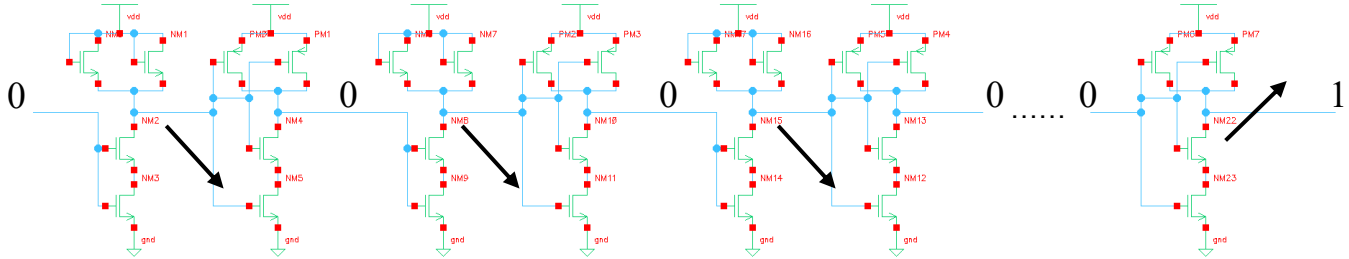
N-Ratioed NAND and NAND



P-Ratioed NOR and NOR

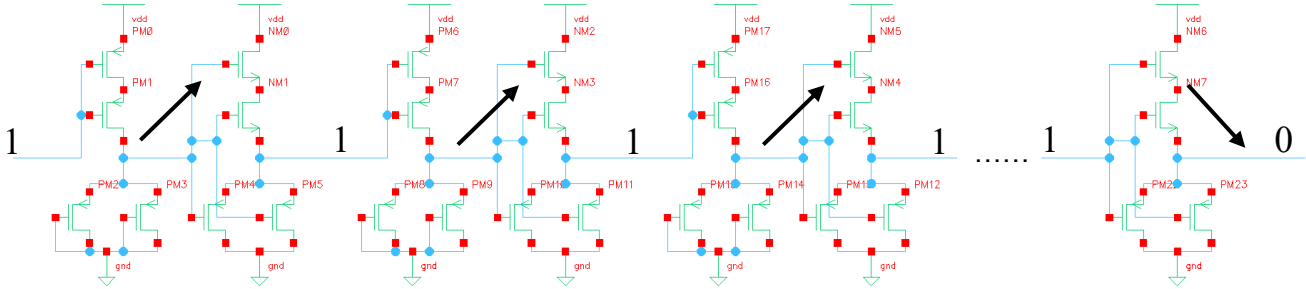
Working Principle

- In N-sensitivity, the delay path for logic-0 transition involves only nMOS transistors of all stages. Thus, this delay is more prominent towards change in threshold voltage of nMOS and hence its process variation.



Working Principle

- In P-sensitivity, the delay path for logic-1 transition involves only pMOS transistors of all stages. Thus, this delay is more prominent towards change in threshold voltage of pMOS and hence its process variation.



Simulations & Results

Transients.

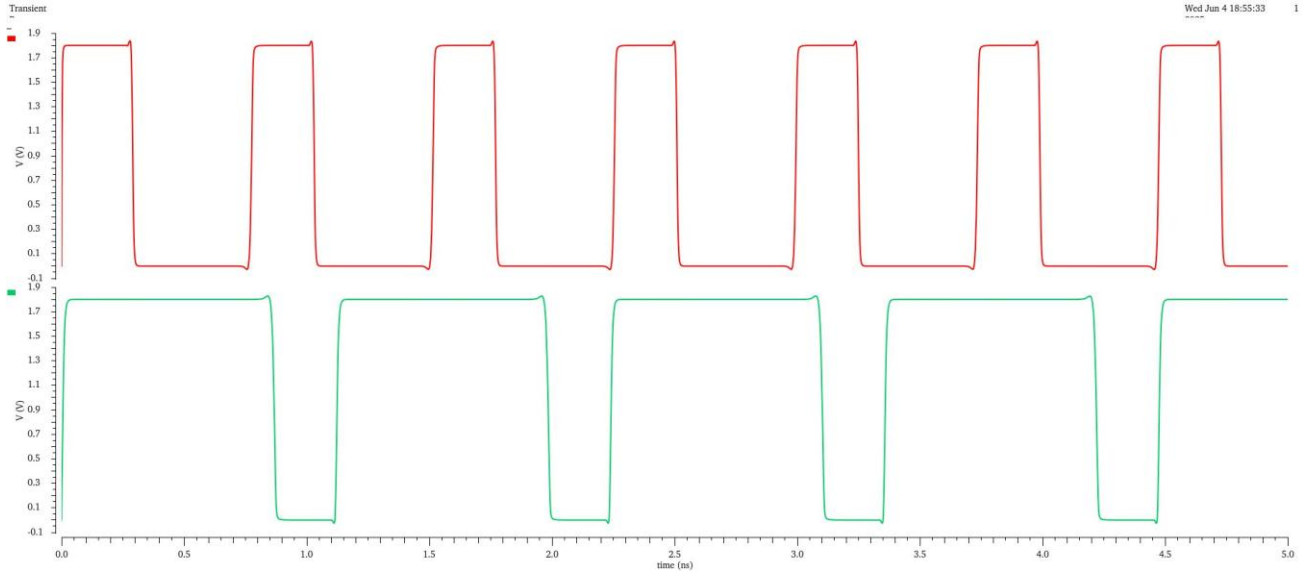
- Time period of N-delay-cell RO has pulse width of logic-0 is greater than logic-1, which signifies the increased n-sensitivity.
- Similarly, time period of P-delay-cell RO shows pulse width of logic-1 is greater than logic-0 indicating its p-sensitivity.

Simulations & Results

Transients.

nMOS

pMOS



Simulations & Results

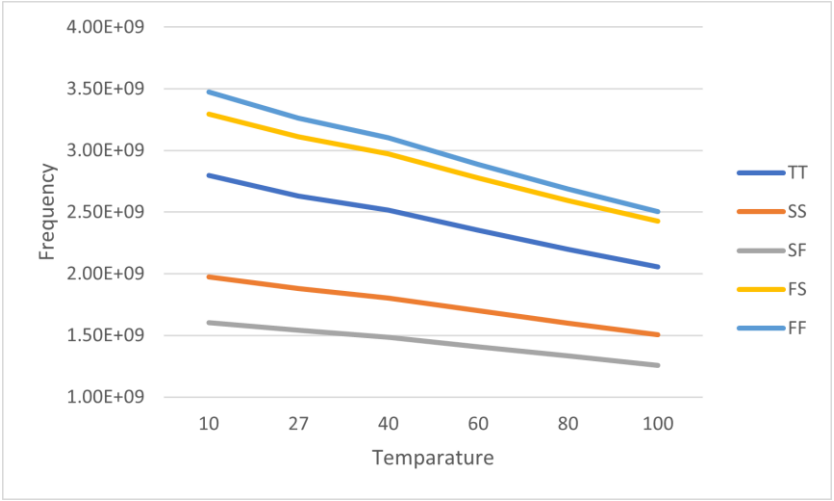
Frequency analysis.

- Using N-delay-cell RO, the order of the frequency plots observed is FF > FS > TT > SS > SF. This is because of the fact that (FF, FS) are corners with fast nMOS, while the (SF, SS) are corners with slow nMOS.

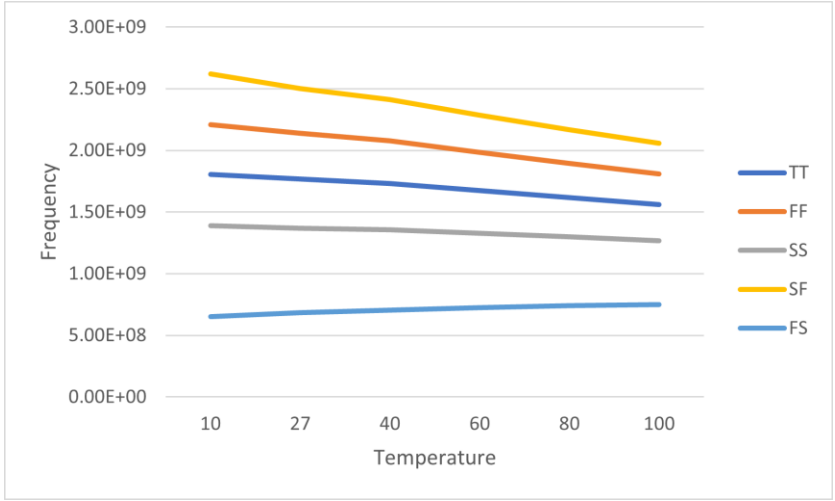
- Using P-delay-cell RO, the order of the frequency plots observed is SF > FF > TT > SS > FS. This shows that the (FF, SF) are corners of fast pMOS, while the (FS, SS) are corners of slow pMOS.

Simulations & Results

Frequency analysis.



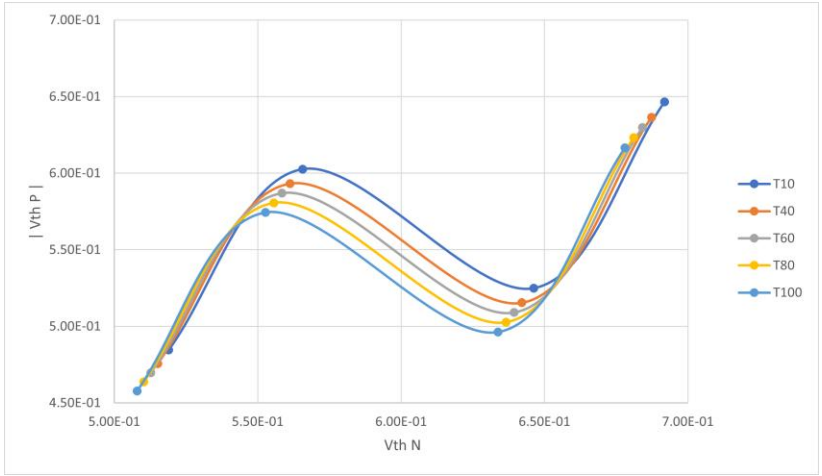
N-delay-cell RO frequency



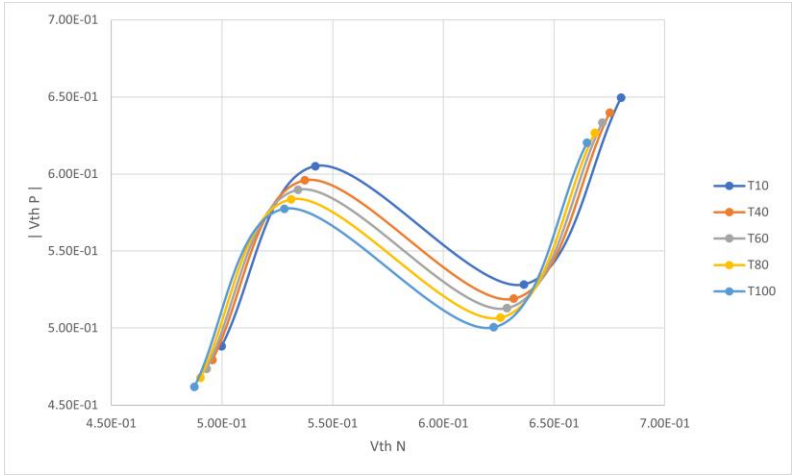
P-delay-cell RO frequency

Simulations & Results

Process corner maps.



nMOS process corner

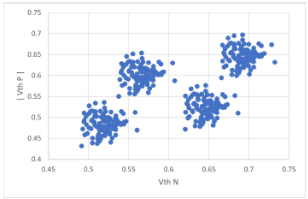


pMOS process corner

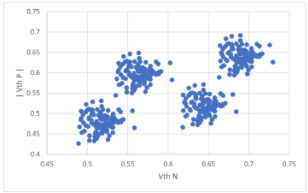
Simulations & Results

Monte-Carlo simulation & Threshold voltage analysis.

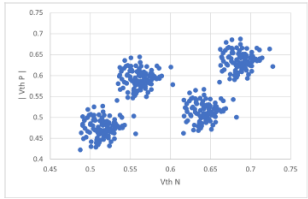
- The mean threshold voltage of nMOS and pMOS is obtained from the proposed N-delay-cell and P-delay-cell for various temperatures respectively. These values are plotted/fit into the process corner map.



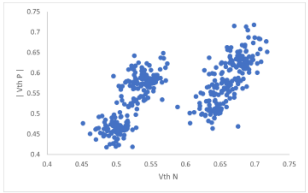
(a) N-delay-cell at 10^0C



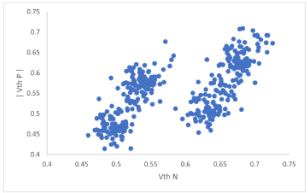
(b) N-delay-cell at 27^0C



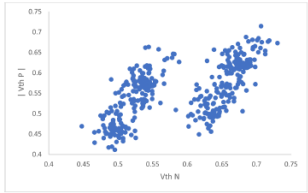
(c) N-delay-cell at 40^0C



(d) P-delay-cell at 10^0C



(e) P-delay-cell at 27^0C



(f) P-delay-cell at 40^0C

Simulations & Results

Sensitivity comparison.

Design	N Sensitivity	P Sensitivity	Power (mW)
Heterogeneous structures [5]	0.865	1.335	0.291
Ratioed Inverters[1]	1.934	3.189	3.288
Proposed Design	4.086	7.223	2.902

Conclusion

- The proposed process sensor has got a sensitivity that is more than 100% of the work presented in [1] and more than 300% the sensor presented in [5].
- The process corner cluster are almost stable to temperature variation and while using 12% less power. However, this improvement comes at the expense of compromising the chip-area.

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