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A Brief about Ripple Counter with Circuit Timing Diagrams

While carefully observing the production line of glass bottles, which were being packed package by machines, an inquisitive mind questions – How does the machine knows to of bottles? What teaches the machines how to count? Searching an answer to solve this to a very interesting invention named – "Counter's". Counters are the circuit which c clock pulses. These are usually designed using flip-flops. Based on the way clock is functioning counters are classified as **Synchronous and Asynchronous counters**. In look at an Asynchronous counter which is notoriously known as **Ripple counter**.

Before jumping to Ripple Counter let's get familiarized with the terms **Synchronous ar counters**. Counters are circuits made using flip-flops. Synchronous counter, as the nar all **the flip-flops** working in sync with clock pulse as well as each other. Here clock pevery flip flop.

Whereas in Asynchronous counter clock pulse is applied only to the initial flip flop who considered as LSB. Instead of the clock pulse, the output of first flip-flop acts as a clock flip flop, whose output is used as a clock to the next in line flip-flop and so on.

Thus, in Asynchronous counter after the transition of the previous flip flop transition of takes place, not at the same time as seen in Synchronous counter. Here flip-flops Master-Slave arrangement.

Ripple Counter: Ripple counter is an Asynchronous counter. It got its name becaus ripples through the circuit. An n-MOD ripple counter contains n number of flip-flops a count up to 2ⁿ values before it resets itself to the initial value.

These counters can count in different ways based on their circuitry.

UP COUNTER: Counts the values in ascending order.

DOWN COUNTER: Counts the values in descending order.

UP-DOWN COUNTER: A counter which can count values either in the forward did direction is called an up-down counter or reversible counter.

DIVIDE by N COUNTER: Instead of a binary, we may sometimes require to count up to 10. Ripple counter which can count up to value N which is not a power of 2 is called Divide



Ripple Counter Circuit Diagram and Timing Diagram

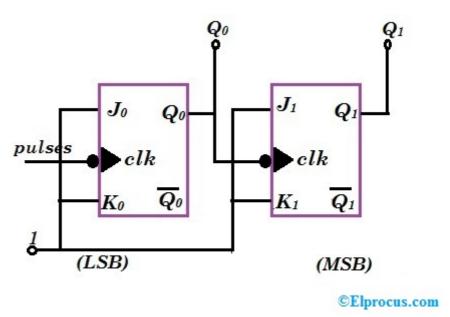
The **working of the ripple counter** can be best understood with the help of an exam number of flip flops used there are 2-bit, 3-bit, 4-bit..... ripple counters can be designed. working of a 2-bit **binary ripple counter** to understand the concept.

A binary counter can count up to 2-bit values .i.e. **2-MOD** counter can count $2^2 = 4$ value is 2 we use 2 flip-flops. While choosing the type of flip-flop it should be remer counters can be designed only using those flip-flops which have a condition for toggling flip flops.

Binary Ripple Counter using JK Flip Flop

The circuit arrangement of a **binary ripple counter** is as shown in the figure below. Here J0K0 and J1K1 are used. JK inputs of flip flops are supplied with high voltage signal ma state 1. The symbol for the clock pulse indicates a negative triggered clock pulse. From be observed that the output Q0 of the first flip flop is applied as a clock pulse to the second





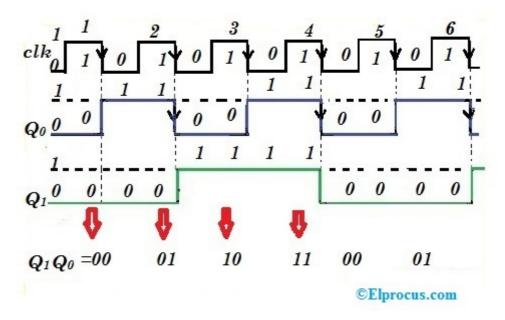
Binary Ripple Counter Using JK Flip Flop

Here the output Q0 is the LSB and the output Q1 is the MSB bit. The functioning of the easily understood using the Truth Table of JK flip flop.

J _n	K _n	Q _{n+1}
0	0	Q _n
1	0	1
0	1	0

1

So, according to the Truth table, when both the inputs are 1 the next state will be the operations state. This condition is used in ripple flip flop. As we have applied a high voinputs of flip-flops they are at the state 1, so they must toggle the state at the negative clock pulse i.e. at the transition 1 to 0 of the clock pulse. The timing diagram of the bir clearly explains the operation.



Timing Diagram of Binary Ripple Counter

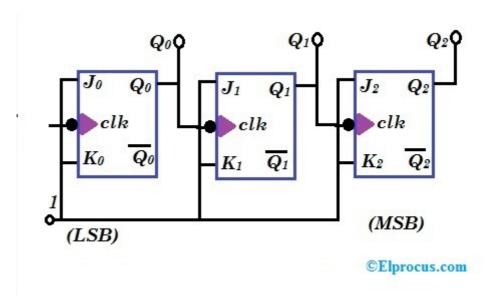
From the timing diagram, we can observe that Q0 changes state only during the negapplied clock. Initially, the flip flop is at state 0. Flip-flop stays in the state until the applie 1 to 0. As the JK values are 1, the flip flop should toggle. So, it changes state from 0 continues for all pulses of the clock.

Number of input pulses	Q ₁
0	_
1	0
2	0
3	1

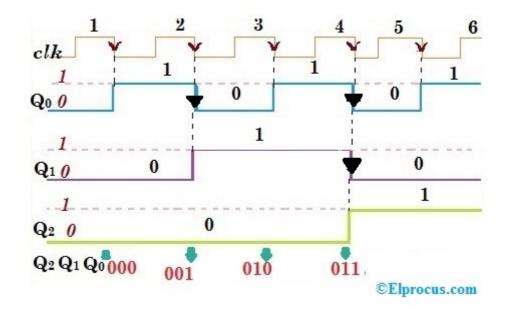
Coming to the second flip flop, here the waveform generated by flip flop 1 is given as c we can see in the timing diagram when Q0 goes transition from 1 to 0 the state of Q1 cr consider the above clock pulse, only follow the waveform of Q0. Note that the output considered as LSB and Q1 are considered as MSB. From the timing diagram, we can counter counts the values 00,01,10,11 then resets itself and starts again from 00,01,... are applied to J0K0 flip flop.

3-bit Ripple counter using JK flip-flop – Truth Table/Timing Diagram

In the 3-bit ripple counter, three flip-flops are used in the circuit. As here 'n' value is thre count up to $2^3 = 8$ values .i.e. 000,001,010,011,100,101,110,111. The circuit diagram a are given below.



Binary Ripple Counter Using JK Flip Flop



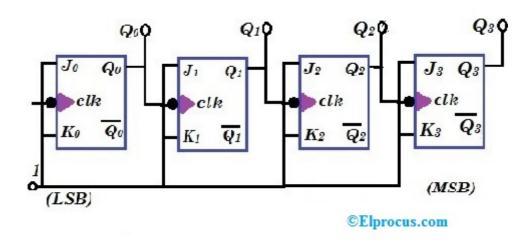
3 bit Ripple Counter Timing Diagram

Here the output waveform of Q1 is given as clock pulse to the flip flop J2K2. So, when Q transitions, the state of Q2 is changed. The output of Q2 is the MSB.

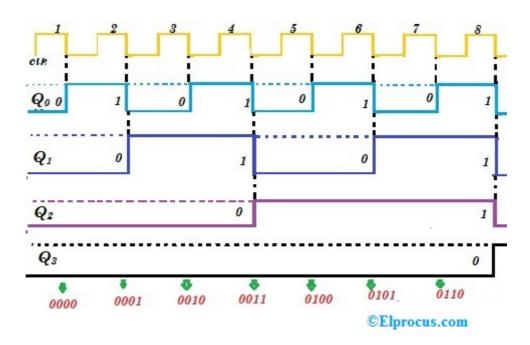
Number of pulses	Q_2	Q ₁
0	_	_
1	0	0
2	0	0
3	0	1
4	0	1
5	1	0
6	1	0
7	1	1
8	1	1
8	1	1

4-bit Ripple Counter Using JK Flip flop - Circuit Diagram and Timin

In 4-bit ripple counter, n value is 4 so, 4 JK flip flops are used and the counter can cour Below the **circuit diagram and timing diagram** are given along with the truth table.



4 bit Ripple Counter using JK Flip Flop



4 bit Ripple Counter Timing Diagram

4 bit Ripple Counter Using D Flip Flop

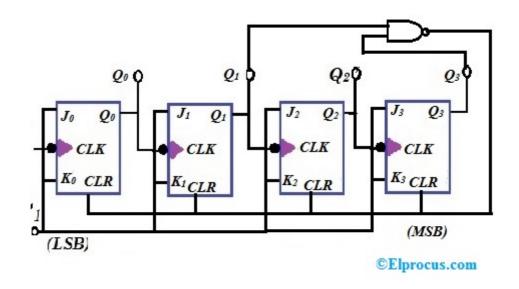
When it comes to selecting a Flip Flop for Ripple counter designing an important point t that the flip flop should contain a condition for toggling of states. This condition is satis JK flip flops.

From the truth table of **D** flip flop, it can be clearly seen that it doesn't contain the togg when a used as Ripple counter D flip flop has initial value as 1. When book pull

transition from 1 to 0 the flip flop should change the state. But according to truth table w stays on 1 until D value is changed to 0. So, the waveform of D0-flip flop will always so useful for counting. So, D flip flop is not considered for construction of Ripple Counters.

Divide by N counter

Ripple counter counts values up to 2ⁿ. So, to count values which are not powers of 2 is the circuitry that we have seen till now. But by modification, we can make ripple counter which cannot be expressed as a power of 2. Such a counter is called **Divide by N count**



Decade Counter

The number of flip flops n to be used in this design are chosen in such a way that $2^n > 0$ count of the counter. Along with flip flops, a feedback gate is added so that at count N ϵ reset to zero. This feedback circuit is simply a **NAND gate** whose inputs are the outp flops whose output Q = 1 at the count N.

Let us see the circuit of a counter for which N value is 10. This counter is also known as as it counts up to 10. Here the number of flip flops should be 4 because of 2^4 = 16 > 10. N= 10 the outputs Q1 and Q3 will be 1. So, these are given as inputs to the NAND gate NAND gate is applied to all the flip flops thereby resetting them to zero.

Drawbacks of Ripple Counter

The carry propagation time is the time taken by a counter to complete its response pulse. As in ripple counter, the clock pulse is Asynchronous, it requir to time

Applications of Ripple Counter

These counters are frequently used for measurement of Time, Measurement of Freque of Distance, Measurement of Speed, Waveform generation, Frequency Division, Digital Counting etc....

Thus this is all about brief information about ripple counter, the working of bina counters construction using JK-Flip Flop along with circuit diagram, ripple counter and truth table. The main reason behind the construction of the ripple counter disadvantages and applications of Ripple Counter. here is a question for you, what Counter?

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