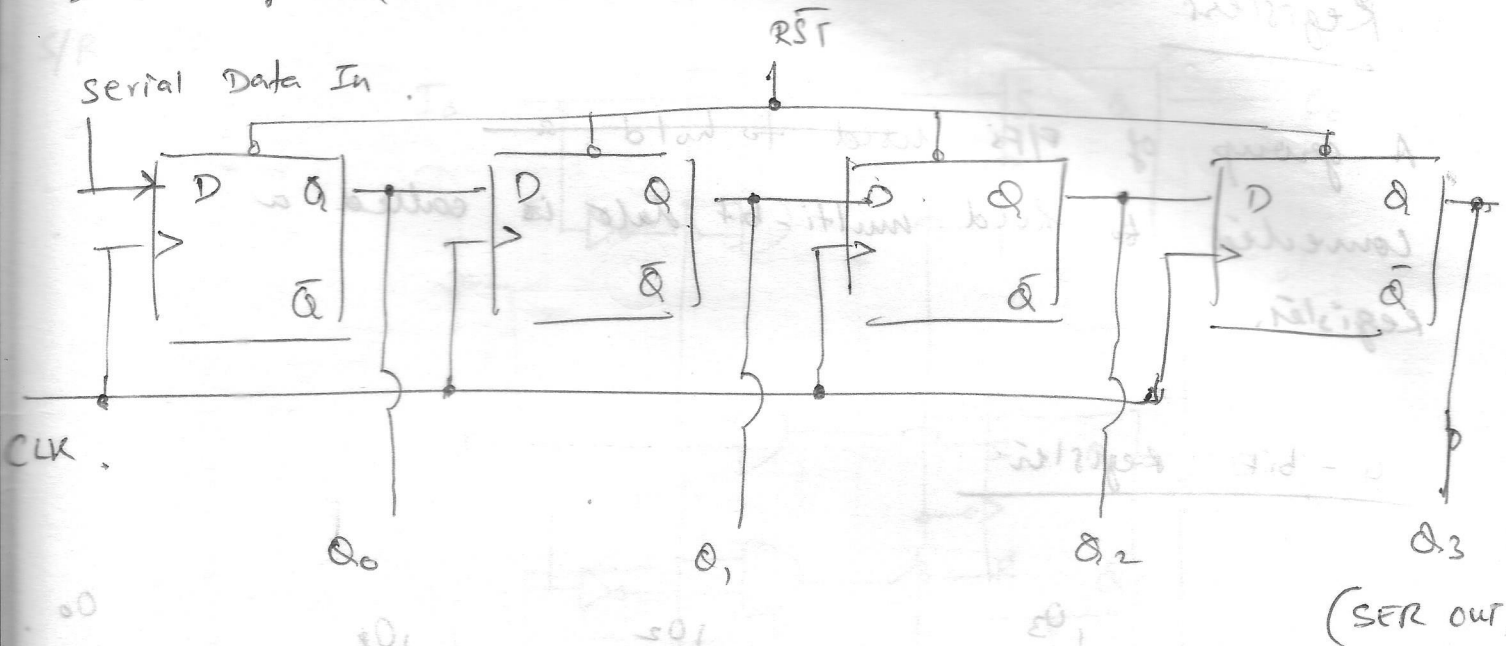
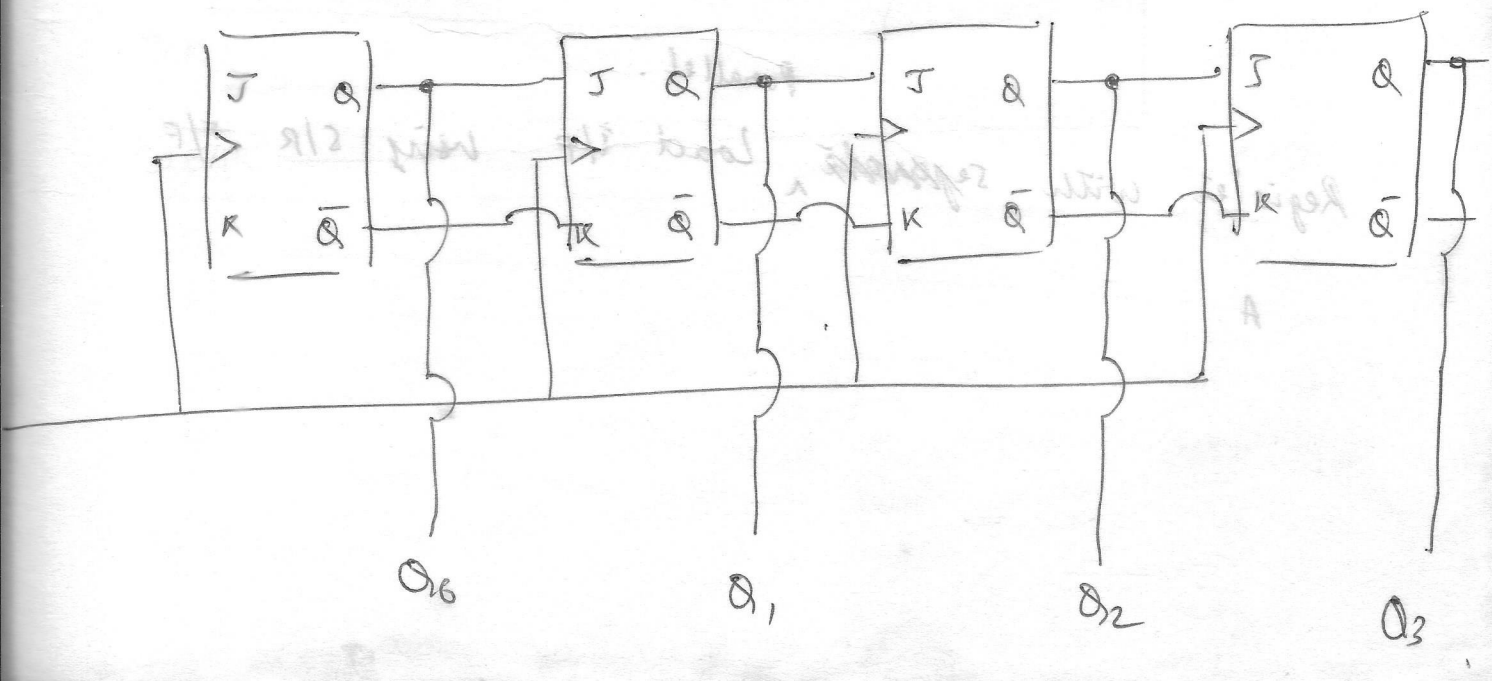
Shift Register (shift right)



Serial Data = 1 0 1 0 1 0 1 0.

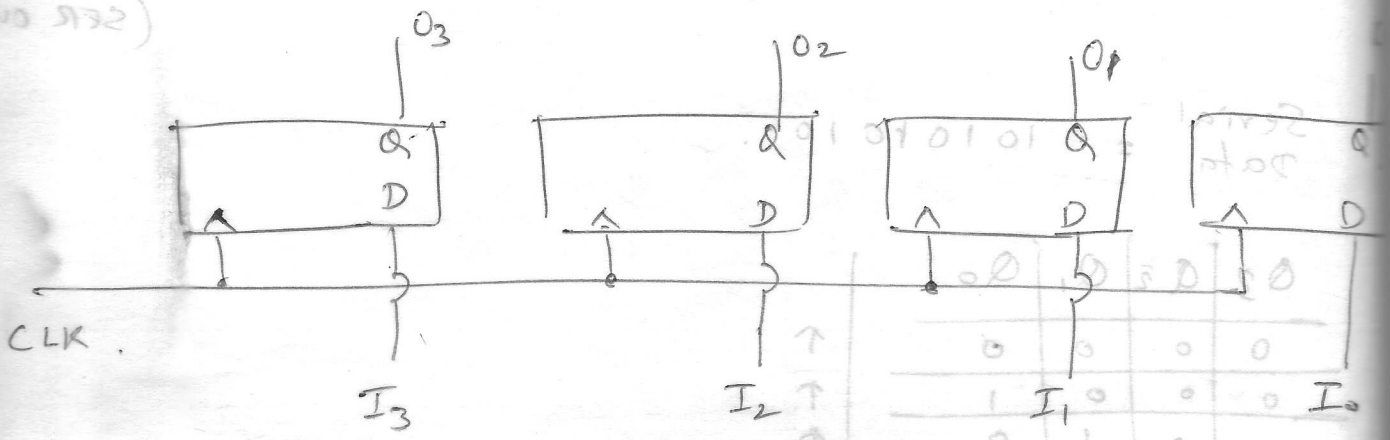
Q_3	Q_2	Q_1	Q_0	
0	0	0	0	↑
0	0	0	1	↑
0	0	1	0	↑
0	1	0	1	↑
1	0	1	0	↑
0	1	0	1	↑



Registers

A group of F/Fs ~~used to hold a~~ connected to hold multi-bit data is called a register.

4 - bit Register



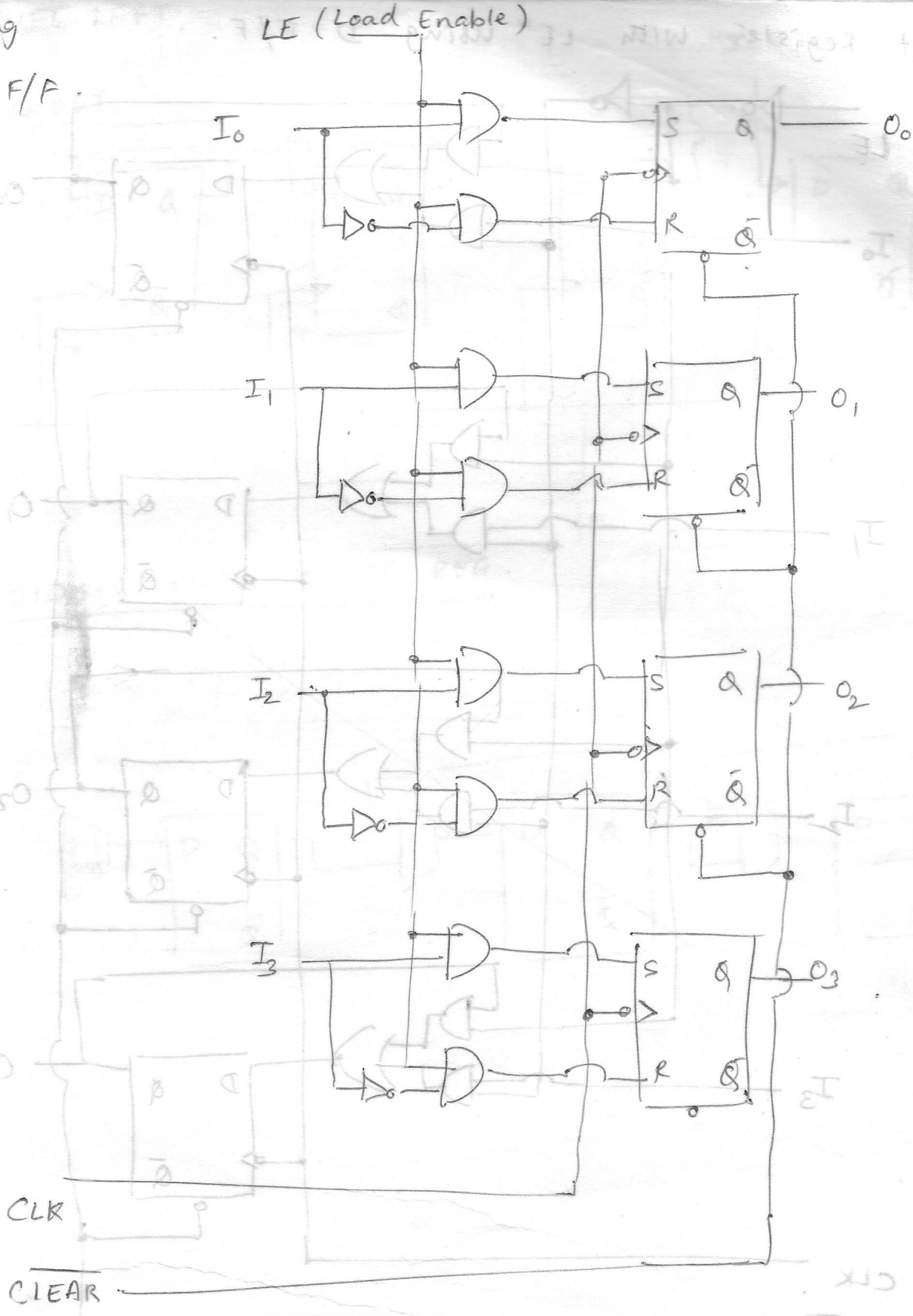
A group of F/Fs sensitive to pulse-duration (level-triggered clock) is called a latch.

A group of F/Fs sensitive to pulse-transition (edge-triggered clock) is called a register.

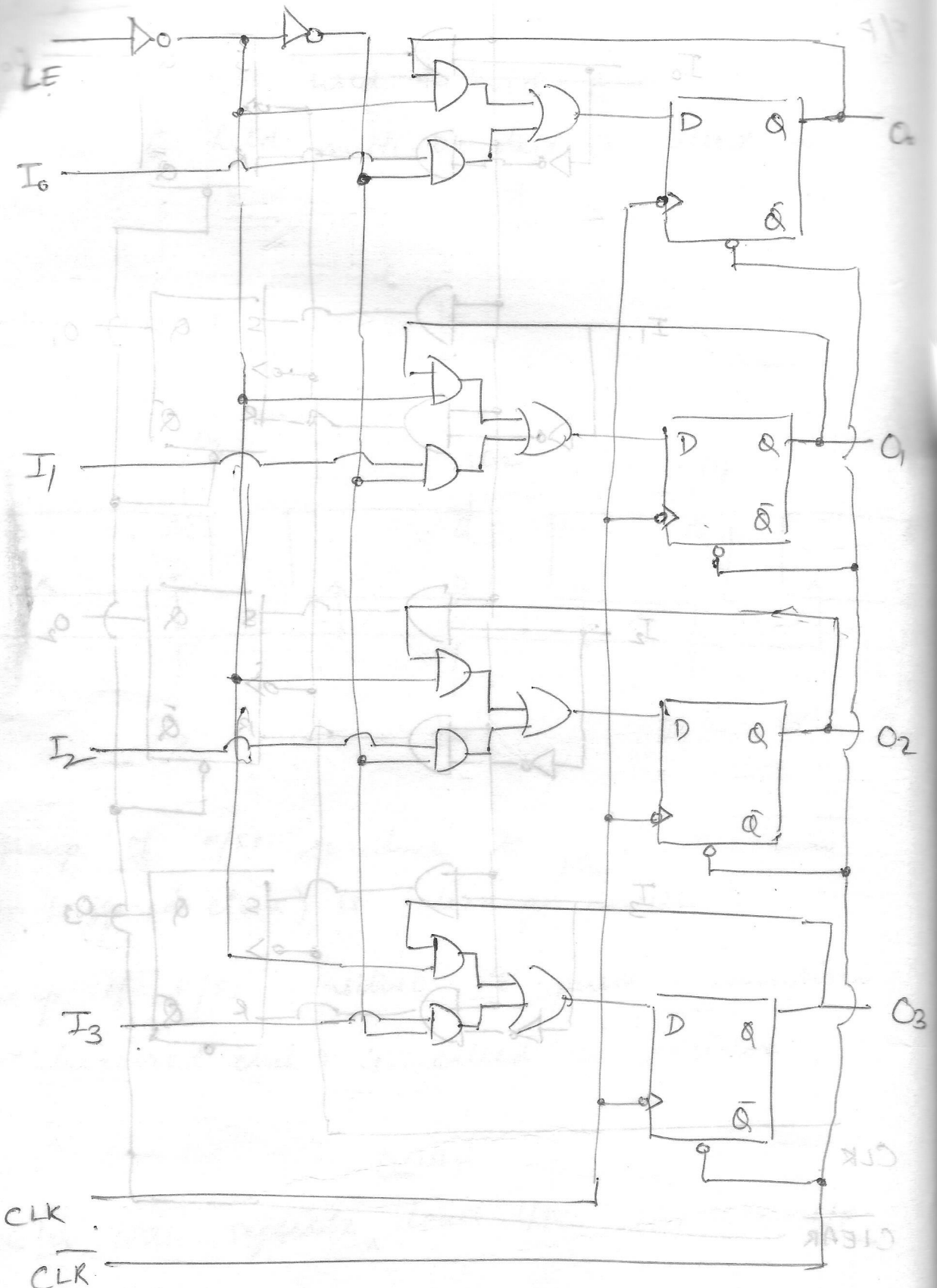
Register with separate parallel Load I/P using S/R F/F.

A

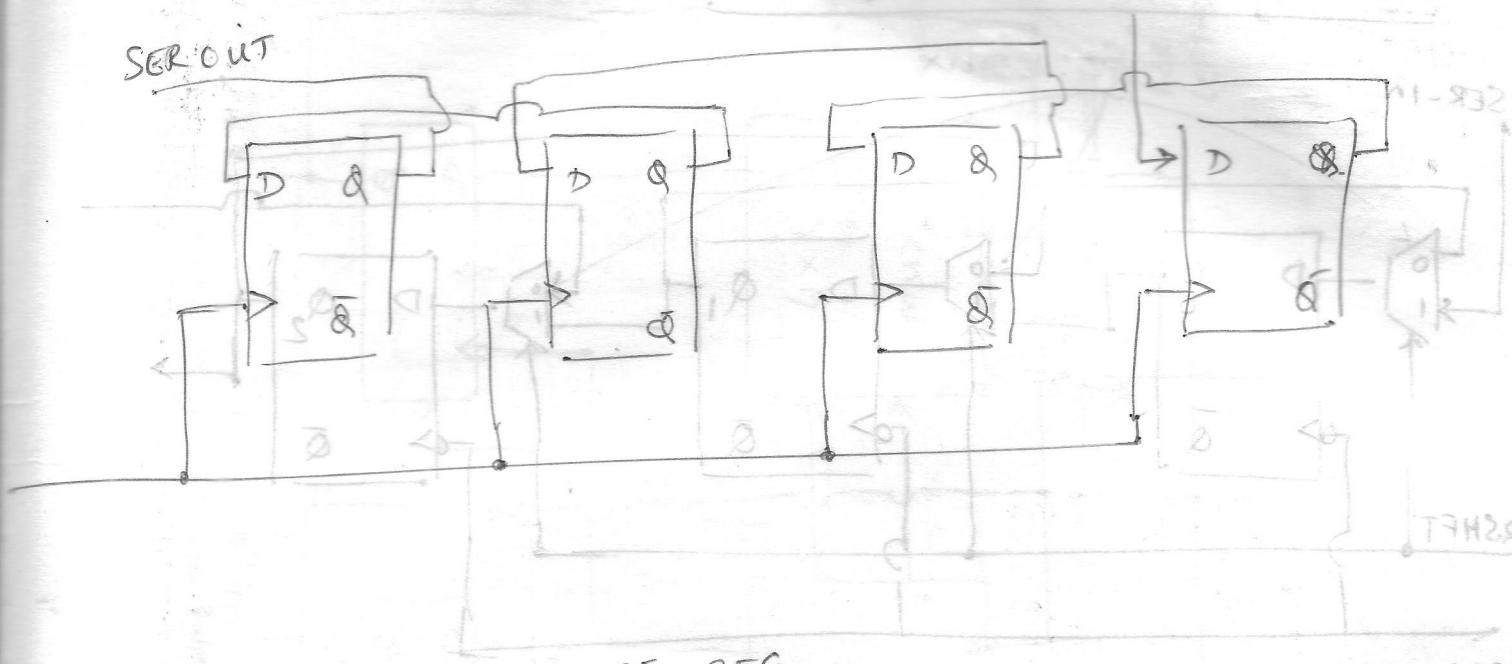
using S/R F/F.



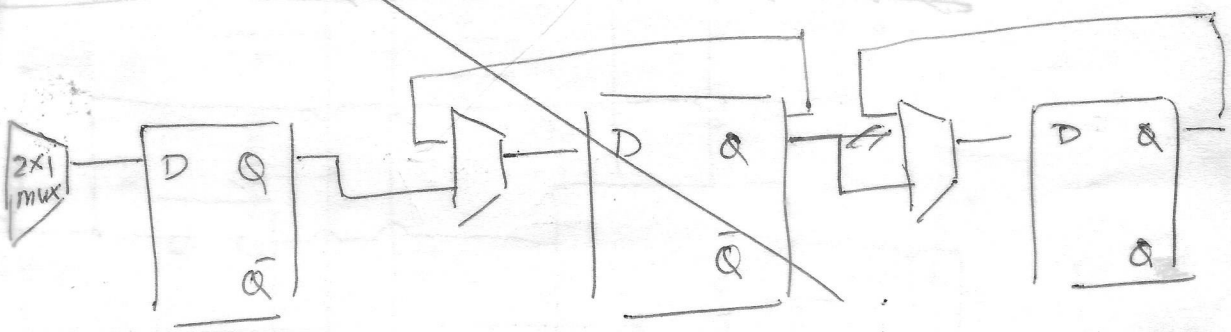
4 bit Register with LE using D F/F.



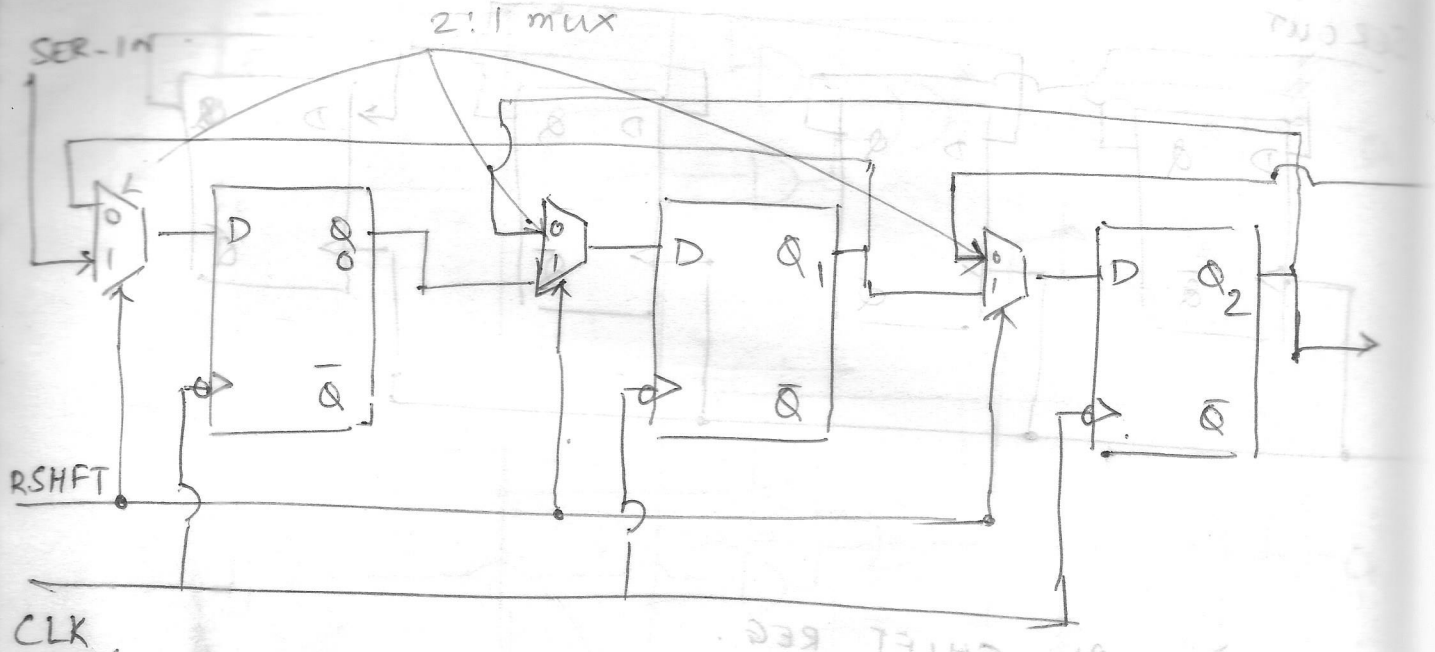
SHIFT LEFT.



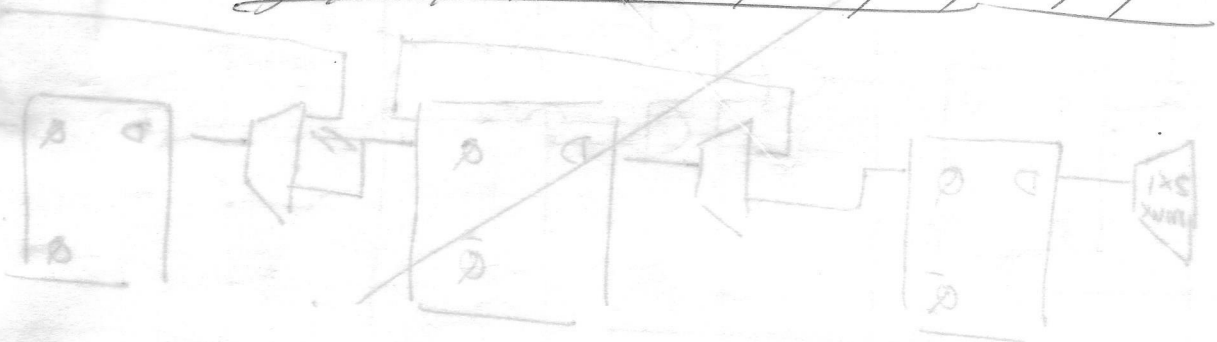
BIDIRECTIONAL SHIFT REG.



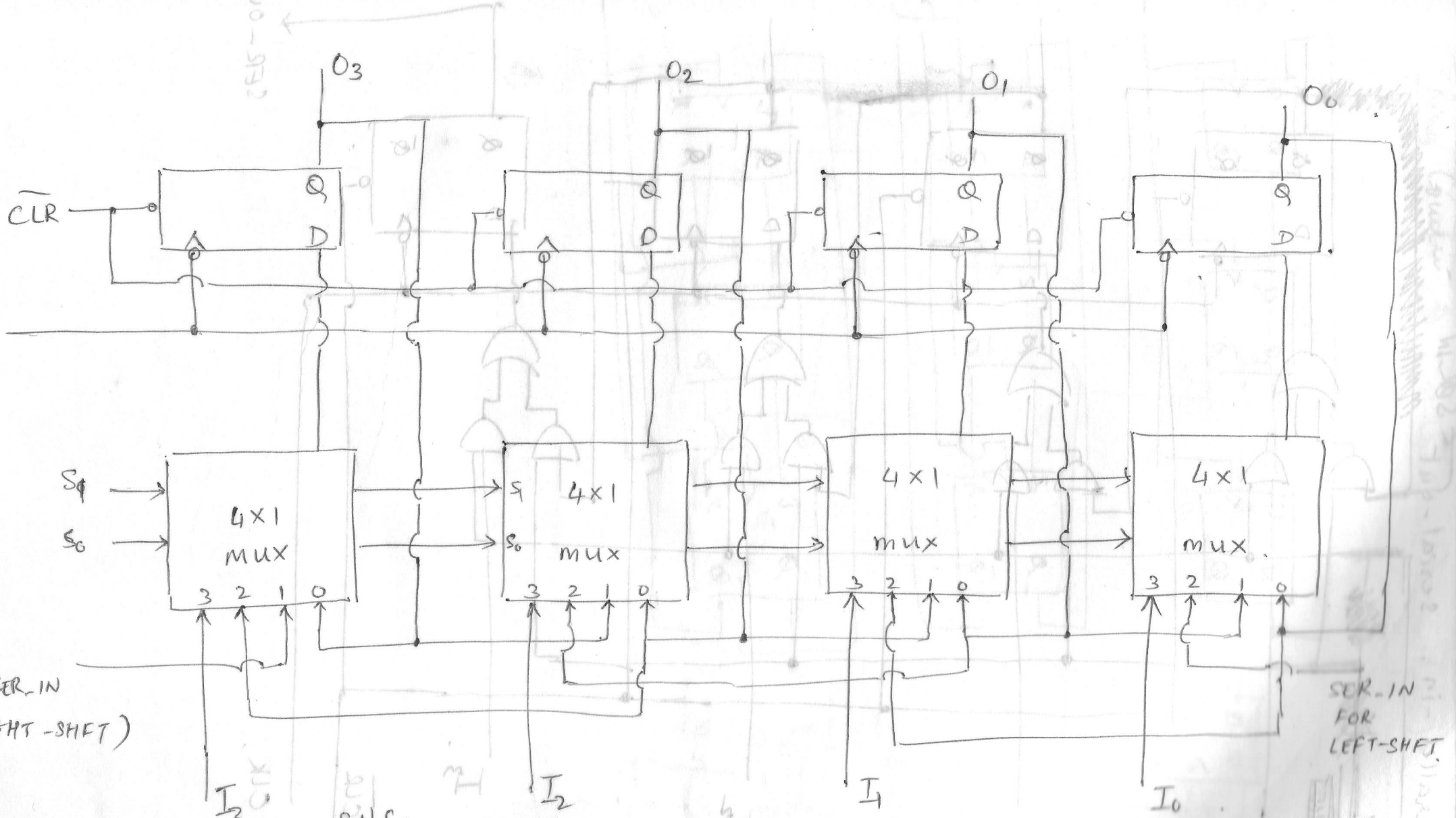
Bidirectional Shift Register



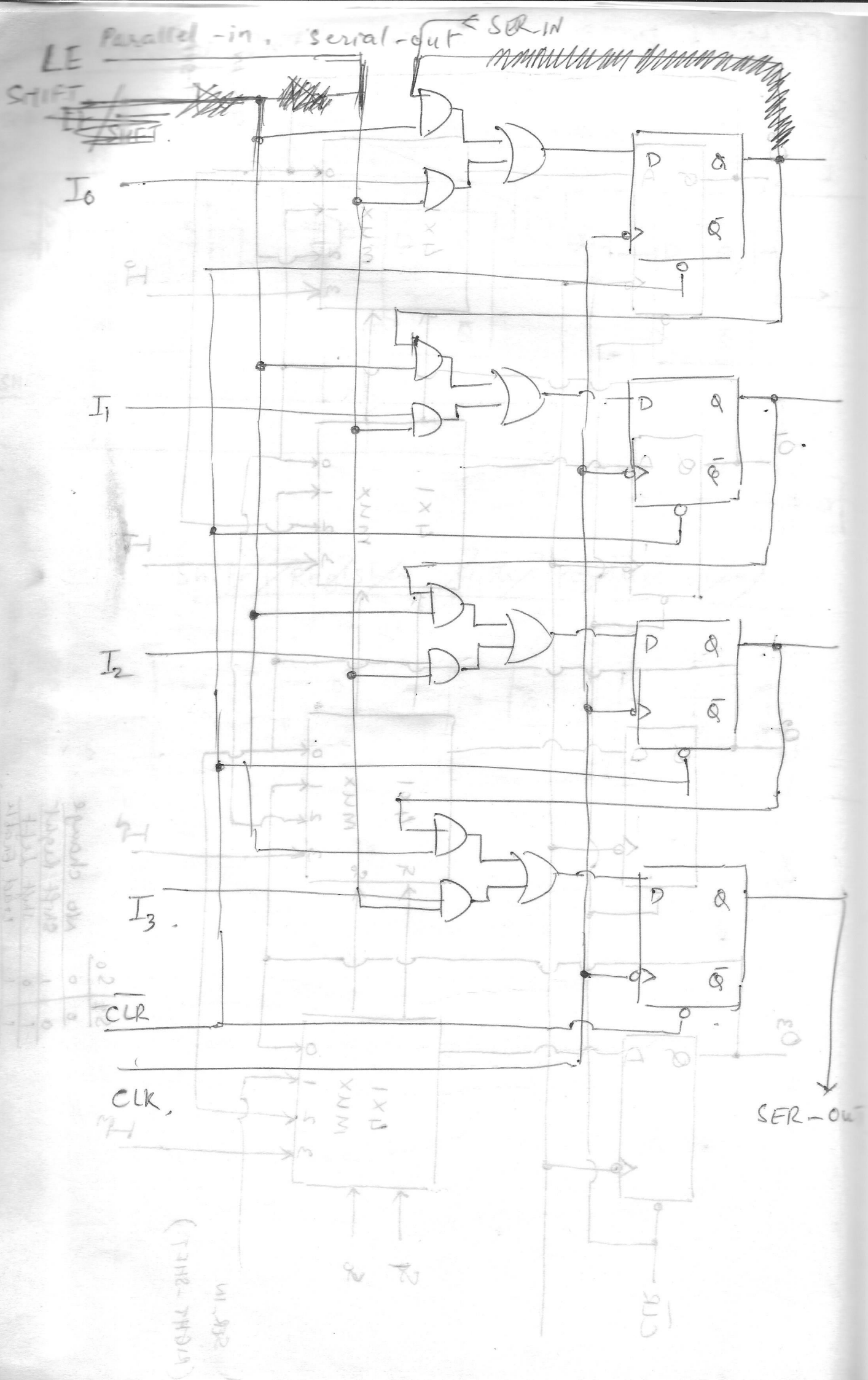
Shift Register with Parallel Load.



Bidirectional Shift Register with Parallel Load.



S_1	S_0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Load Enable


Parallel-in, Serial-out
SER_IN
LE
SHIFT
I_0
I_1
I_2
I_3
D
Q
$\bar{Q}$
$\overline{CLR}$
CLK
SER_OUT