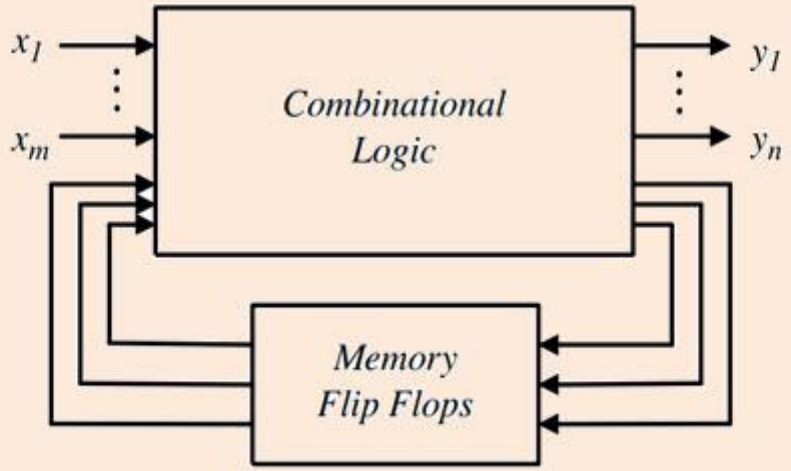
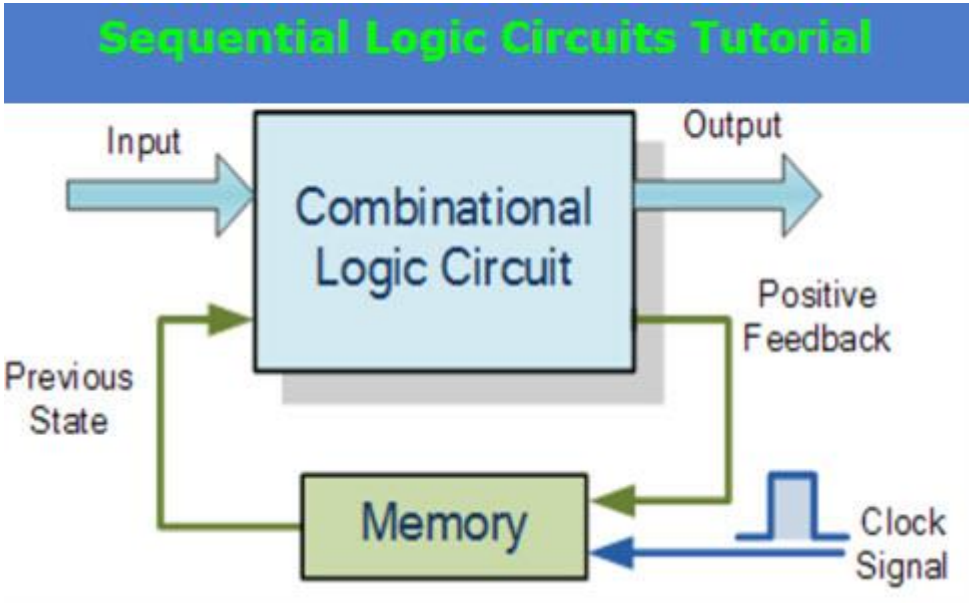
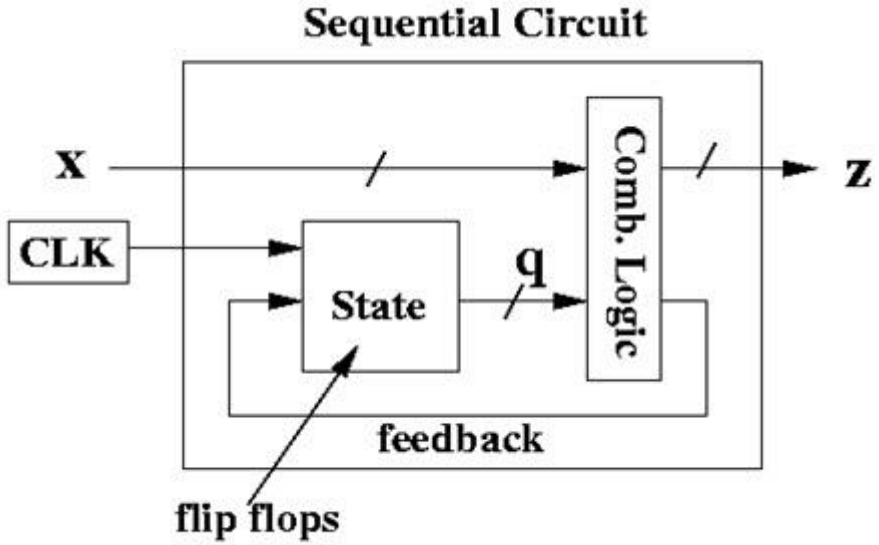
Sequential Circuits Basics

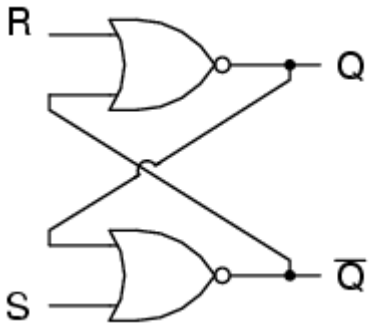



Sequential Logic Circuits Tutorial
Input
Combinational
Logic Circuit
Output
Positive
Feedback
Previous
State
Memory
Clock
Signal


Sequential Circuit
x
z
CLK
State
q
Comb. Logic
feedback
flip flops

LATCHES and FLIP-FLOPS

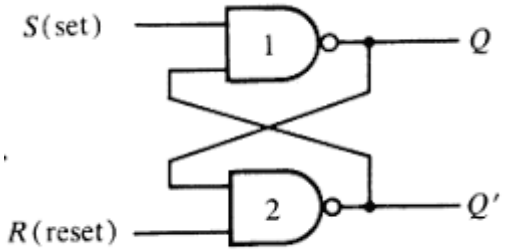
Basic RS Latch using NOR gates:



S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

Basic RS Latch using NAND gates:

- Here the inputs R and S are active low



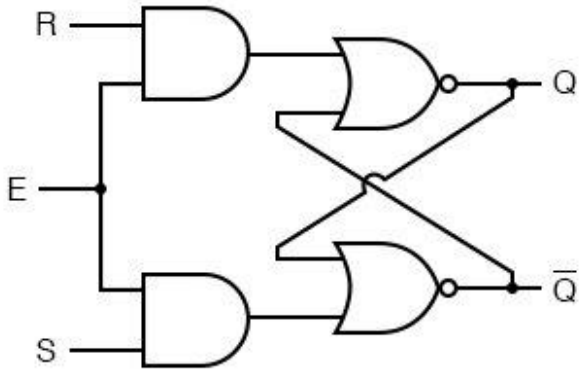
(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Truth table

Gated RS latch

Only when the E (enable signal) is 1 the changes in the inputs are transferred to the output.



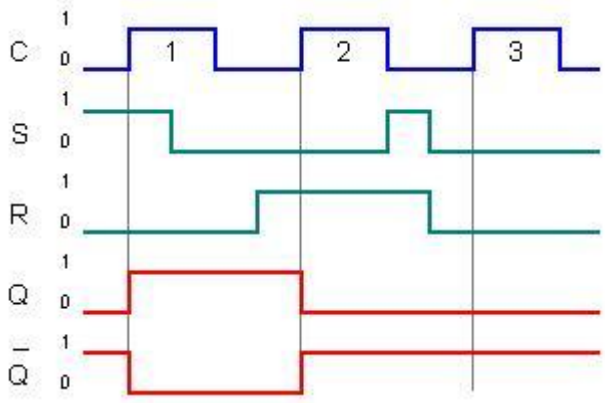
E	S	R	Q	$\overline{Q}$
0	0	0	latch	latch
0	0	1	latch	latch
0	1	0	latch	latch
0	1	1	latch	latch
1	0	0	latch	latch
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

SR Latch vs SR Flip-flop:

Usually a latch does not involve a clock; so the gated RS latch above is actually a

SR flip-flop.

Timing diagram for a SR flip-flop:

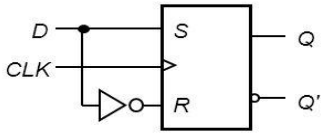


D FLIP-FLOP

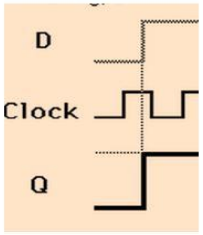
To avoid the illegal state in RS flip flop, we connect a NOT gate between

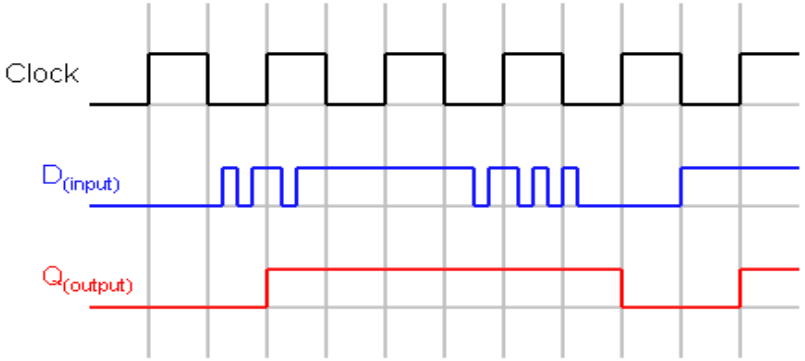
R and S inputs. That becomes a D flip flop.

Truth table D flip flop

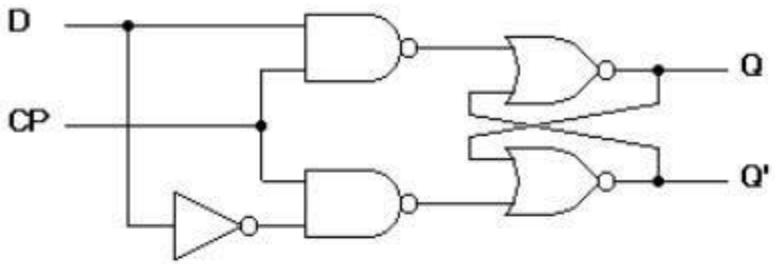


D	CLK	Q(t+1)	Comments
1	↑	1	Set
0	↑	0	Reset

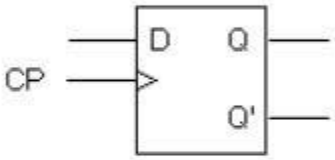




Circuit diagram of D flip flop:



(a) Logic diagram with NAND gates



(b) Graphical symbol

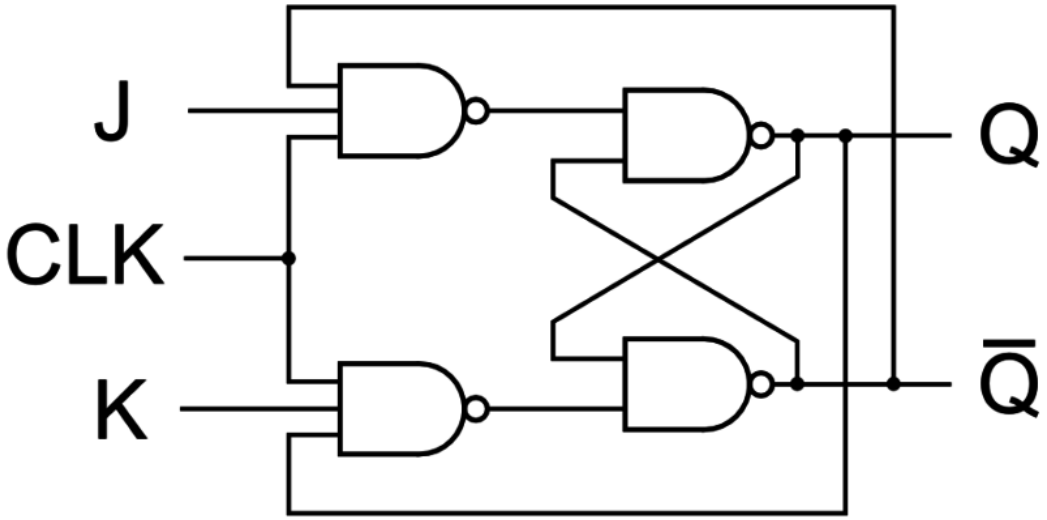
Q D	Q(t+1)
0 0	0
0 1	1
1 0	0
1 1	1

(c) Transition table

Clocked D flip-flop

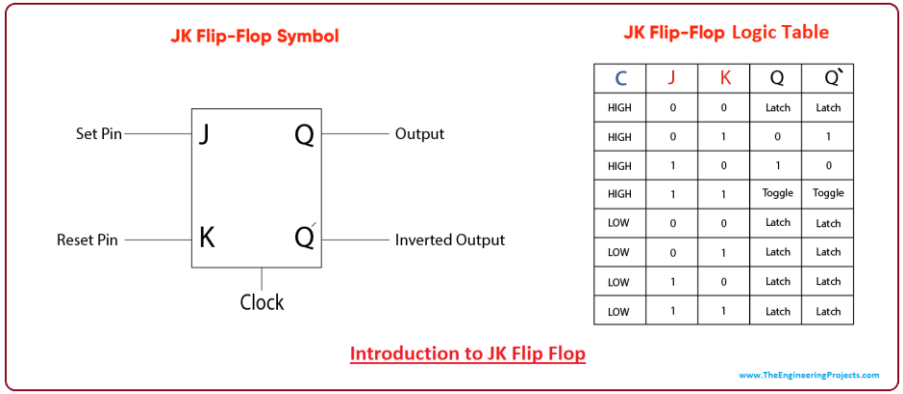
JK Flip-Flop:

- The JK flip-flop does not have any illegal state like SR FF.
- The JK flip-flop has two inputs J and K which make it more useful than a D FF.
- The JK flip-flop has a toggle mode similar to the T FF which is very useful to design counters and state machines.



Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)



C	J	K	Q	Q`
HIGH	0	0	Latch	Latch
HIGH	0	1	0	1
HIGH	1	0	1	0
HIGH	1	1	Toggle	Toggle
LOW	0	0	Latch	Latch
LOW	0	1	Latch	Latch
LOW	1	0	Latch	Latch
LOW	1	1	Latch	Latch

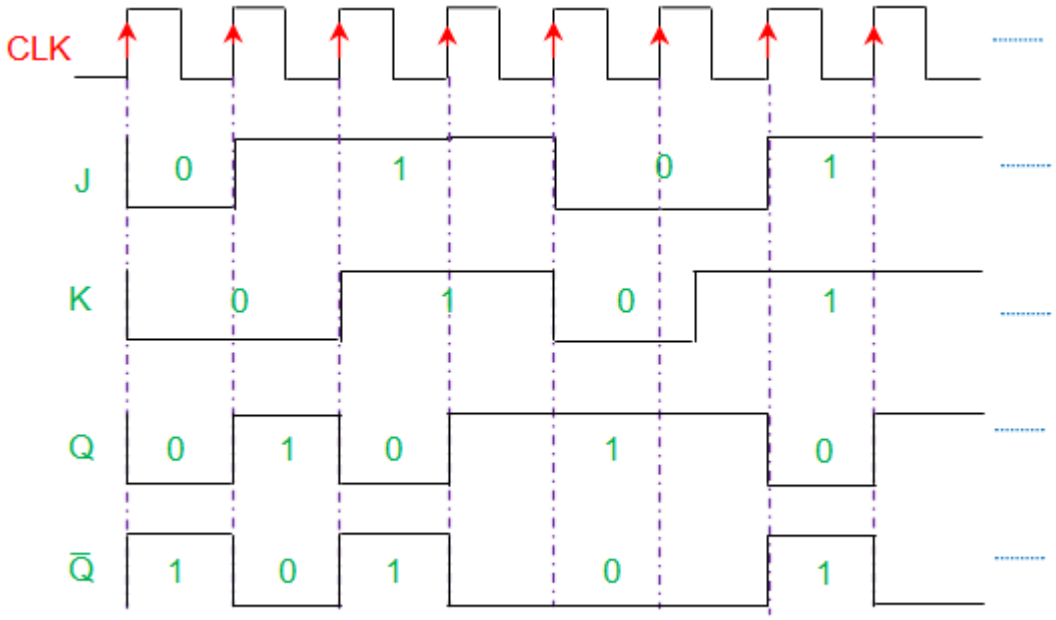
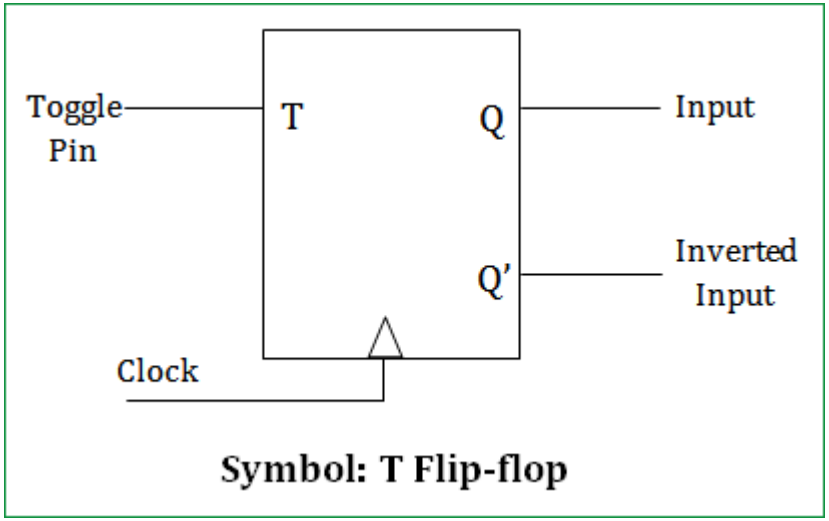


Figure 3 Timing diagram for positive edge-triggered JK flip-flop



Symbol: T Flip-flop

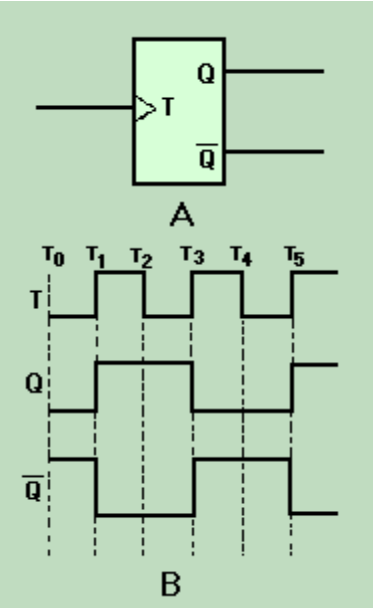
T Flip-Flop:

It has only one input T.

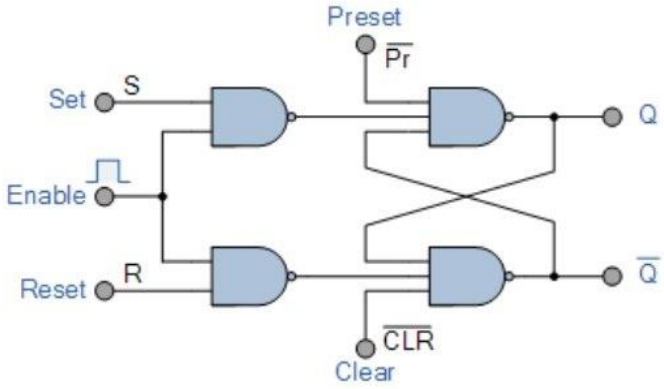
When T =0, no change in output.

When T=1, output reverses ($Q_{t+1} = \sim Q_t$)

T	Q	Q'
0	0	0
1	0	1
0	1	0
1	1	0



JK FF with Preset and Clear:



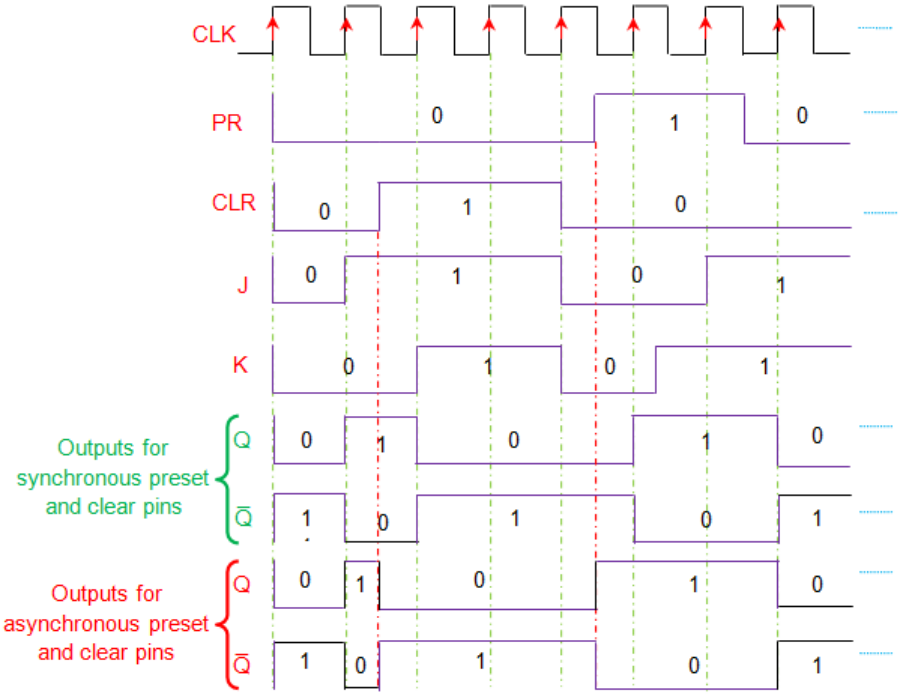
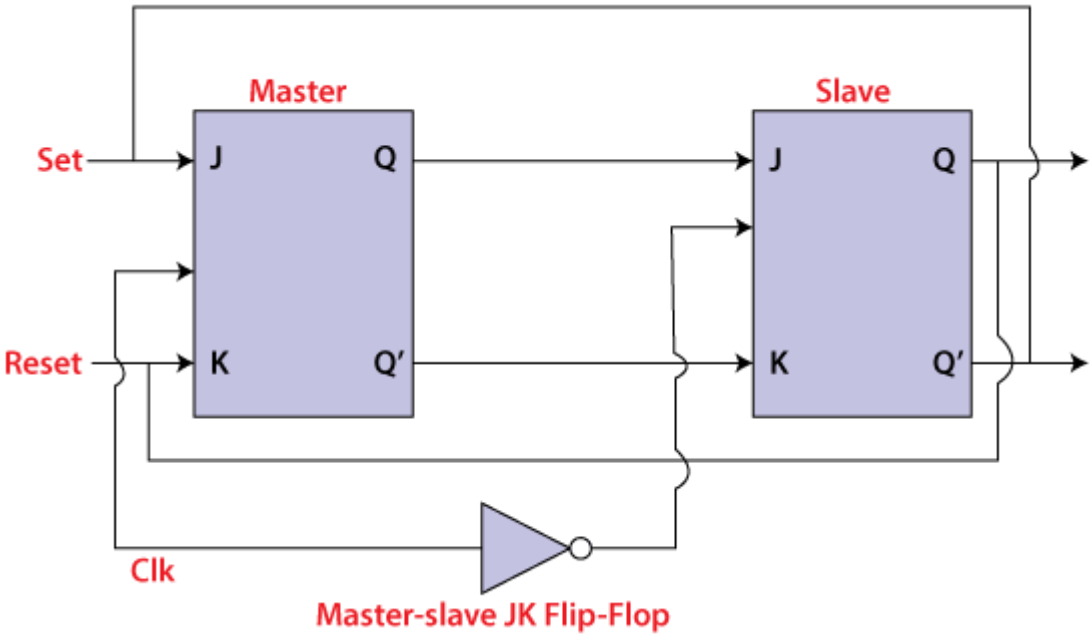


Figure 5 Waveforms for JK flip-flop with active high preset and clear inputs

JK Master-Slave FF:

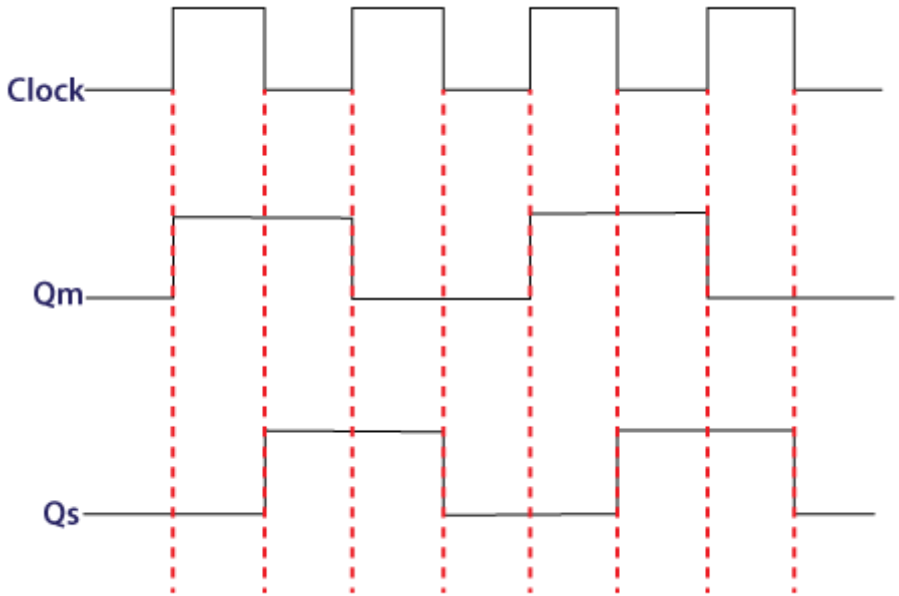


Working:

- When the clock pulse is true, the slave flip flop will be in the isolated state, and the system's state may be affected by the J and K inputs. The "slave" remains isolated until the CP is 1. When the CP set to 0, the master flip-flop passes the information to the slave flip flop to obtain the output.
- The master flip flop responds first from the slave because the master flip flop is the positive level trigger, and the slave flip flop is the negative level trigger.
- The output Q'=1 of the master flip flop is passed to the slave flip flop as an input K when the input J set to 0 and K set to 1. The clock forces the slave flip flop to work as reset, and then the slave copies the master flip flop.
- When J=1, and K=0, the output Q=1 is passed to the J input of the slave. The clock's negative transition sets the slave and copies the master.

- The master flip flop toggles on the clock's positive transition when the inputs J and K set to 1. At that time, the slave flip flop toggles on the clock's negative transition.
- The flip flop will be disabled, and Q remains unchanged when both the inputs of the JK flip flop set to 0.

Timing Diagram of a Master Flip Flop:



- When the clock pulse set to 1, the output of the master flip flop will be one until the clock input remains 0.
- When the clock pulse becomes high again, then the master's output is 0, which will be set to 1 when the clock becomes one again.
- The master flip flop is operational when the clock pulse is 1. The slave's output remains 0 until the clock is not set to 0 because the slave flip flop is not operational.
- The slave flip flop is operational when the clock pulse is 0. The output of the master remains one until the clock is not set to 0 again.
- Toggling occurs during the entire process because the output changes once in the cycle.

Truth Table: A Truth table shows how a logic circuits output responds to various combination of inputs.

Characteristics Table: it defines the next state of flip-flop in terms of flip-flop input and current state.

Excitation Table:it defines the flip-flop input variable as function of the current state and next state.

Table 1. Flip-flop Types

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE
SR	S Q, Clk, R Q'	S R Q(next): 0 0 Q; 0 1 0; 1 0 1; 1 1 ?	$Q_{(next)} = S + R'Q$; $SR = 0$	Q Q(next) S R: 0 0 0 X; 0 1 1 0; 1 0 0 1; 1 1 X 0
JK	J Q, Clk, K Q'	J K Q(next): 0 0 Q; 0 1 0; 1 0 1; 1 1 Q'	$Q_{(next)} = JQ' + K'Q$	Q Q(next) J K: 0 0 0 X; 0 1 1 X; 1 0 X 1; 1 1 X 0
D	D Q, Clk, Q'	D Q(next): 0 0; 1 1	$Q_{(next)} = D$	Q Q(next) D: 0 0 0; 0 1 1; 1 0 0; 1 1 1
T	T Q, Clk, Q'	T Q(next): 0 Q; 1 Q'	$Q_{(next)} = TQ' + T'Q$	Q Q(next) T: 0 0 0; 0 1 1; 1 0 1; 1 1 0

Each of these flip-flops can be uniquely described by its graphical symbol, its characteristic table, its characteristic equation or excitation table. All flip-flops have output signals Q and Q'

(Bigger Image uploaded as a separate file).

Inputs		Outputs	
		Present State	Next State
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

Truth Table of SR Flip-Flop

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table of SR Flip-Flop

Inputs		Outputs	
		Present State	Next State
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table of JK Flip-Flop

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table of JK Flip-Flop

Input	Outputs	
	Present State	Next State
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth Table of D Flip-Flop

Outputs		Input
Present State	Next State	
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

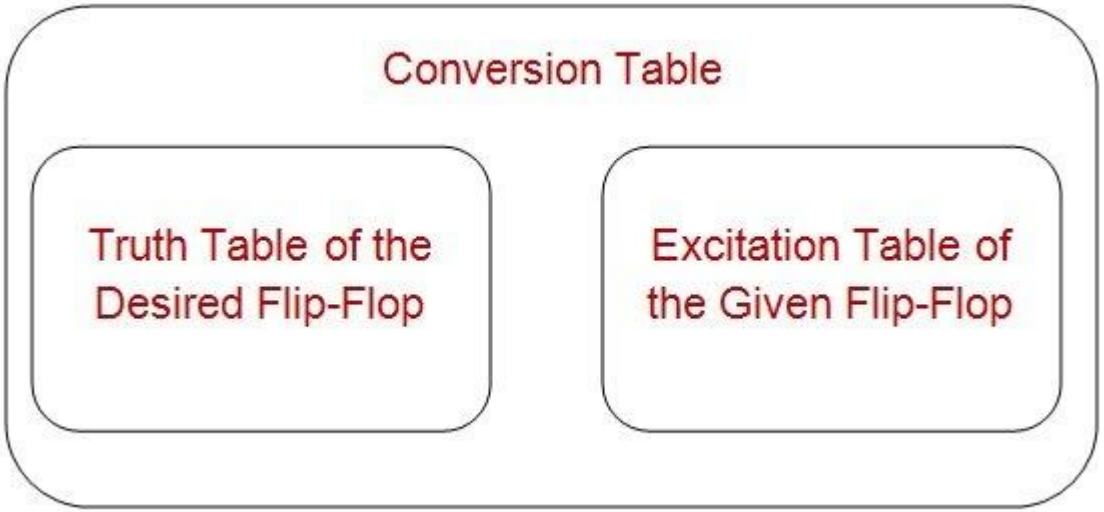
Excitation Table of D Flip-Flop

Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table of T Flip-Flop

Outputs		Input
Present State	Next State	
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table of T Flip-Flop



Truth Table of D Flip-flop

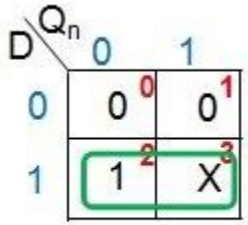
Input	Outputs	
	Present State	Next State
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

D Input	Outputs		SR Inputs	
	Present State	Next State		
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

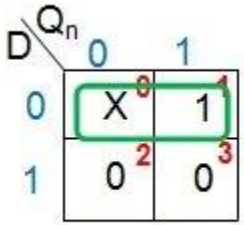
Excitation Table of SR Flip-flop

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

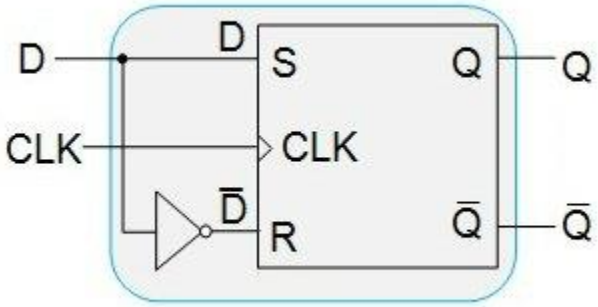
SR to D Conversion Table



S = D



R = $\overline{D}$



Conversion of D flip-flop to JK Flip flop

Step1: Write the characteristic table of the desired FF (JK)

Step2: Excitation table for given flip flop (D)

Step3: Combine the two and draw K map

J	K	Q	Q+1	D
0	0	0	0	0
0	0	0	0	0
0	1	0	0	0
0	1	0	0	0
1	0	0	1	1
1	0	1	1	1
1	1	1	0	0
1	1	0	1	0

D = K’Q + JQ’

0	1	0	0
1	1	0	1

$D = K'Q + JQ'$