Experiment No. 6

Title: To verify the characteristic table of D F/F, JK F/F and T F/F

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Experiment No.: 6

Aim: To verify the characteristic table of the following flip-flops:- D, JK and T.

Resources needed: Simulation Platform (Online Circuitverse Simulator)

Theory:

Theory: "Flip-flop" is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

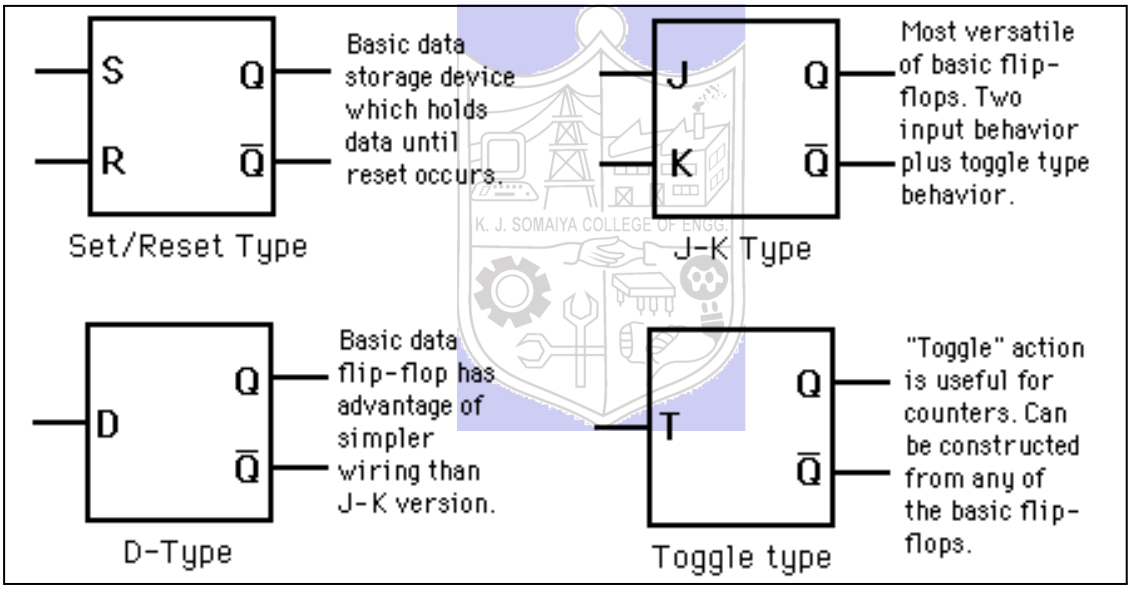


Fig: Types of Flip-flops

Set-Reset FlipFlop:

The set/reset type flip-flop is triggered to a high state at Q by the "set" signal and holds that value until reset to low by a signal at the Reset input. This can be implemented as a NAND gate latch or a NOR gate latch and as a clocked version.

One disadvantage of the S/R flip-flop is that the input S=R=1 gives ambiguous results and must be avoided. The J-K flip-flop gets around that problem.

JK FlipFlop:

JK-flip flop has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

D FlipFlop:

D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate as shown in fig.

T FlipFlop:

T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

Table: Characteristic table and Excitation Table of flipflops

FlipFlop name	Characteristic Table			Characteristic Equation	Excitation Table			
SR	S	R	Qnext		Q	Qnext	S	R
	0	0	Q_n	Qnext= S+R'Q	0	0	0	X
	0	1	0		0	1	1	0
	1	0	1		1	0	0	1
	1	1	Invalid	Where SR=0	1	1	X	0
JK	J	K	Qnext		Q	Qnext	J	K
	0	0	Q_n	Qnext= JQ'+K'Q	0	0	0	X
	0	1	0		0	1	1	X
	1	0	1		1	0	X	1
	1	1	Q_n'		1	1	X	0
D	D		Qnext		Q	Qnext	D	
	0		0	Qnext=D	0	0	0	
	1		1		0	1	1	
					1	0	0	
					1	1	1	
T	T		Qnext		Q	Qnext	T	
	0		Q_n	Qnext= TQ'+T'Q	0	0	0	
	1		Q_n'		0	1	1	
					1	0	1	
					1	1	0	

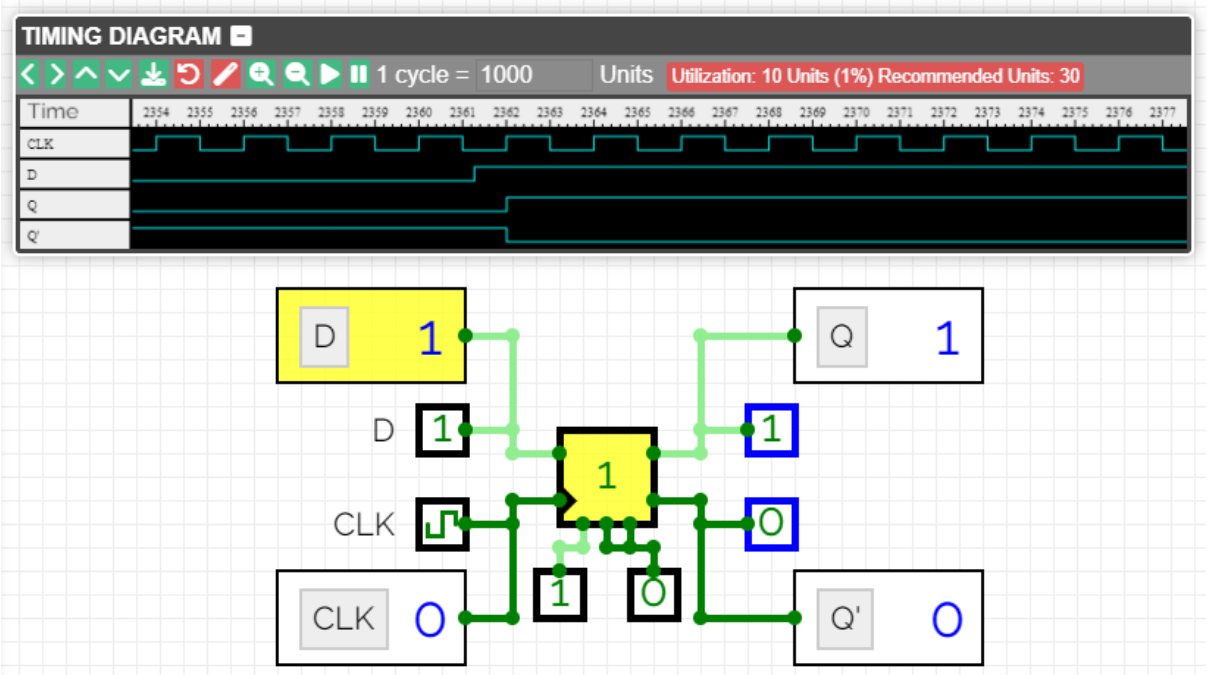
Procedure:

a) Login into your Circuitverse account
b) Open a new project and label it.
c) Draw the circuit diagram for the D Flip-flop. Label the inputs and outputs correctly.
d) Toggle the CLK signal manually for D=0 and D=1 and check if the output changes as expected.
e) Now connect the CLK signal generator (under Sequential elements)
f) Connect Flags (under MISC components) to CLK , D and Q so that the timing diagram window will be automatically activated.
g) Change values of D input and observe changes in the output.
h) Write the testbench and Verify it. Then export the testbench as an xls file.
i) Take a snapshot showing all tests passing.
j) Repeat steps c to i for JK and T flip-flops.
k) Then complete the writeup and upload it

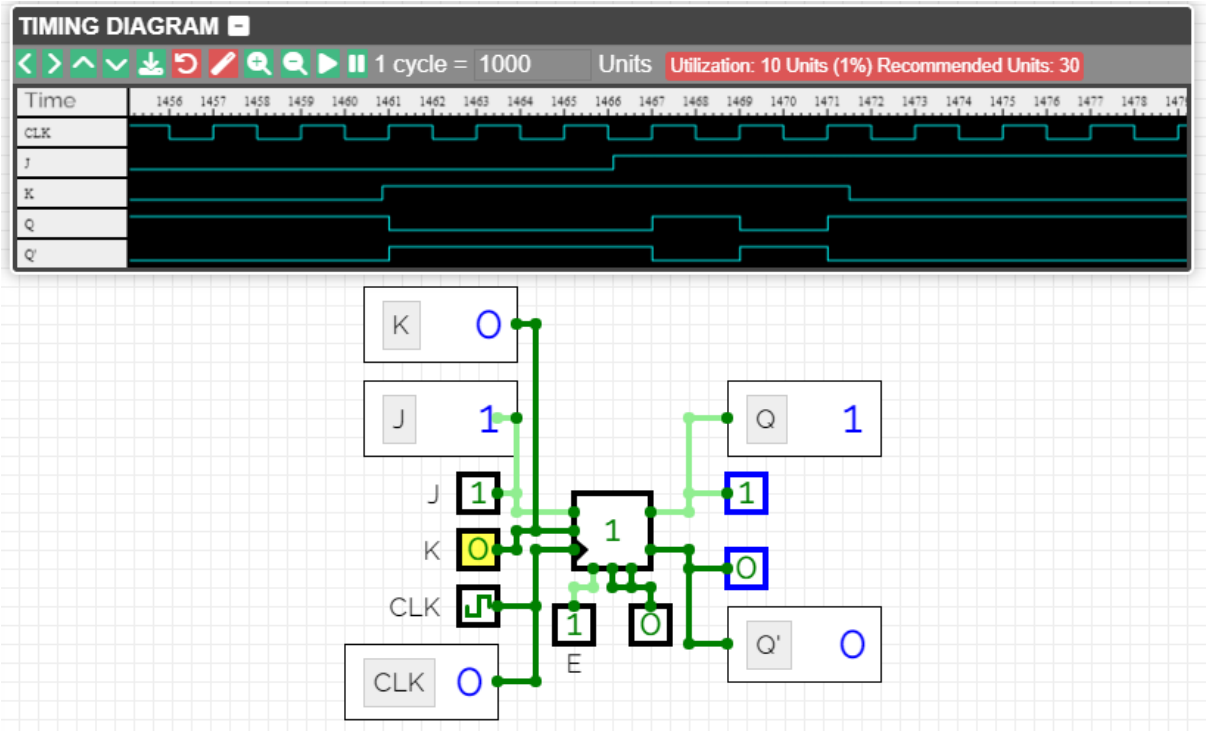
Observations and Results:

1. Complete the Characteristic table for D, JK and T flip flop given above.
2. Paste the circuit diagram, testbench and output snapshots below:
3. COPY-PASTE your files here:-

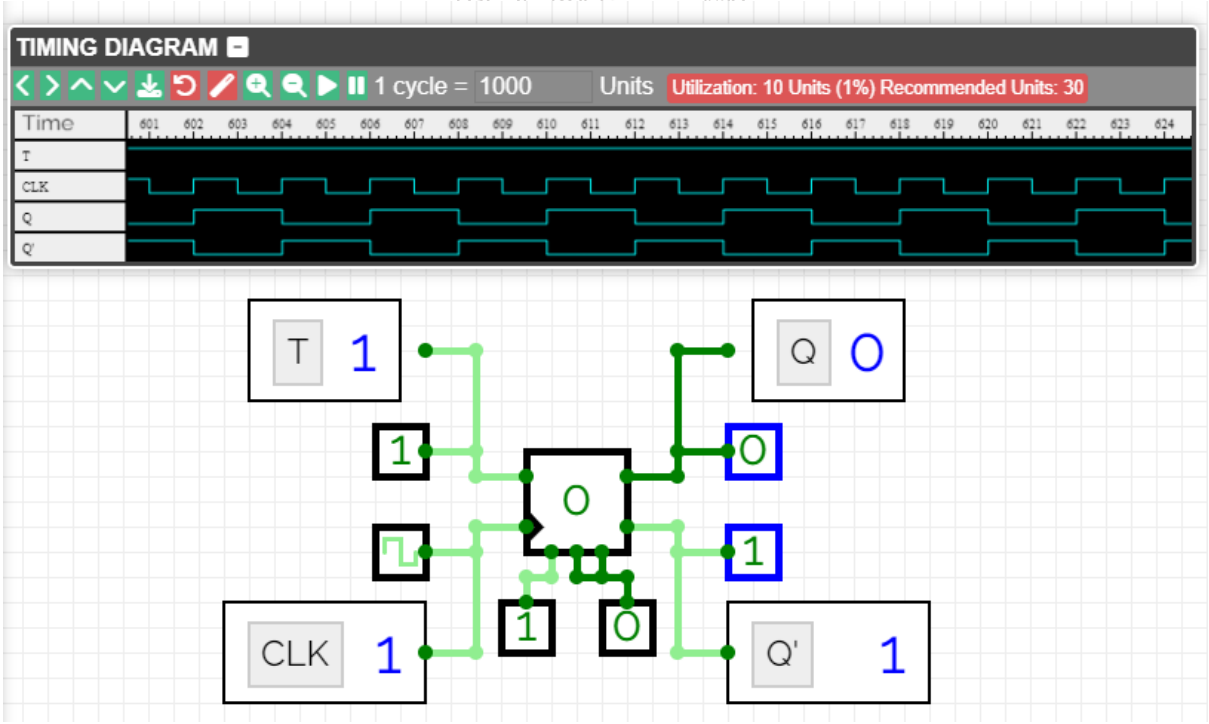
D-Flip Flop



JK-Flip Flop



T-Flip Flop



Outcomes: Design the combinational and sequential circuits using basic building blocks.

Conclusion:
We could successfully verify the characteristic tables and excitation tables of D, JK and T Flip Flops.

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.
2. http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/flipflop.html