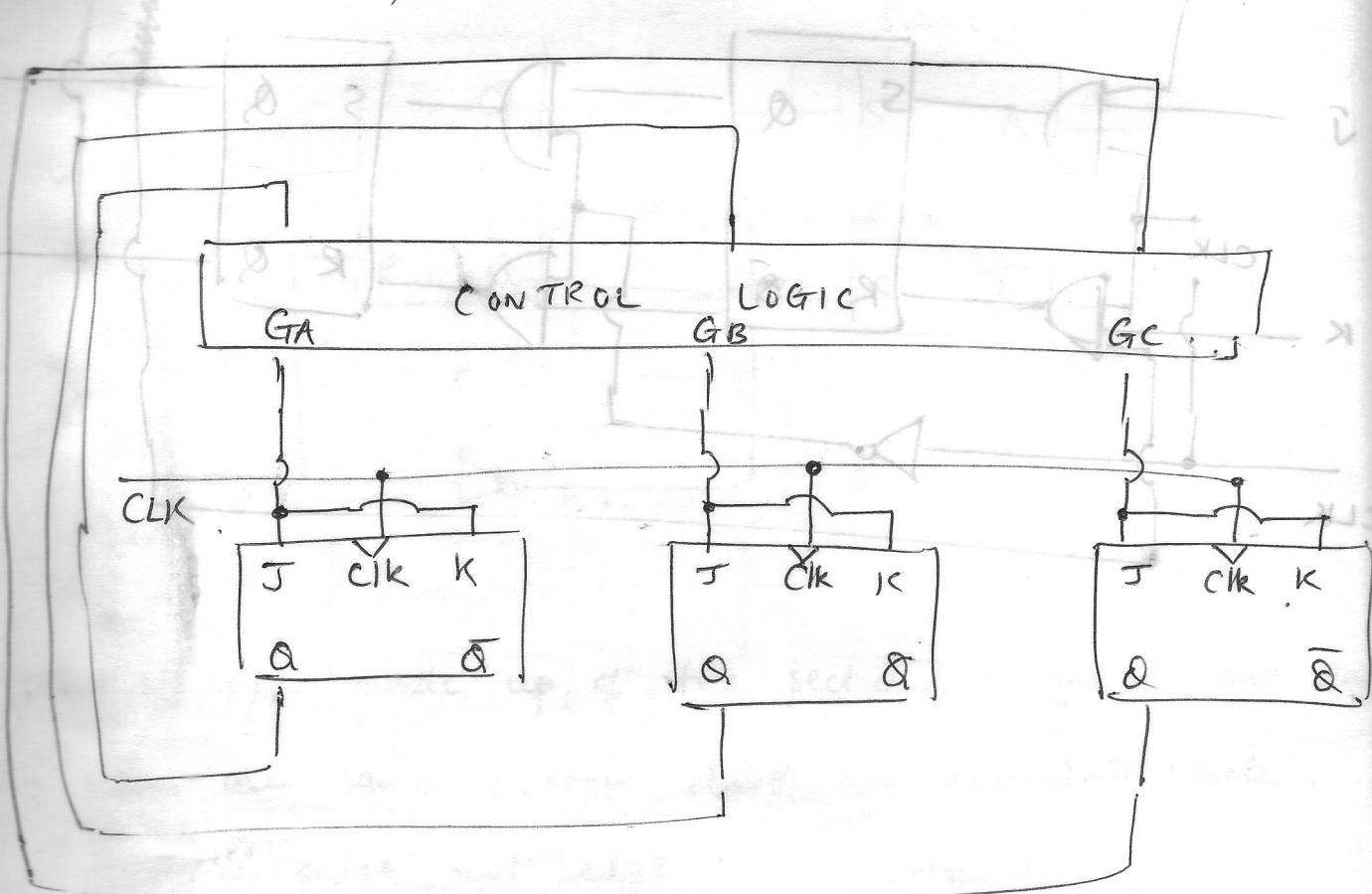


Synchronous Counters Using T/F/F (x2) 712 21m

General Principle:

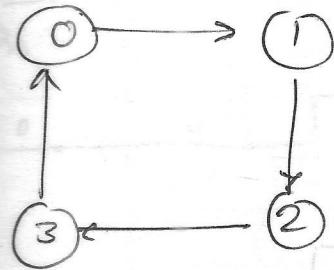


* Synchronous Counter

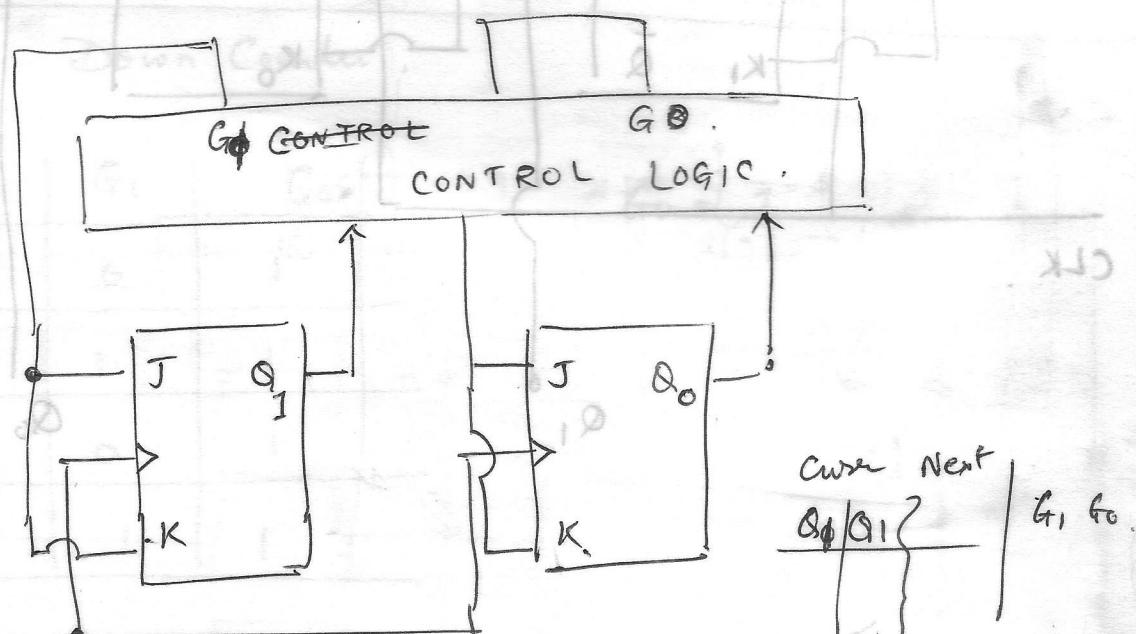
- clk is common to all F/Fs; unlike ripple count
- J-K ips are tied together but not to 'I', instead to a control logic.
- all outputs change simultaneously.

Design a synchronous a_0-3 counter.

(a) State Diagram.



(b)



CLK.

	Q1	Q0
Q1	0	1
Q0	0	0

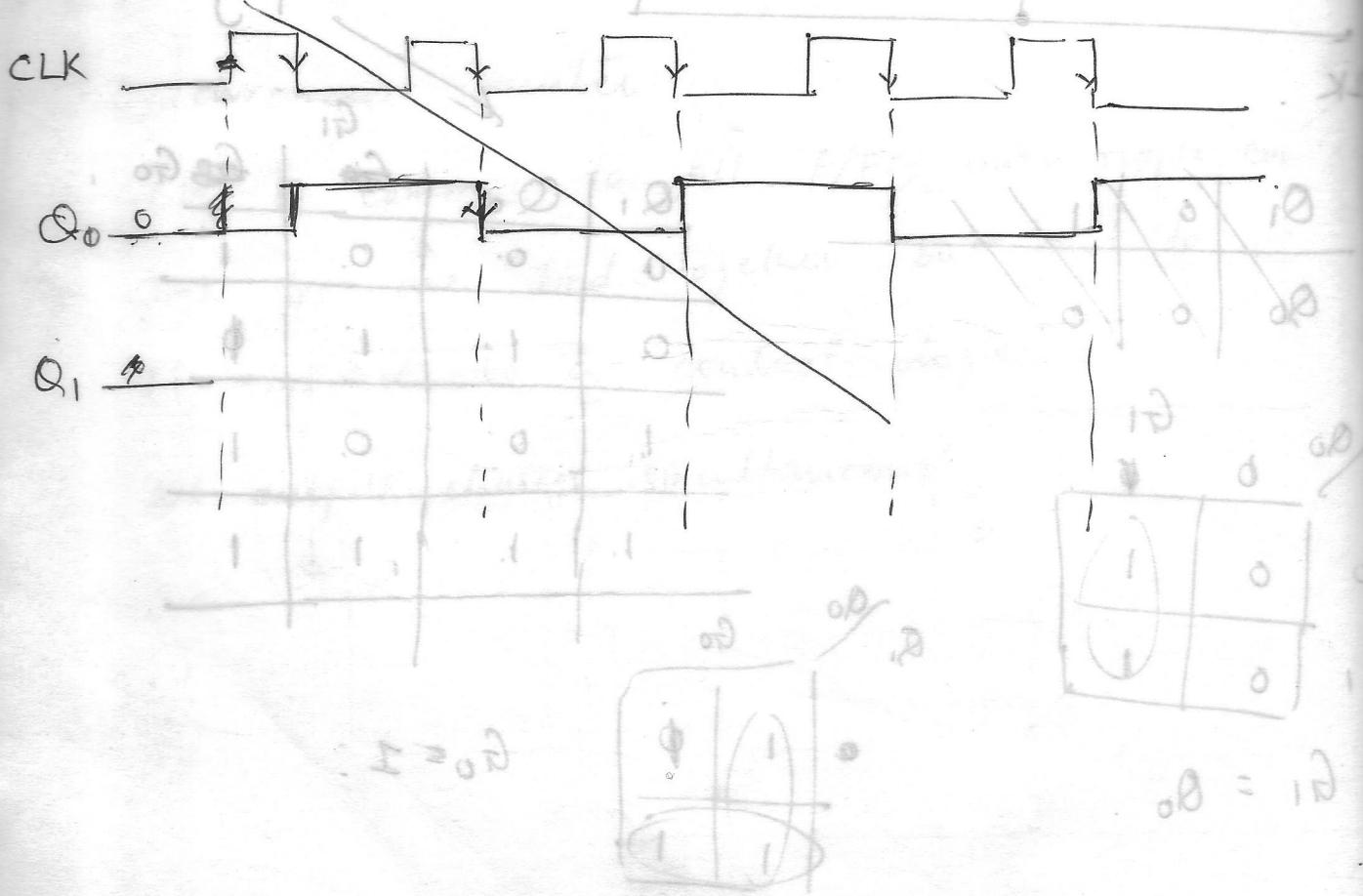
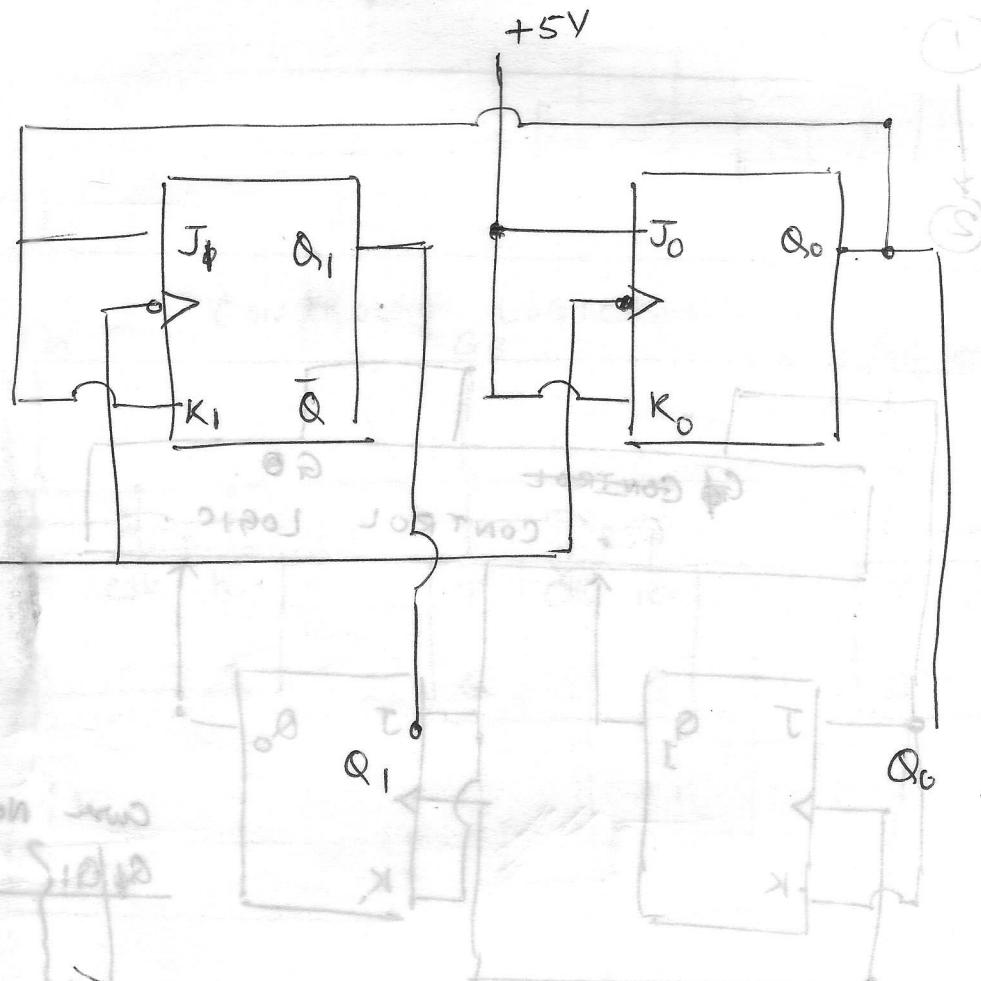
	Q1	Q0	G1	G0
Q1	0	0	0	1
Q0	1	1	1	0
Q1	1	0	0	1
Q0	1	1	1	1

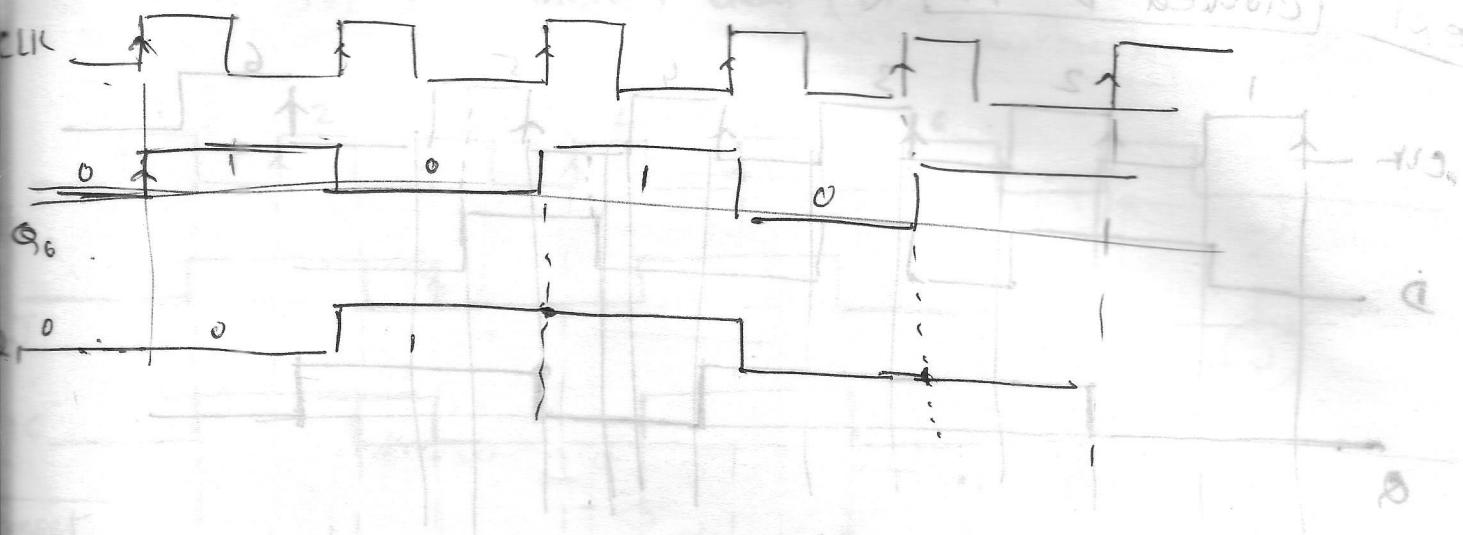
	Q1	Q0
Q1	0	1
Q0	0	1

$$G_1 = Q_0.$$

	Q1	Q0
Q1	1	0
Q0	1	1

$$G_0 = 1.$$

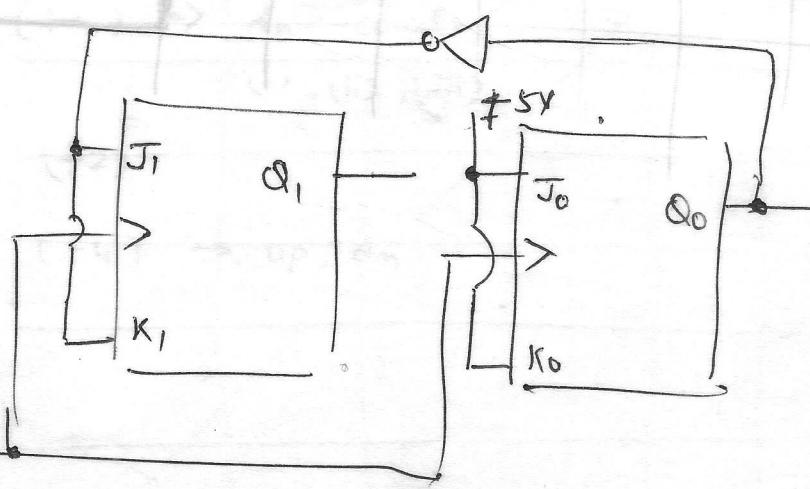
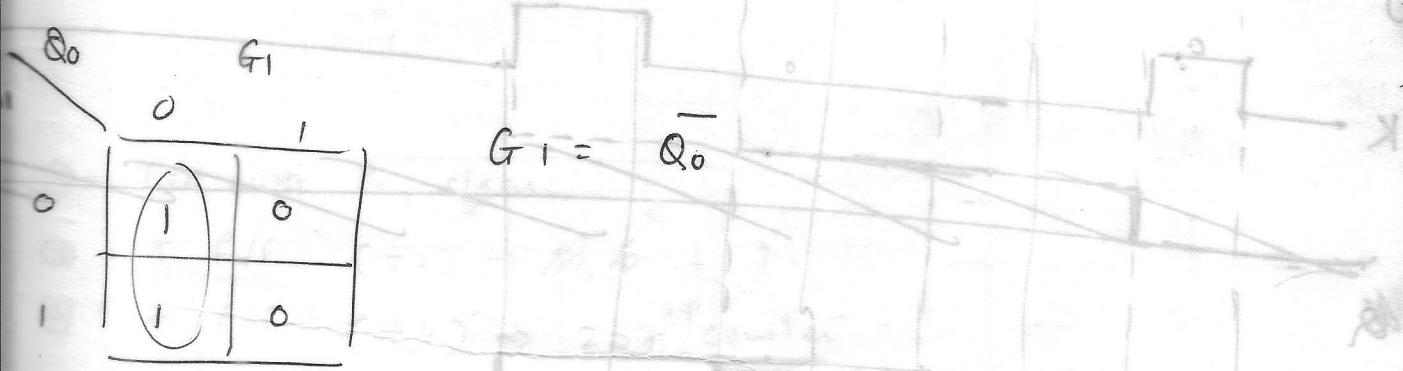




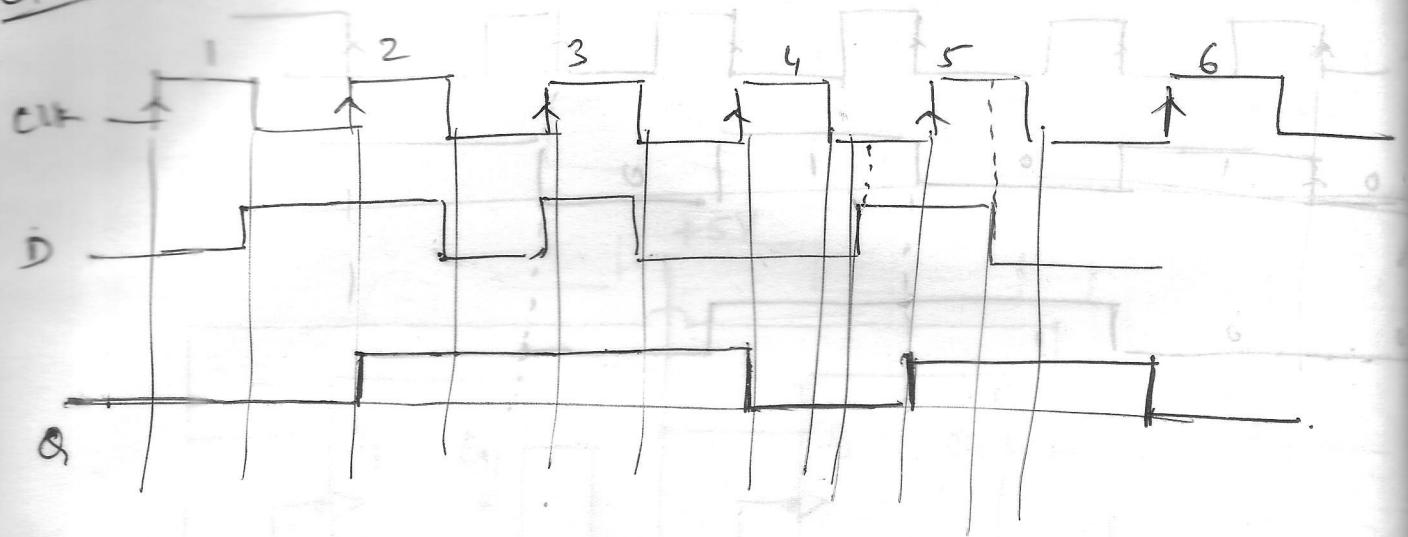
Synchronous Down Counter.

Q_1	Q_0	G_1	G_0
1	1	0	1
1	0	1	1
0	1	0	1
0	0	1	1

$$G_0 = 1$$



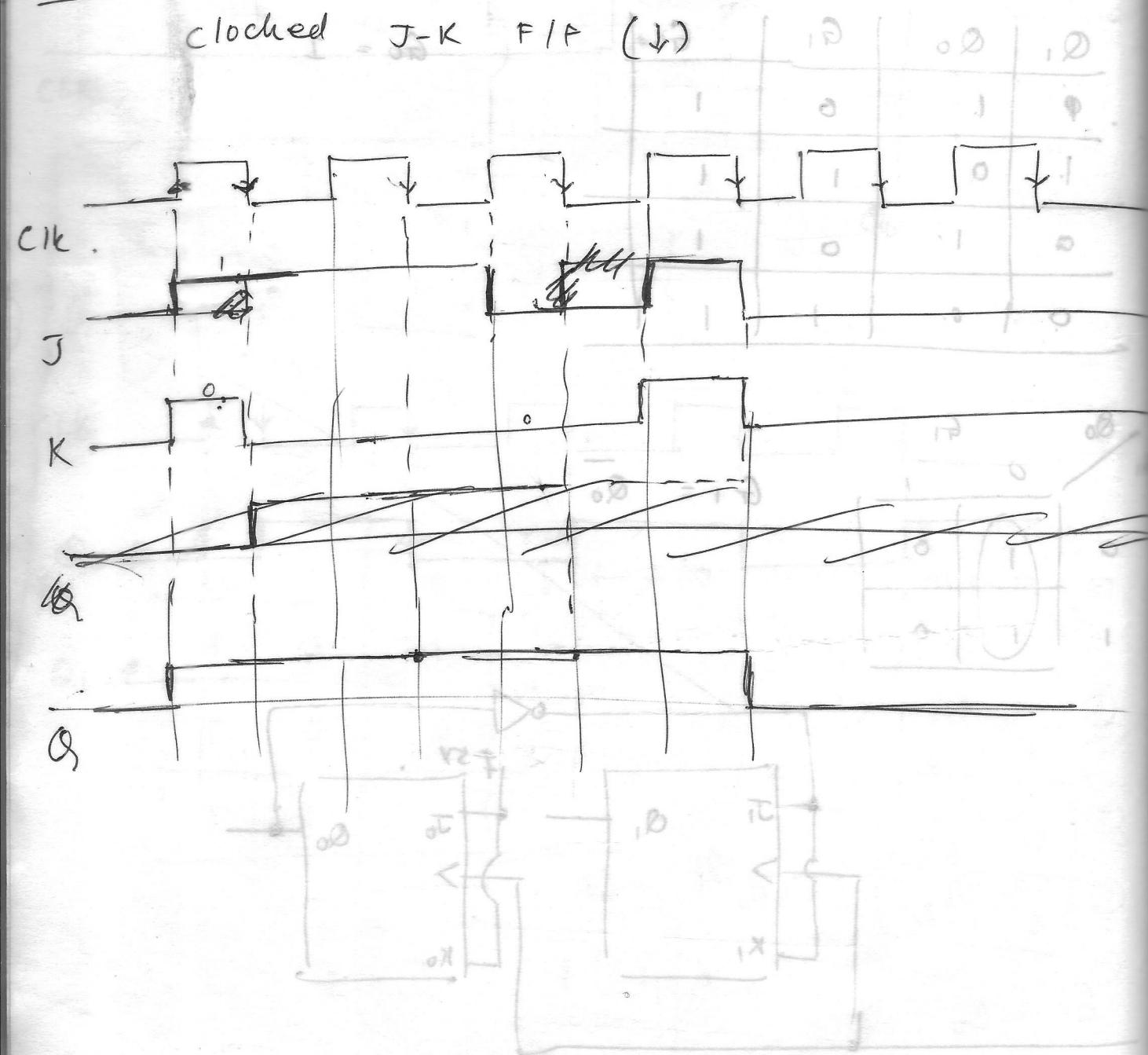
ex1 | clocked D F/F, (\uparrow)



ex2

clocked J-K F/F (\downarrow)

Timing diagram for a clocked J-K flip-flop

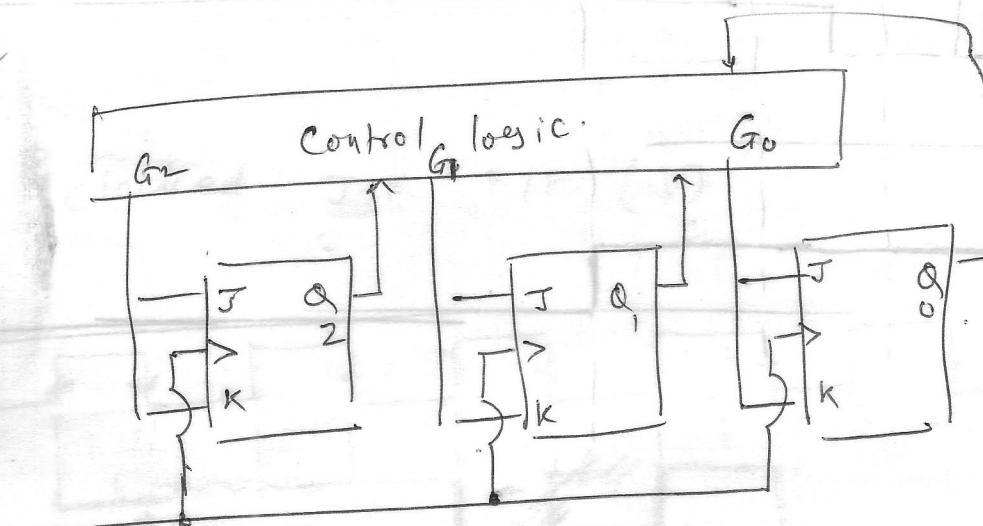
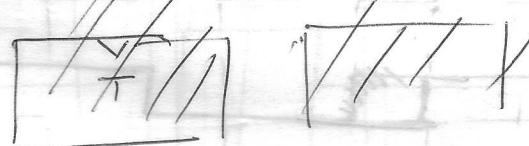
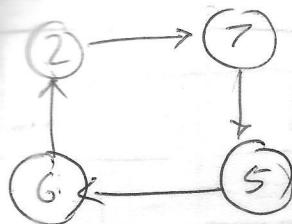


JK F/F with Preset, clear (\uparrow)



- ① J/K with Pr, clear.
- ② T F/F $(\frac{1}{2}) \rightarrow$ ~~Pr, Cl, t, ↑~~.
- ③ T F/F $(\frac{1}{4}) \rightarrow$ 2 bit ^{up} counter.
- ④ T F/F $(\frac{1}{4}) \rightarrow$ dn -counter
(i), (ii), (iii).
- ⑤ D F/F $(\frac{1}{2})$
- ⑥ D F/F $(\frac{1}{4}) \rightarrow$ up, dn.
- ⑦ .

non sequential Counting (sequence Generator)



CLK

Q_2	Q_1	Q_0	G_2	G_1	G_0
0	0	0	*	*	*
0	0	1	*	*	*
0	1	0	1	0	1
0	1	1	*	*	*
1	0	0			
1	0	1			
1	1	0			
1	1	1	0	1	0

>5

Q_2	Q_1	Q_0	G_2	G_1	G_0	$(Q_2 \oplus Q_1 \oplus Q_0)$
0	0	0	x	x	x	
1	1	1	x	x	x	
0	1	1	x	x	x	
1	0	0	x	x	x	
1	0	1	0	1	1	
1	1	0	1	0	0	
1	1	1	0	1	1	

$010 \rightarrow 111$ \rightarrow This is what we want to show -

$\underline{G_2}$

$Q_2 Q_1$	00	01	11	10
Q_0	x	x	1	x
\bar{Q}_0	1	x	0	0

$\underline{G_1}$

$Q_2 Q_1$	00	01	11	10
Q_0	x	x	1	x
\bar{Q}_0	0	1	0	1

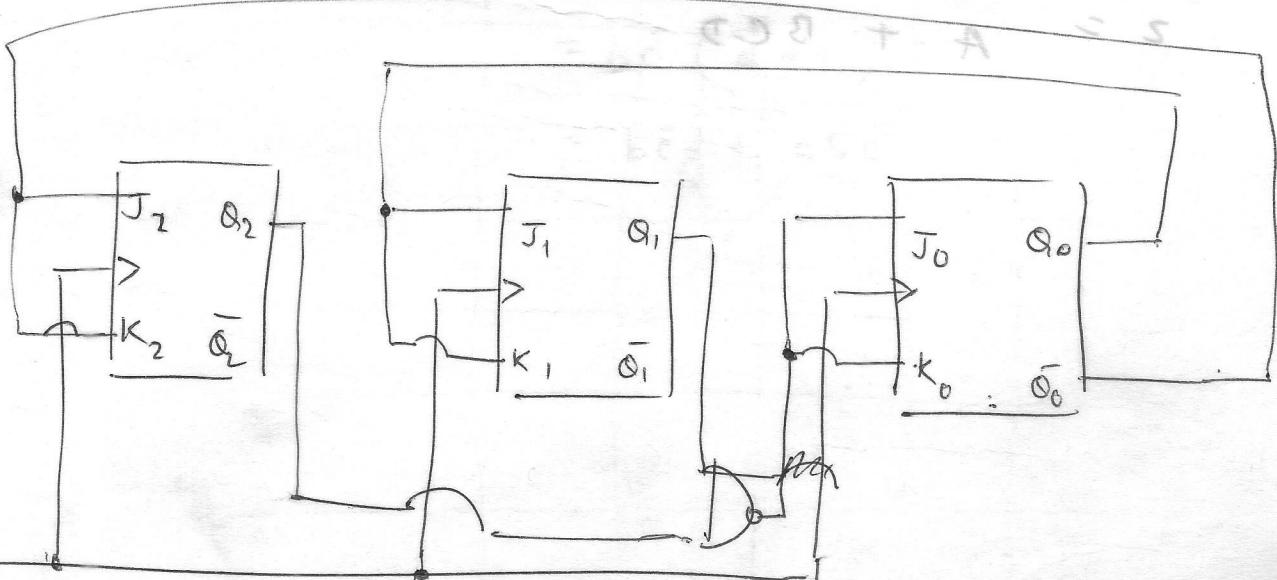
$\underline{G_0}$

$Q_2 Q_1$	00	01	11	10
Q_0	x	x	1	x
\bar{Q}_0	0	0	0	1

$$G_2 = \overline{Q_1} \cdot \overline{Q_0}$$

$$G_1 = Q_0$$

$$G_0 = \overline{Q_2} + \overline{Q_1}$$



CLR