



Experiment No. 3
Title: Design and Implementation of Different Arithmetic Circuits using Vlab.



Batch: B-1

Roll No.: 16010422234

Name: Chandana Ramesh Galgali

Experiment No.: 3

Aim: To Design and Implementation of Different Arithmetic Circuits using Vlab.

Resources needed: internet connection,

Access to- <https://he-coep.vlabs.ac.in/exp/various-arithmetic-circuits/index.html>

Theory:

Explain following points in brief

1. **Binary Adder – Subtractor**
2. **Half Adder**
3. **Full Adder**
4. **4 bit Binary Adder Subtractor**

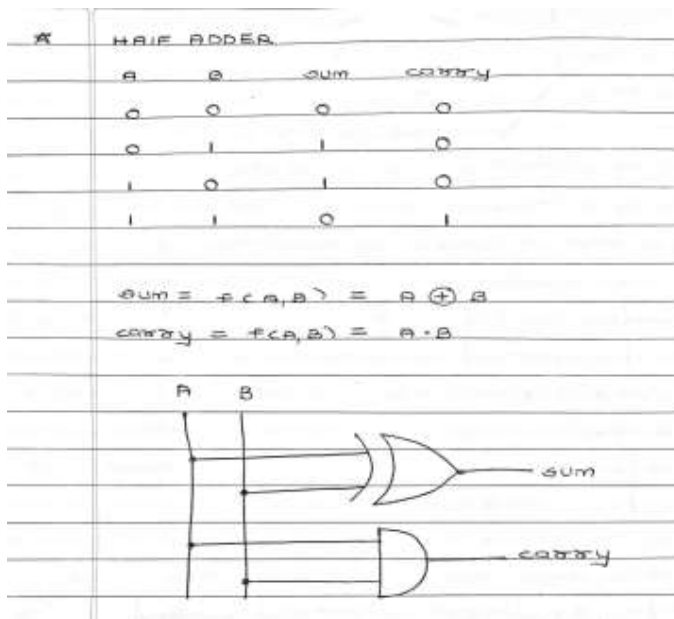
Explore the Theory and lab Manual in References section of the Vlab experiment

Procedure:

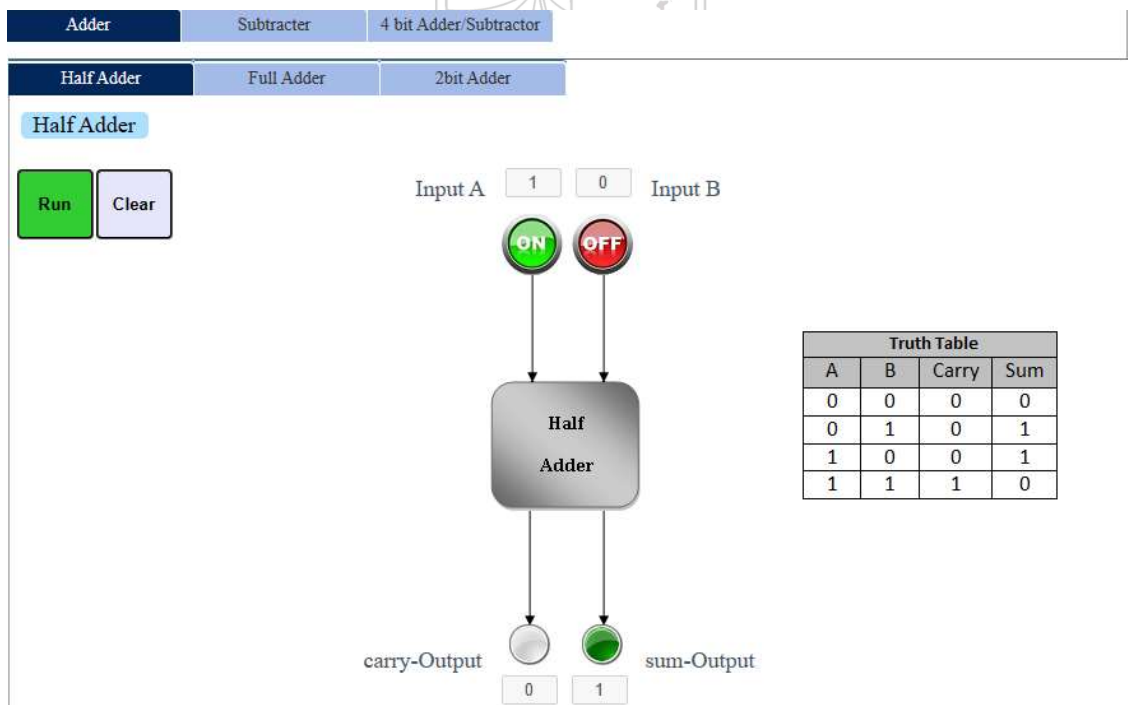
- a) Appear for Pretest and include the screenshot in write-up.
 - b) Design and Realize a Half Adder. Include scanned copy of design in write up.
 - c) Go through Procedure Tab.
 - d) Explore Simulator as per instructions in Procedure include screenshot of every circuit simulated in the writeup.
 - e) Appear for Posttest and include screenshot in write-up.
 - f) Create a document with screenshots mentioned above, Outcome and Conclusion.
 - g) Please note every document uploaded as Lab Writeup should be labelled as Exp_<No>_<RollNo.pdf
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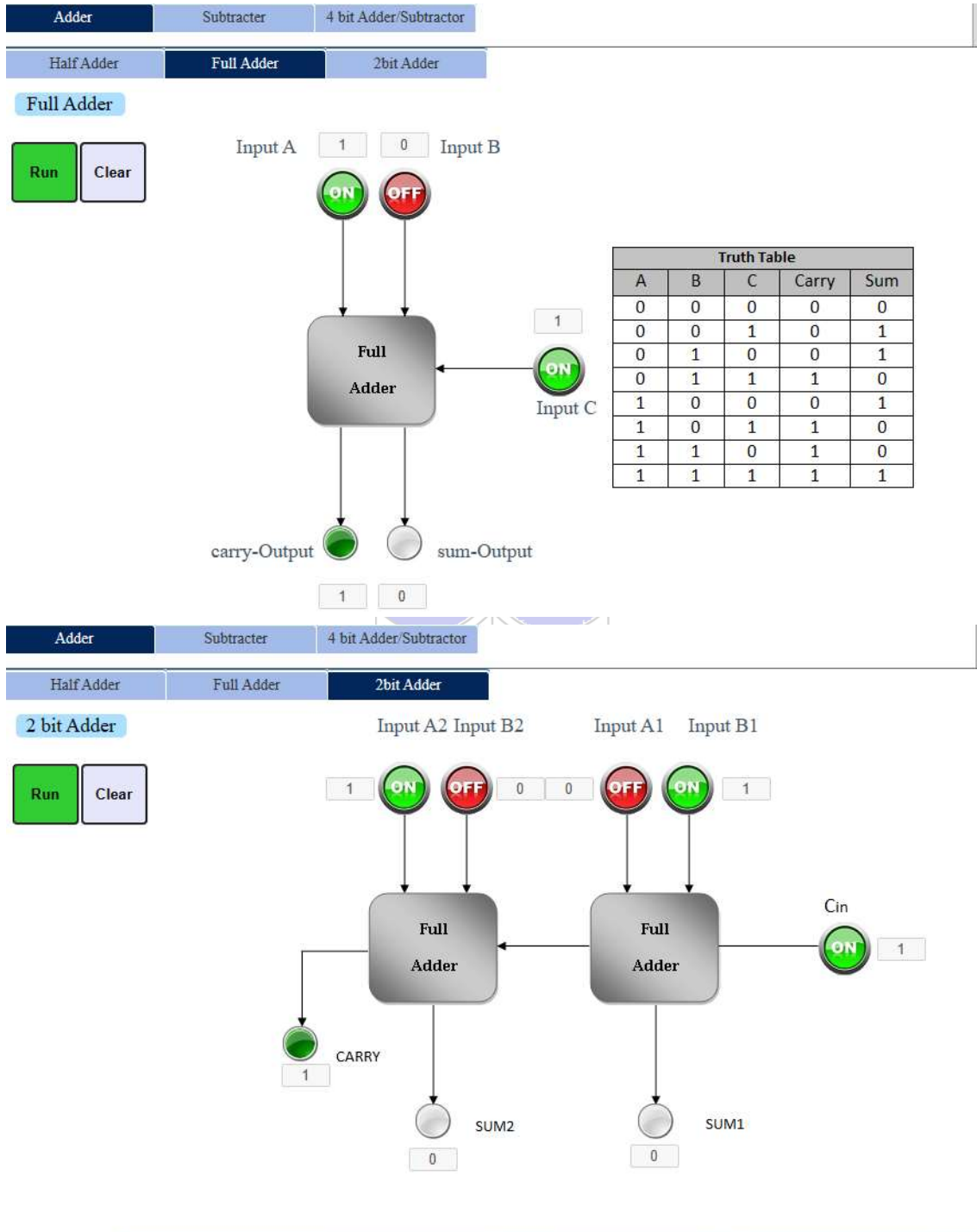
Observations and Results:

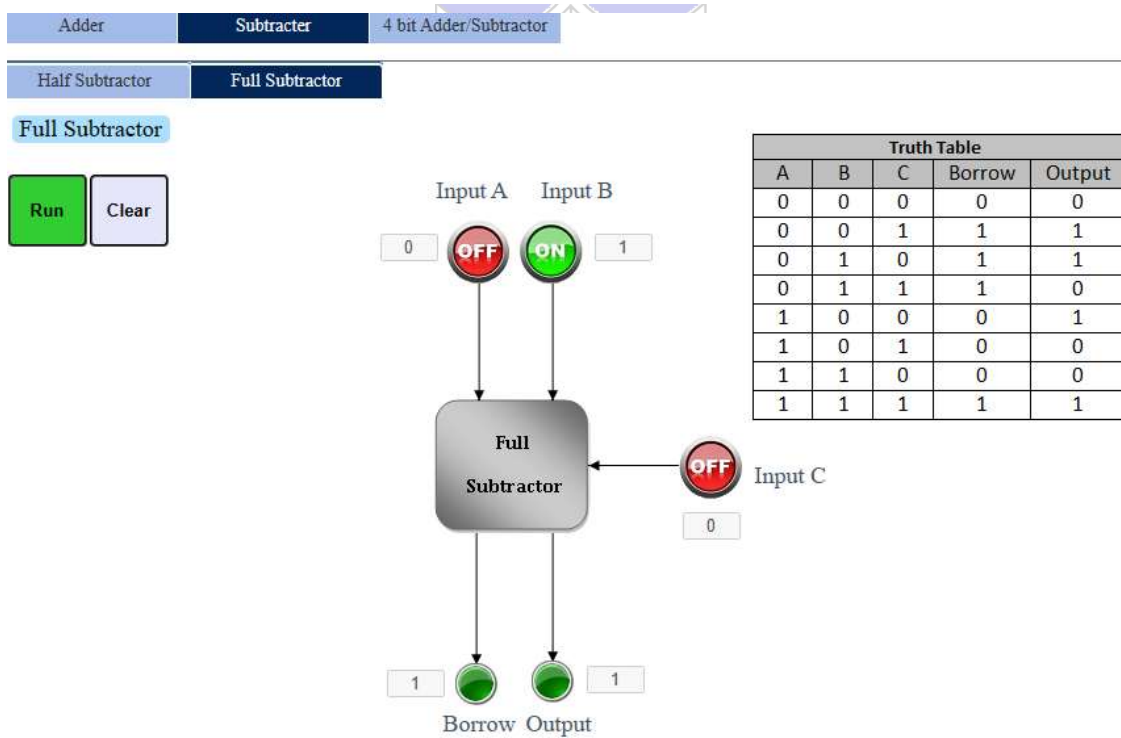
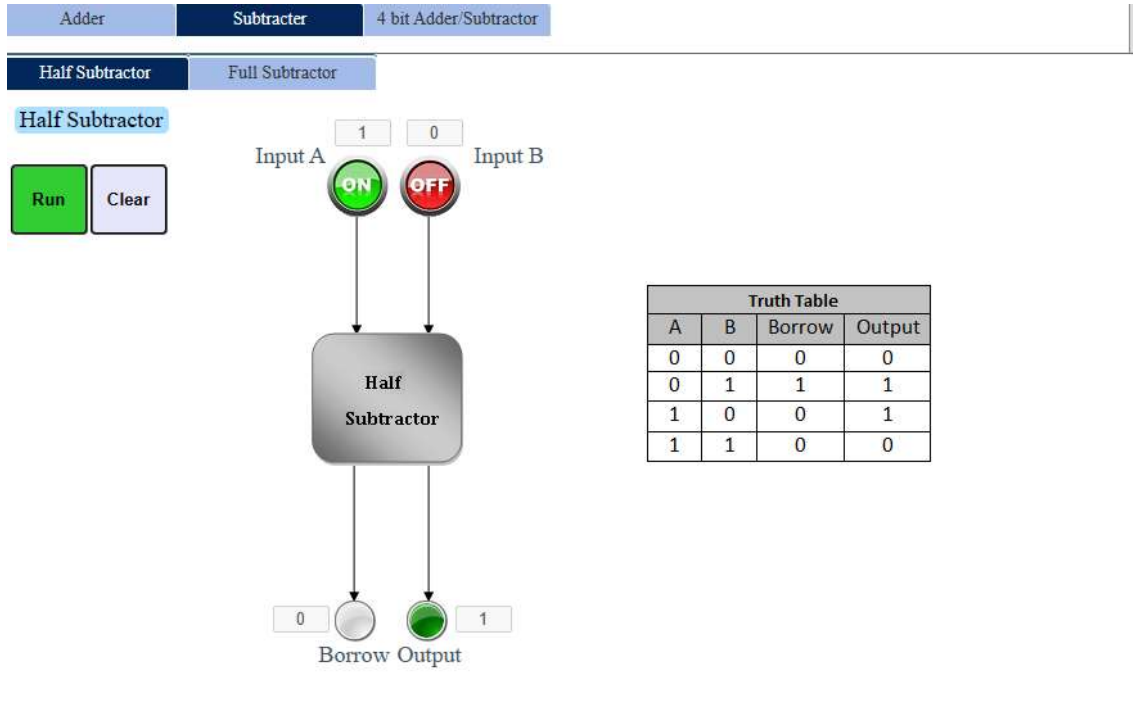
a) Design of Half Adder.

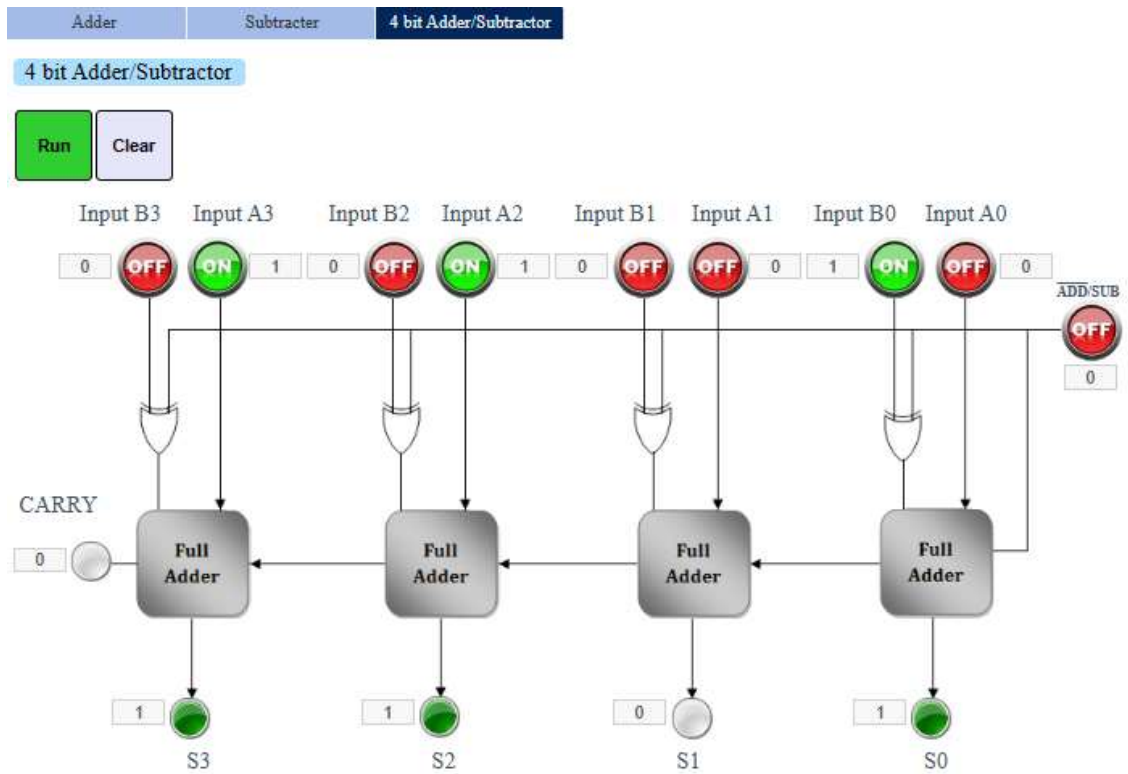


b) Observe and understand the simulated Binary Adders and Subtractors.









Outcomes: Understand the basic building blocks, techniques used in digital logic design.

Post-test:

Add binary numbers 1010 and 0001

☐ a: 1100

☐ b: 1111

☒ c: 1011

☐ d: 1110

Add binary numbers 1011 and 1101

☐ a: 11011

☒ b: 11000

☐ c: 11111

☐ d: 11010

Subtract decimal numbers 73 and 48 using 2s complement arithmetic

☐ a: 10101111

☐ b: 01041111

☐ c: 01101111

☒ d: 00110011

Subtract 1010 from 1111 using 2s complement

☒ a: 0101

☐ b: 1010

☐ c: 1101

☐ d: 1011

Use 2s complement arithmetic to solve expression given in decimal numbers : $58-33 \times 4$

☐ a: 01000100

☐ b: 01110101

☐ c: 01011111

☒ d: 01011101

5 out of 5



Conclusion:

We could successfully design and implement Different Arithmetic Circuits using Vlab.

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.
2. <https://he-coep.vlabs.ac.in/exp/various-arithmetic-circuits/index.html>
3. <https://he-coep.vlabs.ac.in/exp/various-arithmetic-circuits/images/Lab.Manual.Exp.arithmetic.ckt.pdf>