Experiment No. 7

Title: Implementation of synchronous counter using JK flips flops

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Experiment No.: 7

Aim: Implementation of 3 bit synchronous up counter using JK flips flops

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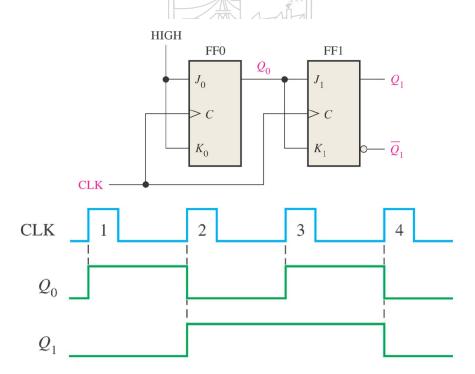**Resources needed:** Trainer kit, connecting cables, Simulation software

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Theory:

Synchronous Counter Operation
Synchronous counters have a common clock pulse applied simultaneously to all flip-flops.

A 2-Bit Synchronous Binary Counter
Note that both the J and K inputs are connected together. The flip-flop will toggle when both are a 1 (FF0) Also the transition at clock pulse 2 works because of propagation delay effects. Q0 is still high on the input of Q1 at the instant clock 2 hits so FF1 changes state. A short time later clock 2 has propagated through FF0 and it goes low.

Truth table of J K flip flop

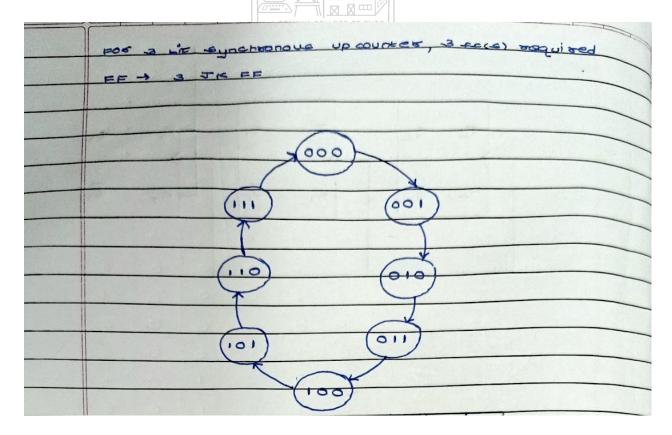| Inputs			Outputs		comments
J	**K**	**CLK**	**Q_1**	**Q'_1**	
0	0	↑	Q_0	Q'_0	No change
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	Q'_0	Q_0	Toggle

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Design procedure of Synchronous counter
1. Find the number of flip-flops.
2. Write the count sequence in tabular form
3. Determine the flip-flop inputs which must be present for the desired next state from the present state using the excitation table of the flip-flops.
4. Prepare K-map for each flip-flop input in terms of flip-flop outputs as the input variables.
5. Simplify the K-maps and get the minimized expressions for each flip-flop input.
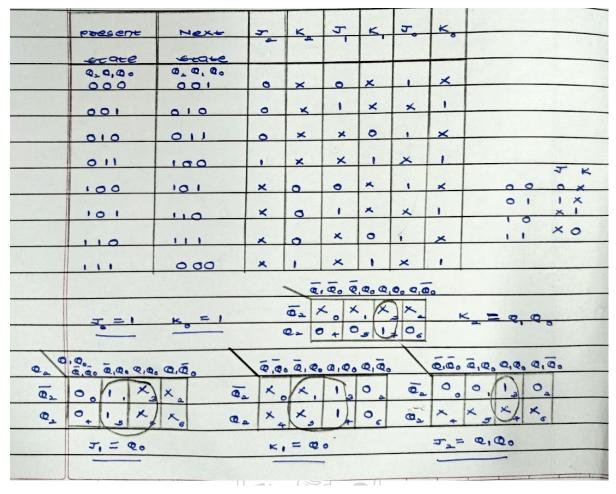6. Connect the circuit using flip-flops and other gates corresponding to the minimized expression

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Procedure:
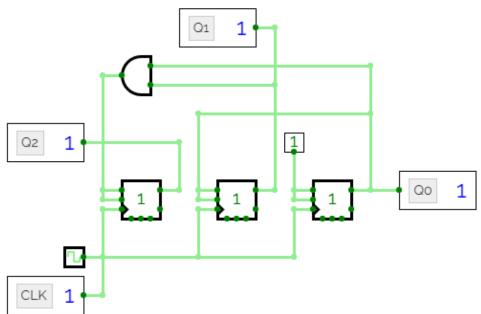
1. Design a 3 bit synchronous up counter using JK flip-flop as per the design procedure mentioned in theory.
2. Simulate the logic design using JK flip-flops on the simulation software.
3. Verify the output of the designed and simulated counter for the proper sequence.
4. Generate the output timing diagram on a simulator.
5. Upload Schematic and Timing Diagram generated on Simulator on Google classroom

Observations and Results: Observe the UP counter timing diagram as per actual outputs and identify the changes needed in the counter circuit to make the circuit work as a 3 bit Down counter.

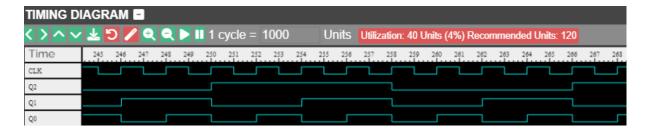| present state $Q_2 Q_1 Q_0$	Next state $Q_2 Q_1 Q_0$	J_2	K_2	J_1	K_1	J_0	K_0
0 0 0	0 0 1	0	x	0	x	1	x
0 0 1	0 1 0	0	x	1	x	x	1
0 1 0	0 1 1	0	x	x	0	1	x
0 1 1	1 0 0	1	x	x	1	x	1
1 0 0	1 0 1	x	0	0	x	1	x
1 0 1	1 1 0	x	0	1	x	x	1
1 1 0	1 1 1	x	0	x	0	1	x
1 1 1	0 0 0	x	1	x	1	x	1

	J	K
0 0	0	x
0 1	1	x
1 0	x	1
1 1	x	0

$$J_0 = 1 \qquad K_0 = 1$$

	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1\,Q_0$	$Q_1\,\overline{Q_0}$
$\overline{Q_2}$	x_0	x_1	x_3	x_2
Q_2	0_4	0_5	1_7	0_6

$$K_2 = Q_1 Q_0$$

$Q_2 \backslash Q_1 Q_0$	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1\,Q_0$	$Q_1\,\overline{Q_0}$
$\overline{Q_2}$	0_0	1_1	x_3	x_2
Q_2	0_4	1_5	x_7	x_6

$$J_1 = Q_0$$

	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1\,Q_0$	$Q_1\,\overline{Q_0}$
$\overline{Q_2}$	x_0	x_1	1_3	0_2
Q_2	x_4	x_5	1_7	0_6

$$K_1 = Q_0$$

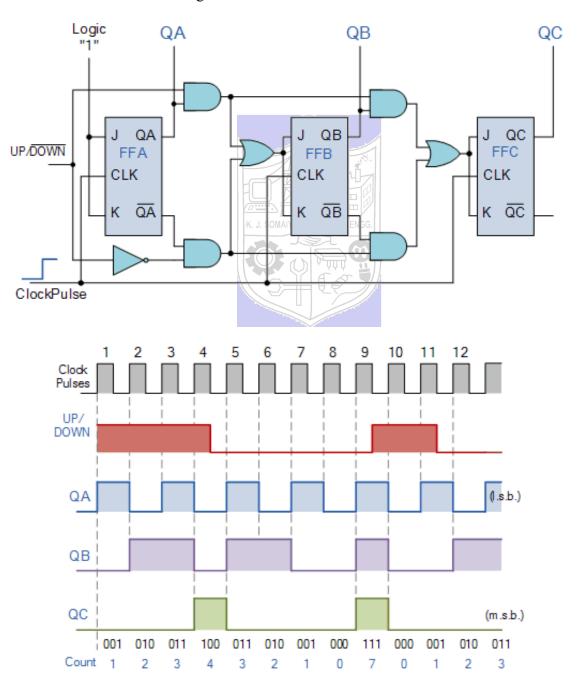|	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1\,Q_0$	$Q_1\,\overline{Q_0}$
$\overline{Q_2}$	0_0	0_1	1_3	0_2
$\overline{Q_2}$	x_4	x_5	x_7	x_6

$$J_2 = Q_1 Q_0$$

Post Lab:

Q1. Analyse the following 3 bit synchronous Up/Down Counter
Schematic diagram and timing diagram with Assumption M=1 for Up count and M=0 for Down count write the working of the same.

A 3-bit synchronous Up/Down counter is a digital circuit that can count up or down based on the input signals. It consists of three flip-flops, labeled as FF2, FF1, and FF0, representing the most significant bit (MSB), middle bit, and least significant bit (LSB) respectively.

The counter has two control inputs: M and CLK. M determines the direction of counting, where M=1 represents an Up count and M=0 represents a Down count. CLK is the clock input that synchronizes the counter's operation.

1. Up Count (M=1):
   - Initially, all flip-flops are reset to 0.
   - When CLK transitions from low to high, the counter increments by 1.
   - The LSB (FF0) toggles on each rising edge of CLK.
   - When FF0 transitions from 1 to 0, it triggers the middle bit (FF1) to toggle.
   - Similarly, when FF1 transitions from 1 to 0, it triggers the MSB (FF2) to toggle.
   - This way, the counter counts up in binary from 000 to 111 and then wraps back to 000.

2. Down Count (M=0):
   - Similar to the Up count, all flip-flops are initially reset to 0.
   - When CLK transitions from low to high, the counter decrements by 1.
   - The LSB (FF0) toggles on each rising edge of CLK.
   - When FF0 transitions from 0 to 1, it triggers the middle bit (FF1) to toggle.
   - Similarly, when FF1 transitions from 0 to 1, it triggers the MSB (FF2) to toggle.
   - This way, the counter counts down in binary from 111 to 000 and then wraps back to 111.

The timing diagram shows the clock signal (CLK) and the outputs of the three flip-flops (FF2, FF1, and FF0) over time, illustrating the transitions and changes in the counter's state.

Outcomes: Design the combinational and sequential circuits using basic building blocks.

Conclusion: We could successfully implement a 3 bit synchronous up counter using JK flip flops.

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:
Books/ Journals/ Websites:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.
2. http://www.electronics-tutorials.ws/counter/count_4.html