Truth Table of JK Flip Flop: Circuit Diagram and Master-Slave

June 11, 2021 by Wira Adhitama

JK Flip Flop is considered to be a universal programmable flip flop. Why is it considered to be a universal flip flop?

JK flip flop has several inputs: J, K, S, and R which can be used like any other flip flop types. The JK flip flop is basically the improved version of R-S flip flop but the output remains the same when the J and K inputs are LOW.

The R-S flip flop circuit may have many advantages and functions in logic circuits but it has two major problems:

- Set = Reset = 0 (S = R = 0) and Set = Reset = 1 (S = R = 1) must be avoided
- If the SET or RESET inputs change logic state when the Clock (CLK) is active HIGH, the correct latching action may not happen.

To solve these major problems, the JK flip flop was constructed.

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3 Sequential Operation of JK Flip Flop
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7 The Drawback of J-K Flip Flop
8 Popular J-K Flip Flop IC
9 Frequently Asked Questions

We can say that the JK flip flop is the most versatile flip flop, because it has inputs like D flip flop with clock input. This flip flop uses two inputs labelled with J and K.

If the J and K input are different, the output Q will have the value of J at the next clock edge cycle. J and K is used to give honor to Jack Kilby as the inventor of this flip flop type.

What is JK Flip Flop

This basic JK flip flop is the most mainly used of all the flip flop circuits and is known as a universal flip flop. This flip flop's inputs are labelled with "J" and "K" just like "S" for SET and "R" for RESET in S-R flip flop.

The J and K stand for Jack Kilby as this flip flop type inventor.

The sequential logic operation of this JK flip flop is the same with the R-S flip flop with the same SET and RESET logic inputs. The only difference is the JK flip flop has no forbidden input combination.

JK flip flop or JK-FF for short, is basically an improved R-S flip flop. This flip flop is a combination of a gated R-S flip flop and a clocked signal input.

The clock input will prevent the invalid or illegal input operation when both S and R equal to logic "1".

- Logic “1”
- Logic “0”
- No change
- Toggle.

There are two responses of JK flip flop:

- When the J and J inputs are both in low state (logic “0”) = no change happens
- When the J and K inputs are both in high state (logic “1”) at the clock edge = the output will change from one logic state to the other (“0” to “1” and vice versa)

This JK flip flop can exactly act as an R-S flip flop while eliminating the ambiguous conditions.

Not only that, but this flip flop can also imitate a T flip flop to do the output flip flop if we tie the J and K inputs together.

This toggle application can be used for extensive binary counters.

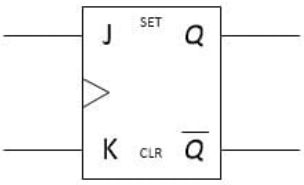
The JK flip flop has the same function as the R-S flip flop, but for one of the responses in the truth table.

The disadvantage of R-S flip flop is the prohibited input combinations below:

- The inputs S = R = 1 (active HIGH logic inputs)
- The inputs S = R = 0 (active LOW logic inputs)

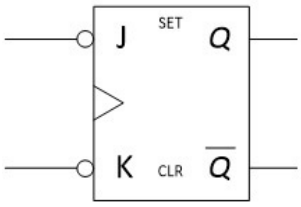
This disadvantage of R-S flip flop has been overcome by JK flip flop in case:

- Active HIGH inputs, the output of the flip flop switch, hence, it changes to the other logic state (for J = K = 1)



Operation Mode	J	K	CLK	Q_{n+1}
SET	1	0	1	1
RESET	0	1	1	0
NO CHANGE	0	0	1	Q_n
TOGGLE	1	1	1	$\bar{Q}_n$

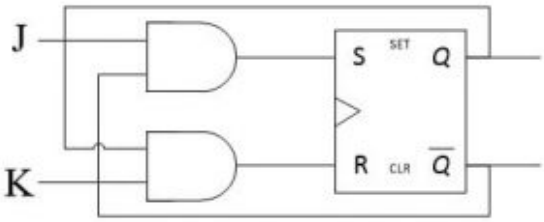
JK flip flop active high inputs



Operation Mode	J	K	CLK	Q_{n+1}
SET	0	1	1	1
RESET	1	0	1	0
NO CHANGE	1	1	1	Q_n
TOGGLE	0	0	1	$\bar{Q}_n$

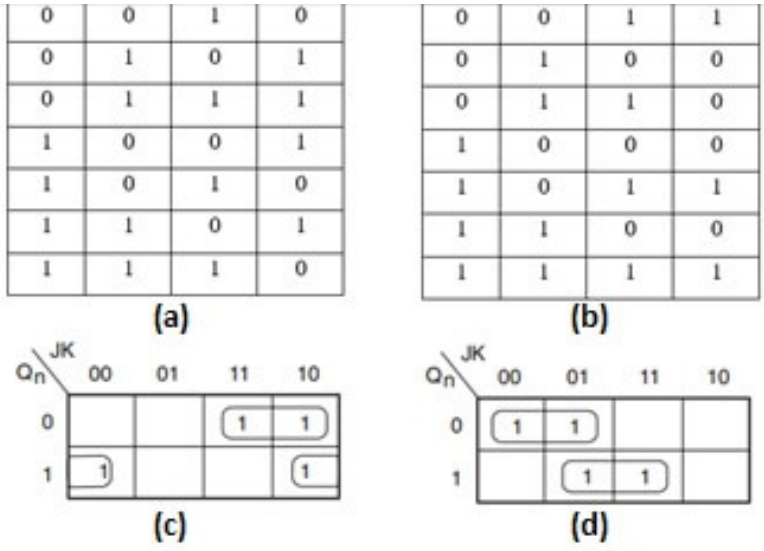
JK flip flop active low inputs

Figures (a) and (b) represent the circuit symbol of level-triggered JK flip flop with active HIGH and LOW inputs respectively, along with the truth table.



Representation of the JK flip flop using an R-S flip flop

The figure above shows us the JK flip flop from R-S flip flop with additional logic gates.



The truth tables of JK flip flop and the Karnaugh map solutions

The tables above show us the truth tables of JK flip flop with:
(a) active HIGH inputs and (b) active low inputs.

The Karnaugh map solution of JK flip flop with:
(c) active HIGH inputs and (d) active LOW inputs.

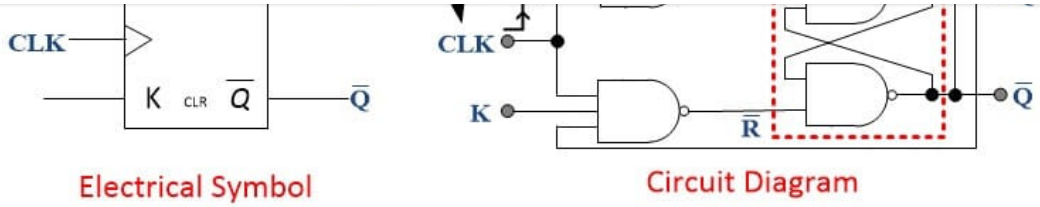
The characteristic equations for the Karnaugh maps of the figure above are respectively,

$$Q_{n+1} = J.\overline{Q_n} + \overline{K}.Q_n$$

$$Q_{n+1} = \overline{J}.\overline{Q_n} + K.Q_n$$

Basic Symbol and Circuit Diagram of JK Flip Flop

The symbol of this JK flip flop is quite similar to the S-R flip flop without the clock input.



The basic symbol of JK flip flop

Like mentioned above, the previous R and S inputs are now replaced by two new inputs: J and K. The inputs become J = S and K = R.

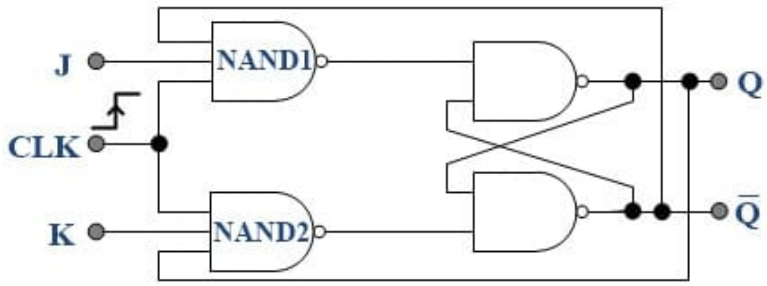
If the R-S flip flop has two 2-inputs AND gates, we need to modify it a little to make a JK flip flop.

We will use two 3-inputs NAND gates and the third input of each gate connected with the outputs of Q and $\overline{Q}$. The NAND gate for J input gets the $\overline{Q}$ state while the NAND gate for K input gets the Q state.

This cross-connected feedback is able to get rid of the invalid condition (S = R = 1 and S = R = 0) because the two inputs are now interlocked.

Sequential Operation of JK Flip Flop

Below is the circuit diagram of a JK flip flop, consisting of 4 NANDs. We will only focus on the first two NANDs: NAND1 and NAND2.



Sequential operation of JK flip flop

Now pay attention to the JK flip flop sequential operation of JK flip flop below:

1. At first, assume that both J and K receive logic inputs 1, Q = 0, $\overline{Q}$ = 1.

4. NAND1 only needs a logic state “1” on its clock signal input to change its output state logic to “0”.
5. Until this point, the NAND2 is still disabled because it only has one logic state “1” on its input K. Its feedback input is logic state “0” from Q.
6. The clock pulse is HIGH.
7. The output of NAND1 changes to the logic state “0”.
8. So, Q = 1 and $\overline{Q} = 0$.
9. NAND2 is enabled and NAND1 is disabled.

There is a problem when the logic state changes at the output side. If the clock signal is still HIGH or in transition period ‘HIGH to LOW’ when the flip flop changes its logic state, the output of NAND2 will change to logic state “0” almost instantly.

This timing problem will reset the flip flop to its very first state. Because this problem occurred, the flip flop will oscillate between the logic state “0” and “1” very quickly.

You will call this problem a **Race-Around Flip-Flop** problem. The name implies the ‘race’ of the output data around the feedback route from output to input before the end of the clock signal.

Truth Table of JK Flip Flop

As Q and $\overline{Q}$ are always different we can use them to control the input. When both inputs J and K are equal to logic “1”, the JK flip flop toggles as shown in the following truth table.

Because Q and $\overline{Q}$ are always different, we can use the outputs to control the inputs. If the J and K are both active HIGH or logic state “1”, the JK flip flop will toggle the outputs as shown in the table below.

R-S flip flop sequences	0	0	-	0	1	No change
	0	1	⎍	1	0	Reset Q = 0
	0	1	-	0	1	
	1	0	⎍	0	1	Set Q = 1
	1	0	-	1	0	
Toggle sequences	1	1	⎍	0	1	Toggle
	1	1	⎍	1	0	

Truth Table of JK Flip Flop

Like mentioned above, the JK flip flop has the same basic principle as R-S flip flop. The JK flip flop has cross feedback to one of the two inputs. These feedbacks will activate the SET or RESET at one time, hence eliminating the forbidden input combination.

Not only that, if we give both the J and K inputs logic state "1" at the same time, but it also will not result in an invalid state. When the clock pulse is HIGH while J = K = 1 then the circuit will change its state from SET to RESET or vice versa.

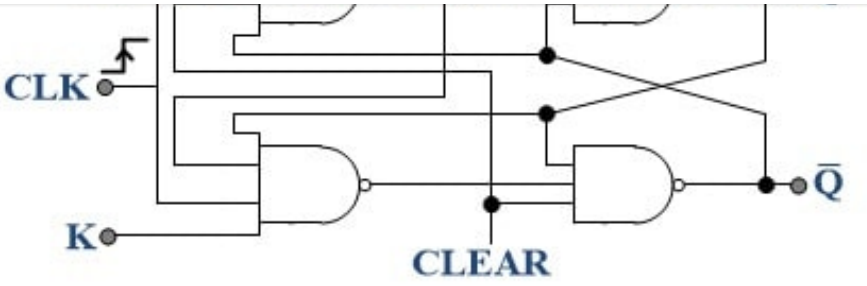
We can assume this flip flop is functioning as a T flip flop when both inputs are HIGH.

Even this JK flip flop is the improved R-S flip flop, this one has one disadvantage. The timing problem called "race" occurs when the output Q changes the logic state before the timing pulse of the clock signal input has not gone "OFF".

In order to eliminate this problem, we must keep the pulse period (T) as short as possible with high frequency.

JK Flip Flop with PRESET and CLEAR Inputs

Often we need to CLEAR the flip flop to logic state "0" ($Q_n = 0$) or PRESET it to logic state "1" ($Q_n = 1$). There is an example in the figure below. It will show how we do it.

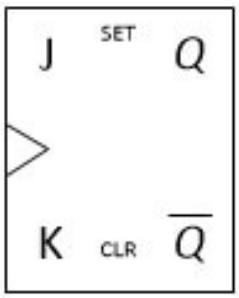


JK flip flop with PRESET and CLEAR

There are two conditions:

- The flip flop will be cleared (Q_n = 0) if we give logic state “0” to the CLEAR inputs and logic state “1” to the PRESET input.
- The flip flop is in preset logic state “1” condition (Q_n = 1) if we give logic state “1” to the CLEAR inputs and logic state “0” to the PRESET inputs.

Here, the PRESET and CLEAR inputs are active when low.



JK flip flop with PRESET and CLEAR

The image above is the circuit symbol of clocked JK flip flop which is presettable and clearable.

0	0	X	X	X	-	-
1	1	1	0	0	Q_n	$\overline{Q_n}$
1	1	1	1	0	1	0
1	1	1	0	1	0	1
1	1	1	1	1	Toggle	
1	1	0	X	X	Q_n	$\overline{Q_n}$

The truth table of JK flip flop with PRESET and CLEAR

The table above is the truth table of JK flip flop with PRESET and CLEAR.

From the table, we conclude that, if the PRESET input is active, the output changes to logic state “1” regardless of the status of the clock, J, and K inputs.

Otherwise, if the CLEAR input is active, the output changes to logic state “0” regardless of the status of the clock, J, and K inputs.

There is an exception for this JK flip flop with PRESET and CLEAR: both of the PRESET and CLEAR inputs should not be activated at the same time.

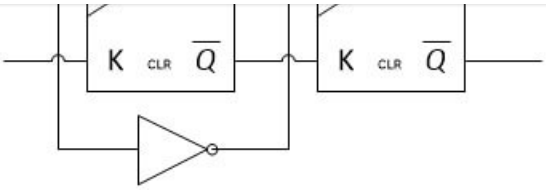
Master Slave of JK Flip Flop

When the width of the clock pulse of the flip flop is greater than the delay of the flip flop’s propagation, the change of the flip flop’s output is not reliable.

To overcome this problem, we will use the pulse generated by the edge-triggered flip flop. This pulse generated by the edge-detector portion of the flip flop would be the trigger, instead of the pulse width generated by the clock input signal.

This phenomenon is referred to as a race problem. Because the propagation delay is usually very small, the likelihood of race conditions occurring is quite high.

The most known solution to solve this problem is to use the slave-master flip flop configuration.



Master-slave J-K flip flop

Above is the master-slave J-K flip flop built with two J-K flip flops. There are two parts of this type of flip flop:

- The first flip flop = the master flip flop
- The second flip flop = the slave flip flop

The clock signal input will be complemented to the slave flip flop, while the master receives the clock input signal directly.

The operation steps of this master-slave J-K flip flop are:

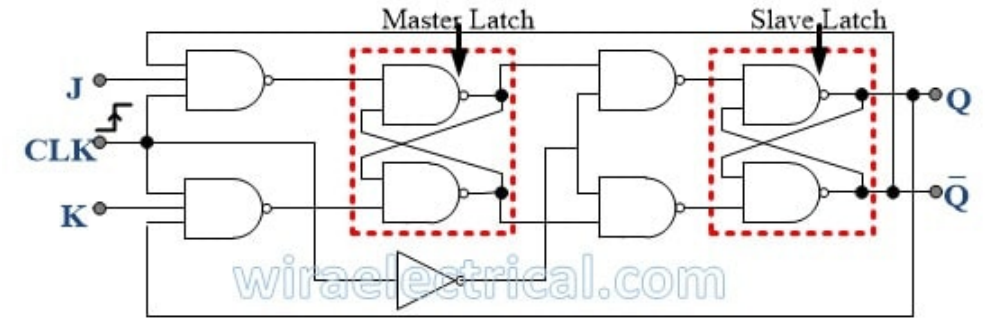
1. The clock signal pulse is HIGH,
2. The master flip flop is enabled, but the slave flip flop is disabled,
3. As the result, the master flip flop is able to change its output logic state, but the slave flip flop is unable,
4. The clock signal pulse is LOW,
5. The master flip flop is disabled, but the slave flip flop is enabled,
6. Hence, the logic state of the slave J-K flip flop changes as per logic state J-K logic inputs.
7. The logic state of the master flip flop is transferred to the slave flip flop, and the disabled master flip flop can acquire new inputs without affecting the output.

From the steps above, it should be clear that a master-slave flip flop is a pulse-triggered flip flop, not an edge-triggered flip flop.

The table below will show us the truth table of a master-slave J-K flip flop along with active LOW PRESET and CLEAR inputs, and also the active HIGH J and K

But, the master-slave J-K flip flop has become obsolete. The modern IC such as 74LS, 74AL, 74ALS, 74HC, and 74HCT don't have master-slave flip flops in their series.

Below we will observe how the master-slave of J-K flip flop works using its circuit diagram.



Master Slave J-K flip flop

Both input signals J, K, and clock input are connected to the "master" R-S flip flop which is able to lock the inputs when the clock input 'CLK' signal is HIGH or at logic state "1".

The CLK signal is complemented as the timing pulse for the "slave" R-S flip flop. This will make both flip flops work alternately.

Looking from the circuit diagram above, we can conclude the steps as:

1. CLK is HIGH or at logic state "1"
2. CLK input is at logic state "1" for the "master" and "0" for the "slave"
3. The inputs of the "master" are locked, but the outputs are only seen by the "slave" flip flop.
4. CLK is LOW or at logic state "0"
5. CLK input is at logic state "0" for the "master" and "1" for the "slave"
6. The outputs from the "master" latched and the flip flop does not read any inputs.
7. The "slave" flip flop is reading its input from the transferred outputs from the "master"

'LOW to HIGH': the "master" will transfer its outputs. This transition is complemented to the "slave" as 'HIGH to LOW' and makes the inputs processed by the "slave".

This timing operation makes this flip flop as edge or pulse-triggered.

The flip flop receives input logic state when the CLK is HIGH and sends the data to the output when the clock signal is in falling-edge.

Hence, we can assume that the Master-Slave J-K flip flop is a "Synchronous" electric device because it only sends data at specific clock input timing.

The Drawback of J-K Flip Flop

The main and the only drawback of the J-K flip flop has been mentioned above, the Race Around Condition. This problem occurs when the J and K inputs are in logic state "1".

The race around condition is when the output toggles the outputs more than one time after the output is complemented once.

If this problem happens, it will be very difficult to predict the next outputs. Assume if we give J and K a logic state "1", in the next clock pulse the output will toggle.

What will happen if the J and K remain same at logic state "1"?

The output will toggle one more time and continue the pattern 0101010 in real scenario.. We need the master slave J-K flip flop in order to prevent this drawback.

We also need the clock interval is less than the delay propagation of the flip flop. If this is not achieved, the inputs won't be able to read the inputs before the clock

Popular J-K Flip Flop IC

If you are looking for J-K flip flop IC, you may consider buying the IC listed below:

Serial Number	Description
74LS107	Dual J-K Flip-Flop
74LS109	Dual J-K Flip-Flop
74LS73	Dual J-K Negative-Edge-Triggered Flip-flop
74LS112	Dual J-K Negative-Edge-Triggered Flip-flop
74LS76	Dual J-K Positive-Edge-Triggered Flip-Flop
74LS114	Dual J-K Negative-Edge-Triggered Flip-Flops DIP-14
74LS78	Dual J-K Negative-Edge-Triggered Flip-Flops DIP-14
NTE74LS76A	TTL Dual J-K Flip-Flop with Preset and Clear DIP-16
74LS113	Dual J-K Negative-Edge-Triggered Flip-Flops DIP-14

Frequently Asked Questions

Now we will try to answer the frequently asked questions about J-K flip flop:

What is JK flip flop truth table?

The J-K flip flop is basically the improved version of R-S flip flop but the output remains the same when the J and K inputs are LOW. The sequential logic operation of this J-K flip flop is the same with the R-S flip flop with the same SET and RESET logic inputs. The only difference is the J-K flip flop has no forbidden input combination.

What is the working of JK flip flop?

J-K flip flop has several inputs: J, K, S, and R which can be used like any other flip flop types. The J-K flip flop is basically the improved version of R-S flip flop but the output

What is JK flip flop with logic diagram?

As Q and Q' are always different we can use them to control the input. When both inputs J and K are equal to logic "1", the JK flip flop toggles. Because Q and Q' are always different, we can use the outputs to control the inputs. If the J and K are both active HIGH or logic state "1", the J-K flip flop will toggle the outputs

What is the drawback of JK flip flop?

The main and the only drawback of the J-K flip flop has been mentioned above, the Race Around Condition. This problem occurs when the J and K inputs are in logic state "1". The race around condition is when the output toggles the outputs more than one time after the output is complemented once.

Why JK flip flop is called universal flip flop?

J-K Flip Flop is considered to be a universal programmable flip flop. J-K flip flop has several inputs: J, K, S, and R which can be used like any other flip flop types. The J-K flip flop is basically the improved version of R-S flip flop but the output remains the same when the J and K inputs are LOW.

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29 thoughts on "Truth Table of JK Flip Flop: Circuit Diagram and Master-Slave"

EdisonmeagE

May 7, 2021 at 8:58 am

Hello my friend!
I want to say that this post is awesome, nice written and include

posts like this !

Reply

slotxo
June 16, 2021 at 12:37 am

Everything is very open with a clear explanation of the issues.
It was truly informative. Your site is very useful. Many thanks
for sharing!

Reply

Air conditioning Nottingham
June 18, 2021 at 3:49 am

I am really grateful to the holder of this website
who has shared this wonderful paragraph at at this place.

Reply

Азартмания TPG: Highway Kings
July 1, 2021 at 12:39 am

I've been browsing online more than 2 hours today, yet I never found any
interesting article
like yours. It is pretty worth enough for me. Personally,

Reply

saigonrecordings
July 4, 2021 at 6:21 pm

Thanks for a marvelous posting! I quite enjoyed reading it, you can be a great author.I will make sure to bookmark your blog and definitely will come back later on. I want to encourage you to continue your great job, have a nice afternoon!

Reply

Play Fortuna Kingdom of Gold Mystic Ways High5
July 5, 2021 at 1:02 am

It’s amazing designed for me to have a website, which is good designed for my knowledge.
thanks admin

Reply

online sabong betting
July 11, 2021 at 8:43 am

Heya i am for the first time here. I found this board and I find It truly useful & it helped

Reply

online dispensary
July 13, 2021 at 1:04 pm

Heya i am for the first time here. I came across
this board and I find It really useful & it helped me out much.

I hope to give something back and help others like you aided me.

Reply

have a look at
July 14, 2021 at 9:04 am

I simply could not go away your site before suggesting
that I extremely enjoyed the usual information a person provide for your guests?

Is going to be back often to investigate cross-check new posts

Reply

lpg
July 15, 2021 at 5:33 pm

mention that I have really
enjoyed surfing around your blog posts. After all I'll be
subscribing in your rss feed and I hope you
write again soon!

Reply

homepage
July 15, 2021 at 10:03 pm

Does your site have a contact page? I'm having problems
locating itt but, I'd like to sennd you an e-mail. I'vegot some ideas for your
blog you might be interested in hearing.
Either way, great site and I look forward
to seeing it improve over time.
homepage

Reply

car insurance ontario calculator
July 17, 2021 at 7:16 am

Hi, its fastidious post regarding media print, we all be aware of media is
a impressive source of information.

Reply

July 17, 2021 at 4:10 pm

Hey there! I'm at work browsing your blog from my new apple iphone! Just wanted to say I love reading through your blog and look forward to all your posts!

Carry on the excellent work!

Also visit my web blog; zburdalnic01

Reply

betflix

July 18, 2021 at 8:01 am

This article gives clear idea in favor of the new users of blogging, that really how to do blogging and site-building.

Reply

Ekonomia Definicja

July 18, 2021 at 7:18 pm

It is best to participate in a contest for probably the greatest blogs on the web. Ill recommend this website!

Reply

July 21, 2021 at 8:07 am

SA Gaming หรือ เอสเอเกมมิ่ง คาสิโนออนไลน์แบรนด์ดังยอดฮิตที่ไม่ว่าคุณจะเข้าไปในเว็บคาสิโนออนไลน์ใดก็ต้องเจอชื่อของ SA
Gaming อยู่ในนั้นแน่นอน SA คือค่ายเกมที่ได้รับรางวัลคาสิโนดีเลิศด้วยรูปแบบการให้บริการถ่ายทอดสดคาสิโนออนไลน์ที่มีภาพรวมทั้งเสียงชัด รวมทั้งจอการพนันที่ใช้งานง่ายมีตัวอักษรรวมทั้งเสียงนำเสนอภาษาไทยแนะนำขั้นตอนการพนัน และก็โต๊ะบาคาร่าอีกกว่า 50
โต๊ะให้ท่านเลือกเข้าวางเดิมพัน

ไม่เพียงเท่านั้นรางวัลคาสิโนออนไลน์ของ SA ไม่ได้มาเนื่องจากโชคช่วย คาสิโนออนไลนีแห่งนี้มีความพิเศษตรงที่ว่า คุณสามารถเลือกมุมมองโต๊ะพนันได้ด้วยตัวเองทั้งระยะใกล้ ระยะไกล เพิ่มโต๊ะพิเศษให้คุณเปิดไพ่ลุ้นได้ด้วยตัวเอง และที่ทันสมัยสุดๆก็คือฟังก์ชั่นวางเดิมพันพร้อมกันหลายโต๊ะ ที่เปิดโอกาสให้ท่านสามารถเข้าวางเดิมพันบาคาร่าออนไลน์ถึง 4 โต๊ะได้พร้อมๆกันใน 1 จอ เรียกได้ว่าทำเงินคูณสี่อย่างยิ่งจริงๆ

Reply

หวย

July 28, 2021 at 11:30 pm

I think this is one of the so much significant info for me.
And i am glad studying your article. However wanna statement on some general things,
The website taste is wonderful, the articles is actually excellent :
D. Excellent activity, cheers

Reply

July 31, 2021 at 7:23 pm

always i used to read smaller posts that as well clear
their motive, and that is also happening with this article which
I am reading at this time.

Reply

หวย

August 2, 2021 at 7:31 pm

This site certainly has all the information and facts I
needed concerning this subject and didn't know who to ask.

Reply

바카라룰

August 4, 2021 at 11:33 am

You're so cool! I don't suppose I've truly read through something like that
before.
So good to discover somebody with a few genuine thoughts
on this subject matter. Seriously.. thanks for starting this up.
This site is something that is needed on the web,
someone with a bit of originality!

Reply

Simply desire to say your article is as astonishing.
The clarity in your post is simply nice and i can assume you're an expert on this subject.

Well with your permission let me to grab your RSS feed to keep up to date with forthcoming post.
Thanks a million and please keep up the gratifying work.

Reply

메이저사이트 주소
August 8, 2021 at 4:56 pm

I like it when individuals get together and share ideas. Great site, keep it up!

Reply

Anatomia
August 9, 2021 at 8:01 am

This was a definitely extremely superior publish. In theory I'd like to write like this also getting time and actual effort to make a good piece of writing but what can I say I procrastinate alot and by no means appear to obtain anything done.

Reply

August 9, 2021 at 6:59 pm

I was suggested this website by my cousin. I'm not sure whether this post is written by
him as nobody else know such detailed about my trouble.
You are amazing! Thanks!

Reply

메이저사이트
August 10, 2021 at 1:08 am

Very nice post. I just stumbled upon your blog and wanted to say that I've really enjoyed surfing
around your blog posts. In any case I'll be subscribing to your feed and I hope you
write again very soon!

Reply

메이저 사이트
August 13, 2021 at 7:35 am

Hey! This is my first visit to your blog! We are a team of volunteers and starting a new project in a
community in the same niche. Your blog provided us useful information to work on. You have done a marvellous job!

Reply

Joker 123
August 19, 2021 at 2:48 am

wonderful issues altogether, you simply received a new reader.
What could you recommend about your put up that you simply made a few days ago?
Any certain?

Reply

osg 777
August 20, 2021 at 2:00 am

Hi there, I discovered your website by the use of Google even as looking for a similar subject, your website came up, it appears to be like good.
I have bookmarked it in my google bookmarks.
Hello there, simply changed into aware of your weblog thru
Google, and located that it is really informative.
I'm going to watch out for brussels. I will appreciate should you continue this in future.
A lot of other people will be benefited out of your
writing. Cheers!

Reply

https://mphclub.com/exotic-car-rental/
August 28, 2021 at 4:19 pm

a very well written article. I'll be sure to bookmark it and return to read extra of your useful info. Thank you for the post. I'll definitely comeback.

Reply

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Email *

Website

Save my name, email, and website in this browser for the next time I comment.

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