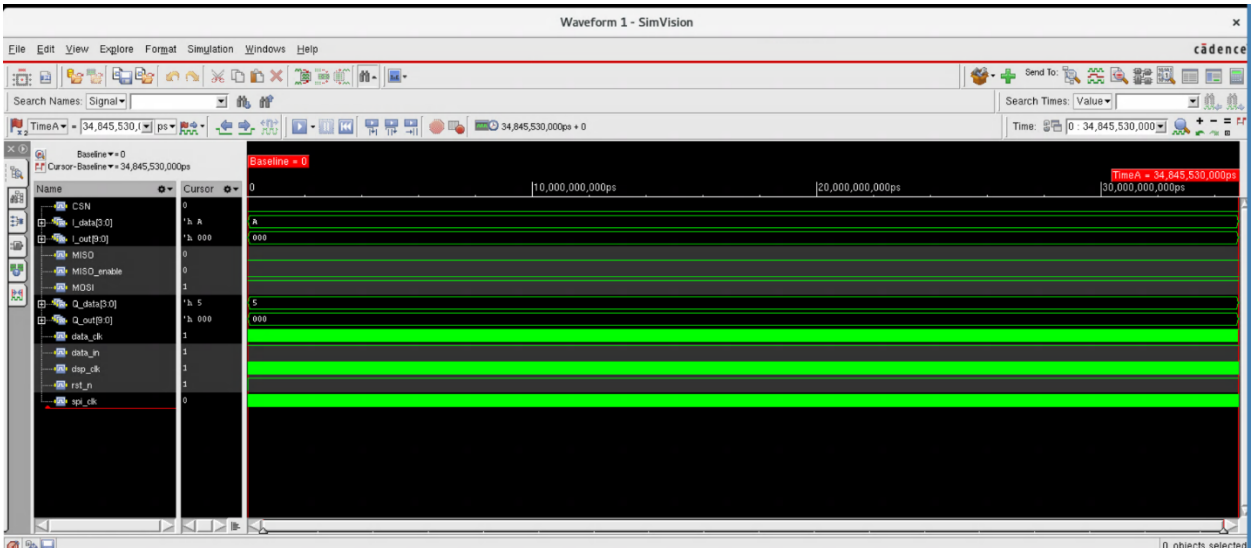
ECE 6214 Project 7

Final Modulator Simulation Results:



ECE 6214 Project 9

a. Notes on required HDL changes to synthesize design

1. Corrected all the port sizes of the FIR Filter
2. Traced and checked all the reset and clock inputs
3. Modified the dspslice connections in the final modulator.

b. Final synthesis constraints

Attached

c. Synthesized netlist

Attached

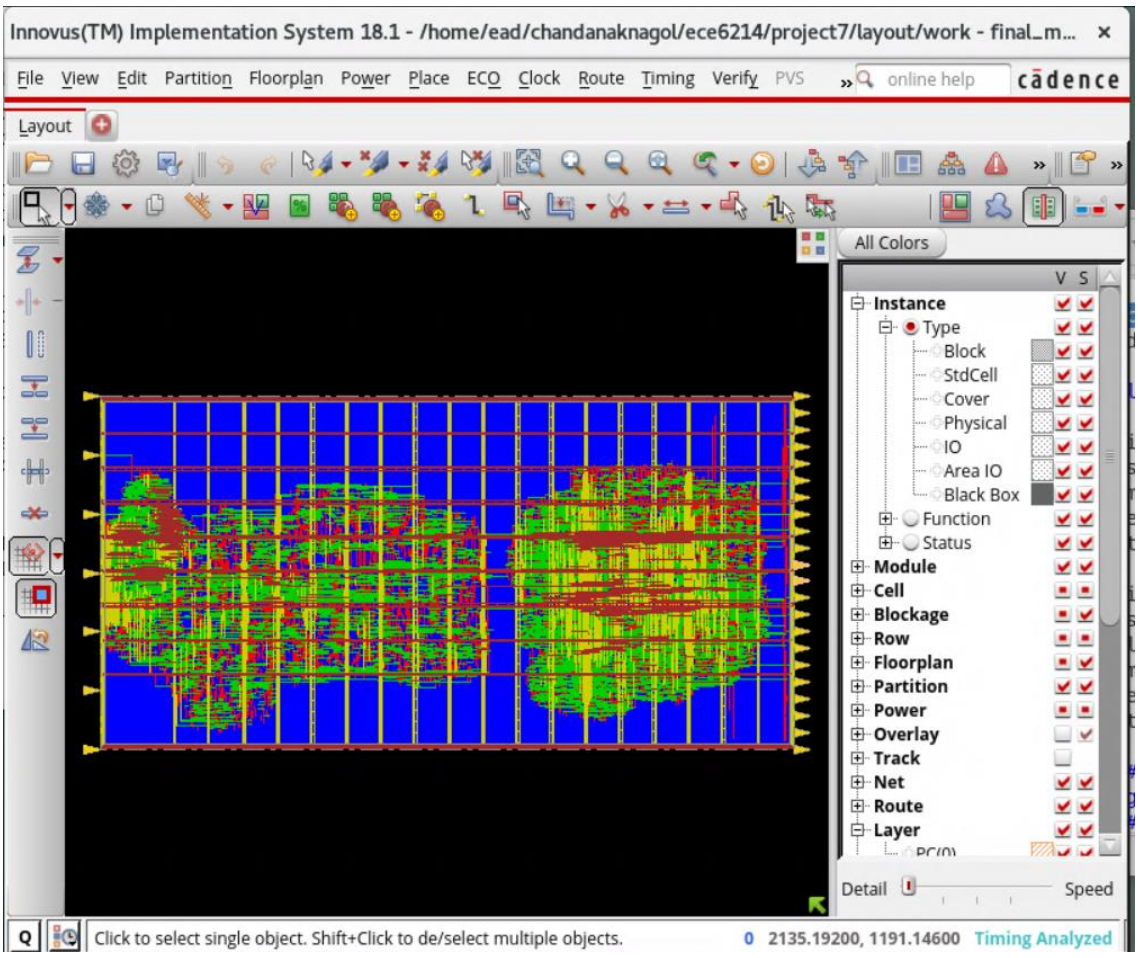
d. Synthesis area report

Attached

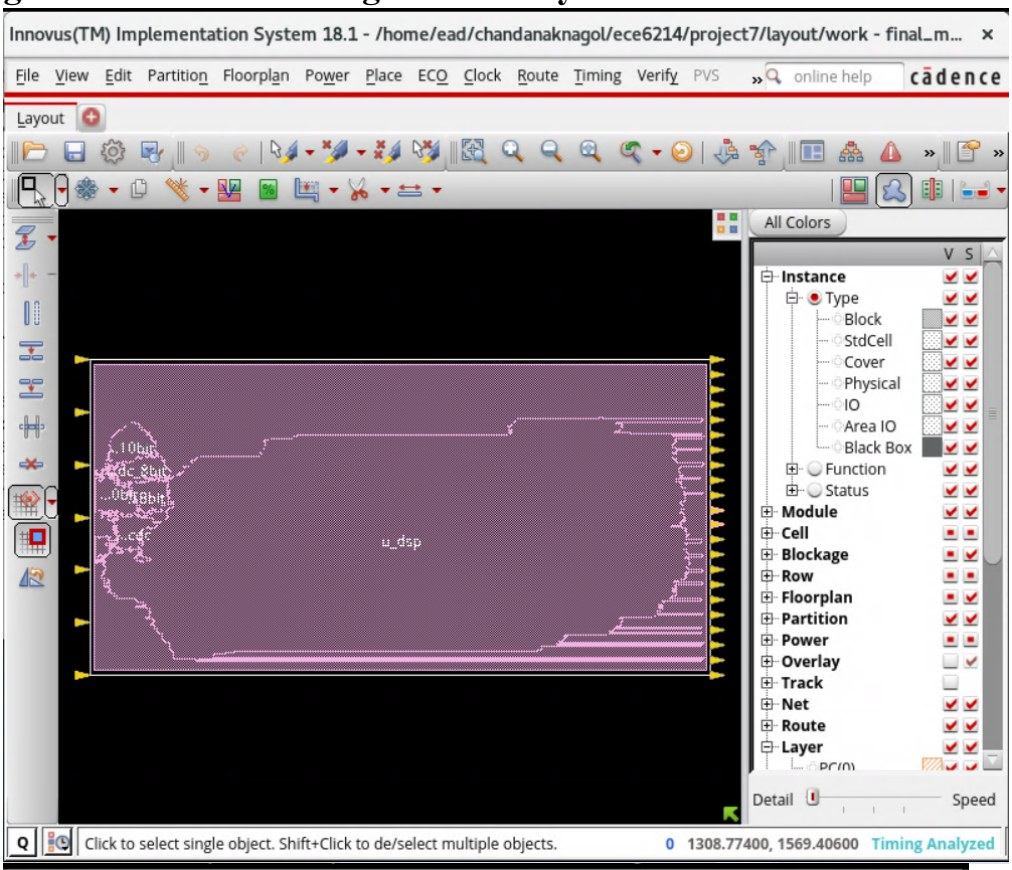
e. Synthesis timing reports

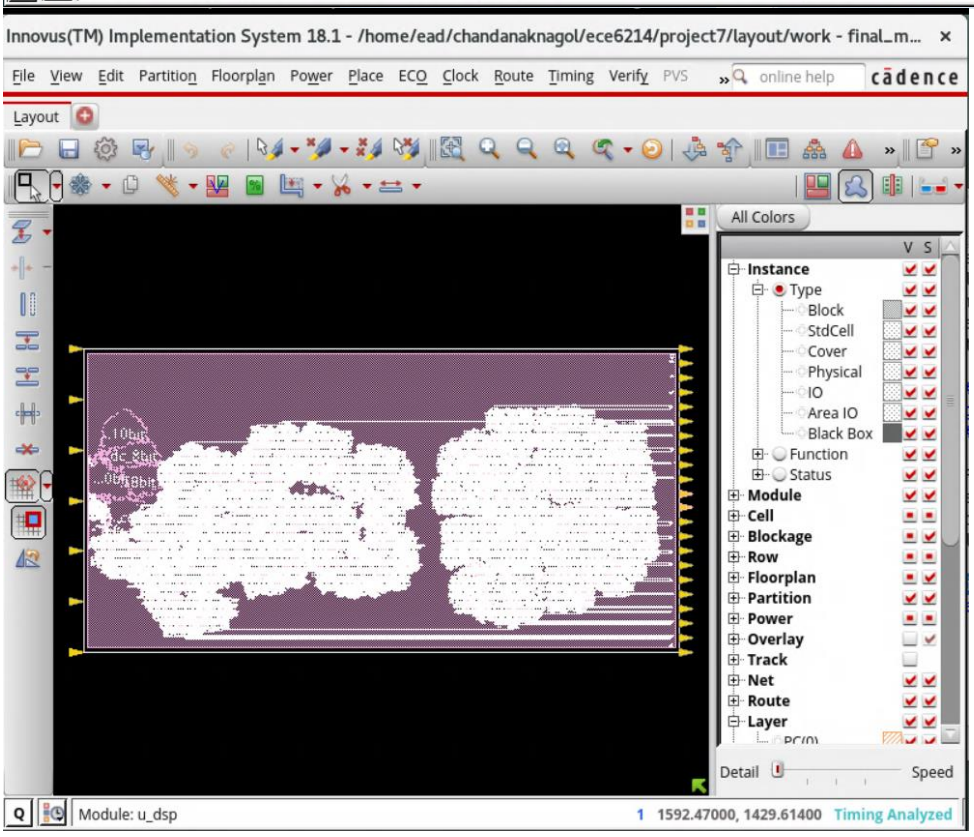
Attached

f. “Floorplan view” image of final layout (view select button on upper right of innovus GUI)

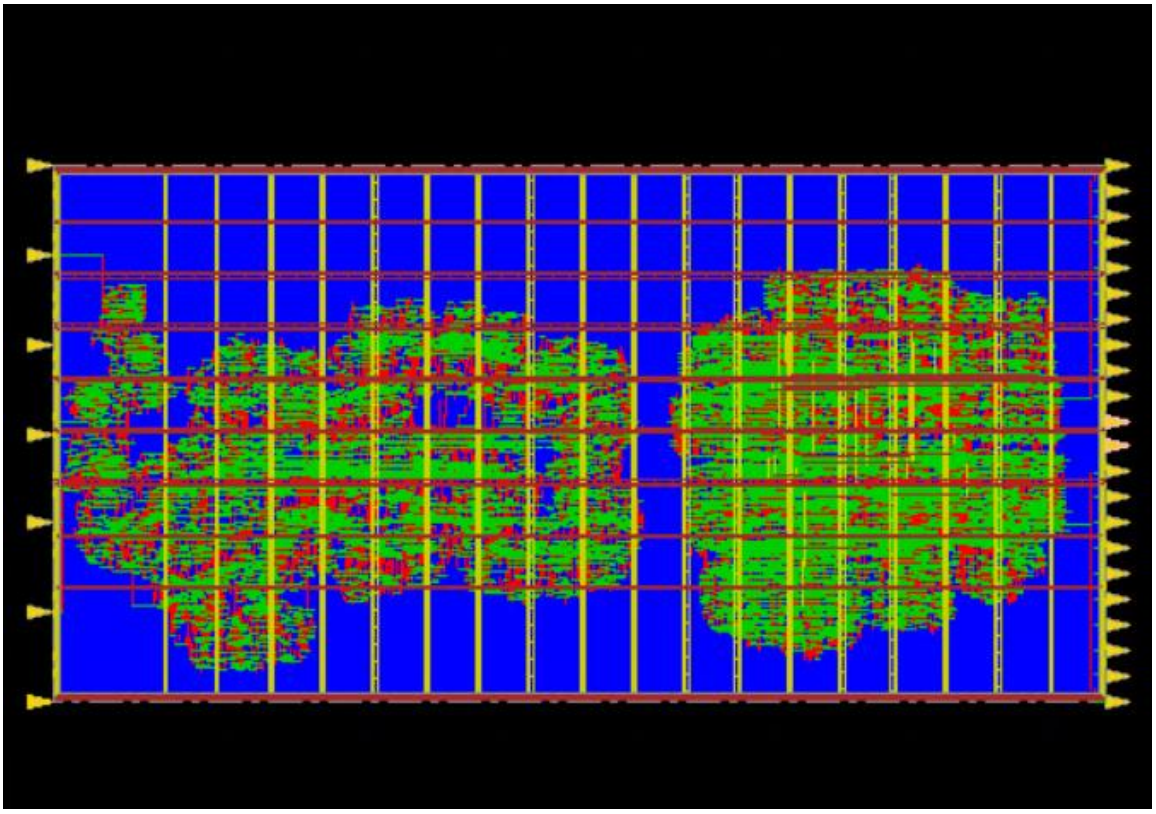

Innovus(TM) Implementation System 18.1 - /home/ead/chandanaknagol/ece6214/project7/layout/work - final_m...
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS
online help
cadence
Layout
All Colors
V S
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
0 2135.19200, 1191.14600
Timing Analyzed

g. “Amoeba view” image of final layout

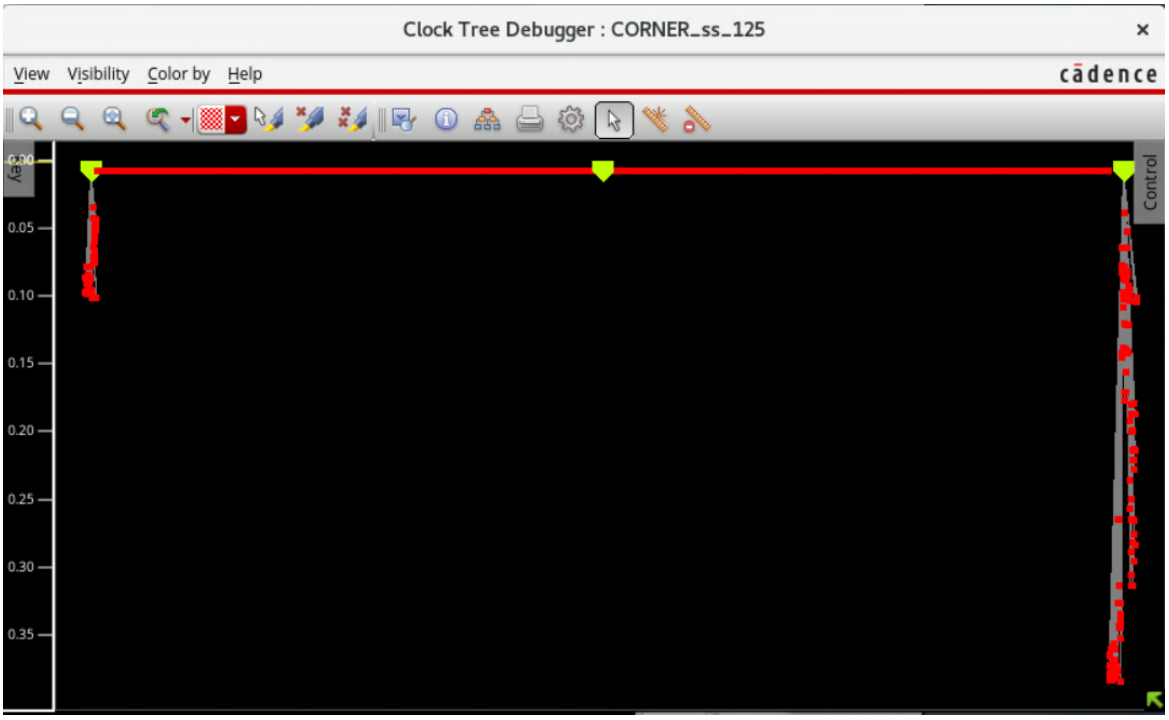




h. “Layout view” image of final layout



i. Image of clock tree



j. Final setup timing analysis report

Attached

k. Final hold timing analysis report

Attached