LAB 6

1. Design a combinational circuit that multiplies two signals A and B (4-bit each).

2. Design a 8 x 4 memory with asynchronous read. Ports are CLK (Clock), WE (write enable), DIN (Data Input), Dout (Data Output), W_ADDR (Write Address), R_ADDR (Read Address).

3. Design a 4 x 8 memory with asynchronous read and Output Enable (OE). Output is available when OE='1' and set to "00000000" when OE='0'.

4. Design a 4 x 5 memory with synchronous read. Ports are CLK (Clock), WE (Write Enable), ADDR (Address), DIN (Data Input), Dout (Data Output).

5. Design a 8 x 5 bidirectional memory with asynchronous read. Ports are CLK (Clock), WE/RE (Write / Read Enable), ADDR (Address), DIN/DOUT (Data In / Data Out).

6. Design a 6 x 3 memory with synchronous read .Ports are CLK (Clock), Write Enable (WE), Output Enable (OE), Write Address/Read Address1 (WADDR/RADDR1), Read address 2 (RADDR2), Data in (DIN), Data out 1 (DOUT1) and Data out 2 (DOUT2).