LAB Rules

1. Create doc, sim, src and synth folder for every lab question.
2. Add design source files inside src folder.
3. Use sim folder for creating new simultion project and add all simulation related files in this folder.
4. Add all synthesis and Implementation related files inside synth folder.
5. Add documentation word file inside doc folder. This file should contain diagram for Top level module, design approach and problems encountered during design process with their solutions.
6. Force test vectors using Test benches (Stimulus) only.
7. You can use any editor for writing source and Stimulus files (Emacs recommended).
8. Use Questasim for verifying waveforms and Xilinx ISE for synthesis.
9. All steps starting form creating project, compiling etc. has to be performed using commands in the Transcript. Use of GUI is not recommended.
10. Once over with given lab question, explore language constructs and design tools.
11. Maintain proper lab records, they would be used for Lab Evaluation.