Lab 5

1. Using Core generator Design and Verify functionality of following blocks
   i. 5x5 unsigned multiplier
   ii. 32x4 Simple Dual Port Ram
   iii. 5 Bit Adder/Subtractor Circuit using Fabric(Verify using FPGA Editor)
   iv. 3 Bit Adder/Subtractor Circuit using DSP48(Verify using FPGA Editor)
   v. 8x8 ROM with initial value provided from .coe file

2. Design positive edge triggered D Flip Flop, with asynchronous active low clear and active high preset using **procedural continuous assignments** (assign and deassign). Also verify concept of force and release using stimulus.

3. Design a 4-bit counter with asynchronous reset, synchronous load and enable inputs. On reset the counter is set to 1000 and counts sequence in the order specified below (top to bottom and loop back). Counter can be loaded with any value present in the sequence. Counter should go back to reset state if loaded with some invalid count. Enable pin can be used to halt the counter if set to 0. Use $monitor to verify the functionality of the counter.

   1000
   0111
   1011
   0100
   1001
   0010
   0101
   1100
   0110
   0011
   1111
   0001
   1110
   1101

4. Design an 8x8 sequential multiplier. The multiplier has asynchronous reset, synchronous load and output valid signal. Use the concept of self-testing Test Bench to verify that multiplication result is correct.