Lab 1

1. Write the code for single bit full adder using
    a. Data flow modeling
        i. Extend the above approach to create a 4-bit full adder.
        ii. Extend the above approach to create a 8-bit full adder.
    b. Gate level modeling
        i. Create 4-bit full adder using single bit full adders (designed at gate level).
        ii. Create 8-bit full adder using 4-bit full adders (designed above).
2. Write code for 2:1 multiplexer using
    a. Gate level modeling
        i. Create 4:1 mux using 2:1 designed above.
    b. Ternary Operator
        i. Extend the concept to build 4:1 mux using Ternary operation only.
3. Design D Latch using logic gate. (Hint: design D Latch from SR Latch).
        a. NAND Gates only.
        b. NOR Gates only.
4. Design T Flip Flop using Latches having asynchronous set and clear (Refer to page 502 of Digital Design by Wakerly).
5. Design frequency divide by 8 circuit using T Flip Flop. Identify if there would be any problem if reset and set were synchronous.