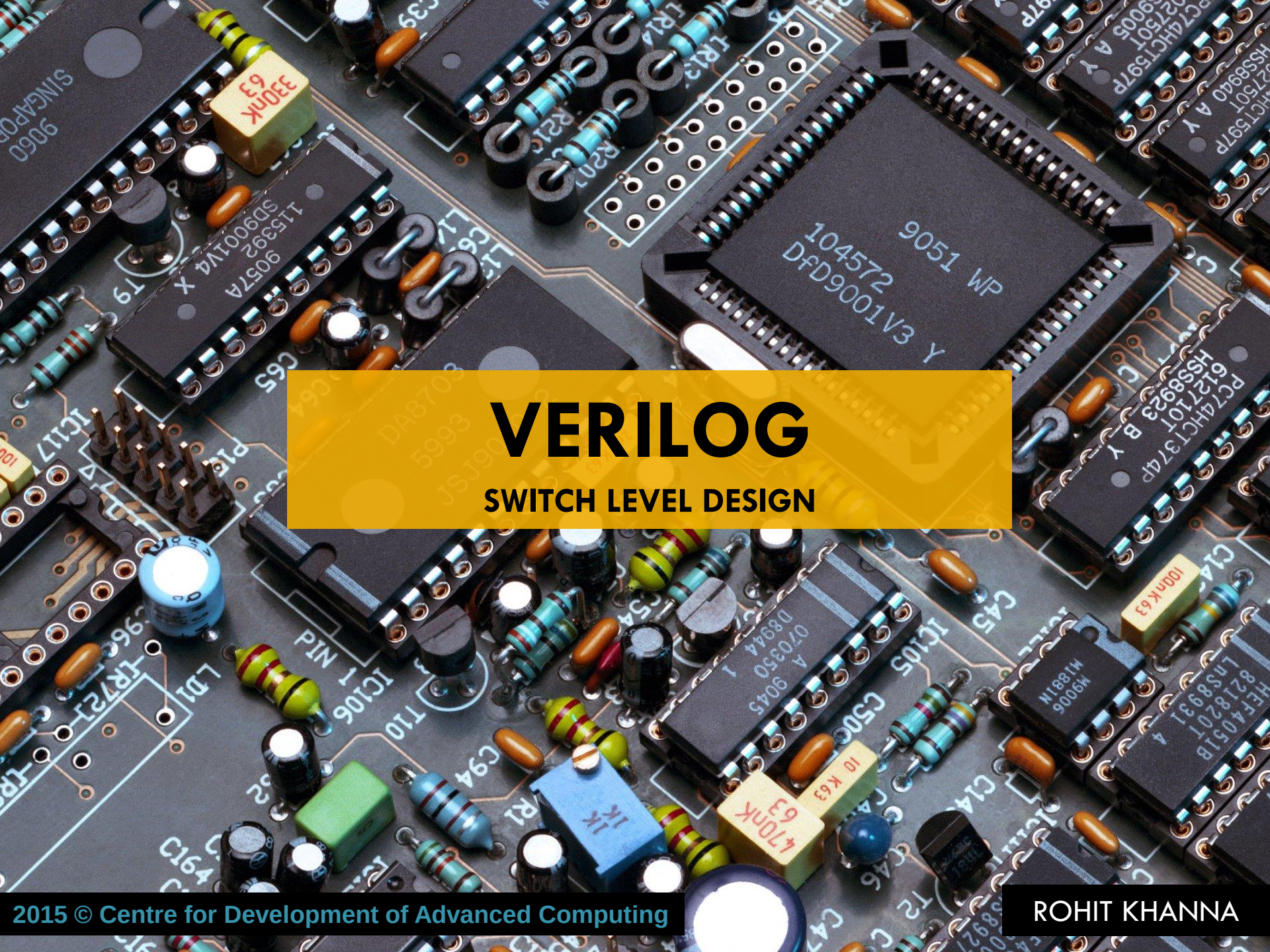


VERILOG

SWITCH LEVEL DESIGN

ROHIT KHANNA

Switch Level Modeling

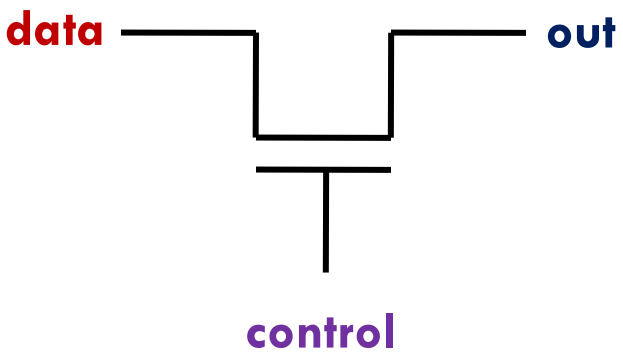
- Verilog allows user to model design with help of transistors.
- This style of representing user design is called as switch level modeling.
- Verilog provides following switching elements to design a digital circuit.

nmos	cmos	tranif0
pmos	tran	tranif1

- Resistive versions of these switches are also available.

MOS Switches

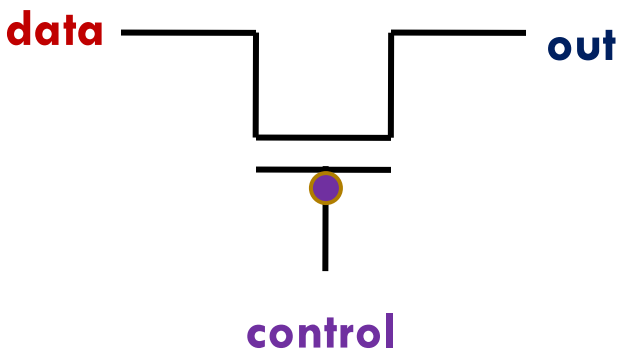
nmos



control==0, out=Z
control==1, out=data

nmos n1 (out, data, control)
nmos (out, data, control)

pmos

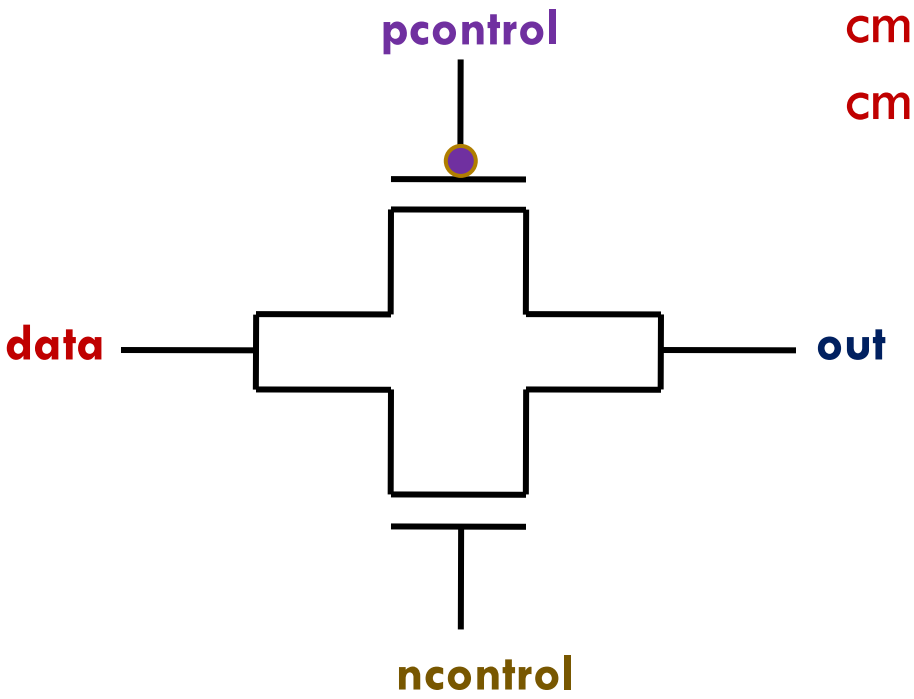


control==0, out=data
control==1, out=Z

pmos n1 (out, data, control)
pmos (out, data, control)

CMOS Switch

cmos



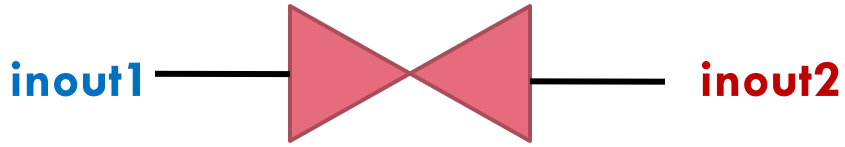

```
cmos n1 (out, data, ncontrol, pcontrol)
cmos    (out, data, ncontrol, pcontrol)
```

```
pmos    (out, data, pcontrol)
nmos    (out, data, ncontrol)
```

pcontrol and ncontrol are usually complements of each other

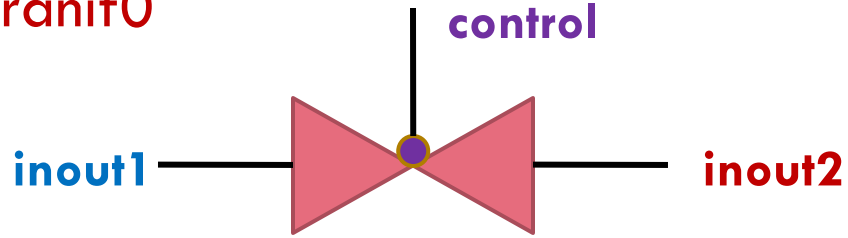
Bi-directional Switches

tran



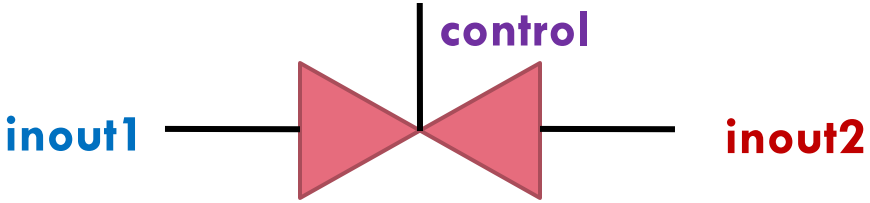
tran (inout1, inout2)

tranif0



tranif0 (inout1, inout2, control)

tranif1



tranif1 (inout1, inout2, control)

Resistive Switches

- Resistive switches offers source to drain impedance, which reduces signal strength when signal passes through it.
- Verilog provides following resistive switches.

rnmos
rpmos
rcmos
rtran
rtranif0
rtranif1

- Port ordering of resistive switches are same as that of their corresponding basic switch.

Strength Table

Input vs. Output Strength for Resistive Switches

Input Strength	Output Strength
supply	pull
strong	pull
pull	weak
weak	medium
large	medium
medium	small
small	small
high	high

Switch Delays

Switch	Delay Allowed	Examples
pmos, nmos	Rise, Fall, Turnoff	pmos #(3) (out, data, control)
rpmos, rnmos	Rise, Fall, Turnoff	rpmos #(3, 2) (out, data, control)
cmos, rcmos	Rise, Fall, Turnoff	cmos #(3, 2, 1) (out, data, ncontrol, pcontrol)
tran, rtran	None	tran (inout1, inout2)
tranif0, rtranif0	Turn-On, Turn-Off	tranif0 #(3) (inout1, inout2, control)
tranif1, rtranif1	Turn-On, Turn-Off	tranif1 #(3, 2) (inout1, inout2, control)