LAB 5

1. Using generic design a parallel in serial out (PISO) shift register with synchronous load and synchronous enable. Verify the functionality of this design with help of 5-bit and 8-bit PISO.

2. Design 6-bit rotational left Shift register with synchronous load and synchronous enable using
   (i) Behaviour Modeling
   (ii) Structured Modeling

3. Design a serial in parallel out shift register (SIPO) with asynchronous reset (clear). The circuit accepts serial data (din) and generates 8 bit parallel data (dout).

4. Design an 8-bit Shift Register which supports parallel load, rotational right shift and rotational left shift operation.

Type	Name	Size	Function
Control Inputs	Ld_shift	1-bit	Load when set to 1, Shift when set to 0
	Rs_Ls		Right shift when set to 1, Left shift when set to 0
	Rst		Reset when Rst is set to 1.
	Clk		Clk is same as clock.
Data output	Data_out		Serial data output during shift operation
Data Input	Data_in	8-bit	Data input during Load Operation

   (a) Behaviour Style.
   (b) Structural Style.

5. Design a D-Flip Flop with clock to output delay (assume as per requirement). Assume that Setup window is 2 ns and Hold window is 3 ns. Use assert statement to report set-up and hold-violations. Also display the output and the time at which output is generated on the transcript. Example "Output is 1 at time 3 ns". Validate you chosen clock to output delay by designing a 2-bit shift register with this D-Flip Flop.

6. Design a 4 bit linear feedback shift register. Make three copy of this LFSR, initialise them with different values. The outputs of these LFSR will serve as test pattern inputs to a full adder. The parallel output of first LFSR will serves as input A of a Full Adder. The parallel output of second LFSR will serve as input B of a Full Adder. The serial output of third will serve as Carry input of a Full Adder. Add a circuit which decides whether your full adder is in test or execution mode. If in execution mode, it should accept inputs from user instead of LFSRs.