Lab 4

1. Design a circuit which is capable of detecting “10110” pattern in an incoming sequence (serial input first bit is '1’ then ‘0’ then ‘1’ and so on) using :
    a. Non Overlapping Mealy model
    b. Overlapping Mealy model

2. Use Gate Level modeling to design a sequence detector for“1010011” pattern using:
    a. Overlapping Mealy
    b. Non Overlapping Mealy

3. Design 16 x 16 synchronous memory using:
    a. Behavior Modeling
    b. Gate Level Modeling

4. Design 16 x 16 bidirectional memory. Use gate primitive bufif1or bufif0 to design bidirectional data bus. Use Tri-state buffer only at the data output from the memory, it should not be present at data input to memory.