LAB 3

1. Magnitude Comparator with two inputs A and B (3-bit each) using Schematic.

2. NOR based SR Latch with enable input using Schematic.

3. 8 x 3 Priority Encoder using concurrent statements

4. Use concept of array and with select statement to design ROM which implements the following functions:
   F1= A'BC + AB + A'BC'
   F2= ABC' + A'B'C' + A'C
   F3= ABC + AB'C' + A'B'C
   F4= AB + BC + CA

5. Design a T latch using
   (i) Concurrent Statement
   (ii) Sequential Statements
   Note: First design without any delay and simulate design (Identify the problem) then add delay of 3ns and verify the simulation results

6. Design D Flip Flop with
   (i) Asynchronous Reset
   (ii) Synchronous Reset
   (iii) Asynchronous Reset and Preset
   (iv) Asynchronous Reset and Preset with Enable

7. Ring Counter (6-bits) using Schematic

8. Johnson Counter (6-bits) using Schematic