Zed Board

1. Write code for 4-bit full adder. Verify Simulation, RTL Analysis, Synthesis and Implementation of this design. Provide user constraints with help of .xdc file and program (PL-side) of Zed-Board.

2. Write a code to
    a. Find and print factorial of a given number.
    b. Print all prime numbers below the given number
    c. Accept three inputs, a (0 to 15), b (0 to 15) and c (0 to 1). Find Sum and print result on the console.

    Use PS side of zed board to verify these codes.

3. Use PS to accept input a (0 to 255) from user and display this data on LED's using FPGA Resources (PL). Also display current switch status on the console (0 to 255).

4. Boot Zed Board from Zed Board Linux given on FTP. Write a shell script to design a 8-bit counter, with each count separated by a delay of 1 sec. Use write_led command to show result on LED's and read_sw to halt/resume the counter.

5. Accept 3 inputs from user (PS side), a (0 to 15), b (0 to 15) and c (0 to 1). Send that data to Full Adder implemented on FPGA (PL side), Full adder output pins will drive the LED's.

6. Design a Block Ram (128 x 8) using (PL Side). Accept WE (write enable), RE (read enable), Read Address, Write Address, Din (Data Input) from PS-side. Display dout (Data Output) on LED's as well as the console.

7. Create binary files to boot (PS-PL) from SD Card, try this for questions 2,3 and 5.