Lab 2

1. Design Decoders with following specifications
   a. 2:4 using gate level modeling.
   b. 4:16 using shift operator.

2. Design 8:3 priority encoder using dataflow modeling.

3. Design configurable full adder using parameter construct (Test it for 8 bit and 16 bit full adder). Use $Strobe for Displaying result on transcript.

4. Implement Y= A|B|C + A.B.E + |B.C + C|D using delay value 3 for and gates, 2 for or gates and 4 for not gates. Use two inputs and, or gates only. Use $Monitor for displaying result on transcript ,also turn off display for 50 time units and then continue displaying the results.
   Note: |B|C means (not B) and (not c)

5. Design parallel in parallel out 8-bit rotational right shift register with a clock, synchronous load input using
   a. Blocking
   b. Non-Blocking.

6. Design 16:1 mux using case statements.

7. Design 8:3 priority encoder using casez statements.

8. Design the following circuits
   a. D latch with reset using if-else statement.
   b. D flip-flop using latch designed above. Verify whether flip-flop has synchronous or asynchronous reset.
   c. D flip-flop with asynchronous reset using If-else Statement.