Practice Questions

1. Design a 2 x 4 memory with synchronous read. Ports are CLK (Clock), Output Enable (OE), Write Enable (WE), Write Address (WADDR), Read address (RADDR), Data in (DIN) and Data out (DOUT).

2. Design a 16 x 7 memory with synchronous read. . Ports are CLK (Clock), Write Enable (WE), Write Address/Read Address1 (WADDR/RADDR1), Read address 2 (RADDR2), Read address 3 (RADDR3), Read address 4 (RADDR4), Data in (DIN), Data out 1 (DOUT1), Data out 2 (DOUT2), Data out 3 (DOUT3) and Data out 4 (DOUT4).

3. Design a circuit that detects positive edge on signal Data.