

**NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION  
TECHNOLOGY, CALICUT**



**NPTEL Lab Workshop Manual**

**Lab Workshop on FPGA Architecture and Programming using  
Verilog HDL**



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## Introduction to Combinational Circuit Simulation Lab: 1

### Logic gates

#### Introduction

The purpose of this experiment is to simulate the behavior of several of the basic logic gates and you will connect several logic gates together to create simple digital model.

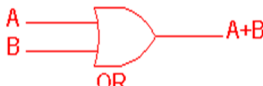
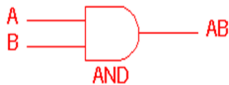
#### Software tools Requirement

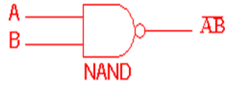

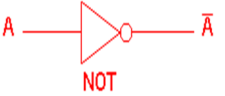
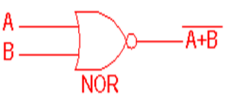
Modelsim (Siemens)

Xilinx Vivado



#### Logic Gates and their Properties

Gate	Description	Truth Table			Logic Symbol
OR	The output is active high if any one of the input is in active high state, Mathematically, $Q = A+B$	A 0	B 0	Output Q	
		0	1	0	
		1	0	1	
		1	1	1	
AND	The output is active high only if both the inputs are in active high state, Mathematically, $Q = A.B$	A	B	Output	
		0	0	Q 0	
		0	1	0	
		1	0	0	
		1	1	0	

NAND	The output is active high only if any one of the input is in active low state, Mathematically, $Q = (A.B)'$	A 0 0 1 1	B 0 1 0 1	Output Q 1 1 1 0	
XOR	The output is active high only if any one of the input is in active high state, Mathematically, $Q = A.B' + B.A'$	A 0 0 1 1	B 0 1 0 1	Output Q 0 1 1 0	
NOT	In this gate the output is opposite to the input state, Mathematically, $Q = A'$	A 0 1		Output Q 1 0	
NOR	The output is active high only if both the inputs are in active low state, Mathematically, $Q = (A+B)'$	A 0 0 1 1	B 0 1 0 1	Output Q 1 0 0	

## Describe the following basic logic gates in Verilog HDL and capture the Waveforms

Questions to answered after this lab

1. What is meant by ports?
2. Write the different types of port modes.
3. What are different types of operators?
4. What is difference b/w  $\leq$  and  $=$  operators?
5. What is meant by simulation?