Introduction to Combinational Circuit Simulation Lab: 3

Half Subtractor

Student : Chandani Lapasia

User id : fpga0522-chan50

Code snippet for Half Subtractor DATA flow modelling.

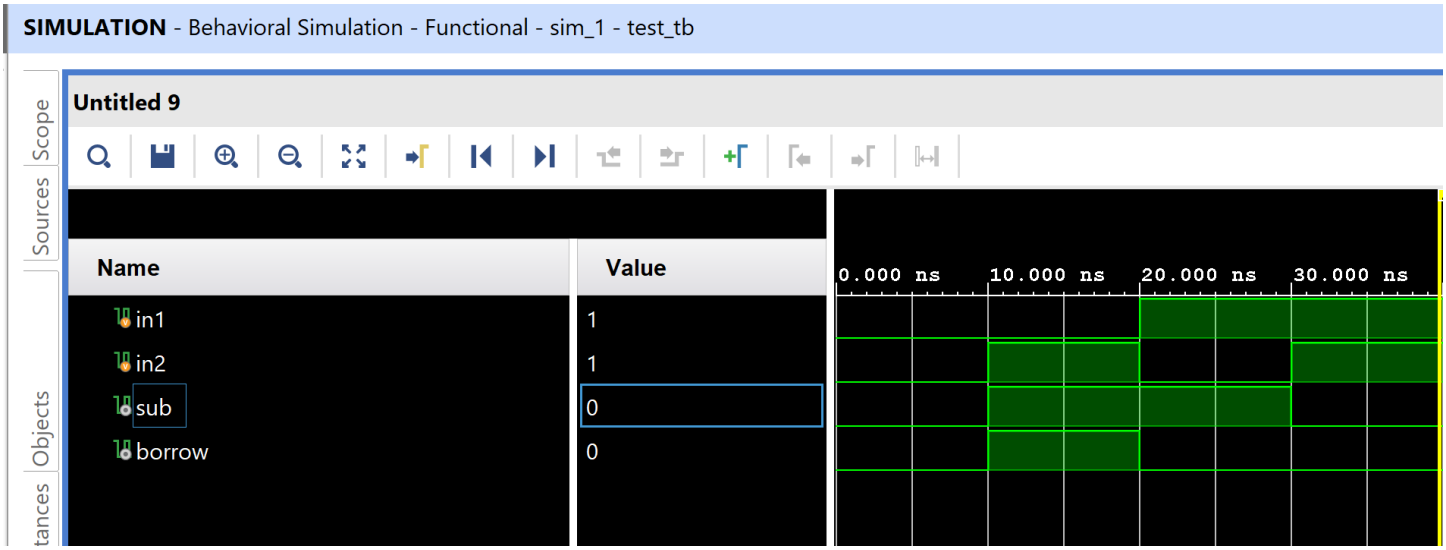
Design:

```
module half_sub(sub,borrow,in1,in2);
input in1, in2;
output sub, borrow;
assign sub= in1 ^ in2;
assign borrow=(~in1 && in2);
endmodule
```

Testbench:

```
module test_tb();
reg in1,in2;
wire sub, borrow;
half_sub u0 (sub,borrow,in1,in2);
initial begin
in1=0; in2=0;
#10 in1=0; in2=1;
#10 in1=1; in2=0;
#10 in1=1; in2=1;
end
initial begin
$monitor($time, "in1=%d in2=%d borrow=%d sub=%d", in1, in2,borrow, sub);
end
endmodule
```

Output waveform:



Output console :

0 in1=0 in2=0 borrow=0 sub=0

10 in1=0 in2=1 borrow=1 sub=1

20 in1=1 in2=0 borrow=0 sub=1

30 in1=1 in2=1 borrow=0 sub=0

Code snippet for Half Subtractor BEHAVORAL flow modelling.

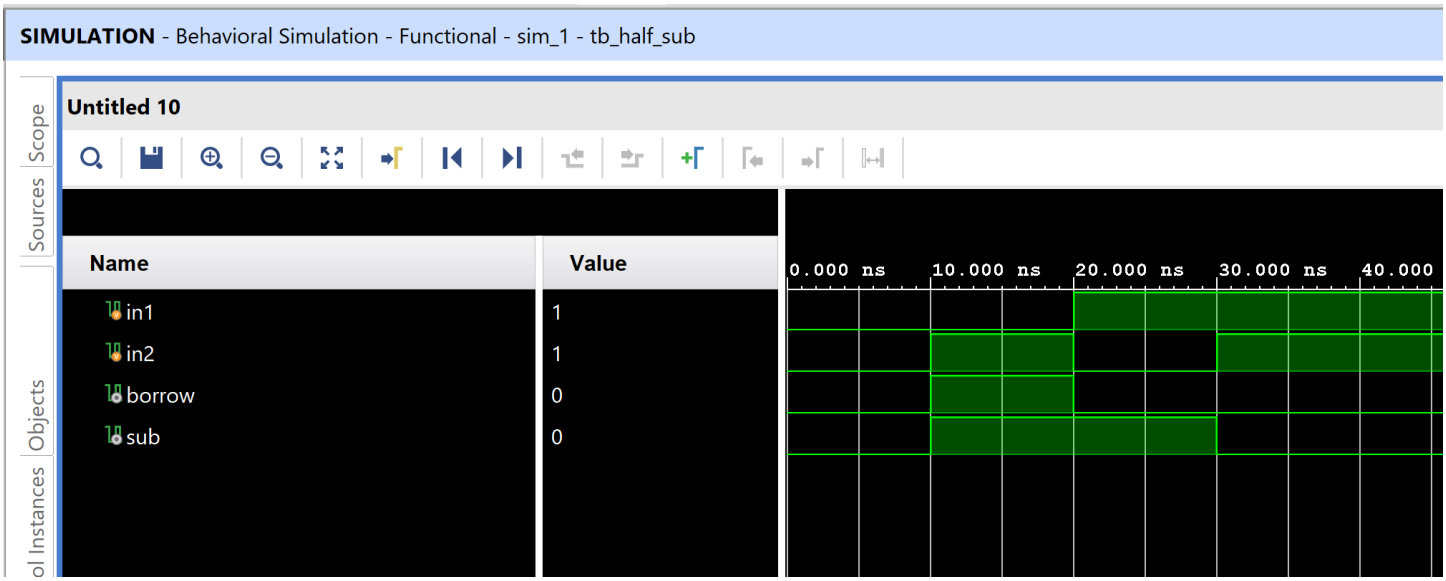
Design code :

```
module half_sub_beh(borrow,sub,in1,in2);
input in1, in2;
output sub, borrow;
reg sub,borrow;
always @(in1 or in2)
begin
sub= in1^in2;
borrow= ((~in1) && in2);
end
endmodule
```

Testbench code :

```
module tb_half_sub();
reg in1, in2;
wire borrow, sub;
half_sub_beh u0(borrow,sub,in1,in2);
initial begin
in1=0; in2=0;
#10 in1=0; in2=1;
#10 in1=1; in2=0;
#10 in1=1; in2=1;
end
initial begin
$monitor($time, "in1=%d in2=%d borrow=%d sub=%d", in1, in2,borrow, sub);
end
endmodule
```

Output waveform :



Output console :

0 in1=0 in2=0 borrow=0 sub=0

10 in1=0 in2=1 borrow=1 sub=1

20 in1=1 in2=0 borrow=0 sub=1

30 in1=1 in2=1 borrow=0 sub=0

Code snippet for Half Subtractor STRUCTURAL flow modelling.

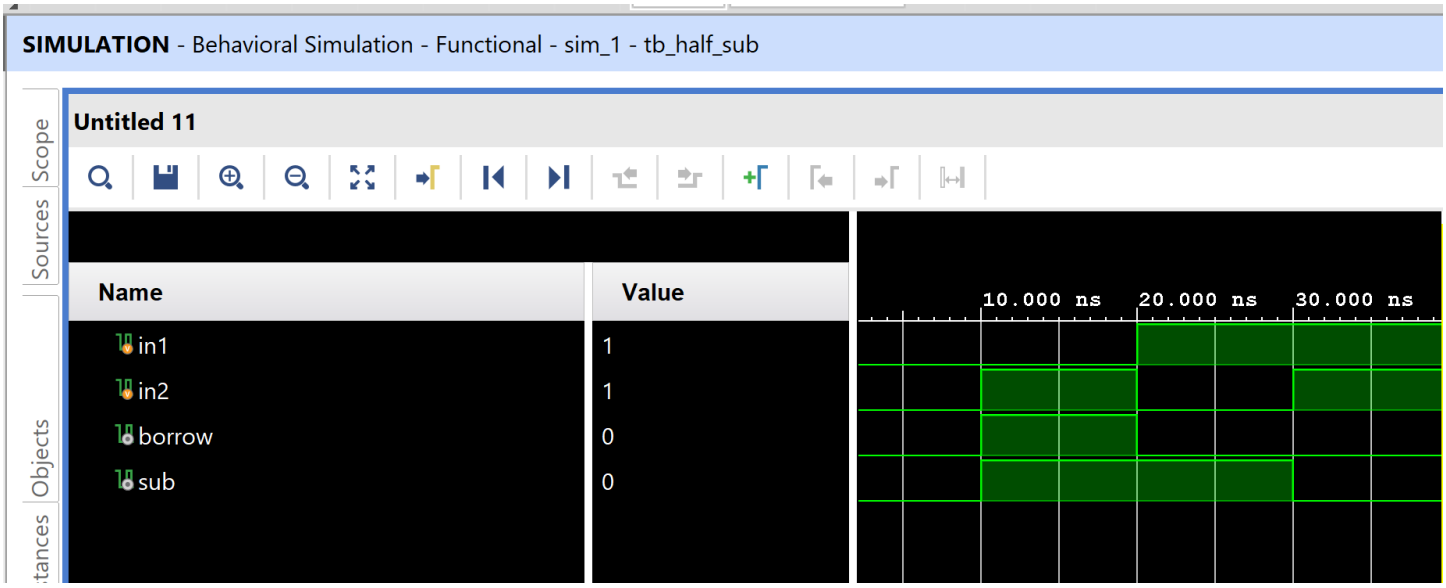
Design code :

```
module half_sub_str(borrow,sub,in1,in2);
input in1, in2;
output sub, borrow;
xor(sub,in1,in2);
not(temp,in1);
and(borrow,temp,in2);
endmodule
```

Testbench code :

```
module tb_half_sub();
reg in1, in2;
wire borrow, sub;
half_sub_str u0(borrow,sub,in1,in2);
initial begin
in1=0; in2=0;
#10 in1=0; in2=1;
#10 in1=1; in2=0;
#10 in1=1; in2=1;
end
initial begin
$monitor($time, "in1=%d in2=%d borrow=%d sub=%d", in1, in2,borrow, sub);
end
endmodule
```

Output waveform :



Output console :

0 in1=0 in2=0 borrow=0 sub=0

10 in1=0 in2=1 borrow=1 sub=1

20 in1=1 in2=0 borrow=0 sub=1

30 in1=1 in2=1 borrow=0 sub=0

========== END==========