Introduction to Combinational Circuit Simulation Lab: 1

Logic gates

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Code snippet:

Design:

```
module logic_gates(in1,in2,o1,o2,o3,o4,o5,o6);
input in1, in2;
output o1,o2,o3,o4,o5,o6;
and(o1,in1,in2);
or(o2,in1,in2);
nand(o3,in1,in2);
xor(o4,in1,in2);
not(o5,in1);
nor(o6,in1,in2);
endmodule
```

Testbench:

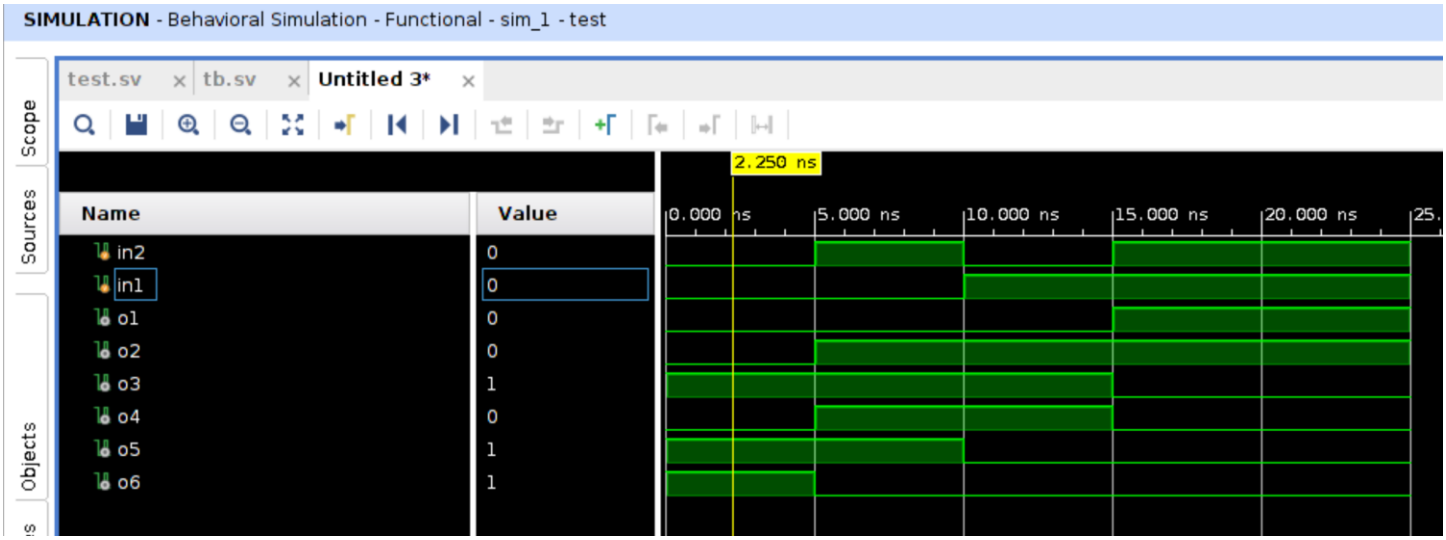
```
module test();
wire o1,o2,o3,o4,o5,o6;
reg in1,in2;
logic_gates u0 (in1,in2,o1,o2,o3,o4,o5,o6);
initial begin
in1= 0 ; in2=0;
#5 in1= 0 ; in2=1;
#5 in1= 1 ; in2=0;
#5 in1= 1 ; in2=1;
```

```
#10 $finish;

end

endmodule
```

Output waveform:



Question and Answers :

1. What is meant by ports?
   Ports are the Input – Output at the boundary of the module which help in communicating with other modules. In port declaration, we specify the port direction (input, output or inout) and datatype of the port.

   Example :

   ```
   module test(input a, b, output d);
   wire a,b; reg d;
   endmodule
   ```

2. Write the different types of port modes.
   The different types of port direction are input, output, inout.

   Input : All the data is received into the design through using input port.
   Output : All the data is sent into the design/other module using output port.
   Inout : All the data is received and sent into the design through inout port. It is bi-directional port.

   Example :

   ```
   input a;
   output b;
   inout c;
   ```

3. What are different types of operators?
   There are various operators such as logical operator , bitwise operator, relational operator, conditional operator, replication operator, concatenation operator, shift operators, equality/inequality and case equality/inequality operator and arthimetic operator.

   Arithmetic: + - * /

   Modulus: %

   Relational: < <= > >=

   Logical: ! && ||

   Logical equality: == !=

   Case equality: === !==

   Bit-wise: ~ & | ^ ~^ ^~

   Reduction: & ~& | ~| ^ ~^ ^~

   Shift: << >>

   Conditional: ?:

   Concatenations and replication: {} {{}}

4. What is difference b/w <= and = operators?

<= is Non-blocking assignment operator. This operator helps in evaluating the expression value in the active region but the updation to the LHS side takes place in the Non blocking region in the Verilog stratified event queue. Hence, we get the previous value on LHS in the current time stamp. Here the execution of the other statements are not blocked.

= is a blocking assignment operator. The evaluation as well as the updation on the LHS takes place in the active region of the Verilog stratified event queue. The other statement are not executed until all the events in the active region queue is completed.

5. What is meant by simulation?
   Simulation is a process of applying the stimuli for a duration of time to check the behavior of the RTL code. Simulation helps in testing all the possible input combinations over the hardware designed and shows the output of device. Simulation is done using a software Electronic design Automation tool. This can help in catching the bugs before the hardware is fabricated.