NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION

TECHNOLOGY, CALICUT

NPTEL Lab Workshop Manual

Lab Workshop on FPGA Architecture and Programming using Verilog HDL

Contact Point for the Lab

Mr. Sreejeesh SG

Senior Technical Officer

Email: sreejeesh@nielit.gov.in

Ph.: 9447769756 (WhatsApp Preferred)

Circuit Simulation Lab: 2

Binary Adders

Introduction

The purpose of this experiment is to introduce the design of simple combinational circuits, in this case half adders, and full adders.

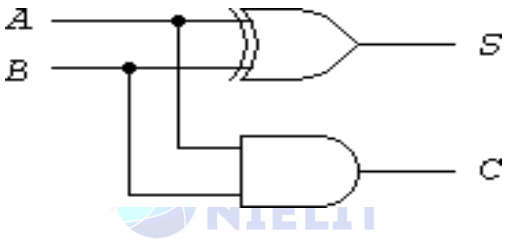
Software tools Requirement

Modelsim (Siemens)

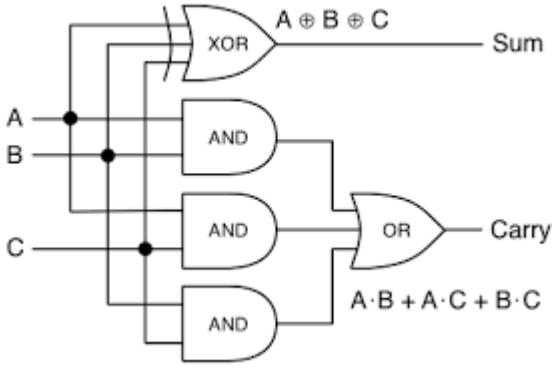
Xilinx Vivado

Logic Diagram

Half adder



Full adder



Describe the following basic adders in Verilog HDL and capture the Waveforms

Dataflow modeling

Behavior modeling

Structural modeling

Questions to answered after this lab

1. *What is meant by combinational circuits?*
2. *Write the sum and carry expression for half and full adder.*
3. *What is signal? How it is declared?*