**NIELIT**

**LAB Workshop on 'FPGA Architecture and Programming using Verilog HDL' Batch 2**

**MINIPROJECT**

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**Design Code Snippet:**

module top(i3,i2,i1,i0,clk,reset,Y,data);

input i3, i2, i1, i0, clk, reset;

output [3:0] Y;

output data;

wire [3:0] temp1;

wire temp2,temp3,temp4;

ila\_0 my\_ila\_new (.clk(clk),.probe0({temp2,temp3}));

my\_clk\_div u\_my\_clk\_div(.clk(clk),.clk\_div(temp4));

my\_latch u\_latch(.I(temp1), .clk(clk),.reset(reset),.Y(Y));

my\_decoder u\_decoder(.i0(temp3),.i1(temp2),.en(data), .y(temp1));

my\_mux u\_mux(.data(data), .i3(i3),.i2(i2),.i1(i1),.i0(i0),.s1(temp2),.s0(temp3));

my\_counter u\_counter(.clk(temp4),.s1(temp2),.s0(temp3));

endmodule

module my\_latch(I, clk,reset,Y);

input [3:0] I;

input clk,reset;

output [3:0] Y;

reg [3:0] Y;

always @( clk or I or reset)

begin

if(!reset)

Y<=4'b0000;

else

Y<=I;

end

endmodule

module my\_decoder(i0,i1,en,y);

input i0,i1,en;

output [3:0] y;

reg [3:0] y;

always @(en or i0 or i1)

begin

if(en)

begin

case({i1,i0})

2'b00: y=4'b1000;

2'b01:y=4'b0100;

2'b10:y=4'b0010;

2'b11:y=4'b0001;

endcase

end

else

y=4'b0000;

end

endmodule

module my\_clk\_div(clk,clk\_div);

input clk;

output reg clk\_div;

reg [25:0] temp=26'd0;

always @(posedge clk)

begin

temp<=temp+26'd1;

clk\_div<=temp[20];

end

endmodule

module my\_counter(clk,s0,s1);

input clk;

output s0,s1;

c\_counter\_binary\_0 u6 ( .CLK(clk), .Q({s1,s0}) );

endmodule

module my\_mux(data, i3,i2,i1,i0,s1,s0);

input i3,i2,i1,i0,s0,s1;

output data;

assign data = (i0 && ~s1 && ~s0) || (i1 && ~s1 && s0) || (i2 && s1 && ~s0) || (i3 && s1 && s0);

endmodule

**Testbench Code Snippet:**

module tb();

reg i3,i2,i1,i0,clk,reset;

wire [3:0] Y;

wire data;

top u0\_top(i3,i2,i1,i0,clk,reset,Y,data);

initial begin

reset=1'b0;clk=0; i3=1;i2=0;i1=1;i0=0;

#10 reset= 1'b1;i3=0;i2=0;i1=0;i0=1;

#10 reset= 1'b1;i3=1;i2=1;i1=1;i0=1;

end

always forever #5 clk = ~clk;

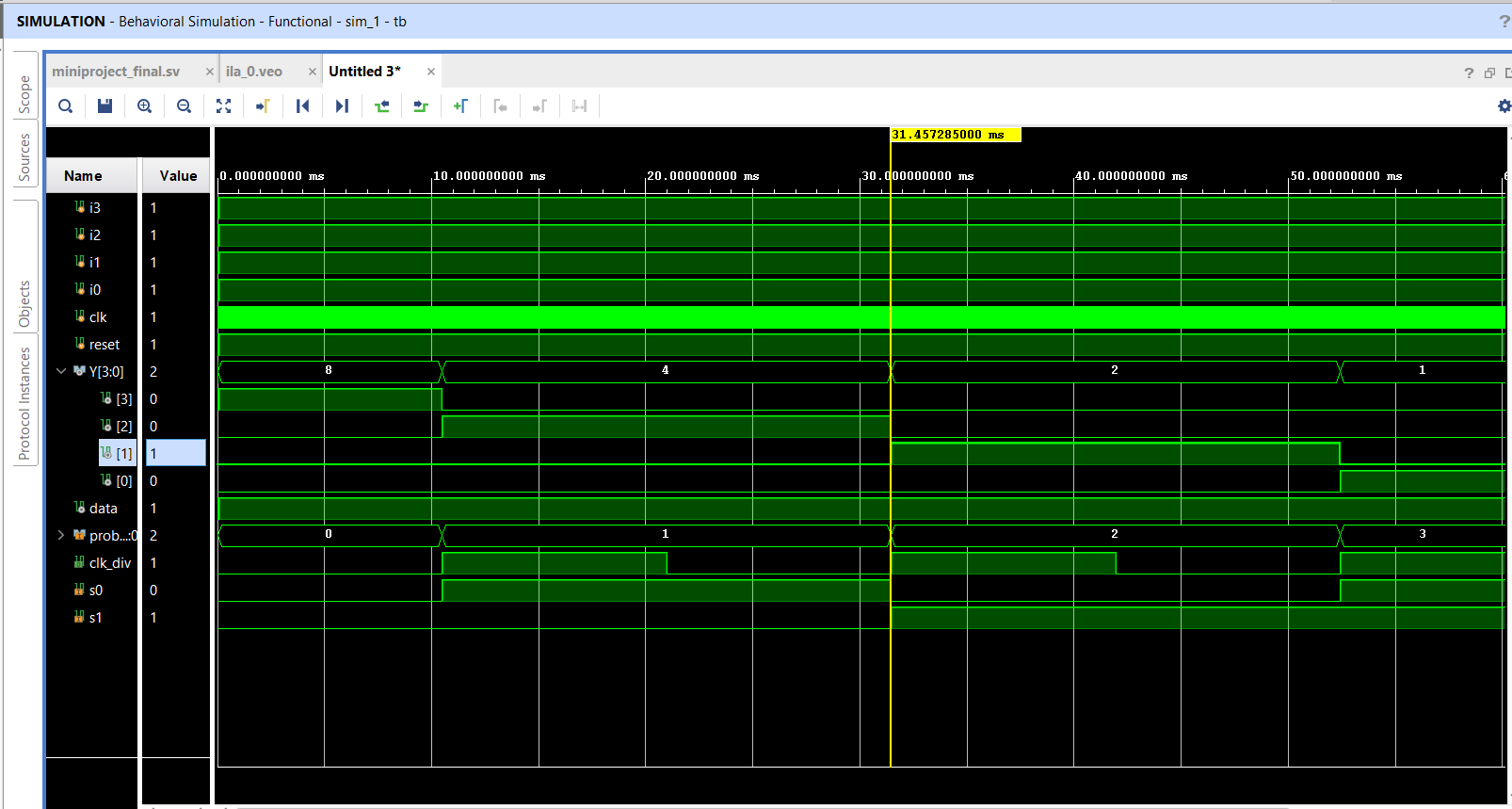
initial begin

$monitor ($time, "\t", "i3=%d i2=%d i1=%d i0=%d Y=%d ", i3,i2,i1,i0,Y);

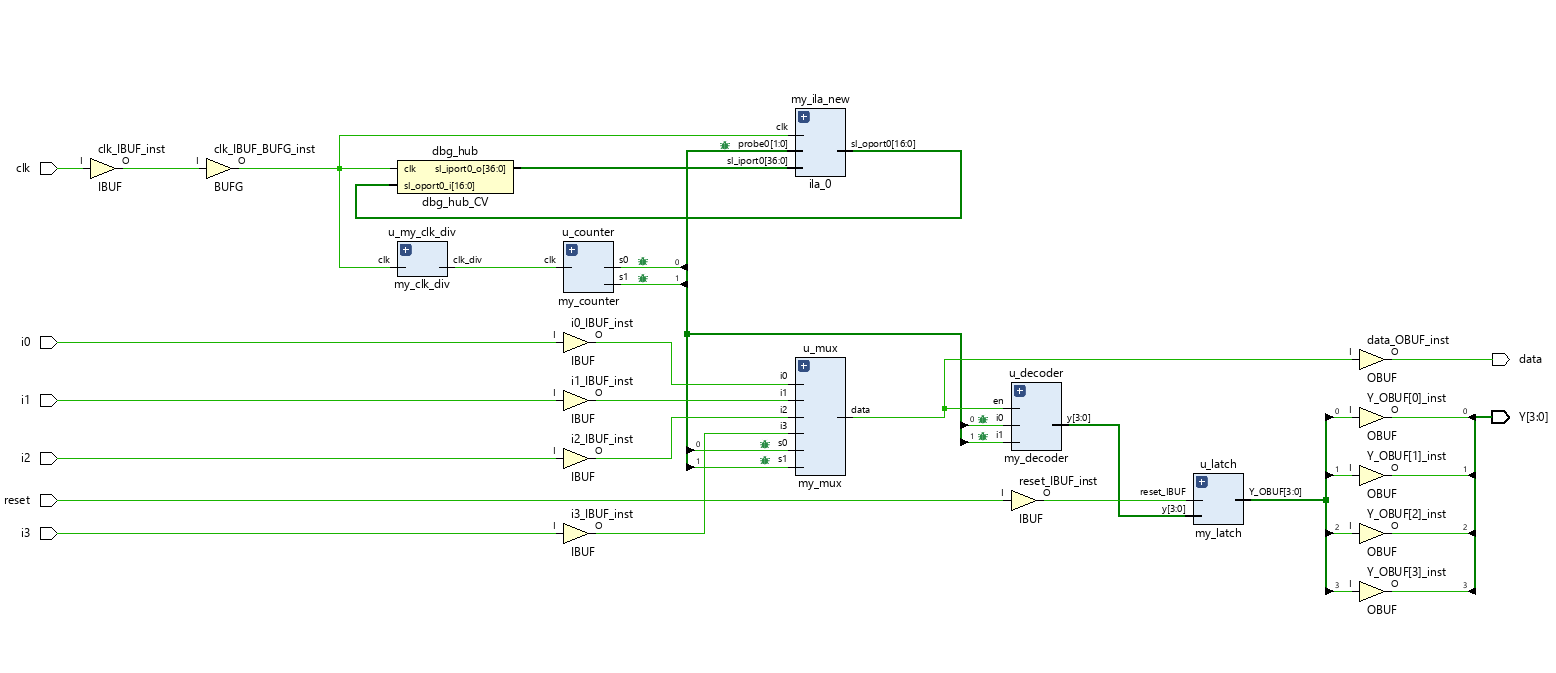
end

endmodule

**Simulation Output :**



**Schematic Report:**



**Synthesis Report:**

Start Writing Synthesis Report

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Report BlackBoxes:

+------+-------------------+----------+

| |BlackBox name |Instances |

+------+-------------------+----------+

|1 |c\_counter\_binary\_0 | 1|

|2 |ila\_0 | 1|

+------+-------------------+----------+

Report Cell Usage:

+------+-----------------+------+

| |Cell |Count |

+------+-----------------+------+

|1 |c\_counter\_binary | 1|

|2 |ila | 1|

|3 |BUFG | 1|

|4 |CARRY4 | 6|

|5 |LUT1 | 1|

|6 |LUT2 | 4|

|7 |LUT3 | 4|

|8 |LUT6 | 1|

|9 |FDRE | 22|

|10 |IBUF | 6|

|11 |OBUF | 5|

+------+-----------------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:25 ; elapsed = 00:00:26 . Memory (MB): peak = 1132.832 ; gain = 112.043

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

**Output Waveform:**

