CHANDANI LAPASIA
Application Engineer II
SYNOPSYS INDIA PVT LTD.

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ABOUT ME:

- 5+ years and working in Semiconductor domain. Exposure to various technologies and complete design and verification flow. Strong logical and debugging skills. Looking forward for more complex and challenging projects in **Front-end Design and Verification**.
- Ability to adapt to a wide variety of situation. Demonstrating a motivated attitude with comprehensive analytical and problem-solving skills. Fluent in English, Hindi, Telugu, Gujarati.

EXPERIENCE:

- Corporate Application Engineer II at **Synopsys India Pvt. Ltd, Hyderabad.**
  November-2020 to Present

- Corporate Application Engineer I at **Synopsys India Pvt. Ltd, Hyderabad.**
  April-2017 to November-2020

- Technical Intern at **Synopsys India Pvt. Ltd, Hyderabad.**
  May-2016 to April-2017

WORK:

- Providing pre-sale and post-sale support of Synopsys VCS, VCSMX, DVE and Verdi.
- Partition Compile technology deployment on the Broadcom Designs.
- Debugging various tool issues reported during deployment and customer engagements.
- Proposing new enhancements of the tool and closely working with R&D team to fix the tool bugs.
- Developing scripts and running regressions and benchmark designs of VCSMX, VCS, DVE and Verdi versions.
- Worked with 200+ customers worldwide including big giants of Semiconductor industry. Understanding the customer requirement, their design plans, debugging the errors, helping customer re-code their design for better optimization, helping in improving performance of the design, successfully driving towards closure.
- Trained 2 of my colleagues with the existing Regression Workflow.
- Delivering presentations to the team on VCS on Cloud.
- Received multiple direct customer appreciations for providing the best and accurate solutions and helping them move forward in their projects.

APPRECIATIONS FROM CUSTOMERS AND R&D TEAM:

- **Sr Staff R&D**: I was very impressed with the way Chandani explained the problem over the phone as well as e-mail. More importantly, happy to see that She understood the problem statement very well as well as the impact of the work-around she proposed. She created a small example and tried few alternatives so that customer can move ahead for now.

- **Words from Director, Synopsys:** Thanks, Chandani, for continuing to do **good work on deploying the VCS build on the Broadcom design**. It is an important engagement.

- **NXP Semiconductor**: Received **appreciation and certificate from NXP** on successfully bringing their project to tape-out by the VCS and Verdi tool.

- **Marvell Semiconductor** says that the initial response was correct and solved my issue.

- **Graphcore:** Received appreciation from end-customer as well Synopsys Management on bring closure to this multiple issue seen by Graphcore. Graphcore says **Thank you very much Chandani for your support so far. This was probably the longest investigation ever!**

- **Synopsys Higher Management on above Graphcore engagement:** Thanks, Chandani for being on top of this Graphcore case! I know it's a long story with multiple issues (capacity issue, crash etc) that were debugged using this case. Thanks for being on top of all of them with close follow-ups (both customer and RND) and finally customer is up and running on their project with 1906. **Good Job! Appreciate all your efforts!**

- **Open Silicon:** Received appreciation from the customer on their project for providing solution and testcase, where they were stuck and did not wanted to change the RTL code. Thankyou a Lot Chandani. **Appreciate your outstanding support.**

- **Sharp Semiconductor Innovation**
  Customer wanted to know the process to create and using waveform aliases in Verdi GUI. AE provided the solution. Received appreciation for the quick response from customer. We, Sharp Semiconductor **appreciate your quick response, Chandani. This problem was resolved thanks to your support.**

- **ARM France SAS : Received 5/5 rating on** the time it took to receive an answer/workaround and **the Chandani's technical ability to understand the issue & providing solutions.**

- **Yoshikawakogyo RF Semicon Co**. Received **5 on 5** for **Chandani's technical ability to understand the issue and delivering solution.**

- **HP Enterprise :** Received **5 / 5** rating **the Chandani's technical ability to understand the issue and providing solution to the customer.**

VLSI RTL Design Trainee (August 2015 - February 2016) at CDAC-ACTS, Pune.
- Hands on design experience from RTL coding to generating GDSII file of Digital circuits.
- Functional Verification, Synthesis and Mapping the .bit file to FPGA.
- Designed hardware for FIFO, I2C, SPI, Memories using Verilog.
- Created Layouts of some basic digital circuits using Micro Magic.

TECHNICAL EXPOSURE:
- **VLSI/ASIC Design flow:** RTL Coding, Functional Simulation, Verification using SV, UVM, Synthesis, Static Timing Analysis concepts.
- **Protocols :** Knowledge about the AMBA APB protocol.
- **Technologies:** Partition Compile technology, X-prop, Functional and Code coverage.
- **EDA Tools:** VCSMX, DVE, Verdi, Spyglass Lint, DC Compiler QuestaSim, Xilinx Design Suite (Vivado), Micro magic.
- **Languages:** Verilog HDL, System Verilog, C, C++, Shell Scripting.

- **Platform & Software:** UNIX, Windows, MS-Office.

EDUCATION:

Course	Name & Address of Institutions	Board/University	%age of Marks	Year of Passing
M.Tech (VLSI System Design)	CMR Institute of Technology, Sec-bad	J.N.T.U, Hyderabad	68.50	2017
PG Diploma in VLSI Design	CDAC-ACTS, Pune	Scientific society of Ministry of Communication & IT, GoI.	65.83	2016
B.Tech (E.C.E)	Malla Reddy Engineering college for women, Sec-bad	J.N.T.U, Hyderabad	80.52	2013
Intermediate (MPC)	Narayana Junior College, Sec-bad	Board of Intermediate	89.80	2009
S.S.C	Gujrati High School, Sec-bad	Board of Secondary Education	86.33	2007

PROJECTS:

Title: Serial Peripheral Interface SPI Protocol.
Designed and Implemented Serial Peripheral Interface SPI Master Controller using Verilog HDL.
Simulated successfully using Synopsys VCS compiler. Linting checks done using the Synopsys Spyglass Lint tool.

Title: DUAL PORT ASYNCHRONOUS RAM.
Designed and Implemented Dual Port RAM using Verilog HDL.
Simulated successfully using Synopsys VCS compiler. Linting checks done using the Synopsys Spyglass Lint tool.

ACHIEVEMENTS & EXTRA CURRICULAR ACTIVITIES:
- Participated in 'Circuit making' competition at VNR Vignan Jyothi Institute of Engineering and Technology.
- Participated and won Technical quizzes organized by MRECW.
- Participated in various literature activities in college and school level.
- Have taken sole responsibility in organizing workshop and seminar on leadership skills at the college and have rendered voluntary service to various charitable institutions (People with hearing impaired network PHIN and Bharat Soka Gakkai).

PERSONAL SKILLS & INFORMATION:
- Ability to adapt to a wide variety of situation.
- Comprehensive analytical and problem-solving skills.
- Languages Known: English, Hindi, Telugu, Gujarati.