CHANDANI H LAPASIA
CAE at Synopsys

Phone: +91- 9703300787
Email:chandanilapasia9@gmail.com

CAREER OBJECTIVE:

2+ years and working in Verification domain. Exposure to various technologies and complete verification flow. Looking forward for more complex and challenging projects.

EXPERIENCE:

- Corporate Application Engineer at **Synopsys India Pvt. Ltd, Hyderabad.**
  April-2017 to Present

- Technical Intern at **Synopsys India Pvt. Ltd, Hyderabad.**
  May-2016 to April-2017

WORK:

- Providing pre-sale and post-sale support of Synopsys VCS, VCSMX, DVE and Verdi.
- Partition Compile technology deployment of the Customer Designs.
- Debugging various tool issues reported during deployment.
- Proposing new enhancements of the tool and closely working with R&D team to fix the tool bugs.
- Developing scripts and running regressions and benchmark designs of VCSMX, VCS, DVE and Verdi versions 2017.12,2017.03,2016.06,2015.09.
- Trained 2 of my colleagues with the existing Regression Work Flow.

VLSI RTL Design Trainee (August 2015 - February 2016) at CDAC-ACTS, Pune.

- Hands on design experience from RTL coding to generating GDSII file of Digital circuits.
- Functional Verification, Synthesis and Mapping the .bit file to FPGA.
- Designed hardware for UART, FIFO , SPI, Memories using Verilog.
- Created Layouts of some basic digital circuits using Micro Magic.

VLSI Intern (December 2012 - August 2013) at Vedic School of VLSI Design, Hyderabad.

- Designed an (15, K) Encoder using BCH code.
- Tested its functionality and Implemented upon FPGA.

EMBEDDED Intern (May 2012 - July 2012) at Magni5 Technologies, Hyderabad.

- Designed an artificial vision system for blind using sensor technology.
- Implemented the circuit on Breadboard and Tested its functionality.

TECHNICAL EXPOSURE:

- **VLSI/ASIC Design flow:** RTL Coding, Functional Simulation, Verification using SV, UVM, Synthesis, Static Timing Analysis concepts.
- **Technologies:** Partition Compile technology, X-prop, SDF annotation, Directed and constrained random testing, Functional and Code coverage.
- **EDA Tools:** VCSMX, DVE, Verdi, QuestaSim, Xilinx Design Suite (ISE 14.7, Vivado),Micro magic.
- **Languages:** VHDL, Verilog HDL, System Verilog, C, C++, Shell Scripting.
- **Methodologies:** UVM

- **Platform & Software:** UNIX, Windows,MS-Office.

EDUCATIONAL QUALIFICATION:

Course	Name & Address of Institutions	Board/University	%age of Marks	Year of Passing
M.Tech (VLSI System Design)	CMR Institute of Technology, Sec-bad	J.N.T.U, Hyderabad	68.50	2017
PG Diploma in VLSI Design	CDAC-ACTS, Pune	Scientific society of Ministry of Communication & IT,GoI.	65.83	2016
B.Tech (E.C.E)	Malla Reddy Engineering college for women, Sec-bad	J.N.T.U, Hyderabad	80.52	2013
Intermediate (MPC)	Narayana Junior College, Sec-bad	Board of Intermediate	89.80	2009
S.S.C	Gujrati High School, Sec-bad	Board of Secondary Education	86.33	2007

ACADEMIC PROJECTS DONE:

Title: IMPLEMENTATION OF CONTROLLER DESIGN USING GSM MODEM IN XILINX FPGA VERTEX 4.

This project aims at designing and implementation of a remote and sensing, control and home security system based on GSM (Global System for Mobile). This system offers a complete, low cost, powerful and user friendly way of 24 hours of real time monitoring and remote control of a home and industrial security. The system works as a remote sensing for the electrical appliances at home to check whether it is on or off, at the same time the user can control the electrical appliances at home by sending SMS.

- Tools Used: Mentors Questa Sim, Xilinx ISE Design Suite, Tera Term.
- Language Used: VHDL and Verilog.
- Team Size:4

Title: DESIGN AND FPGA IMPLEMENTATION OF (15, K) ENCODER USING BCH CODE.

This project aims to design a binary encoder for multiple error correction at the receiver's side using BCH code of the size (15,K) for reliable data transfer in the communication channel.

- Tools Used: Mentors QuestaSim, Xilinx ISE Design Suite.
- Language Used: VHDL.
- Team Size:3

Title: DUAL PORT ASYNCHRONOUS RAM.

Designed and Implemented Dual Port RAM using Verilog HDL.

Title: ARTIFICIAL VISION FOR BLIND USING ULTRA SONIC TECHNIQUES.

This project aims at the usage of the ultrasonic range finders to measure the distance of an object by the ultrasound beam and represents it via variable tone sound signals. Thus, building an effective and efficient vision system which helps the blind orienting in the surround space.

Title: KEYPAD CONTROLLED ROBOT

The aim of the project was to make a robot which is can be operated and controlled using a keypad.

Title: WALL FOLLOWER ROBOT

This project aims at designing a robot which follows the wall and navigates its path when encountered by the curves of the wall.

Title: TRAFFIC LIGHT CONTROLLER USING MICRO CONTROLLER.

The function of traffic lights requires sophisticated control and coordination to ensure that traffic moves as smoothly and safely as possible. This project is developed to meet the requirements of solid state traffic light controller by adopting micro controller as the main controlling element, and led's as the indication of light. A micro controller is interfaced to led's provide for centralized control of the traffic signals. Micro controller is programmed in such a way to adjust their timing and phasing to meet changing traffic conditions.

ACHIEVEMENTS & EXTRA CURRICULAR ACTIVITIES:

- Participated in 'Circuit making' competition at VNR Vignan Jyothi Institute of Engineering and Technology.
- Participated and won Technical quizzes organized by MRECW.
- Participated in various literature activities in college and school level.
- Have taken sole responsibility in organizing workshop and seminar on leadership skills at the college and Have rendered voluntary service to various charitable institutions.

PERSONAL SKILLS & INFORMATION:

- Ability to adapt to a wide variety of situation.
- Comprehensive analytical and problem solving skills.
- Languages Known: English, Hindi, Telugu.