# Pipesim.xise

Files required:

* Vgatop.vhd
* Cell\_matrix.vhd
* DCM\_25.xaw
* VgaRefComp.vhd
* Map\_ram.xco (forms a RAM for map storage from the COE files created through make\_coe.m)
* Cell.vhd (the basic cell unit which is to be inserted in the pipeline for final computation)
* Vga\_selector.vhd
* Vga\_controller\_640\_60.vhd
* Vga\_controller\_800\_60.vhd

The code forms a 6x6 matrix of the computational cells and forms required data connections between them so as to facilitate local stream of data from one cell to the other.

The code was successfully simulated for the cell\_grid by initializing data bit in each cell to 1 by the use of a clock-controlled data pipeline.